On the Doping of Silicon Nanowires Grown by Molecular Beam Epitaxy

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This thesis is dedicated to my former supervisor and director of the Max Planck Institute of Microstructure Physics, Halle, Prof. Ulrich Gösele who left for his heavenly abode in November, 2009.

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Last but not least, I acknowledge my family back home in India and friends allover the world. All of them have consistently given me moral support when I decided to pursue a Ph.D. leaving a job in the semiconductor industry.

"There is no place for dogma in science. The scientist is free, and must be free to ask any question, to doubt any assertion, to seek for any evidence, to correct any errors."

J. Robert Oppenheimer

Abstract

Silicon nanowires (Si NWs) are expected to offer a viable solution for an alternative downscaling of the complementary metal oxide semiconductor (CMOS) circuits beyond Moore's law and for harvesting alternative energy. Because of their quasi one-dimensional structure and tunable semiconducting properties, they are one of the most well researched nano-materials in recent years. Two of the most crucial requirements for using the NWs in real devices are controlled doping and a reliable carrier profiling with a nanoscale resolution. In this work, doping of Si NWs is explored in details. The NWs are grown by molecular beam epitaxy (MBE) with gold as the growth-initiator and doped both in-situ as well as ex-situ. In-situ doping was performed by co-evaporating boron and silicon in the MBE chamber while ex-situ doping was achieved by separately implanting the NWs with boron, phosphorus and arsenic ions. Along with a uniformly doped NW, an intra-NW p-n junction was also fabricated by combining modulated in-situ doping with ion implantation. Scanning electron microscope (SEM) imaging revealed that the NWs are mostly of uniform cylindrical shape implying that the dopant incorporation did not affect the morphology by altering the silicon deposition rate which is often the case in other growth techniques. Transmission electron microscopy (TEM) revealed a single-crystalline structure of the NWs, oriented in the <111> direction. A special investigation was done on the recrystallization of the NWs that were fully amorphized by heavy arsenic ion implantation. It was observed that a sequential annealing comprising of a low temperature (~550°C) first annealing and a high temperature (~950°C) second annealing is required to completely recover the single-crystalline structure of the amorphized NWs. Electrical characterization of individual NWs was performed by two different techniques. By contacting the NWs with a Pt/Ir metal tip fitted to a micro-manipulator inside an SEM, the current-voltage characteristics of the NWs was measured. This provided information about the NW resistivity, the free carrier concentration and the effect of carrier compensation by surface charges. It was observed that in-situ boron doped NWs are heavily depleted by surface charges unless the doping level is above 10^{18} cm^{-3}. In case of implanted NWs, the boron implanted ones showed the expected resistivity indicating 100% electrical activation of the implanted dopant atoms. The phosphorus and arsenic implanted ones, however, showed 1-2 orders of magnitude higher resistivity than expected, indicating low electrical activation and/or dopant deactivation. The p-n junction NWs showed diode characteristics with an ideality factor of around 2 indicating heavy recombination through the surface states. The second electrical characterization was done by scanning spreading resistance microscopy (SSRM) across the radial and axial cross-section of a NW. The measured spreading resistance was duly converted to carrier concentration using an

appropriate calibration with respect to the growth substrate of known carrier concentration. It revealed a significant segregation of electrically active dopant atoms in all cases.

Preface

The prerequisite for any scientific literature that demonstrates a scientific phenomenon is that it must follow a logical sequence. Therefore, this thesis is divided into five chapters that maintain a smooth flow of logic, and are briefly discussed below.

The first chapter, i.e. *Introduction and Literature Review* begins with the background of silicon nanowire (Si NW) based one dimensional electronics and illustrates it with several examples. It briefly discusses the vapor-liquid-solid (VLS) growth of Si NWs and subsequently introduces the topic of doping the NWs which is the central theme of this thesis. Different doping techniques that have been used to dope Si NWs are discussed. The difficulties in controlled doping and reliable dopant profiling are pointed out and they subsequently served as the motivation for this work.

In the second chapter titled *Growth and Doping Techniques for Molecular Beam Epitaxy (MBE)-Grown Silicon Nanowires (Si NWs)*, the physics the growth and characterization techniques used for this work are briefly discussed. It is explained how the Si NW growth by molecular beam epitaxy (MBE) is different from that by chemical vapor deposition (CVD), the most widely used growth technique for Si NWs. It is also explained how in-situ doping is achieved by co-evaporation of silicon and a dopant in the MBE chamber, and how ex-situ doping by implanting the dopants onto the Si NWs is performed. The two different electrical characterizations to asses the doping levels in the Si NWs are briefly discussed next. In the first one, the current-voltage characteristics of the whole NW is measured inside a scanning electron microscope (SEM) by contacting the NW with a micro-manipulator, while in the second one local spreading resistance of a NW is measured by scanning spreading resistance microscopy (SSRM) and it is duly converted to a carrier profile in the NW. In addition, it is also discussed how structural and morphological characterizations of the NWs are to be done by electron microscopy.

After setting up the stage in the first two chapters, the third chapter titled *Experimental Details on Nanowire Growth and Doping* provides the actual experimental data. The key growth parameters including those for control experiments on silicon thin films are provided along with the key doping parameters, both for the case of in-situ and implant doping. For implant doping, an additional step is to activate the dopants by a thermal annealing for which the time and temperature are provided. Some specific details on the sample preparation for transmission electron microscopy (TEM) and electrical characterizations are given and the possible sources of error are mentioned.

The fourth chapter titled *Results and Discussions* elaborates the experimental results followed by relevant discussions. The results are often explained with respect to some of the physical

models available and compared with the results of other groups working in this field. Overall, the results show that Si NWs can be doped both in-situ and ex-situ. However, the electrical properties of the doped NWs are heavily curtailed by the surface states.

The fifth and final chapter titled *Conclusions and Outlook* provides the conclusions drawn from this work. These included the results from which a definite conclusion can be drawn, as well as the results for which there still is no definite explanation. An outlook is also provided that can help the reader understand what will be the next steps to carry forward the knowledge gathered from these investigations.

In addition to the main content, the thesis also contains an Appendix that provides some supporting materials for a better understanding of some of the results. Due to a constrain on space, these materials are included in the Appendix.

Chapter 1

Introduction and Literature Review

1.1 The Background of Nanowire (NW) Based Electronics

The modern age of microelectronics started with the fabrication of the first solid-state transistor by Shockley, Bardeen and Brattain at Bell Laboratories, New Jersey in 1947 which earned them the Nobel Prize in Physics in 1956 [1.1]. Although this transistor was made of germanium, eventually silicon based field effect transistors (FETs) took over due to the superior quality of defect free silicon dioxide that can be easily grown on silicon. In 1967, a new technology known as complementary metal oxide semiconductor (CMOS) [1.2] emerged by combining the existing FETs and led to a drastic reduction of static power dissipation, high noise immunity and above all, an ease of very large scale integration (VLSI). Since the end of 1960s, the evolution of silicon based VLSI technology that is the backbone of today's microelectronics industry has followed an empirical relation [1.3] known as Moore's Law predicted by Gordon Moore, a co-founder of Intel Corp., in 1965. Moore's law states that 'the number of transistors that can be placed inexpensively on a logic circuit has doubled approximately every two years.' Figure 1.1(a) shows the evolution of transistor counts in a microprocessor-chip of personal computers from 1971 to 2010 on a semi-logarithmic scale and they generally follow the Moore's Law.

The international technology roadmap for semiconductors (ITRS) [1.4], a guideline published by the leading semiconductor manufacturers compiling the existing trends in research and development, measures the evolution of CMOS technology in terms of technology nodes. A node, expressed in nanometers, refers to the half-pitch between a set of equally wide, equally spaced lines etched into a dynamic random access memory (DRAM) chip [1.4]. From 2003 to 2009/10, the technology moved on from 90nm to 32nm node. This is depicted in Figure 1.1(b) with the corresponding cross-sections of a metal oxide semiconductor field effect transistor (MOSFET) of that node. Along with the half-pitch, the gate width of a MOSFET also decreased (37nm in 2003 and only 13nm in 2009) in successive nodes as shown in Figure 1.1(b), making the transistors smaller and smaller. It is believed [1.4 - 1.8] that aggressive geometric and equivalent scaling of the MOSFETs will keep Moore's law valid for one more decade (i.e. till 2020). But, eventually scaling will saturate as the device size will reach the atomic/molecular scale. However, even before hitting the atomic scale, dealing with the thermal effects can be challenging itself [1.4 – 1.8]. One of the possible solutions in order to overcome the roadblocks

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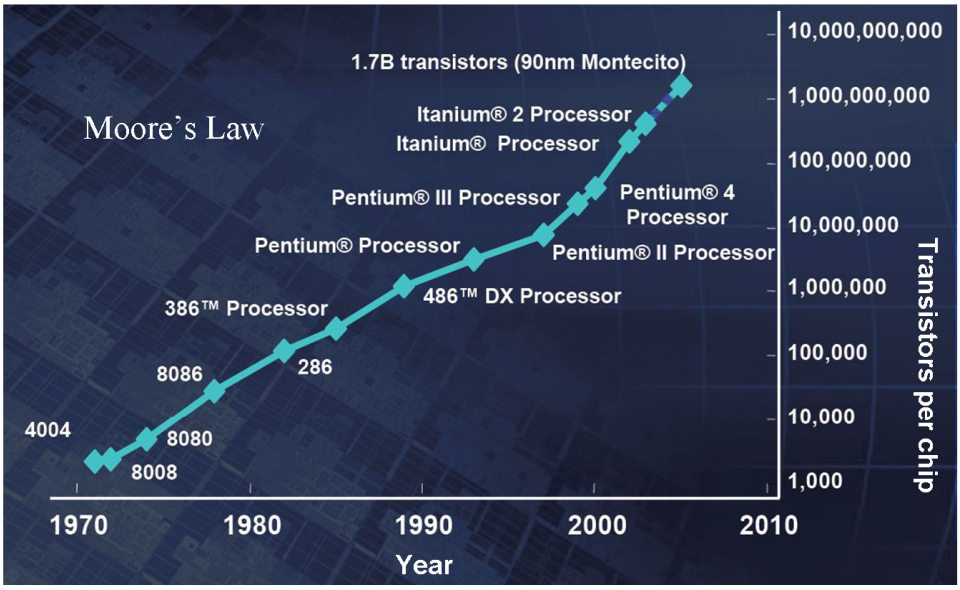

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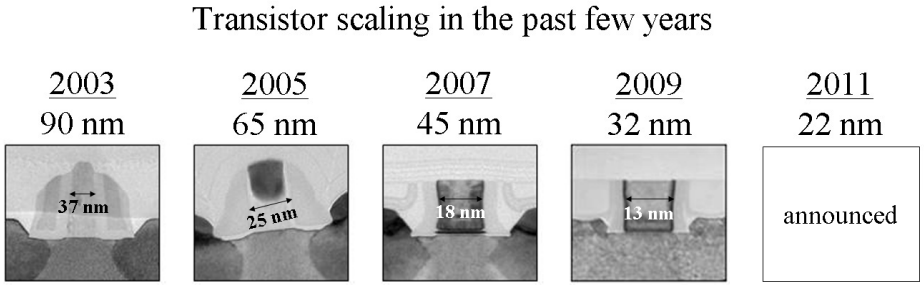

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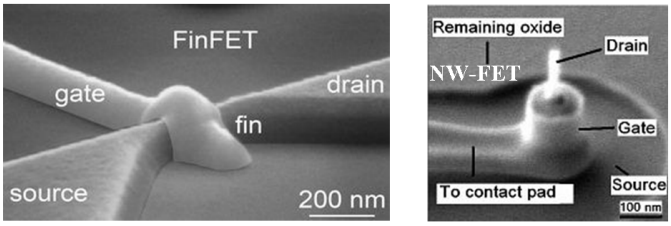

Figure 1.1 (a) Moore's law for microprocessors of personal computers plotted on a semi-logarithmic scale. (Reprinted from Ref. 1.7) (b) Scaling of the MOSFET from 2003 to 2011 with the corresponding cross-sectional transmission electron microscopy (TEM) image. It can be seen from the images that the gate width decreased from 37nm in 2003 to 13nm in 2009. (Reprinted from Ref. 1.7) (c) Scanning electron microscope (SEM) images of future three-dimensional MOSFETs, i.e. a FinFET (Reprinted from Ref. 1.9) and a nanowire (NW)-FET (Reprinted from Ref. 1.10)

on transistor scaling is to change the architecture of the MOSFET itself, i.e. to make it vertical rather than horizontal [1.4 - 1.8] as shown in Figure 1.1(c). Both the MOSFETs shown in Figure 1.1(c) use a vertical nanostructure, an etched Fin and a grown nanowire (NW) respectively, where the current conduction channel is formed. Figure 1.2 illustrates the difference between a planar MOSFET (Figure 1.2(a)) and a vertical nanowire-FET (NW-FET) (Figure 1.2(b)) such as the one shown in Figure 1.1(c). In case of the NW-FET, the gate wraps all around the cylindrical NW which allows a better electrostatic control of the gate potential [1.8] on the electrons in the channel formed in the NW (see Figure 1.2(b)) as compared to the planar MOSFET (see Figure 1.2(a)). This reduces the short-channel effects [1.11] which are the cause of rapid heating up of the planar MOSFETs as their dimensions reduce.

In addition, theoretical calculations showed [1.12 – 1.14] that it is possible to observe new phenomena like quantum confinement of electrons and to engineer the band gap of elemental semiconductor like silicon in nanostructures once their lateral dimension is reduced below their corresponding Bohr radius. The Bohr radius of silicon is around 5 nm. The task for the experimental materials scientists and device physicists is to exploit these new properties to break the barriers set by the fundamental limits on VLSI scaling.

From another perspective, there has been a surge in the effort to find alternative energy resources given the fact that earth's reserve of fossil-fuel is going to run out within a few decades. A plethora of alternative techniques have emerged [1.15, 1.16] to generate 'clean' electricity from non-fossil fuels. Out of them, solar and thermoelectric power generations are particularly promising. However, when compared with the fossil-fuels, the unit cost for these alternative energy generations is astronomical, especially for solar cells (1 - 4 US cents/kWh for coal as compared to 25 – 50 US cents/kWh for solar cells [1.16]). This is primarily because silicon, the starting material for solar cells, is still quite expensive. Recently, theoretical calculations have shown [1.17, 1.18] that an array of silicon NWs with a core-shell p-n junction can provide higher efficiency for conversion of solar energy to electricity than planar silicon. This is schematically shown in Figure 1.3 for a core-shell Si NW array grown on a cheap transparent substrate and contacted with a transparent electrode. The radial junction between the core and shell offers a much shorter charge carrier collection path that should lead to a much higher carrier collection efficiency compared to planar silicon. Parallely, it has also been predicted [1.19] that efficient thermoelectric power generators can be built by assembling arrays of p- and n-type NWs. Since the nanostructures use only a tiny fraction of material, the production cost for these nano-power- generators can be drastically reduced. This opens up the opportunities to develop Si NWs for 'greentech' applications.

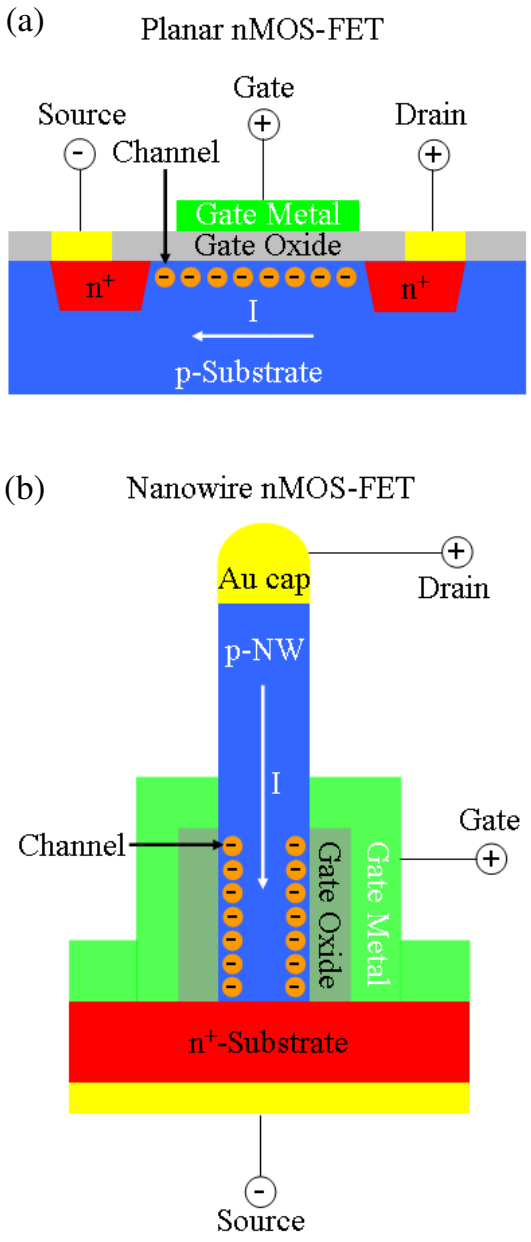

Figure 1.2 (a) Scheme of a planar MOSFET with a horizontal flow of current through the electron channel. (b) Scheme of a vertical wrap-gated NW-FET with a vertical flow of current through the electron conduction channel

The principal approach of VLSI fabrication is the 'top-down' approach. In this approach, small features (up to tens of nm) are patterned on a substrate by different processing steps involving

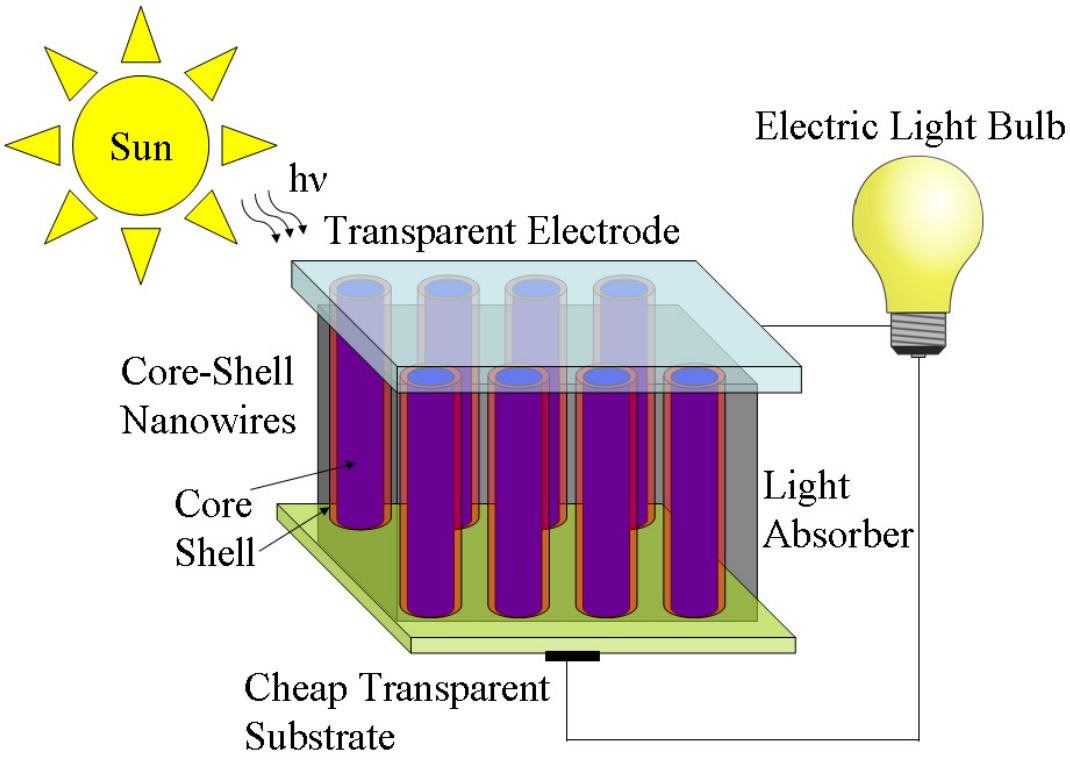

Figure 1.3 Scheme of a core-shell p-n junction Si NW array formed on a cheap transparent substrate and contacted with a transparent electrode to harvest solar energy.

lithography, etching and material deposition [1.20]. Most of the processes used in the sequence of fabrications are self-aligned so that it is easy to build up an IC by interconnecting the patterned building blocks, i.e. the devices. The top-down approach has been well-exploited since 1990s [1.21, 1.22] to fabricate vertical NWs. It is worth noting that Tada et al. [1.21] already achieved sub-10nm diameters in the NWs way back in 1998. Recently, metal assisted chemical etching of patterned or masked silicon wafers [1.23], and deep reactive ion etching [1.24] have been used successfully to form large area arrays of Si NWs. These etched Si NWs are particularly interesting for applications in solar cells because of their superior light absorption capability [1.25 – 1.28] compared to Si wafers. Technologically they are also easy to process and are fully compatible with the VLSI technology. However, it has been observed that the etching process used to fabricate these NWs often introduce unwanted structural changes in them such as porosity and roughness [1.23, 1.29] which can adversely affect the electrical transport properties of them [1.23, 1.29].

An alternative approach to form nanostructures in general and NWs in particular is the 'bottom-up' growth [1.30]. In nanotechnology, bottom-up approach means growing zero or one/quasi-

one dimensional nanostructures from solid/gaseous materials on a solid substrate. In successive steps, the bottom-up grown nanostructures can be processed to form a single electronic device, and even can be assembled to form an integrated circuit. A hierarchical structure of bottom-up electronics with NWs is outlined in Figure 1.4. As indicated in the scheme, along with technological benefits, studying bottom-up grown NWs will also strengthen the basic understanding of solid-state physics.

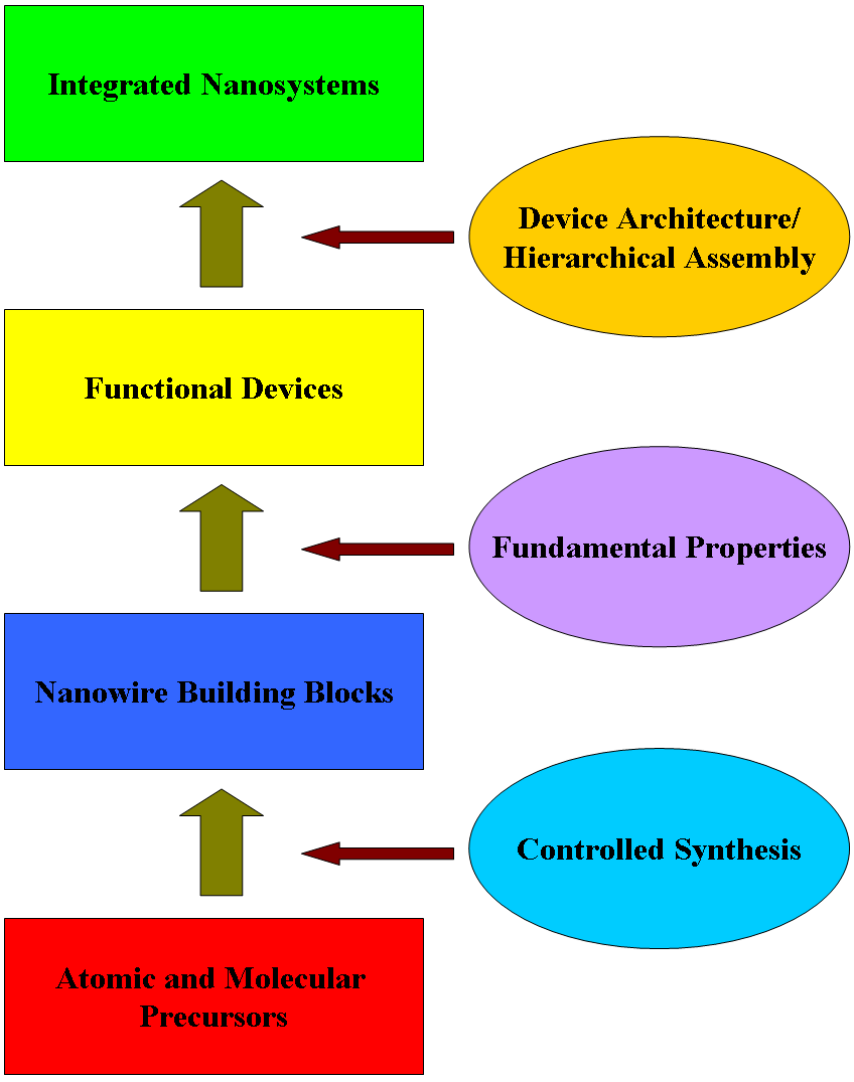

Figure 1.4 A schematic outlining key challenges (rectangles) and specific research areas (ellipses) required to enable the bottom-up approach to functional nanosystems with NWs (adapted from Ref. 1.30)

Interestingly, the first bottom-up growth of Si NWs, referred as whiskers at that time, was observed in 1964 by R. S. Wagner and W. C. Ellis [1.31] at Bell Laboratories, a year before Moore's prophetic law was formulated. However, it did not take the center stage in the materials science research until the end of 1990s when efforts to go 'beyond Moore' gathered momentum. Another important bottom-up grown nanostructure that entered the scene in the 1990s is carbon nanotube (CNT) [1.32]. Both CNT and Si NWs are being projected as 'emerging materials for 'emerging devices' by ITRS since 2005 [1.4]. However, one of the limiting factors for CNTs to be used in real devices is that the same batch of fabrication may contain metallic as well as semiconducting NTs [1.32], which is a heavy compromise with the reliability when it comes to large scale manufacturing. On the other hand, Si NWs can be grown with controlled semiconducting properties [1.30, 1.33 – 1.36], and can easily fit into the hierarchy of device (such as wrap-gated FETs illustrated in Figure 1.2(b)) and circuit fabrication. The NWs are generally cylindrical structures of diameter less than 200nm, and length from several hundred nms to a few microns, although occasionally even millimeter long NWs have been reported [1.37]. This essentially makes them quasi-one dimensional with a high surface to volume ratio. Surface studies of small dimensional Si NWs by scanning tunneling spectroscopy (STS) have already shown evidences of quantum confinement [1.38] which was theoretically predicted before [1.12 – 1.14].

In short, Si NWs are technologically important nanostructures that can offer solutions for post-CMOS microelectronics and cheap, sustainable alternative energy generation, as well as enable observation of intriguing physical phenomena in quasi-one dimension. Therefore, it is worth investigating them in details.

1.2 The Vapor-Liquid-Solid (VLS) Growth of Si NWs

The principal mechanism by which the bottom-up growth of Si NWs proceeds is called the vapor-liquid-solid (VLS) mechanism [1.31, 1.39, 1.40]. Generally a metal is pre-deposited on the growth substrate to catalyze or initiate the growth once the supply of Si in solid or gaseous form starts inside the growth chamber. This metal is most often gold, but can also be Al, Pt, Ni, Pd etc. [1.35]. The basics of the VLS growth are briefly explained with the scheme in Figure 1.5. For the Au-Si phase diagram (see Figure A1.1 in Appendix 1) the Eutectic point is at 363°C at around 19% atomic percentage of Si. When a thin film of Au is deposited on a Si substrate (Figure 1.5(a)), and subsequently the substrate is heated up beyond 363°C, the Au film breaks up into Au/Si Eutectic droplets (loosely referred as Au droplets as well) as shown in Figure 1.5(b). Generally this droplet exists in liquid form, however there are debates over it [1.35]. Since they form on a Si substrate, the composition of the droplets is given by the right hand side

of the liquidus curve of the Au-Si phase diagram (see Figure A1.1 in Appendix 1), i.e. it is Si-rich. When additional Si is supplied in gaseous form (Figure 1.5(c)), i.e. through a precursor gas such as silane (SiH_4) in a chemical vapor deposition (CVD) chamber, the gas preferentially cracks at the droplet rather than at the Si substrate surface due to lower activation energy at the former (19 kcal/mol vs 35 kcal/mol [1.35]). This subsequently increases the Si concentration in the droplet pushing the phase equilibrium further

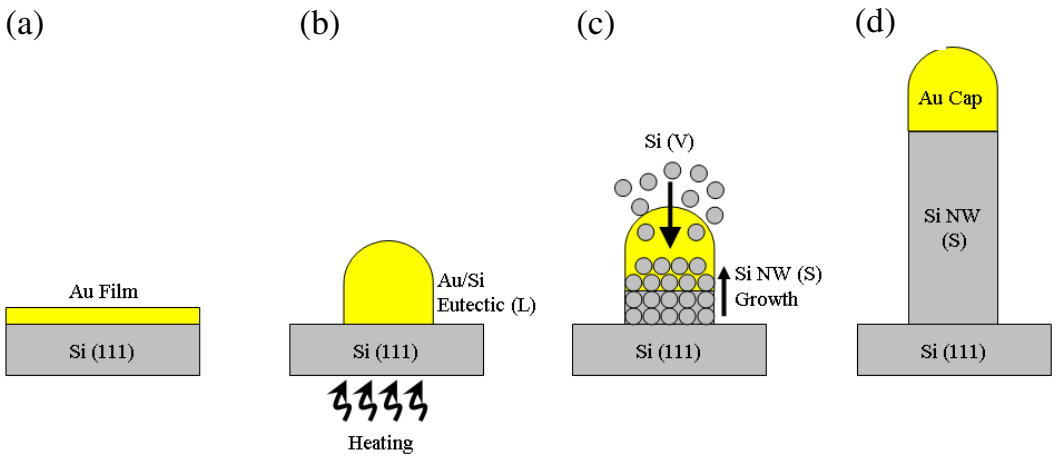

Figure 1.5 Different phases of NW growth by the VLS process. (a) Au film deposition on Si (111) substrate. (b) Heating up the substrate and subsequent formation of liquid (L) Au/Si Eutectic droplets. (c) Deposition of Si vapor (V) and growth of a solid (S) Si NW. (d) A post-growth of Si NW capped with solidified Au that initiated the NW growth.

to the right hand side of the phase diagram. When the liquid droplet is supersaturated with Si, pure Si precipitates as a solid underneath the droplet (Figure 1.5(c)) in the form of a Si NW. The growth is terminated by stopping the silicon supply resulting in a cylindrical Si NW with a gold cap on top (Figure 1.5(d)). The justification of the name VLS comes from the fact that the supplied Si exists in vapor phase, the Au droplet exists in liquid phase and the resulting Si NW exists in solid phase. A comprehensive review of VLS growth can be found in Refs. 1.33 – 1.36. Two of the important aspects of VLS-grown Si NWs, i.e. diameter and crystal orientation, are briefly discussed here.

The diameter of a VLS-grown NW depends on three factors – 1) the size of the Au droplet that catalyzes the growth, 2) the growth temperature that determines the solubility of Si in Au and hence the supersaturation and 3) the vapor pressure of the precursor gas. From thermodynamics, the minimum diameter of a NW can be predicted as [1.30]

$$d_{min} = \frac{4\sigma_{LV}V_L}{RT\ln\sigma} \qquad [1.1]$$

where σ_{LV} is the liquid-vapor surface free energy, V_L is the molar volume of the liquid, σ is the vapor phase supersaturation, R is the gas constant and T is the temperature. The smallest diameter reported for VLS-grown Si NWs is around 3nm [1.30]. It must be mentioned that the diameter distribution of Si NWs for a growth experiment may not exactly correlate to that of the original Au droplets because of Ostwald ripening [1.41], i.e. the coalescence of smaller Au droplets into bigger ones to minimize the surface energy. Thus, the original Au droplet distribution gets modified. In case of classic VLS growth [1.33 – 1.36], the NW growth velocity is determined by the rate of incorporation of Si into the liquid Au droplet and this is inversely proportional to the NW diameter with a negative slope. This implies that for a given growth time, NWs of smaller diameter are shorter than those of larger diameter.

The VLS-grown NWs are generally single-crystalline and free of extended defects like dislocations or stacking faults. Schmidt et al. [1.42] observed and argued that for larger diameter (>20nm), the preferential crystal orientation is <111> as it offers the lowest interface energy between the Au droplet and the solid NW, and for smaller diameter NW (<20nm), the preferential crystal orientation is <110> which offers the lowest surface energy. Therefore, use of a Si (111) wafer leads to an epitaxial growth of Si NWs in most cases.

The first Si NWs were grown by CVD [1.31] and the classical VLS growth model as explained above is essentially based on CVD growth. Since then a variety of techniques such as laser ablation [1.43], super-critical solution [1.44], silicon monoxide evaporation [1.45], and molecular beam epitaxy (MBE) [1.46 – 1.50] have been used to grow Si NWs.

In conclusion, VLS growth of Si NWs results in single crystalline NWs with a range of diameter distribution depending on the size of the growth catalyst droplet, temperature and vapor pressure of the precursor gas.

1.3 Doping Si NWs

Doping in semiconductor technology refers to the process of introducing foreign atoms [1.20, 1.51, 1.52] into the substitutional lattice sites in a semiconductor, and subsequently modifying its electrical properties of the host semiconductor. Dopant atoms known as acceptor or p-type dopant, accept an extra electron each from a single host atom while dopant atoms known as donors or n-type dopant, donate an extra electron each to a single host atom. This is schematically illustrated in Figure 1.6.

For a Group IV element of the periodic table like silicon, common p-type dopants are boron (B) and gallium (Ga), and common n-type dopants are phosphorus (P), arsenic (As) and antimony

(Sb). So, a B atom in a Si lattice accepts an electron from a Si atom, thus reducing the number of electrons or increasing the number 'holes' (see Figure 1.6(a)) that act as the majority charge carriers. On the other hand, a P atom in the Si lattice creates excess electrons (see Figure 1.6(b)) which serve as the majority carriers.

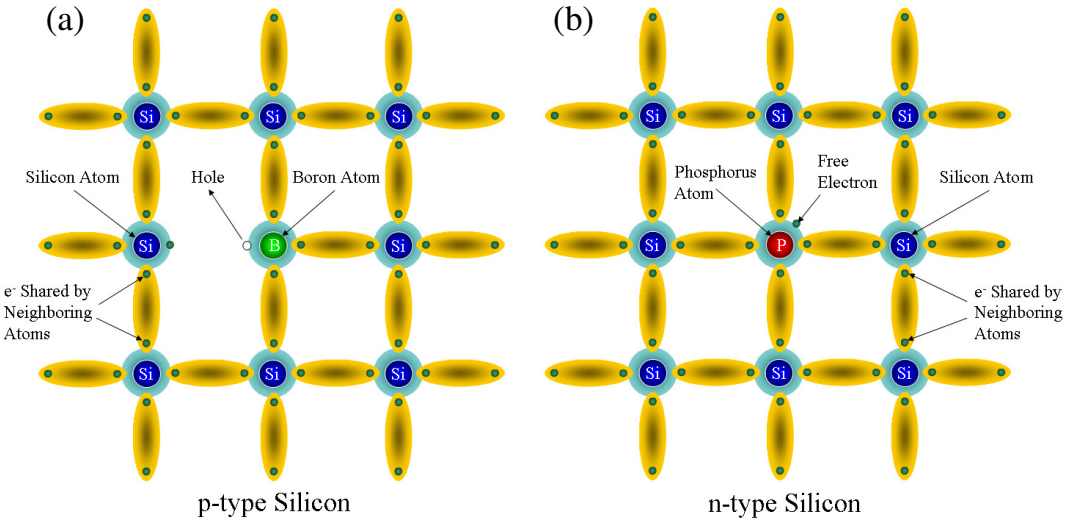

Figure 1.6 Schematics of cross-sections of doped silicon lattices. (a) B-doped p-type silicon with an extra hole (b) P-doped n-type silicon with an extra electron

Controlled doping of silicon is an essential part of device fabrication as the doped silicon forms the active region of the devices where the generation of electrons or holes takes place [1.20, 1.51, 1.52]. In terms of energy band diagram [1.51, 1.52], a p-type dopant lowers the Fermi level (E_i) of an intrinsic or pure Si moving it close to the valence band (E_V) and thus lowering the energy barrier for the holes to contribute to electrical conductivity, while an n-type dopant shifts the Fermi level upward moving it closer to the conduction band (E_C), thus lowering the barrier for electrons. This is illustrated in Figure 1.7(a) where E_{Fp} and E_{Fn} refer to the Fermi levels for p-type and n-type silicon respectively, and $e\chi$ refers to the electron affinity of silicon. When a p-Si is metallurgically joined to an n-Si, a p-n junction is formed (see Figure 1.7(b)) which constitutes the basic building block for most of the microelectronic devices [1.51, 1.52]. The diffusion of the majority charge carriers (electrons in n-type Si, holes in p-type Si) across the junction establishes a built-in electric field (E) that results in a built-in potential ($e\varphi_i$) against further flow of charges (see Figure 1.7(b)). Only upon application of an external bias against the built-in potential, the charge carriers can drift across the junction, and thus allow a unidirectional current flow. This way a current rectification is achieved.

Generally dopants are introduced into Si either in-situ, i.e. during growth, or ex-situ, i.e. post growth [1.20]. In case of Si NWs, doping has mostly been done in-situ [1.53 – 1.62] due to the relative ease of process control. However, ex-situ doping has also been demonstrated [1.63 – 1.68]. In-situ doping of Si NW in connection with VLS growth requires supply of the dopants in gaseous or solid form along with silicon. In case of CVD, the most prevalent VLS growth

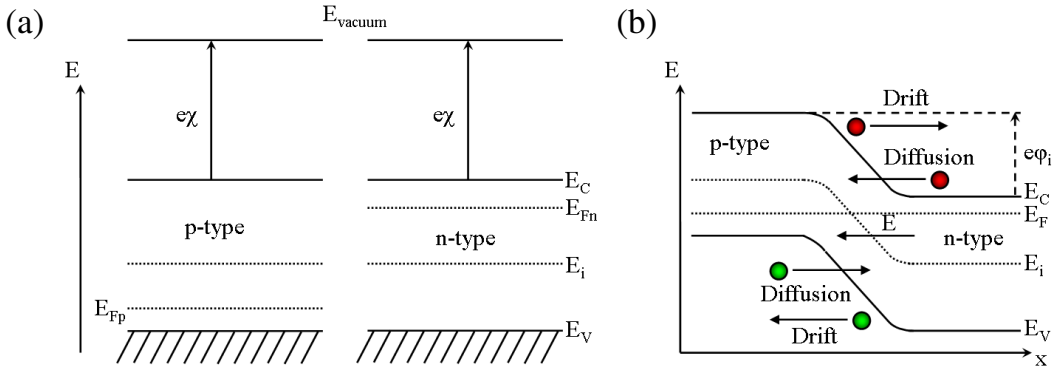

Figure 1.7 Energy band diagram of (a) a p-type (left) and an n-type (right) Si. E_{Fp} and E_{Fn} refer to the Fermi levels of the p-Si and n-Si respectively, eχ the electron affinity of Si (b) Scheme of a p-n junction joining the p- and n-type Si together. The red circles are electrons and green circles are holes. E_{Fp} and E_{Fn} align to form E_F across the junction. As a result a built-in electric field (E) is created forming a built-in potential barrier ($e\varphi_i$) against further flow of charge carriers.

technique, this is achieved by introducing a precursor gas containing the dopant element. For p-doping with boron, diborane (B_2H_6) is most commonly used [1.53, 1.57 – 1.60]. For n-doping with phosphorus, phosphine (PH_3) [1.53 – 1.56] and n-doping with arsenic, arsine (AsH_3) [1.56] have been used. It should be noted that all of these precursor gases are highly toxic. The dopant concentration in the NW which determines its resistivity is modulated by the ratio of the precursor gas for the dopant and silane. Schmid et al. [1.56, 1.57] have shown that for phosphine, the resistivity of the doped NW is inversely proportional to the ratio of phosphine and silane. However, as the ratio is increased, the density of NWs reduces, and beyond a ratio of 0.02 the NW nucleation stops completely [1.56].

Ex-situ doping of Si NWs has been demonstrated by ion implantation [1.63 – 1.66] which is by far the most favored doping process for VLSI technology, and by in-diffusion of spin-on-dopants [1.67, 1.68]. However, ex-situ doping is not as profoundly investigated as the in-situ one.

Overall, doping has worked on Si NWs and allowed certain degree of control over their electrical properties which is discussed in Section 1.4.

1.4 Dopant Profiling and Doping Mechanism in Si NWs

Although doping of Si NWs was first demonstrated in early 2000s [1.53], the exact dopant incorporation mechanism was not clear. A fundamental understanding of the doping process from an atomistic point of view is essential if the NWs are to be used in real devices where a positioning of the dopant atoms is critical.

For planar silicon structures and devices, there are a number of characterization techniques available to chemically map the dopants as well as to electrically profile them along the depth [1.69]. As a result, an atomic concentration profile of the total number of dopants as well as the number of electrically active dopants can be independently measured and compared. This helps to understand how the physical processes that are responsible for doping, such as diffusion, adsorption, interaction between dopants and defects etc are influenced by experimental parameters such as temperature, vapor pressure of the precursor gases, parameters of dopant implantation etc. However, these techniques, designed for two-dimensional structures, can not be directly applied to measure the atomic profiles of dopants in a single NW, primarily because of the nanoscale lateral dimension of the NWs. Neither is high resolution transmission electron microscopy (HRTEM) that allows visualization of the Si lattice with an atomic resolution, sensitive enough to identify the dopant atoms. Therefore, either new characterization techniques are to be invented or the NWs are to be prepared in special ways so that the conventional techniques can be applied to them.

The most direct technique to profile a NW atom by atom is atom probe tomography (APT) [1.70] wherein atoms are evaporated from the tip of a single NW with laser pulses and subsequently detected by a position-sensitive detector. Atoms of each element present can be mapped provided the concentration is above a certain threshold (~$10^{18}$$cm^{-3}$ [1.70]). From the two dimensional mappings of the detected atoms, a three-dimensional reconstruction of the NW can be done with near atomic resolution. This was successfully applied by Perea et al. [1.71] on phosphorus-doped Ge NWs. It was observed that phosphorus, which was introduced into the NWs in-situ by cracking PH_3 was mostly concentrated in a shell as shown in Figure 1.8. They suggested that phosphorus incorporates into the NW via two different pathways at two different rates [1.71 - 1.73]. The first incorporation which proceeds at a faster rate is through the sidewalls via a vapor-solid (VS) mechanism. The VS mechanism results from preferential cracking and subsequent adsorption of the dopants on the sidewalls of the growing NW without involving the liquid catalyst droplet. The slower second incorporation is via the classical VLS

mechanism through the Ge-Si liquid droplet on top. The faster incorporation through VS is also thought to be responsible for the heavily tapered shape of the NW, i. e gradual change of the NW diameter from tip to base. Although the investigation was done with doped Ge NWs,

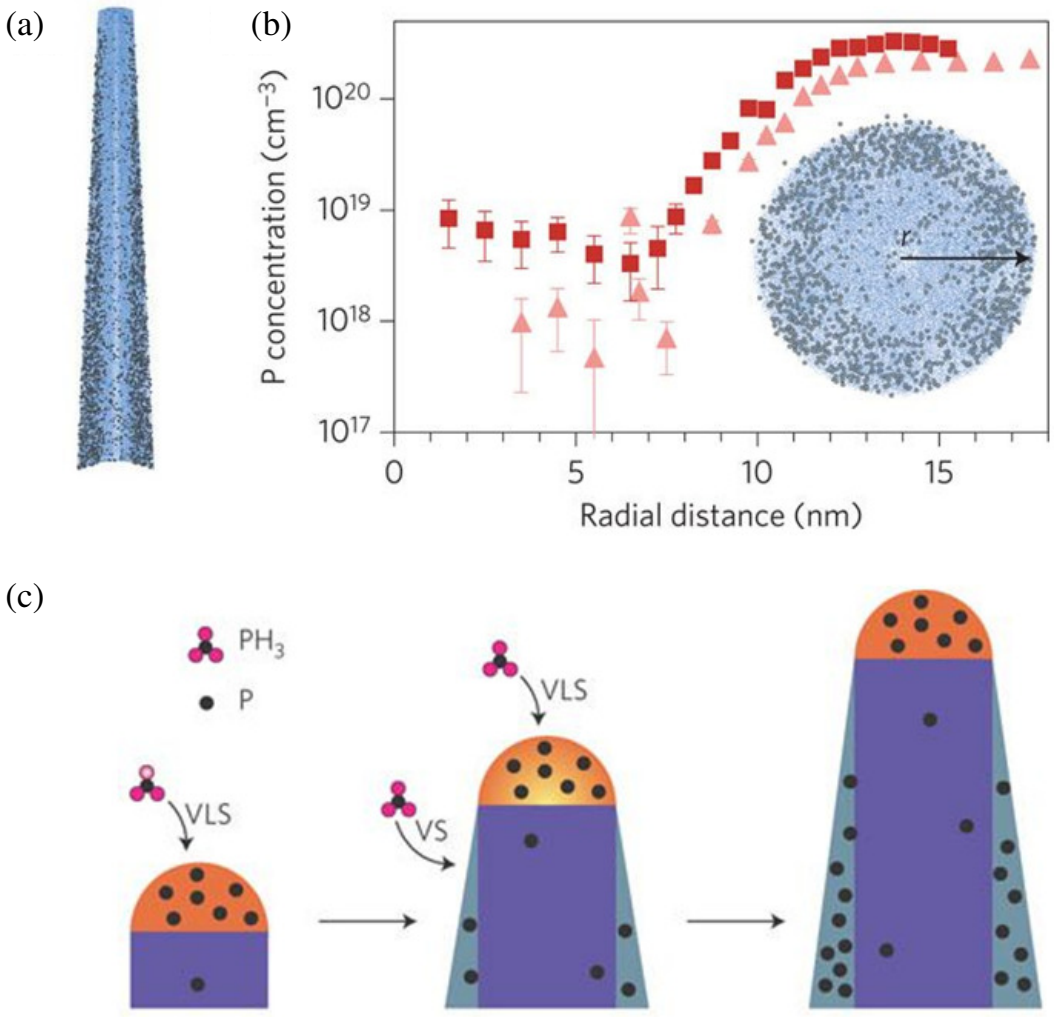

Figure 1.8 Dopant (P) profile in a Ge NW measured by atom probe tomography. (a) Axial profile (b) Radial plot of P concentration for Ge NWs grown at 380°C and PH_3 : GeH_4 ratios of 1 : 1,000 (triangles) and 1 : 500 (squares) with the inset showing the radial profile. The black dots refer to the P atoms. (both reprinted from Ref. 1.71) (c) The two different dopant incorporation pathways into the NW – by cracking of PH_3 at the Au-Ge droplet on top an thus incorporating via Vapor-Liquid-Solid (VLS) mechanism and by cracking at the NW surface leading to uncatalyzed incorporation via Vapor-Solid (VS) mechanism. (Reprinted from Ref. 1.71 and 1.72)

the doping mechanism can be generalized to in-situ doping of NWs as similar conclusions were drawn from different doped NWs as well [1.73].

This technique, however, did not shed any light on what percentage of the total number of dopants were electrically active, i.e. contributed to electrical conduction. It was theoretically calculated by a few workers [1.74, 1.75] that significant surface segregation of the dopants will take place if the NW surface is unpassivated, i.e. if there exists a native silicon oxide at the outer surface of the NW. This Si-oxide interface generally is a sink of broken or in other words dangling bonds that serve as charge traps, i.e. they trap carriers from the volume of the NW rendering them immobile. Schmidt et al. [1.76] have calculated the diameter dependence of this surface depletion and Seo et al. [1.77] have experimentally determined the density of surface states. It was also calculated by Diarra et al. [1.78] that the activation energy of the dopants in the volume of the NW is modified by the mismatch between the dielectric inside (Si) and outside (vacuum) of the NW. As the diameter of the NW decreases the activation energy increases implying that 100% of the dopant atoms may not be electrically active in small diameter NWs. They estimated that for a NW of diameter 15nm, only 50% of the dopants will be electrically active at room temperature. This was indeed manifested in the experimental results obtained by Björk et al. [1.79].

In order to correlate these phenomena more atomistically, Schlitz et al. [1.80] tried to connect the dopant profiles measured by APT with that of the measured carrier concentration by current-voltage measurements. However, the samples for APT and for electrical measurements were of different compositions which may compromise with the reliability. Xie et al. [1.81] have used a sequence of low temperature chemical oxidation and subsequent etching of n-type Ge NWs to sequentially reduce the NW diameter. They measured the electrical transport across the length for each diameter, and observed that as the diameter is reduced the transport mechanism shifts from bulk-like to surface-like, i.e. for small diameter the active dopants reside mostly on the NW surface. Koren et al. [1.82] have reported non-uniform axial and radial doping in n-type Si NW using Kelvin probe force microscopy and scanning photocurrent microscopy. Garnett et al. [1.83] have reported profiles of active boron in Si NWs by capacitance-voltage measurement by fabricating an omega-gated NW FET and observed strong surface segregation of the active dopants as well. Using modulation-doped NWs, Imamura et al. [1.84] have investigated axial doping profiles by Raman microscopy and Hertog et al. [1.85] have investigated the same using off-axis electron holography.

In general, all of the experimental works agree with the theoretical calculations, i.e. a heavy surface segregation of dopants. However, at the same time all of these techniques are indirect and require extensive sample preparation and ultra-sophisticated tools. A direct, easier and more

controllable mapping of the NW conductivity in connection with the active dopant profile is lacking in the literature.

1.5 Devices with Doped Si NWs

As mentioned before, in addition to uniformly doped NWs that merely act as resistors, p-n junction NWs have also been demonstrated, either by in-situ switching of the dopant sources [1.86 – 1.91] or by implanting a NW successively with p and n-dopants [1.66]. Both axial and radial junctions have been realized, and they often performed as nano-solar cells [1.88 – 1.91]. The in-situ axial junction is formed by changing the precursor gas for dopants, e.g. from diborane to phosphine, while the radial junction is formed by modulating the growth temperature and pressure during dopant deposition, i.e. first the p-Si core is grown at a lower temperature and higher pressure and subsequently the n-Si shell is deposited at higher temperature and lower pressure. A radial p-i-n junction NW working as a solar cell is demonstrated in Figure 1.9. The NW was selectively etched to expose the p-core at one side in order to form metal contact to it (see Figure 1.9). The efficiency of this NW solar cell was 3.4% [1.92].

As in the case of the NW in Figure 1.9, for device fabrication, NWs are generally removed from the growth substrate and placed on an insulating substrate. Metal electrodes are formed lithographically to make contacts to the NWs and to measure their electrical properties subsequently.

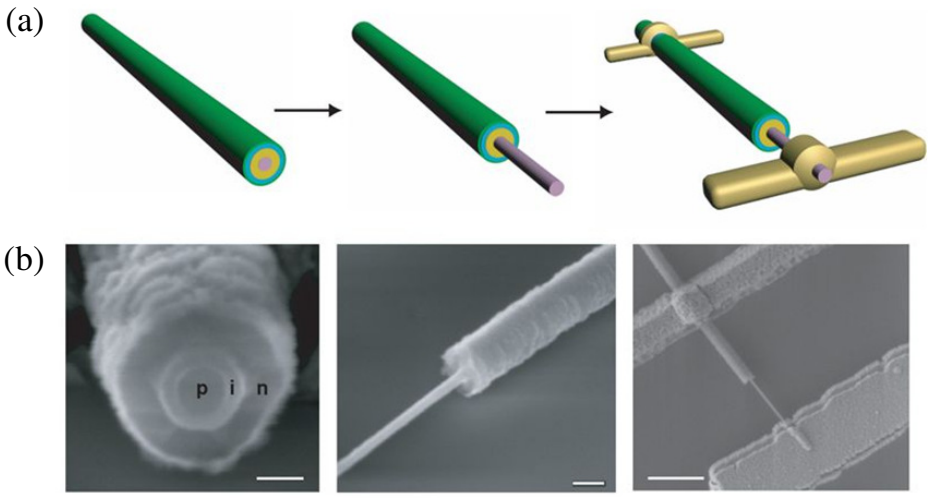

Figure 1.9 (a) Schematic and (b) SEM images of an as-grown coaxial p-i-n Si NW and the subsequent solar cell formed by individually contacting the core and the shell (both reprinted from Ref. 1.92)

Two metal electrodes at the two ends of a NW enable a two-probe current-voltage measurement [1.69] from where the NW resistivity can be calculated. Resistivity in turn depends on carrier concentration and mobility both of which change with doping [1.51, 1.52]. Therefore, an efficient technique often used is fabrication of an FET [1.30]. The areas of the NW directly under the contacts serve as the source and drain respectively, while the channel of the FET is formed in the segment of the NW which is in between the contacts. The insulating layer (most often SiO_2) underneath the NW serves as the gate dielectric and the substrate (most often a highly doped Si wafer) as the back gate. This is illustrated in Figure 1.10(a) and (b) with a scheme and a scanning electron microscope (SEM) image of an actual device. Figure 1.10(a) and (b) actually show four contacts on top of the NW for a four-probe measurement which explicitly removes any influence from the contact resistance [1.69]. From the gate-controlled current-voltage measurements of the NW device, mobility can be extracted [1.52] which in turn can be substituted to calculate the carrier concentration from the measured resistance.

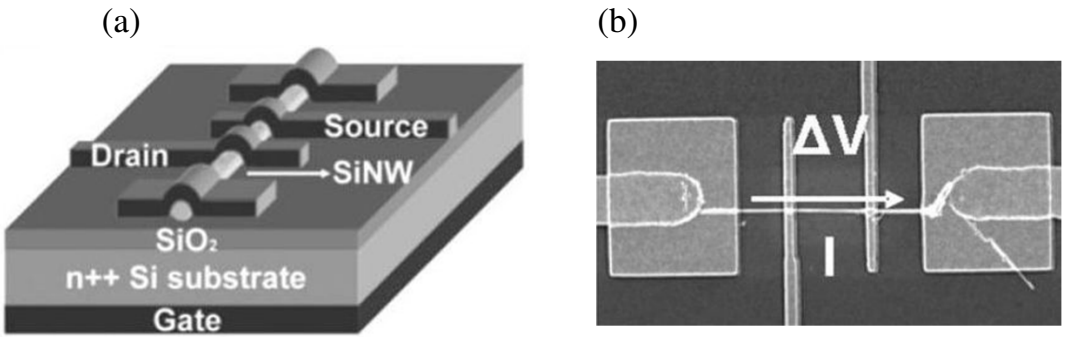

Figure 1.10 (a) Scheme of a B-doped Si NW laid down on thermally grown SiO_2 on a highly doped (n^+) Si substrate, and contacted with metal electrodes. The device constitutes an FET with the channel forming in the segment of the NW in between the contacts, and the segments directly under the contacts serving as source and drain. SiO_2 works as the gate dielectric and the n^+ substrate as the back gate. Four contacts are formed in order to measure resistivity directly by the four-probe method [1.69] (b) An SEM image of the actual device. (Both reprinted from Ref. 1.58)

In addition, wrap-gated vertical NW FETs have been fabricated (see Figure 1.1(c)) by different groups [1.10, 1.93, 1.94]. Even more hierarchical circuits such as logic gates were demonstrated [1.95] using Si NWs as building blocks. Figure 1.11 shows an OR gate built by crossing two p-type NWs with an n-type NW. The two p-type NWs form a p-n junction each at the crossing point with the n-type NW (see Figure 1.10(a)). They are connected in parallel as shown in the scheme of Figure 1.11(a) and form the diode-diode logic [1.95]. The input-output characteristic

is shown in Figure 1.11(b) and the experimental truth table in Figure 1.11(c). They clearly show the operation of an OR gate.

Apart from these, a host of other devices including label free DNA sensors [1.96] and large area thin film transistor [1.97] were fabricated with Si NWs. It has also been shown [1.98, 1.99] that Si NWs indeed possess superior thermoelectric properties compared to bulk silicon, and hence can be used to manufacture nanoscale thermoelectric generators.

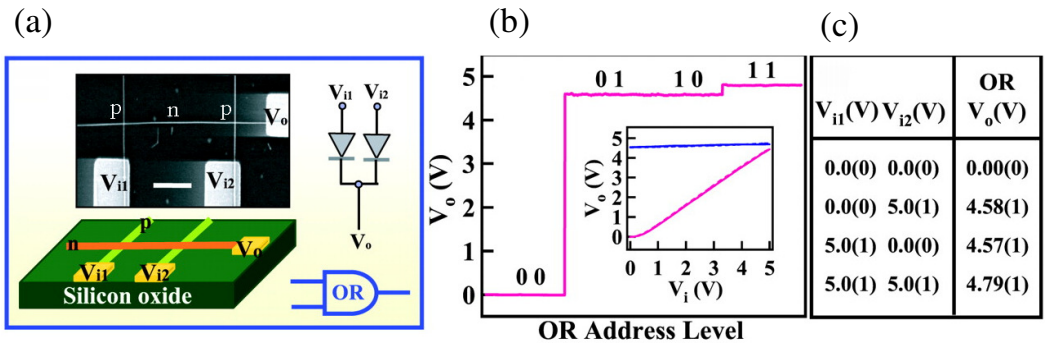

Figure 1.11 Logic gates with crossed NWs. (a) SEM image and schematic of a diode-diode OR logic gate created by crossing an n-type NW with two p-type NWs. V_{i1}, V_{i2} are input voltages and V_o is the output voltage. The scale bar is 1μm. (b) The output-input characteristics for four different input levels. The two input voltages (V_{i1} and V_{i2}) can be HIGH (5V or logic 1) or LOW (0V or logic 0) resulting in either HIGH or LOW output (V_o). Inset shows the output-input (V_o-V_i) relation. The red (blue) lines show V_o-V_{i1} and V_o-V_{i2} when the other input is 0 (1). (c) The experimental truth table for this NW based diode-diode logic gate which shows that it performs the OR operation. (All reprinted from Ref. 1.95)

A comprehensive review of Si NW based devices can be found in Ref. 1.100 – 1.102. Generally speaking, it has been shown that Si NW based devices can perform all the basic electronic operations, and can even be scaled up to form ICs.

1.6 Motivation of this Work

It is clear from the literature review presented above that a significant work has been done on Si NWs in recent years (more than 700 papers on Si NWs published only in 2008 [1.35]). However, there still are open questions on controlled doping and dopant profiling in individual NWs as both of them are technically challenging. The lack of control in in-situ doping in CVD can be seen in the change of morphology [1.58 – 1.60, 1.71, 1.103], and sometimes crystallinity [1.58 - 1.60, 1.103] in case of boron doping of Si or Ge NWs. As mentioned earlier, the precursor gas for the dopant increases the rate of VS growth on the NW sidewalls leading to a significant

tapering of the NW. In case of boron doping with B_2H_6 it often leads to deposition of amorphous Si around a crystalline Si core. These are illustrated with electron microscope images in Figure 1.12(a) and (b).

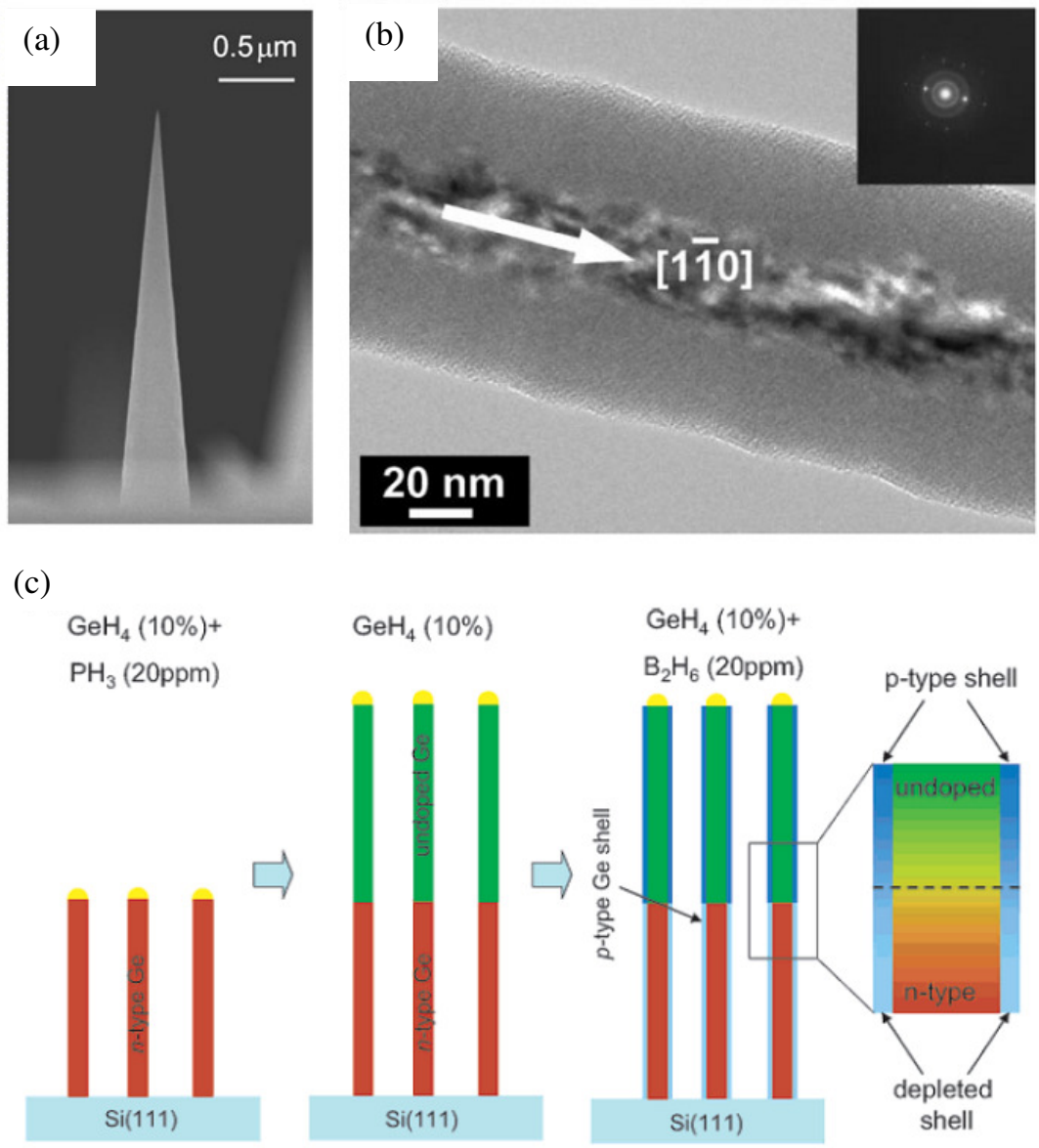

Figure 1.12 (a) SEM image of an extremely tapered Ge NW in-situ doped with diborane (B_2H_6) in CVD. (Reprinted from Ref. 1.103) (b) TEM image of a Si NW in-situ doped with diborane (B_2H_6) in CVD showing an amorphous shell and a crystalline core type structure. (Reprinted from Ref. 1.58) (c) Scheme of an axial NW p-n junction with radial junctions formed by dopant depositions on the sidewalls during growth and in-situ doping. (Reprinted from Ref. 1.105)

Another limitation of pure in-situ doping of CVD-grown NWs is in the formation of a sharp axial p-n junction by simply switching the dopant sources. It has been shown by Li et al. [1.104] with simulations that a long transition region exists between the two different kind of dopants even if the switching is 'abrupt'. They suggested that the transition length is inherently related to the residual first dopant atoms stored in the liquid Au droplet at the onset of introducing the second dopant. Pure in-situ doping of NWs in CVD has also led to unwanted lateral deposition of dopants [1.105] which is detrimental to the formation of an axial p-n junction in a NW (see Figure 1.12(c)). On the other hand, formation of an axial p-n junction purely by ion implantation as demonstrated by Hoffmann et al. [1.66] suffers from the problem that co-diffusion of acceptors and donors during annealing after such dual implantations often lead to the formation of acceptor-donor complexes [1.106, 1.107] that can anomalously increase the solubility of the donors in the acceptor-rich segments, thus affecting the p- and n-profiles.

The motivation of this work is, therefore, to investigate Si NW doping in depth. MBE-grown Si NWs will be used as a model system to study NW doping. MBE growth of nominally undoped Si NWs has already been investigated [1.46 – 1.49] and their electrical properties reported [1.108]. MBE is well known for the ease of forming sharp dopant profiles in planar Si devices [1.109, 1.110]. However, NW doping in MBE has not been attempted upto now.

Si-MBE uses solid elemental dopant sources which do not require cracking of precursor gases as in CVD, and therefore can avoid the unwanted morphological [1.58 – 1.60, 1.71, 1.103] and structural [1.58 - 1.60, 1.103] changes observed in in-situ CVD doping.

In addition, MBE-grown undoped NWs can be doped ex-situ using ion implantation. A modulated MBE doping can be combined with ion implantation to form a sharp axial p-n junction in a NW, thus avoiding the limitations of pure in-situ doping. A number of physical phenomena such as implantation induced damages, solid phase epitaxial recrystallization and electrical activation of implanted dopants etc can be studied in the implanted NWs all of which are important not only for the NW-based electronics, but for post-CMOS three-dimensional FET architectures as well. From the point of view of electrical characterization, fast, easy and inexpensive techniques and sample preparations are needed for measuring a single NW as an alternative to expensive and time-consuming lithographic techniques. This particularly concerns with current-voltage measurements and carrier profiling of a single NW.

With such ample scopes for improvements, this work will present both NW growth and doping. Both in-situ doping in MBE and ex-situ doping by ion implantation will be explored in details including structural and electrical characterizations of individual NWs.

Chapter 2

Growth, Doping and Characterization Techniques for Molecular Beam Epitaxy (MBE)-Grown Silicon Nanowires

2.1 The Si MBE Process

MBE is essentially a surface-mediated crystal growth technique at an ultra high vacuum (UHV, base pressure ~ 10^{-10} mbar) condition [2.1]. The UHV ensures a very clean surface. The incoming atoms first hit the surface and subsequently diffuse to settle at the energetically favorable positions in the growing crystal. A very slow growth rate (~ 1 mono layer/s) assures high quality of the grown film and epitaxial orientation with respect to the underlying substrate. As shown in Figure 2.1, in Si MBE the Si atomic flux is generated by electron beam evaporation from a silicon source and any dopant flux by thermal evaporation from a Knudsen effusion cell [1.109, 1.110, 2.1].

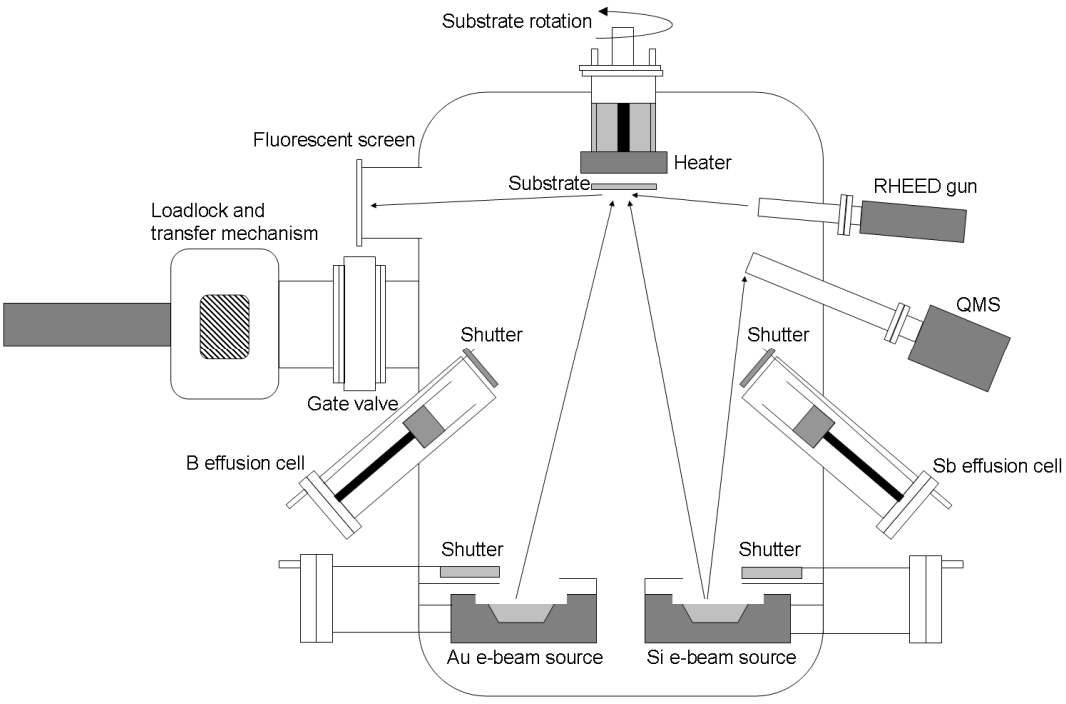

Figure 2.1 Schematic of a silicon MBE chamber showing the Si, Au and the dopant (B and Sb) sources, the rotating sample/substrate and a few other essential components.

The Si source is placed almost directly below (offset by 5-10°) the substrate while the dopant sources are inclined at an angle between 30° and 60° with respect to the normal to the substrate. The substrate is rotated at a constant speed during the deposition to achieve a uniform thickness and doping in the grown film. For Si NW growth, the Si MBE machine used in this work contained a Si and an Au e-beam source for Si NW growth, and a B and a Sb effusion cell (see Figure 2.1) for in-situ doping. The Si flux is measured by a quadruple mass spectrometer (QMS), while the dopant flux has to be calibrated from secondary ions mass spectrometry (SIMS) [2.2]. The shutters in front of the sources (see Figure 2.1) can abruptly cut off the atomic flux emanating from them, thus changing the type of doping, or leaving it undoped. The in-situ morphological characterization of the growing structure can be done by reflection high energy electron diffraction (RHEED) [2.1] which involves shooting of a high energy electron beam at a very low angle to the growth substrate and forming an electron diffraction pattern corresponding to the reciprocal lattice space of the growing structure on a fluorescence screen (see Figure 2.1).

2.2 Si NW Growth in MBE

Since this work is based on MBE-grown Si NWs, it is imperative on me to briefly discuss the mechanism of MBE-growth of Si NWs first. Schubert et al. [1.46] first experimentally demonstrated that epitaxial Si NWs can be grown on Si (111) substrate by MBE using in-situ deposited Au. Further investigations [1.46 – 1.50] revealed that MBE growth differs from the classical VLS growth in the following ways.

Firstly, rather than acting as a catalyst, the Au droplet merely acts as an initiator of NW growth, This is because, unlike CVD there is no cracking of precursor gases involved as the supplied Si comes from elemental Si source. Secondly, in MBE the Si ad-atoms impinge onto the liquid Au droplet as well as onto the Si substrate. This leads to - 1) incorporation of the ad-atoms on the Si substrate forming an epitaxial Si layer, 2) diffusion and incorporation of the ad-atoms through the Au droplet into the growing NW, and 3) a surface diffusion of the ad-atoms in proximity of a growing NW towards and along the NW [1.46 – 1.50]. A schematic of the MBE-growth of Si NW and a NW after growth is shown in Figure 2.2(a) and (b) respectively. Figure 2.2(c) presents snapshots of the NW growth with cross-sectional TEM images taken for NWs grown for different time durations. In Figure 2.2(a), I_1 refers to the Si flux resulting from direct impingement of Si atoms on the Au droplet and I_2 refers to the flux of Si ad-atoms due to surface diffusion. The surface diffusion occurs due to a concentration gradient along the length of the NW since the ad-atom density reduces drastically at the liquid-solid interface on top as they incorporate into the NW (see Figure 2.2(a)).

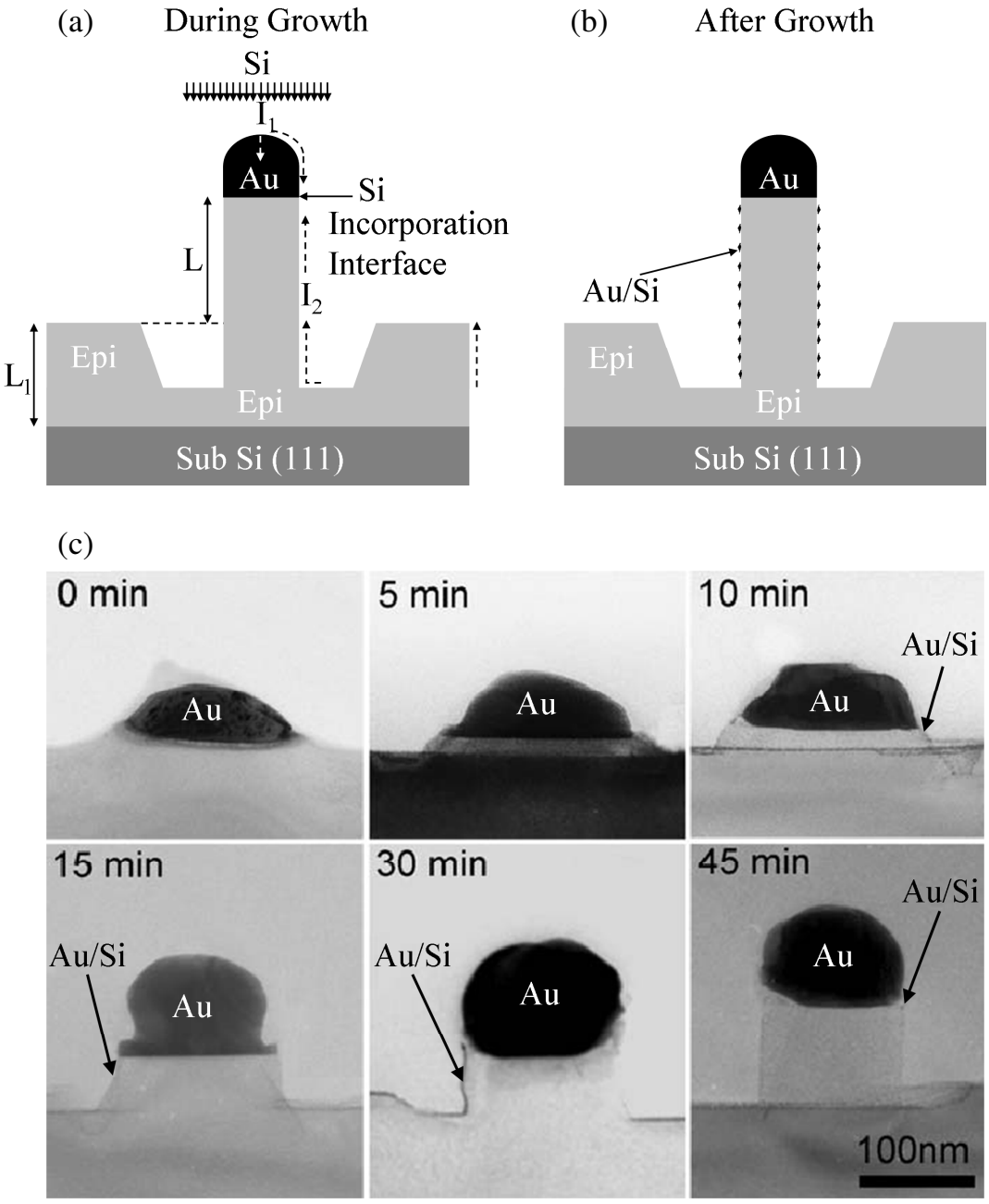

Figure 2.2 (a) Scheme of MBE growth of a Si NW with contributions from the different Si fluxes. (b) Scheme of a Si NW after growth showing the solidified Au droplet as the Au cap on top and Au/Si nanoparticles on the sidewalls. Cross-sectional TEM images of NWs grown for different durations from 0 minutes (no growth) to 45 minutes. The Au cap and Au/Si nanoparticles are indicated for NWs grown for longer times. (Reprinted from Ref. 1.48)

Schubert et al. [1.46] observed that the length of the NWs was inversely proportional to their diameter, i.e. thinner NWs grow faster than thicker ones. Such a dependence, it was suggested [1.46 – 1.50], results when the growth kinetics is primarily determined by the surface diffusion flux I_2. It should be noted that thickness L_l (see Figure 2.2(a)) of the Si epi-layer which grows in parallel with the NW was found to be approximately half the length (L) of the NW [1.46 – 1.49]. The minimum radius of MBE-grown NWs was experimentally found to be around 35nm [1.46 - 1.49]. The optimized growth temperature resulting in maximum NW density was found to be 525°C [1.46 -1.49]. The scheme in Figure 2.2(b) shows that Au exists in the MBE-grown Si NWs in two forms after growth. It is found as a hemispherical cap on top, and as nanoparticle decoration on the sidewall. This is also labeled in some of the TEM images of Figure 2.2(c). The Au cap is the same as the Au droplet that initiated the NW growth. It has been suggested [1.47 – 1.49, 2.3] that the Au nanoparticles migrated to the NW surface from the Au droplet and solidified during post-growth cooling.

In brief, MBE growth of Si NWs is initiated rather than catalyzed by Au and proceeds both via direct impingement and surface diffusion of Si ad-atoms.

2.3 In-situ Doping of Si NWs in MBE

In MBE, in-situ doping is achieved by co-evaporating Si and the dopant [1.109, 1.110, 2.1]. This is done in this work as well. A scheme of the different Si and dopant (boron in this case) fluxes during the NW growth is shown in Figure 2.3. Like in the case of nominally undoped NWs (see Figure 2.2(a)), two different Si fluxes labeled as I_{Si1} and I_{Si2} in Figure 2.3 contribute to the NW growth via direct impingement and surface diffusion respectively. The third Si flux, I_{Si3}, leads to the growth of the Si epi-layer. It is suggested in this work that similar to the Si fluxes, there are three B fluxes, I_{B1}, I_{B2} and I_{B3}. The first one (I_{B1}) hits the liquid Au droplet directly and incorporates at the interface I in Figure 2.3 (Incorporation I), i.e. droplet-NW interface. The second one (I_{B2}) hits the NW surface/sidewall and gets adsorbed and subsequently incorporated there (Incorporation II Figure 2.3), i.e. just below the surface. The third one (I_{B3}) hits the growing Si epi-layer, and gets incorporated there by adsorption as well. Since the diffusion coefficient of boron and most common dopants of silicon are fairly low at the usual growth temperature (525°C) [2.4], there will be negligible surface diffusion of boron. Hence I_{B3} will not contribute significantly to the NW doping. The ratio between I_{B1} and I_{B2} will determine the homogeneity of the doping profiles in axial and radial directions in the NW. However, it is difficult to predict whether I_{B1} or I_{B2} will dominate. Both in case of boron [2.5] and antimony [2.6] it has been observed that the liquid Au droplet contains the dopant atoms suggesting that the incorporation I in Figure 2.3 is significant. The direct incorporation at the

surface through I_{B2}, however, depends on the sticking coefficient of the dopant, i.e. the ratio between the adsorbed and desorbed dopant atoms [1.109, 1.110, 2.7]. At the growth temperature 525°C, boron can incorporate quite well into silicon [2.8 – 2.11] as the desorption of boron from the silicon surface is negligible compared to adsorption, leading to a very high sticking coefficient. This was confirmed with control experiments with silicon films (see Chapter 3). In-situ boron doping, however, is limited by the maximum temperature reachable without damaging the Knudsen cell. In this work, it corresponded to a maximum boron concentration of 10^{19} cm^{-3} (see Chapter 3).

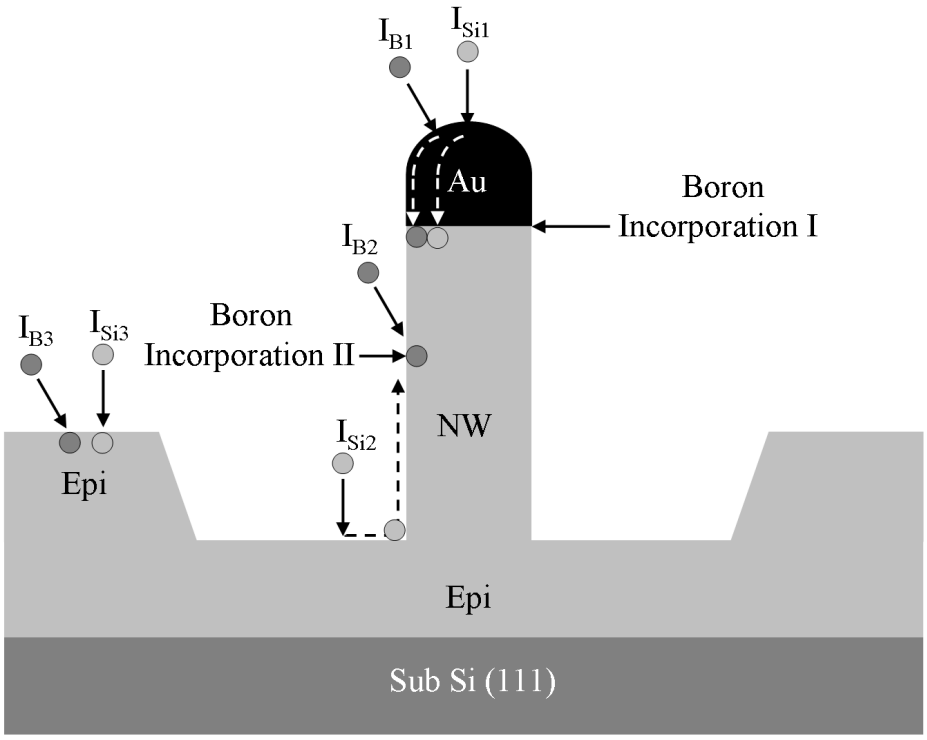

Figure 2.3 A schematic of in-situ boron doping during Si NW growth in MBE. Different Si and B fluxes are indicated along with the relevant B incorporations into the NW. $I_{Si1, 2, 3}$ are silicon fluxes and $I_{B1, B2, B3}$ are boron fluxes.

Antimony on the other hand is known to show poor sticking coefficient at the NW growth temperature of 525°C resulting in heavy segregation [2.11 – 2.15]. In fact, this was observed in the antimony doped Si thin films grown for control experiments in this work and is reported in Chapter 3. This was also observed in case of the antimony doped Si NWs grown by CVD [2.6].

Techniques such as low energy ion embedding [2.16, 2.17], or potential-enhanced MBE [2.18, 2.19] can be incorporated into the MBE system to enhance the incorporation of Sb in Si. However, these expensive techniques were unavailable at the MBE chamber used for this work. Therefore, in-situ n-doping of the Si NWs was not pursued.

In conclusion, it is conjectured that in-situ doping of Si NWs in MBE can proceed via two different pathways which may lead to a dopant inhomogeneity in the radial direction.

2.4 Ion Implantation as an Ex-situ Doping Process

Ion implantation [1.20, 2.20 – 2.23] is the process by which energetic, charged-atoms/molecules are directly introduced to a host semiconductor lattice. It is the most widely used doping technique in VLSI technology due to its high accuracy over many orders of doping levels, customized doping profiles, possibilities of selective doping with appropriate masking etc. Doping semiconductors by ion implantation generally involves two processes – 1) Ion bombardment on the substrate with the bombarded ions reaching up to a range specified by the implantation energy and dose (charge per unit area), and 2) Electrical activation of the implanted ions along with recovery of any implantation-induced damage of the crystal structure of the host semiconductor by a thermal annealing.

An ion implanter primarily consists of (see Figure 2.4) an ion source, an ion extraction and separation magnet, an ion acceleration column, a rastering system and an end station where the target (NWs for this work) resides. The ion source contains the species (dopants to Si, such as B, P, As etc) to be implanted in solid, liquid or gaseous form, and a mechanism to ionize these species. The resulting ions are extracted from the ion source with a small accelerating voltage and are subsequently separated by the separation magnet in accordance with their mass and charge. The spatially separated ions subsequently enter an acceleration tube where they are accelerated to the desired ion-energy which determines their range of penetration into the target substrate. The rastering system which is used next in line, distributes the ions uniformly over the target substrate.

As the energetic ions hit the target, they penetrate inside, lose their kinetic energy through a series of collisions with the atoms in the target (this includes both the nuclei and the bound/free electrons) substrate and finally come to a stop as shown in Figure 2.5(a). The resulting distribution of the implanted ions depends on the ion mass, energy, the target mass and the beam direction with respect to the crystal plane in case the target material is crystalline. The total distance (R) that an implanted ion travels from the surface till it comes to a complete stop in the target material is called the range (see Figure 2.5(a)). However, technologically more important

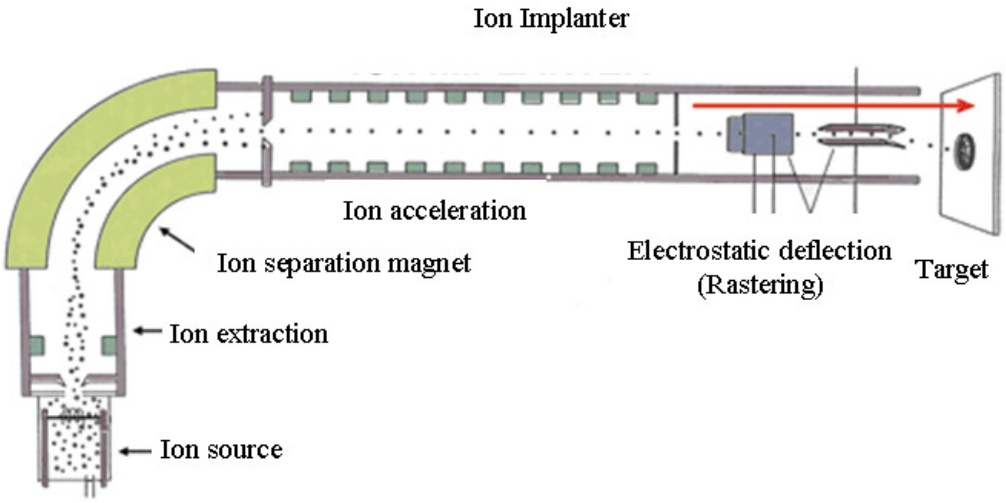

Figure 2.4 A schematic representation of the ion implantation equipments indicating the major parts

term is the distance traveled along the axis of the incident ion beam and is called the projected range (R_p) (see Figure 2.5(a)). As the successive collisions and hence the energy losses are statistical in nature, the projected range (R_p) can be defined as the mean of the resulting distribution of implanted ions [2.21, 2.22], and the standard deviation (ΔR_p) in the same direction as straggle (see Figure 2.5(b)).

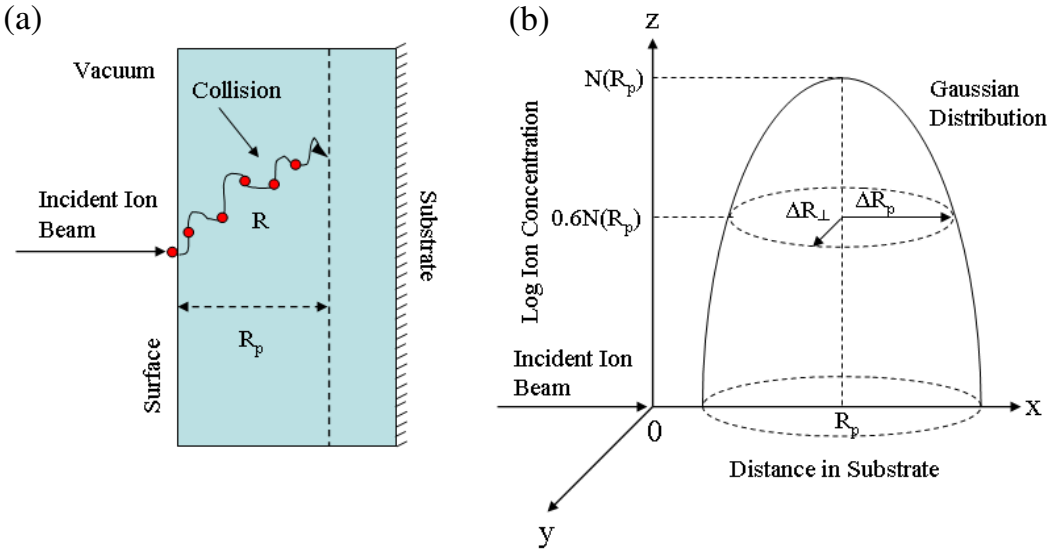

Figure 2.5 (a) Schematic showing the range (R) and projected range (R_p) of an incident ion beam after a series of collisions. (b) Three dimensional Gaussian distribution of the dopant atoms after implantation showing the projected range and straggles in the lateral (ΔR_p) and transverse ($\Delta R_\perp$) directions.

Using the classical theory of scattering [2.21, 2.22], depth profile (N(x)) of the implanted ions can be shown to follow a Gaussian distribution, i.e.

$$N(x) = \frac{Q_0}{(2\pi)^{\frac{1}{2}}\Delta R_p} \exp[-\frac{1}{2}(\frac{x - R_p}{\Delta R_p})^2] \qquad [2.1]$$

where Q_0 is the dose of the incident ions. This is illustrated in Figure 2.5(b). In order to obtain a rectangular shaped doping profile, i.e. to achieve a uniform dopant concentration over a target depth, multiple implantations [2.24] are used. The resulting Gaussian profiles of single implants add up to result in a flat profile over a target depth. For all practical purposes, the implantation profile for a desired projected range is obtained by performing computer simulations. The most widely used simulation program is known as transport of ions in matters (TRIM) developed by Ziegler et al. [2.25]. This program is also used in this work.

As mentioned earlier, when energetic ions strike the Si substrate, they undergo a series of nuclear and electronic collisions before coming to a complete stop. If sufficient energy is transferred the nuclear collisions can result in the displacement of Si atoms leading to isolated or clustered point defects [1.20, 2.20 – 2.22, 2.26, 2.27]. However, if a certain critical ion dose is applied for a certain beam energy, it may result in complete amorphization of the Si crystal, In that case the displaced Si atoms equal the Si density N, i.e. $5x10^{22}$ cm^{-3}. With a beam energy of E_0, the critical dose (N_{crit}) to create a continuous amorphous layer in Si is given by [2.28]

$$N_{crit} \approx \frac{5\Delta R_p N E_d}{E_0} \qquad [2.2]$$

where E_d is an effective displacement threshold energy. Experimental data suggests that [2.28] for light ions N_{crit} is mainly determined by E_0, while for heavier ions it is determined by ΔR_p. The critical dose determines the maximum achievable doping density for a specific dopant.

In order to heal out these damages and to electrically activate the implanted dopant atoms, a post-implantation thermal anneal is necessary. During annealing, the dopant atoms move into the substitutional lattice sites of Si which allows them to contribute electrons or holes for current conduction, thus enhancing the conductivity of Si. However, it should also be noted that during annealing the displaced atoms can coalesce and form secondary defects such as dislocation loops, stacking faults and micro-twins [1.20, 2.20 – 2.22, 2.26, 2.27]. There are a variety of annealing techniques that can be applied depending on the dopant species, the desired doping profile and the priority between structural healing and electrical activation. The conventional annealing, being used since the beginning of semiconductor processing, is the furnace annealing which involves heating of the implanted substrate for a duration ranging from 30 minutes to several hours inside a quartz diffusion furnace in an inert gas (Ar or N_2)

atmosphere. Although this technique can achieve good structural recovery including recrystallization of completely amorphized Si, the longer time scale at an elevated temperature can lead to significant out-diffusion and surface segregation of dopants, and hence is not very suitable for dopant activation in Si NWs. Alternatively, rapid thermal annealing (RTA) in the temperature range of 800°C – 1200°C at a time scale of a few seconds can be performed by radiative heating [2.21, 2.22] of the substrate with tungsten-halogen lamps in an inert gas atmosphere. This better serves the purpose of electrically activating the dopant atoms in Si NWs as the time scale is relatively short for significant out-diffusion of dopants.

To summarize, ion implantation is a very well developed doping technique for semiconductors that can achieve very high (up to 10^{21} cm^{-3}) doping density within a depth of few tens of nanometers, and therefore is suitable for doping Si NWs. This will be used to dope the MBE-grown NWs, both p- and n-type.

2.5 Doping MBE-grown Si NWs by Ion Implantation

The implantation schemes for Si NWs are illustrated in Figure 2.6 for P implantation. The P^+ ions are incident at an angle of 7° with respect to the NW axis (<111> direction) to avoid ion channeling. Channeling refers to travelling of the implanted ions along a crystal direction without encountering any collision. This can result in larger than expected projected range which is calculated by TRIM which treats the target material amorphous.

In order to uniformly dope an entire undoped NW, multiple energy implants that result in a projected range equaling the average NW length were simulated for this work using TRIM (see Chapter 3). Figure 2.6(a) and (b) illustrate an n-type NW resulting from the implantations on an undoped one. Both p- and n-doping were achieved and the details are discussed in Chapter 3. Figure 2.6(c) and (d) illustrate the P implantation process on a modulation-doped p-i type NW covered with a spin-on-glass (SOG), to form an intra-NW p-n junction. In this case the lower segment of the NW is already p-type due to in-situ doping. Therefore, the projected range for the TRIM simulations should amount to half the average NW length, i.e. only the upper segment. The resulting p-n junction NW is shown in Figure 2.6(d).

In addition, heavy As implantation was used to completely amorphize the as-grown Si NWs and subsequently study their recrystallization upon thermal annealing. It should be noted that the TRIM program used to simulate the implantation profiles for this work is originally meant for semi-infinite planar targets. Therefore no constrain regarding the dimension of the system for the ion collision cascades are considered, and the surface effects are not taken into account. Both furnace annealing and RTA were used on the implanted NWs. Furnace annealing was used to study the recrystallization of completely amorphized NWs, while RTA was used primarily for

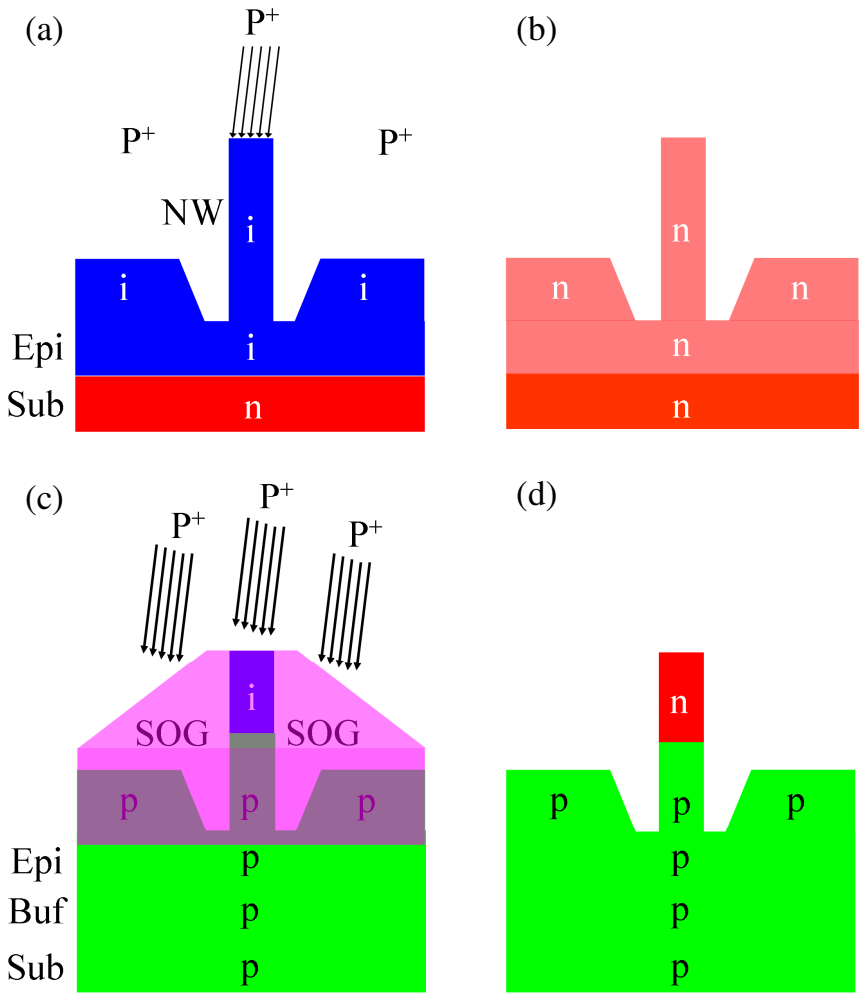

Figure 2.6 Implantation schemes illustrating (a) P^+ ion impingement on an undoped (i-type) Si NW (b) the resulting n-type Si NW. (c) P^+ ion impingement on a modulation-doped (p-i-type) Si NW covered with a spin-on-glass (SOG). (d) The resulting p-n junction NW.

electrically activating the dopants in case of non-amorphizing doses. Details are provided in Chapter 3.

2.6 Electrical Transport Measurements

This section is further subdivided into four, discussing the basics of transport properties first, and subsequently elaborating the two different transport measurements used in this work.

2.6.1 Basics of Transport Properties of Semiconductors

As already mentioned in Chapter 1, the most significant change brought by the dopant atoms occupying substitutional lattice sites in Si is in the electrical properties. This is manifested in a significant increase of the electrical conductivity and corresponding decrease of the resistivity of Si owing to extra free carriers from the dopants. The resistivity (ρ) of a semiconductor depends on the free carrier concentration (n for electron/p for hole) and mobility (μ_n for electron/μ_p for hole) as follows [1.51, 1.52]

$$\rho = \frac{1}{e(n\mu_e + p\mu_p)} \qquad [2.3]$$

For a doped semiconductor of either p- or n-type, the number of majority carriers is orders of magnitude higher than the number of minority carriers, implying that for an n-type semiconductor, where n>>p

$$\rho_n = \frac{1}{en\mu_e} \qquad [2.4]$$

and for a p-type semiconductor, where p>>n

$$\rho_p = \frac{1}{ep\mu_p} \qquad [2.5]$$

Resistivity of a material/structure can be extracted from two-point or four-point transport measurement [1.69] which is discussed in the next section. However, to get an accurate idea of the free carrier concentration (n/p) contributed by the dopants, the mobility must be known. Although doping increases n or p, it simultaneously decreases μ_n or μ_p at room temperature or above. The free carrier concentration (n/p) is temperature dependent and is given as [1.51]

$$n = n_i \exp\left(\frac{E_{Fn} - E_i}{kT}\right) \qquad [2.6]$$

and

$$p = n_i \exp\left(\frac{E_i - E_{Fp}}{kT}\right) \qquad [2.7]$$

where n_i, is the intrinsic carrier concentration of the semiconductor, E_i is the intrinsic Fermi level, E_{Fn} and E_{Fp} are the Fermi levels of the n- and p-type semiconductor respectively, k is the Boltzmann constant and T is the temperature. At room temperature and above, the free carrier concentration in n-/p-type semiconductors is significantly higher than in an intrinsic semiconductor. This gives rise to the so called ionized impurity scattering on the application of an external electric field, i.e. the scattering between the free carriers and the ionized donors/acceptors contributing them. At room temperature and above, the semiconductor

mobility is mainly determined by the ionized impurity scattering. If all donor/acceptor atoms are ionized, mobility (μ_n/μ_p) is given by

$$\mu_n/\mu_p \alpha \frac{T^{\frac{3}{2}}}{n/p} \qquad [2.8]$$

An empirical-fit relationship between μ_n/μ_p and n/p can be formulated as [1.51, 1.52]

$$\mu_n/\mu_p = \mu_{min} + \frac{\mu_0}{1+(\frac{n/p}{N_{ref}})^{\alpha}} \qquad [2.9]$$

where μ_{min}, μ_0, N_{ref} and α are fit parameters and all of them exhibit a temperature dependence of the form [1.51]

$$A = A_0(\frac{T}{300})^{\eta} \qquad [2.10]$$

where A_0 is a temperature independent constant and η is the temperature exponent for the given fit parameter. Combining Equations 2.4/2.5 with Equation 2.9

$$\rho_n/\rho_p = \frac{1}{e[n/p(\mu_{min} + \frac{\mu_0}{1+(\frac{n/p}{N_{ref}})^{\alpha}})]} \qquad [2.11]$$

This empirical variation of resistivity with carrier concentration in Si has been plotted in Ref. 1.51 and is included in the Appendix 2 (see Figure A2.1) and is utilized in this work to derive local carrier concentration for a measured local resistivity (see Section 2.6.4).

Mobility measurement by standard techniques such as Hall-effect [1.50, 1.51] is challenging for a vertical Si NW due to its very small lateral dimension, i.e. diameter. Therefore, Hall mobility of Si layers doped to the same levels as the NWs was measured in this work (details in Chapter 3 and 4) and it was assumed that the mobility values remain the same in the NWs. Unless the NW diameters are below the quantum confinement regime (~5nm) this assumption is reasonable [1.30].

2.6.2 Current-Voltage Measurement

A scheme of a current-voltage measurement to a semiconductor with two point-contacts is shown in Figure 2.7. The total resistance (R_{Tot}) measured in a two-point measurement is the sum of the probe resistance (R_p), contact resistance (R_C), device resistance (R_d), and spreading resistance (R_S) connected in series, i.e.

$$R_{Tot} = \frac{V}{I} = R_p + R_C + R_d + R_S \qquad [2.12]$$

The device is generally a semiconductor, and for this work a Si NW. For metal/highly doped semiconductor probes, R_p is very small (a few Ohms) and hence can be neglected. R_C depends on the Schottky barrier height [1.51, 1.52] at the interface between the metal/highly doped semiconductor probe – semiconductor device. A Schottky barrier height is the potential barrier an electron or hole encounters while crossing from metal to semiconductor. This is shown as $e\Phi_B$ in the metal-semiconductor band diagram in Figure 2.7(b). In this band diagram a direct contact between the metal and highly doped n^+ is shown for reasons explained latter. Beyond the contact area, the semiconductor is normal doped n-type. For an n-type semiconductor, $e\Phi_B$ is given as the difference between the work function of the metal ($e\Phi_M$) and the electron affinity ($e\chi$) of Si. The depletion width (w), i.e. the distance over which the Schottky barrier extends into the semiconductor is inversely proportional to the square root of the doping density. For a lower doping level (n/p $<10^{18}$ cm^{-3}), the carrier transport across the metal-semiconductor junction is mainly dominated by thermionic emission and the dimension independent specific contact resistance (ρ_C) is given by [2.30]

$$\rho_C = \frac{k}{eA^*T}\exp\left(\frac{e\varphi_B}{kT}\right) \qquad [2.13]$$

where k and A^* are the Boltzmann and Richardson constant respectively, T is the temperature. R_C can then be calculated by simply dividing the ρ_C with the contact area (A_C), i.e.

$$R_C = \frac{\rho_C}{A_C} \qquad [2.14]$$

Naturally, a small barrier height leads to a low value of R_C. In case of highly doped(n^+ or p^+) semiconductors (n/p > $10^{18}cm^{-3}$), carrier transport across the junction is determined by the so-called field emission [2.30]. This leads to narrowing down of the Schottky barrier which allows electrons or holes to tunnel through the barrier as shown for the case of a metal-n^+ semiconductor junction in Figure 2.7(b). When this happens, ρ_C reduces exponentially with the square root of the doping density (n/p) [2.30].

An Ohmic contact is said to be established when R_C is independent of the applied bias and this leads to a linear or quasi-linear current-voltage characteristic. From the above discussion, one can conclude that for low/medium doped semiconductors, a small barrier height is essential for an Ohmic contact, while for highly doped semiconductors (see Figure 2.7(b)) the barrier height difference is not very critical as electron tunneling effectively dominates in the transport. With a single two-point measurement, it is not possible to measure the absolute value of R_C. However, it can be estimated for low/medium doped Si NWs by using Equation 2.13. For highly doped

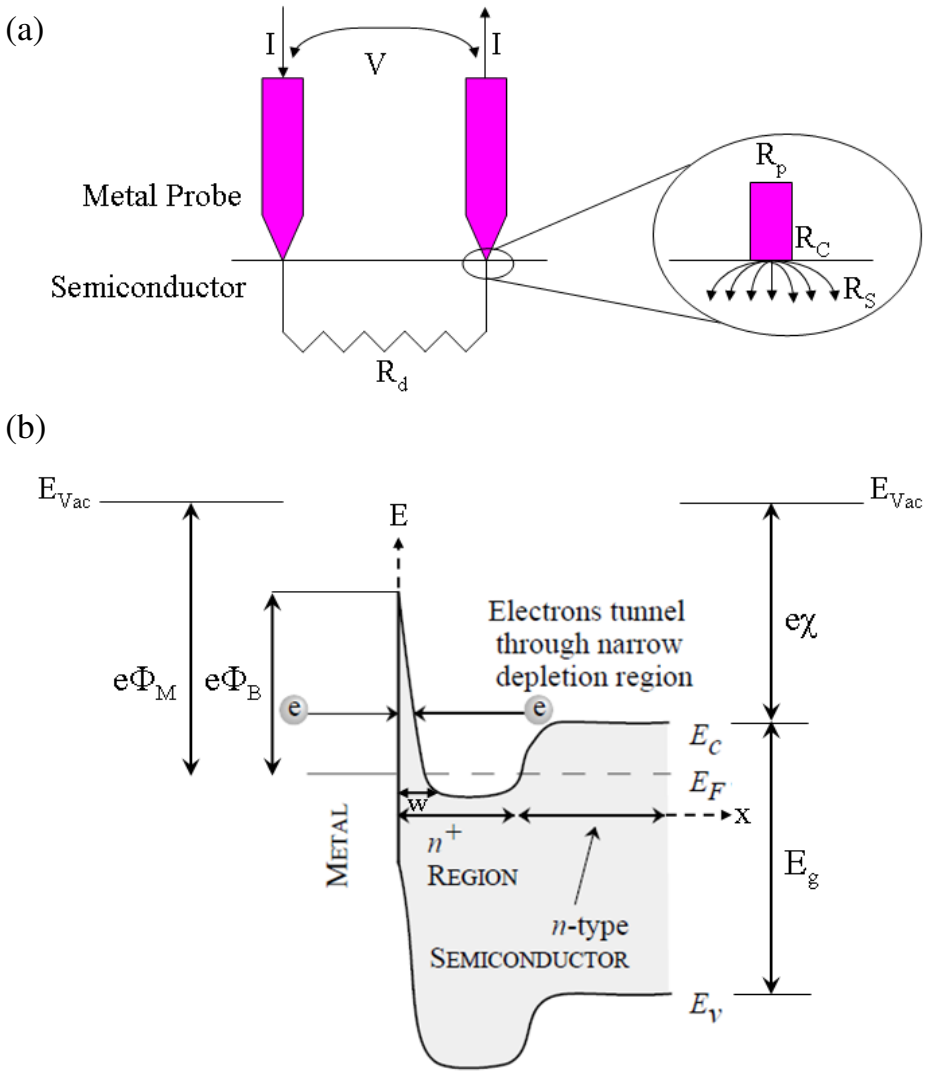

Figure 2.7 (a) Scheme of a two probe measurement with metal probes on a semiconductor sample of resistance R_d. Inset is the illustration of the different resistance components measured in the total resistance. (b) The energy band diagram of a metal in contact with a heavily doped (n^+) semiconductor. The contact resistance arises because of the Schottky barrier height $e\Phi_B$ at the metal semiconductor interface. As the semiconductor is heavily doped, the depletion width (w) is thin enough to let the electrons tunnel through the barrier, thus effectively resulting in an Ohmic contact with a low contact resistance.

NWs, R_C will reduce exponentially and for practical purposes it can be neglected. Disregarding R_C, the main contribution to R_{Tot} in Equation 2.12 comes from R_d and R_S. R_S originates from the current fringes [1.69] spreading out from the probe tip as illustrated at the inset of Figure 2.7(a).

Depending on the probe size and the device geometry, either of them can be dominant, and each provides valuable information regarding the electrical property of the device.

2.6.3 Measurement of the NW Resistance

The spreading resistance is inversely proportional to the apex diameter of the probe tip. By choosing appropriate probes with larger diameter (smaller spreading resistance), the resistance of a NW can be accurately measured. Figure 2.8 illustrates the measurement set-up used for measuring the resistance of MBE-grown Si NWs reported in this work.

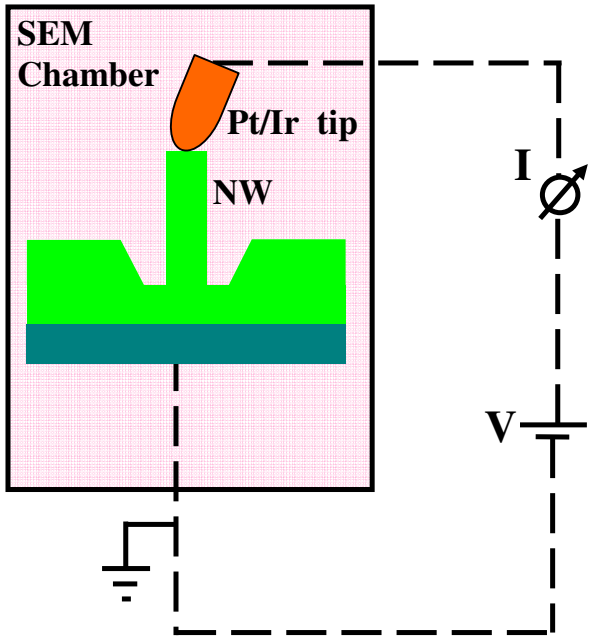

Figure 2.8 Schematic of the two-point electrical measurement set-up inside an SEM. The Pt/Ir tip contacts the n-type NW grown on n-type substrate in this case. The voltage (V) is swept from positive to negative using a picoammeter and the resulting current (I) is measured by the same.

A metal Pt/Ir tip of diameter ~ 200nm fitted to a micromanipulator fixed with the stage of a scanning electron microscope (SEM) is used to contact individual NWs. The NWs as well as the tip are imaged in the SEM so that the exact dimensions of each are known. Experimental details are reported in Chapter 3. In this case, R_{Tot} mainly comes from R_d which consists of the NW and the epi-layer, and the substrate underneath. The cross sectional area of the epi-layer and the substrate is much larger (~mm^2) compared to that of a NW (~nm^2) resulting in the fact that the dominant part of the measured resistance comes from the NW. Therefore, attributing the

measured resistance fully to the NW, it can be related to its resistivity (ρ), length (l) and diameter (D) assuming a cylindrical shape for the NW, i.e.

$$R = \frac{\rho l}{(\frac{\pi D^2}{4})} \qquad [2.15]$$

From the measured resistance of a NW, its resistivity can be calculated using Equation 2.15. This is an average resistivity of the entire NW which should correspond to its doping level according to Equations 2.4 or 2.5.

2.6.4 Measurement of the NW Carrier Profile

The spreading resistance provides a local measure of the resistivity. Considering a metal probe with a circular interface of diameter 2a contacting a flat semiconductor surface of resistivity ρ around the contact area, the spreading resistance (R_S) is given by [1.69]

$$R_S = \frac{\rho}{4a} \qquad [2.16]$$

For a sufficiently small probe-tip, R_S can be the dominating term in Equation 2.12, thus providing local resistivity at a specific contact point in the NW. From the local resistivity, local carrier concentration can be calculated following the standard calibration curve (see Figure A2.1 in Appendix 2). For a cross-section of a Si NW, this can be very effectively done by scanning spreading resistance microscopy (SSRM) [2.31 – 2.34] and the same was adopted for this work. SSRM is a technique based on conductive atomic force microscopy (CAFM). A constant force in terms of the deflection voltage is maintained between a conductive tip and the sample, measuring the local spreading resistance in the material in a nanoscale volume. The key to measure the spreading resistance [2.33] is to apply a high force (>μN) on a stiff AFM cantilever (10 – 100N.m) so that the probe indents the surface (~1nm) and an intimate contact is established. This allows R_S to dominate over R_C and R_d in Equation 2.12. As the tip scans over the entire cross section of the sample, a two-dimensional profile of the spreading resistance can be obtained which can be duly converted to carrier concentration as mentioned already.

A schematic of the SSRM measurement used for this work is shown in Figure 2.9(a). The vertical NW is first embedded in an oxide matrix. In order to probe the axial cross-section, the NW is cut and planarized along its axis. On the other hand, to probe the radial cross-section it is planarized at the top. Experimental details are provided in Chapter 3. Figure 2.9(b) shows how the spreading resistance originates when the probe contacts the embedded NW. The underlying substrate of known resistivity serves the purpose of calibration which will be illustrated along with the results in Chapter 4. Unlike in the case of current-voltage measurements discussed in

Section 2.6.3, the NW resistance is significantly smaller than the spreading resistance due to the smaller tip size (CAFM tips ~ 10nm). It should be mentioned here that the measured R_S depends on the actual radius of the tip apex known as the 'electrical radius' that contacts the sample. Therefore, the quantity 'a' in Equation 2.16 is the 'electrical radius' which can be orders of magnitude smaller than the physical radius of the tip [2.34]. The spatial resolution of SSRM

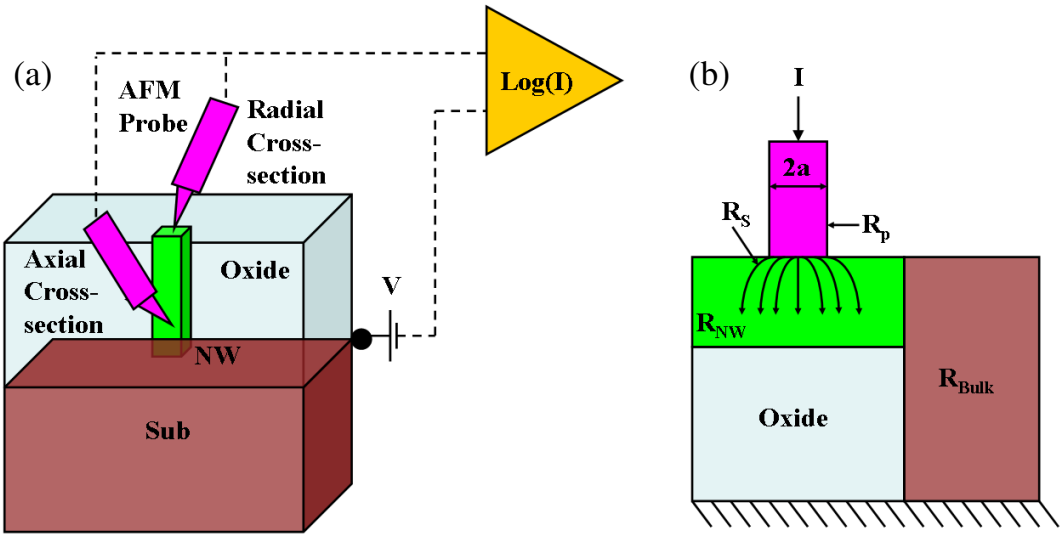

Figure 2.9 Measurement scheme for SSRM on Si NWs. (a) Circuit diagram showing the embedded NW, the AFM probe, the voltage source and the logarithmic amplifier. Both axial and radial profiling can be done by an appropriate sample preparation and tip scanning. (b) Illustration of the spreading resistance measured on the NW with a cylindrical probe tip of diameter 2a.

mainly depends on the electrical radius of the tip, the penetration depth into the sample and the nano-roughness of the tip (< 10nm), [2.34]. Typically, SSRM can achieve a spatial resolution of about 10nm [2.34] for a perfectly sharp and fresh tip and has a dynamic range of carrier concentration measured between 10^{15} and 10^{20} cm^{-3}.

2.7 Morphological and Structural Characterization by Electron Microscopy (SEM and TEM)

Both SEM and TEM were used to for morphological and structural characterizations of the MBE-grown Si NWs in this work. SEM investigation requires minimal sample preparations and it provides an accurate measure of the diameter and length of the NWs, as well as their density on the substrate. These are helpful to understand how the growth parameters control the morphology of the NWs.

TEM enables a detailed understanding of the microstructure of the NWs as well as an elemental analysis on a nanoscale [2.35, 2.36]. TEM samples are very thin (<100nm) so that they allow transmission of a high energy (>100kV) electron beam through them. TEM can be used to investigate the morphology, crystallinity and crystal defects when used in diffraction contrast mode [2.35, 2.36]. Using a suitable aperture, electron diffraction pattern from a selected area on the sample can be obtained. This provides detailed information about the crystal structure of the sample. A special technique called phase contrast imaging [2.35, 2.36] can be used to obtain high resolution TEM (HRTEM) images that enable observation of the lattice planes in a crystal. Elemental analysis can be done by collecting the X-rays emitted from the sample surface on being hit by the electron beam in TEM. A lateral mapping of elements with a nanoscale resolution can provide detailed chemical composition of the sample surface.

All of the above TEM techniques were used for the Si NWs investigated in this work. The TEM sample preparations are briefly described in Chapter 3. Both SEM and TEM images of the NWs grown in this work are shown in Chapter 4 in connection with specific results.

In conclusion, MBE-growth, doping and various characterization techniques used for this work are briefly discussed here. They will be helpful to understand the experimental details (Chapter 3) and results (Chapter 4).

Chapter 3

Experimental Details on Nanowire Growth and Doping

3.1 In-situ Doping of Si NWs in MBE

This chapter is focused on the details of the experimental techniques used for this work. An image of the MBE machine (Riber SiVa45) used which roughly corresponds to the scheme in Figure 2.1 is shown in Figure 3.1. The growth process was semi-automated, i.e. the wafer loading was manual, but the temperature control, shutter opening, and flux measurements etc were automated.

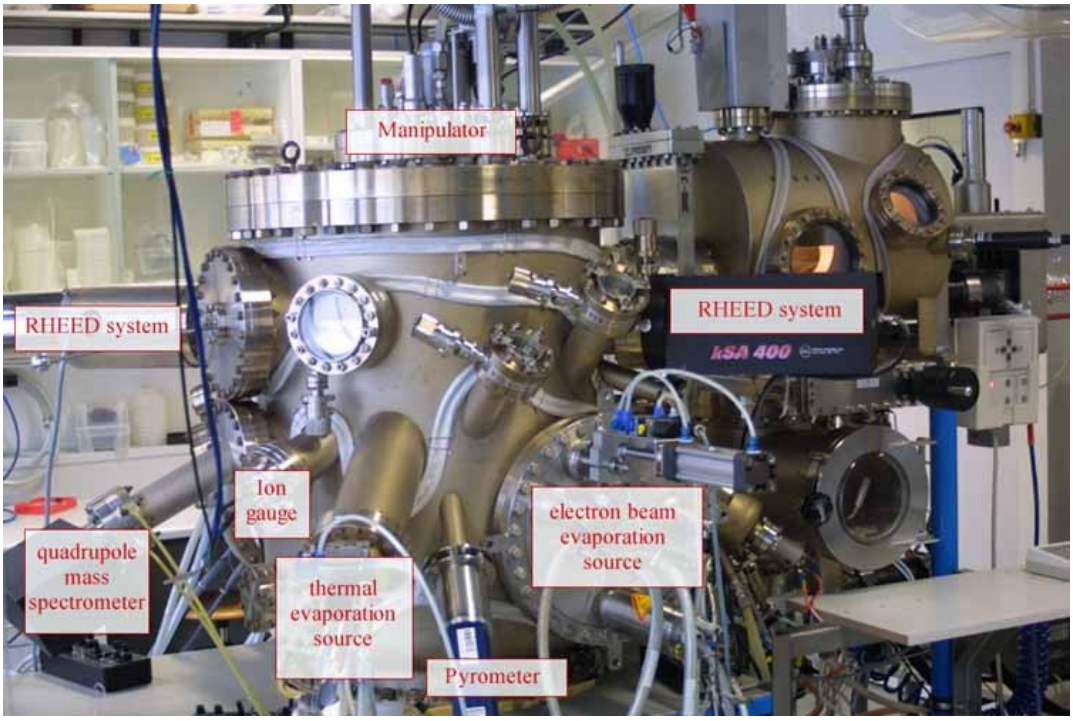

Figure 3.1 An image of the Riber SiVa45 MBE machine used for the experiments with its main parts labeled.

The prerequisite for in-situ doping is an appropriate calibration of the dopant fluxes. The dopants are heated inside a crucible in a Knudsen cell leading to effusion from an aperture at the end of the cell. The temperatures of the dopant sources are measured by thermocouples and regulated by Eurotherm^{TM} temperature controllers.

3.1.1 Calibration of the Dopant Sources

A useful way of calibrating a dopant flux with the dopant source temperature is to measure the SIMS profile of that dopant used to uniformly dope a Si layer. By varying the source temperature the dopant fluxes can be varied which is reflected in the measured dopant density in the grown Si film. Thus, a dopant calibration can be obtained by plotting the measured dopant density against the dopant source temperature. SIMS measurements (CAMECA IMS4F at RTG Mikroanalyse GmbH, Berlin) were performed for both B and Sb doped Si films grown at 525°C (the optimized Si NW growth temperature). Nominally undoped Si layers were grown just before introducing the dopants in order to achieve higher sensitivity during SIMS measurements. Details of these multi-layered structures are provided in Table 3.1 and typical SIMS spectra for B and Sb are shown in Figures 3.2. The growth substrate for all the experiments was phosphorus-doped 5" Si (111) wafer of resistivity 10 – 20 Ω-cm. All wafers were cleaned by RCA1 and RCA2 [3.1] before loading into the MBE chamber and the native oxide was removed by in-situ annealing at 870°C for 20 minutes prior to starting the Si layer growth.

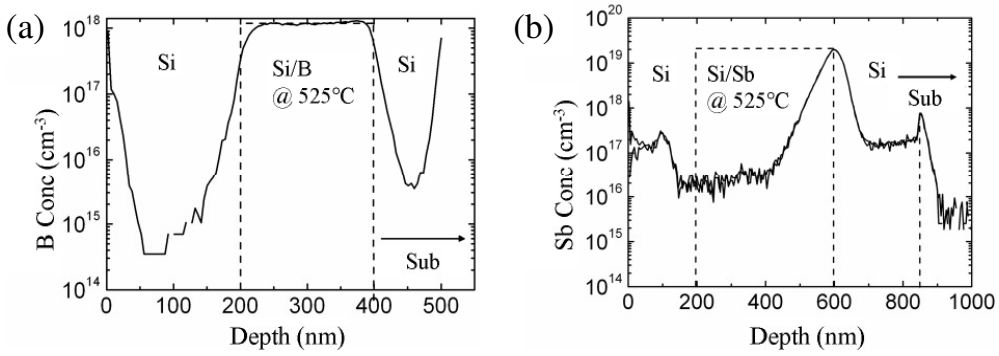

Figure 3.2 SIMS profile from segments of uniformly in-situ doped Si layers. (a) B from the sample B2 in Table 3.1 (b) Sb from the sample Sb1 in Table 3.1.

A remarkable difference between the B and Sb profiles are observed. The B profile (Figure 3.2 (a)) is almost flat at a B concentration of 10^{18} cm^{-3} over the entire depth of 200nm, and the transition length is within 20nm. On the other hand, the Sb profile (Figure 3.2 (b)) peaks at the interface between the nominally undoped and the Sb doped layer. The depth profile ($N_D(x)$) of dopants in in-situ doped MBE-grown Si layers is given as [2.11]

$$N_D(x) = N_{D0}\{1 - \exp(\frac{K_1 x}{SV})\} \qquad [3.1]$$

where N_{D0} is a constant, K_I is the incorporation coefficient, s is the sticking coefficient of the dopant and v is the film growth velocity. At the growth temperature of 525°C Sb is known to segregate significantly [2.11 – 2.14] owing to a very low value of the sticking coefficient while B is known to fully incorporate [2.7 – 2.10]. These results confirmed the same. Since a uniform doping profile is essential for a calibration, in-situ Sb doping of Si NWs was not pursued henceforward.

B calibration was done by plotting the B concentration values obtained from the flat B profiles at five different source temperatures (see Table 3.1) and this is shown in Figure 3.3. The measured doping levels were kept relatively high (>10^{17} cm^{-3}) keeping in mind the resolution limit of SIMS (~10^{14} cm^{-3}). However, the calibration curve can be safely extrapolated down to the doping level of 10^{15} cm^{-3} as shown in Figure 3.3.

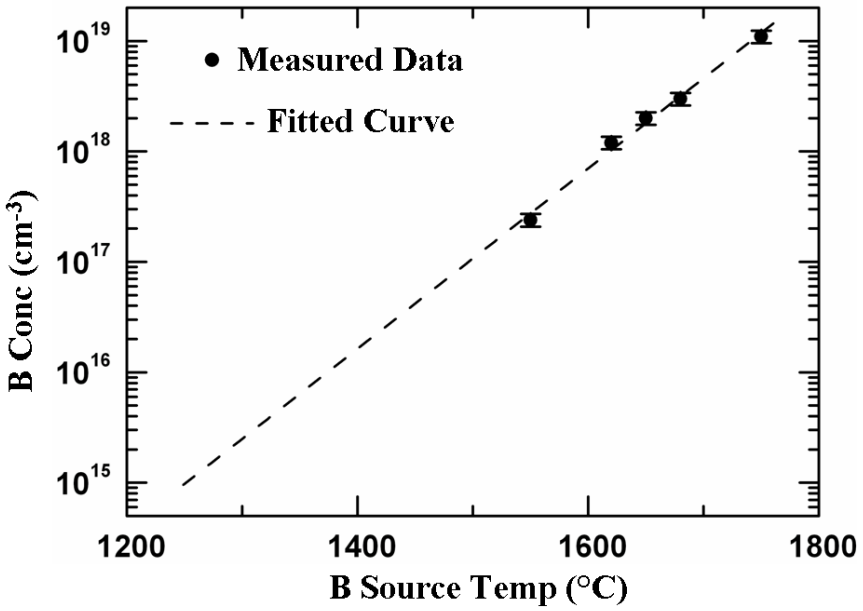

Figure 3.3 Calibration curve of B concentration in the grown Si film vs the B source temperature. The error bar is ~ 10%. The fitted curve is an exponential fit that looks like a straight line on a semi-logartihmic scale.

3.1.2 Uniform Boron Doping of Si NWs

With the calibration done, B doping of Si NWs was carried out for different B concentrations. It should be noted that these B concentrations in Si NWs are only 'expected'. Since SIMS can't be applied directly to measure the dopant concentration in a NW owing to the size constraints, the 'real' electrically active dopant concentration inside a NW is verified latter with electrical

Sample Number	Layer 1	Layer 2	Layer 3	Layer 4	Layer 5	Layer 6
B1	200nm Si @ T = 580°C	50nm Si during T ramp-down	200nm Si/B @ T = 525°C (B source T = 1700°C)	50nm Si during T ramp-up	200nm Si @ T = 580°C	___
B2	200nm Si @ T = 580°C	50nm Si during T ramp-down	200nm Si/B @ T = 525°C (B source T = 1650°C)	100nm Si @ T = 525°C	200nm Si/B @ T = 525°C (B source T = 1620°C)	200nm Si @ T = 525°C
B3	200nm Si @ T = 580°C	50nm Si during T ramp-down	200nm Si/B @ T = 525°C (B source T = 1750°C)	200nm Si @ T = 525°C	200nm Si/B @ T = 525°C (B source T = 1550°C)	200nm Si @ T = 525°C
Sb1	200nm Si @ T = 580°C	50nm Si during T ramp-down	200nm Si/Sb @ T = 525°C (Sb source T = 350°C)	50nm Si during T ramp-up	200nm Si @ T = 580°C	___
Sb2	200nm Si @ T = 580°C	50nm Si during T ramp-down	400nm Si/Sb @ T = 525°C (Sb source T = 300°C)	200nm Si @ T = 525°C	___	___

Table 3.1 Key growth parameters for the in-situ doped multi-layers used for calibrations of dopant sources. All samples were grown on RCA-cleaned phosphorus-doped 5" Si (111) wafers (resistivity 10 – 20 Ω-cm) with a Si deposition rate always at 0.5Å/s. The chamber pressure during growth was around 10^{-9} mbar.

measurements (see Chapter 4). For B-doping of Si NWs, p-type Si wafers were chosen as the substrate so that during electrical measurements no additional bipolar junction between the NW and the substrate is formed that can modify the current output. Like the B-doped Si layers, RCA-cleaned 5" p-type Si wafers (resistivity ~ 5 – 10 Ω-cm) were loaded into the MBE chamber and the native oxide was removed by an in-situ annealing at 870°C for 20 minutes. Afterwards, the substrate temperature was reduced to 525°C and a 200nm B-doped Si buffer layer was grown with a Si growth rate of 0.5Å/s. It was observed that the buffer layer increases the density of Si NWs probably by offering a cleaner surface than the substrate, and hence enhancing the surface diffusion of Si atoms which is the main driving force for NW growth in MBE. A higher density of NWs is very helpful for their characterizations. Immediately after the growth of the buffer layer, an Au layer of thickness around 2nm was deposited at the same temperature. The Au thickness was measured in-situ with a quartz-crystal oscillator. Since the growth temperature (525°C) was higher than the Au-Si Eutectic temperature (363°C) the Au layer subsequently broke into liquid Au/Si droplets that acted as the initiator for the Si NW growth [1.46 – 1.49]. Si and B were co-evaporated again for one and a half hour maintaining the same Si growth rate and keeping the B source temperature same as that for the buffer layer. This should result in the growth of B-doped Si NWs. A number of B-doped Si NWs with the B-doping levels varying from 10^{15} cm^{-3} to 10^{19} cm^{-3} were grown and all the key growth parameters are listed in Table 3.2 (NWB1 – NWB5).

3.1.3 Nominally Undoped Si NWs

In addition to the B-doped Si NWs, nominally undoped Si NWs were also grown using the same recipe as above except evaporating B with Si. Undoped Si NWs have two uses – 1) to serve as a reference for comparison of the electrical properties with the doped ones, 2) to serve as targets for ex-situ doping with ion implantation. In case of undoped NWs, both p and n-type substrates were used in order to avoid bipolar junctions between the NW and the substrate once they are doped by implantations, i.e. the NWs meant for B implantation were grown on p-type substrates and the ones meant for P/As implantations were grown on n-type substrates. Experimental details on growth are provided in Table 3.2 (UNWB, UNWAs)

3.1.4 Modulated Boron Doping of Si NWs

Modulation-doped Si NWs were also grown in order to form an intra-NW p-i junction first and subsequently transform it to an intra-NW p-n junction following the scheme shown in Figure 2.6(c) and (d). For these NWs, the B source was switched off at half of the total growth time so

that only the lower segments of the NWs turned p-type while the upper segments remained intrinsic (i-type). The experimental details are provided in Table 3.2 (MNWB).

3.1.5 Boron Doped Si Films for Mobility Measurements

In order to measure the carrier mobility by Hall effect, uniformly doped Si layers with doping levels matching that of the Si NWs were also grown. Hall measurements require the electrical conduction confined within the layer [1.69]. An efficient way of achieving this is to grow B-doped Si layers on n-type wafers and use the space charge region at the film-wafer interface to block the current flow in vertical direction during measurements. The same was done here and the details are provided in Table 3.3 (HB1 – HB5).

3.2 Removal of Gold from Si NWs

As mentioned in Chapter 2, the MBE-grown Si NWs contain an Au cap on top and Au/Si nanoparticles on the sidewalls (see Figure 2.2). Au in Si NWs is unwanted for two reasons. Firstly, if diffused inside, Au can act as a mid-gap trap [3.2] in Si providing easy recombination centers for the charge carrier, and thus degrading the electrical conductivity. This is discussed more in details in connection with the results in Chapter 4. Secondly, the Au cap on a Si NW is unwanted for the following reasons. For electrical measurements, a direct Au-p-Si contact can be less Ohmic than the Pt/Ir-p-Si due to higher Schottky barrier height of the former [1.52, 3.3]. Due to heavy mass of Au, it can act as an effective ion-stopper during ex-situ doping of the NWs by ion implantation.

Therefore the Au caps on the Si NWs were removed by a wet etching with an aqueous solution of KI and I_2 prepared by mixing 20g of KI and 5g of I_2 with 100ml of deionized water (DI). The etch rate of a similar commercial etchant at room temperature is around 3nm/second [3.4]. The NWs were dipped in the etching solution for 5 minutes. However, this room-temperature etching did not remove the Au nanoparticles decorating the sidewalls of the NWs. Büttner et al. [3.5] found that these nanoparticles are much more strongly bound to the Si NW compared to the Au cap. However, it is possible to remove them in the following way. First the Au cap is removed from the Si NW at room temperature with the above Au-etchant. This was followed by a high temperature oxidation or annealing (at around 800°C) of the NWs. The thermal oxide grown during the oxidation process is removed with HF and subsequently the Au/Si nanoparticles on the lateral surface of the NWs are etched away with reapplication of the Au-etchant. However, the dopants in the NWs can diffuse and redistribute themselves during the high temperature (800°C) oxidation or annealing for an extended time, thus changing the original carrier profile.

Sample Number	Substrate 5" Si(111)		Buffer Layer	Au deposition	NW Growth	
	Type	Resistivity (Ω-cm)				
NWB1	p	5 - 10	200 nm Si/B @ T = 525°C (B source T = 1250°C)	2 nm Au @ T = 525°C	270 nm Si/B @ T = 525°C (B source T = 1250°C)	__
NWB2	p	5 - 10	200 nm Si/B @ T = 525°C (B source T = 1450°C)	2 nm Au @ T = 525°C	270 nm Si/B @ T = 525°C (B source T = 1450°C)	__
NWB3	p	5 - 10	200 nm Si/B @ T = 525°C (B source T = 1500°C)	2 nm Au @ T = 525°C	270 nm Si/B @ T = 525°C (B source T = 1500°C)	__
NWB4	p	5 - 10	200 nm Si/B @ T = 525°C (B source T = 1620°C)	2 nm Au @ T = 525°C	270 nm Si/B @ T = 525°C (B source T = 1620°C)	__
NWB5	p	5 - 10	200 nm Si/B @ @ T = 525°C (B source T = 1750°C)	2 nm Au @ T = 525°C	270 nm Si/B @ T = 525°C (B source T = 1750°C)	__
UNWB	p	5 - 10	200 nm Si/B @ T = 525°C (B source T = 1620°C)	2 nm Au @ T = 525°C	270 nm Si @ T = 525°C	__
UNWAs	n	0.001 – 0.006	__	2 nm Au @ T = 525°C	270 nm Si @ T = 525°C	__
MNWB	p	5 - 10	200 nm Si/B @ T = 525°C (B source T = 1620°C)	2 nm Au @ T = 525°C	135 nm Si/B @ T = 525°C (B source T = 1620°C)	135 nm Si @ T = 525°C

Table 3.2 Key growth parameters for the uniform in-situ B-doped (NWB1-5), undoped (UNWB and UNWAs) and in-situ modulation B-doped (MNWB) Si NWs. The Si deposition rate was always at 0.5Å/s from which the thicknesses are calculated. The chamber pressure during growth was around 10^{-9} mbar.

Sample Number	Layer
HB1	200nm Si/B @ T = 525°C (B source T = 1250°C)
HB2	200nm Si/B @ T = 525°C (B source T = 1450°C)
HB3	200nm Si/B @ T = 525°C (B source T = 1500°C)
HB4	200nm Si/B @ T = 525°C (B source T = 1620°C)
HB5	200nm Si/B @ T = 525°C (B source T = 1750°C)

Table 3.3 Key growth parameters for the uniform in-situ B-doped Si layers grown for measurement of carrier mobility by Hall effect with B-doping levels matching that of the uniform in-situ B-doped Si NWs reported in Table 3.2. All layers were grown on RCA-cleaned n-type 5" Si (111) wafers (resistivity 10 – 20 Ω-cm) with a Si deposition rate always at 0.5Å/s.

Therefore, for the Si NWs used for electrical measurements as well as ion implantation, only the Au caps were removed at room temperature leaving the Au/Si decorations on their lateral surface unaltered. It is worth noting that an attempt is made in this work to detect any Au diffused in the NW during growth, and the possible implications on the existence of Au in the Si NWs are discussed in Chapter 4.

3.3 Ex-situ Doping of Si NWs by Ion Implantation

As mentioned in Chapter 2, ion implantation for doping the Si NWs used in this work was carried out by first simulating the expected doping profiles with TRIM and then implanting them with the required ion energy and dose to achieve those profiles. Implantations were used to both uniformly dope the nominally undoped Si NWs with a single dopant specie, as well as to form an intra-NW p-n junction on the in-situ modulation-doped NWs. These two cases are described below. All implantations were carried out in Forschugszentrum Dresden-Rossendorf, Germany. Both high and low energy implanters (High Voltage Engineering Europa B.V.) were used as per the requirements.

3.3.1 Uniform Doping with a Single Dopant Specie

Nominally undoped NWs (samples from UNWB and UNWAs in Table 3.2) with their Au caps removed from top were chosen for the implantations in this case. The average length of the NWs was around 300nm. Multi-energy implantations were performed to obtain a uniform doping profile over the entire length of a NW, i.e. the final projected range was 300 nm. Boron implantation was performed on undoped Si NWs grown on p-type Si (111) wafers (UNWB in Table 3.2). The simulated/expected boron concentration was 10^{18} cm^{-3}. Both phosphorus and arsenic implantations were performed on undoped Si NWs grown on n-type Si (111) wafers (UNWAs in Table 3.2). The simulated/expected dopant concentration for phosphorus was 10^{19} cm^{-3} and for arsenic was 10^{18} cm^{-3}. In addition, high dose arsenic implantations were carried out to completely amorphize the Si NWs, and study their recrystallization upon annealing. The simulated dopant profiles are shown in Figure 3.4 and the implantation parameters for all the implantations are listed in Table 3.4. For each implantation, along with the NWs, a bare Si wafer was also included in order to measure the Hall mobility for the implanted doping level (WafAs, WafB1 and WafB2 in Table 3.4).

3.3.2 Formation of an Intra-NW p-n Junction

The p-n junction Si NWs were formed on the modulation-doped p-i NWs described in section 3.2 (MNWB in Table 3.2). After removal of their Au caps, these NWs were spin-coated with a spin-on-glass (SOG) silicon dioxide (Silicafilm, Emulsitone Co., USA) for 30 seconds at 3000 RPM. This thereby protected the substrate and the B-doped lower segment of the NWs from being implanted with P ions from the sides in the subsequent step. A two-step implantation of phosphorus ions at room temperature was used to obtain a rectangular dopant profile with a uniform phosphorus concentration of 10^{19} cm^{-3} over half the average length of the NWs. This should convert the i-type upper segment of the p-i-NWs to n-type and result in the p-n junction. The implantation parameters are listed in Table 3.4 (MNWB) and the resulting doping profiles along with a NW scheme are shown in Figure 3.5. After the post-implant annealing (see section 3.3.3), the remaining SOG was removed by a 60 seconds dip in HF (5%).

3.3.3 Post-implantation Annealing

Two types of thermal annealing were used in this work. For electrical activation of dopants in the NWs as well as the bare Si wafers that were not amorphized, RTA (Addax R100 at Forschungszentrum Dresden-Rossendorf) for 30 seconds was used. The experimental details are listed in Table 3.5. For boron implanted NWs and wafer (UNWB and WafAs in Table 3.5), an

annealing temperature of 850°C was used whereas for phosphorus and arsenic implanted NWs and wafers (UNWAs1, WafB1 and UNWAs2, WafB2 respectively in Table 3.5) two different annealing temperatures, 850°C and 1100°C, were used.

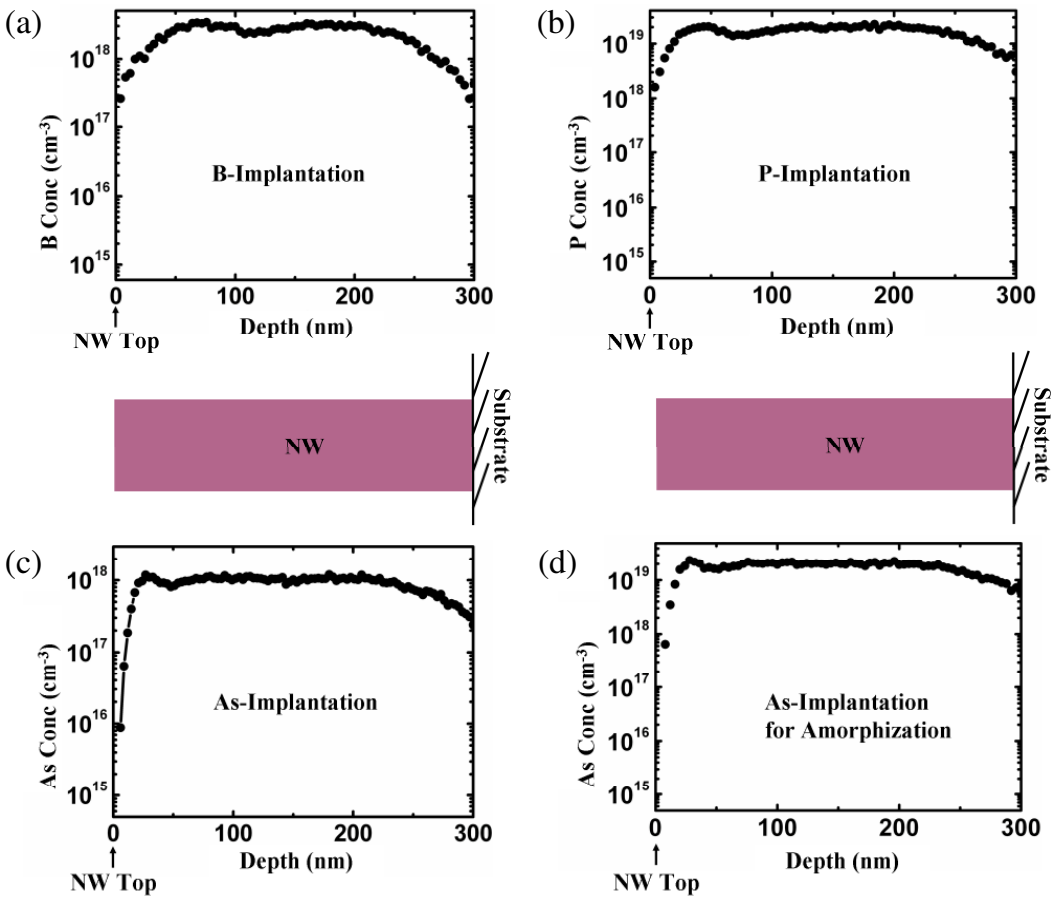

Figure 3.4 Dopant profiles in the implanted NWs simulated by TRIM for (a) B (b) P (c) As (d) As with an amorphizing dose. The 0 in the X-axis corresponds to the top of the NW.

For the recrystallization of fully amorphized NWs, both RTA and conventional furnace annealing were used. In this case, both a single step anneal and a sequential anneal were tried. The single step annealing by RTA was done at 800°C, 900°C, 950°C and 1050°C for 30 seconds each (UNWAs3a in Table 3.5) and in a furnace at 600°C and 650°C for five hours each (UNWAs3b in Table 3.5). For the sequential annealing, first a low temperature annealing at 550°C for one hour was performed which was followed by a high temperature annealing at 950°C for 30 minutes in a furnace (UNWAs3c in Table 3.5) and for 30 seconds by RTA (UNWAs3d in Table 3.5). In all cases the annealing was done in argon atmosphere.

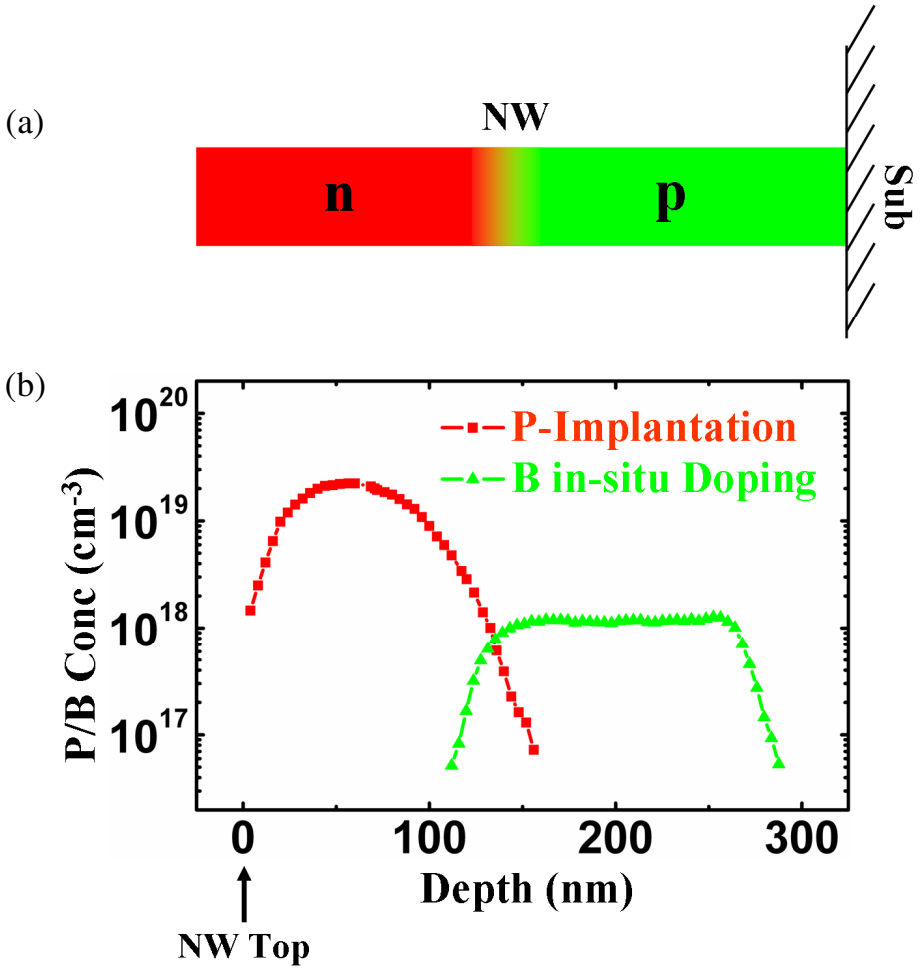

Figure 3.5 Intra NW p-n junction formation. (a) Scheme of a p-n junction NW. (b) Simulated implant profile for P (red) superposed with in-situ modulation doped profile of B measured by SIMS on an in-situ doped layer with the same doping level.

3.4 TEM Sample Preparations

For structural investigation, cross-sectional TEM samples were prepared using the conventional technique involving gluing two pieces together with an epoxy (M-Bond 610, Vishy Micro-Measurements, USA), cutting 3mm discs, polishing, argon ion milling and finally attaching them to a copper ring for support. Details of the sample preparation can be found in Ref. 2.35.

For analytical TEM, i.e. energy dispersive x-ray spectroscopy to detect any infiltration of Au into the NW, plan view samples were prepared using focused ion beam (FIB, Nova 600 NanoLab, FEI Company, Netherlands). TEM lamellas were prepared by embedding the free-

Sample Number	**Implant**		**First Implantation**		**Second Implantation**		**Third Implantation**		**Fourth Implantation**	
	Specie	**Expected Conc (cm^{-3})**	**Energy (keV)**	**Dose (cm^{-2})**	**Energy (keV)**	**Dose (cm^{-2})**	**Energy (keV)**	**Dose (cm^{-2})**	**Energy (keV)**	**Dose (cm^{-2})**
UNWB WafAs	B	$3x10^{18}$	55	$3.4x10^{13}$	35	$1.7x10^{13}$	15	$1.7x10^{13}$	____	____
UNWAs1 WafB1	P	10^{19}	140	$3.2x10^{14}$	70	$1.3x10^{13}$	25	$6.7x10^{13}$	____	____
UNWAs2 WafB2	As	10^{18}	300	$1.7x10^{13}$	140	$5.5x10^{12}$	80	$2.2x10^{12}$	30	$2.2x10^{12}$
UNWAs3	As	10^{19}	300	$3.3x10^{14}$	140	$1.1x10^{14}$	80	$4.45x10^{14}$	30	$4.45x10^{14}$
MNWB	P	10^{19}	45	$1.3x10^{14}$	25	$3.2x10^{13}$	____	____	____	____

Table 3.4 Implantation energies and doses for all the implantations used in this work. In each case, along with the NWs, a wafer was also implanted for measurement of carrier mobility by Hall effect. For details of the NWs refer to Table 3.2. WafAs was n-type Si (111) wafer (resistivity 10-20 Ω-cm), WafB1,2 were p-type Si (111) wafers (resistivity 5-10 Ω-cm)

Sample Number	Implant		First Anneal			Second Anneal		
	Specie	**Expected Conc**	**Type**	**T(°C)**	**Time**	**Type**	**T(°C)**	**Time**
UNWB WafAs	B	10^{18} cm^{-3}	RTA	850	30s	__	__	__
UNWAs1 WafB1	P	10^{19} cm^{-3}	RTA	850/1100	30s	__	__	__
UNWAs2 WafB2	As	10^{18} cm^{-3}	RTA	850/1100	30s	__	__	__
UNWAs3a	As	10^{19} cm^{-3}	RTA	800/900/950/1050	30s	__	__	__
UNWAs3b	As	10^{19} cm^{-3}	Furnace	600/650	5h	__	__	__
UNWAs3c	As	10^{19} cm^{-3}	Furnace	550	1h	Furnace	950	30m
UNWAs3d	As	10^{19} cm^{-3}	Furnace	550	1h	RTA	950	30s
MNWB	P	10^{19} cm^{-3}	RTA	850	30s	__	__	__

Table 3.5 Annealing type, temperature and time for all the implantations used. Refer to table 3.4 for the implantation doses and energies.

standing Si NWs in carbon and then lifting them out by cutting trenches with the FIB. Details of the sample preparation can be found in Ref. 3.6.

3.5 Electrical Measurement Setups

Three different electrical measurements were performed on the doped NWs and Si wafers/layers. They are briefly described below.

3.5.1 Measurement of Hall Mobility in Doped Si Wafers/Films

Hall measurements were performed on both the in-situ doped (HB1-5 in Table 3.3) silicon films and implanted (WafAs, WafB1, WafB2) silicon wafers using Ecopia HMS-3000 (Bridge Technology, USA) Hall measurement system. A scheme and an image of the actual measurement setup are shown in Figure 3.6(a) and (b) respectively. In-Ga alloy droplets (Alfa Aesar, USA) were applied on the four corners of a 1cm x 1cm sample (See Figure 3.6(b)) in order to obtain the Van der Pauw geometry [1.69, 3.8] for measuring Hall effect. Subsequently electrical connections were made to the contact pads by copper wire bonding. Ohmic contacts were first confirmed by measuring linear current-voltage characteristics between any two contacts of 1, 2, 3, 4 in Figure 3.6. Subsequently, reciprocal current-voltage measurements [1.69, 3.8] were done without applying any magnetic field and the sheet resistance was extracted from them. From the sheet resistance the computer program associated with the measurements calculated the resistivity of the in-situ doped/implanted layer taking into account the layer thickness. A permanent magnet of 0.55T was used and was mechanically reversed as shown in Figure 3.6(b) to change the direction of the magnetic field perpendicular to the sample. Hall voltage was measured by averaging the net voltages measured across specific contacts [1.69, 3.8] of 1, 2, 3 and 4 in Figure 3.6 under positive and negative magnetic field. From the measured Hall voltage, the program automatically calculated the doping density and mobility using the measured sheet resistance and supplied layer thickness. The measured Hall mobilities are reported in Chapter 4.

3.5.2 Measurement of the NW Resistance

For measuring the resistance of a NW, current-voltage measurements were performed by contacting individual NWs with a Pt/Ir tip inside an SEM (JSM6400, JEOL). Samples of 1cm x 0.5cm were cleaved and glued at the backside with highly conductive silver paste (G 302, Plano GmbH) to a copper stage which was attached to a chip carrier fitted to the stage of the SEM. Figure 3.7 shows an image of the setup. The pins of the chip carrier on which the copper stage

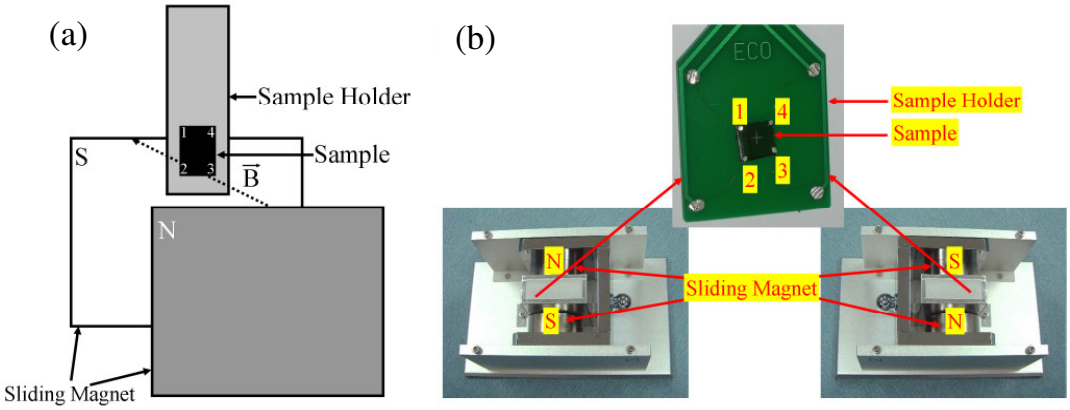

Figure 3.6 The Hall measurement set-up. (a) The schematic showing the sliding permanent magnet, sample holder and sample. (b) The actual measurement setup. (Reprinted from Ref. 3.7)

sits were electrically grounded along with the SEM stage. On the SEM stage, two micro-manipulators (MM3A-EM, Kleindiek Nanotechnik) were also fixed to which electrochemically etched Pt/Ir tips made from 25µm thick wires (Pt/Ir 80:20, GoodFellow) were attached. The tips were etched by the same procedure described in Ref. 3.9 and their average apex diameter was around 200nm. The micro-manipulators were operated with a joystick and had three degrees of freedom (r, θ, φ in spherical coordinate system) with a radial (r) resolution of 0.25nm, and angular resolution (θ, φ) of 0.1µrad each. The Pt/Ir tip attached to one of the micro-manipulators was connected to a picoammeter with an internal voltage source (Keithley 6487, ≤ 2fA noise) for the current-voltage measurements. The applied voltage could be varied between -12V to 12V and it could measure between 20fA to 20mA with a resolution of 10fA. With the electron beam on, the Si NWs as well as the Pt/Ir tip were imaged first. Subsequently the tip was moved with the joystick so that it makes a good contact with the top of the NW (see Chapter 4). The existence of an electrical contact was confirmed by the detection of a current by the picoammeter on application of a small voltage (~10mV). However, a 'good' contact strongly depended on the contact area between the tip and the NW and the force applied to the tip. It was not possible to measure the force on the tip. However a comparison between a 'good' and a bad 'contact' was made and it is included in the Appendix 4. With a 'good' contact established, the voltage was swiped stepwise from a positive to a negative value (confined within -1V to +1V due to the problem of self heating effect, see Appendix 4) with a step time of 1 second and the current was measured by the picoammeter. During the measurement, the electron beam was blanked to avoid its influence on the measured current. Differently doped NWs were measured with this technique and the results are discussed in Chapter 4.

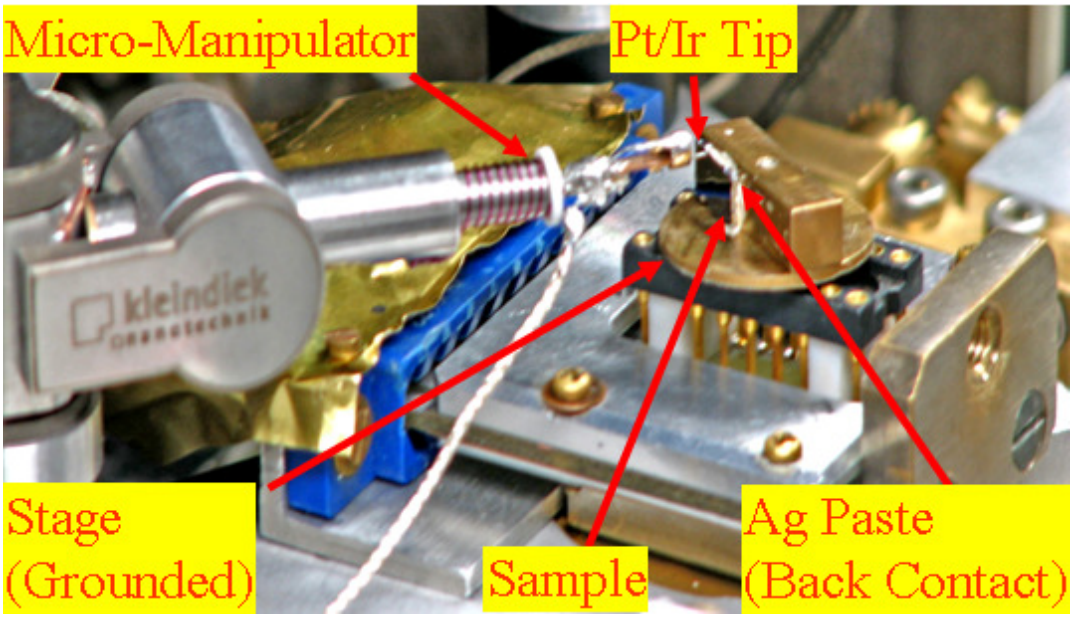

Figure 3.7 An image of the actual current-voltage, i.e. NW resistance measurement setup inside an SEM (JSM 6400, JEOL)

3.5.3 Measurement of NW Carrier Profiles

As discussed in Chapter 2, carrier profiles in individual NWs were extracted by measuring the local spreading resistance through scanning spreading resistance microscopy (SSRM). For the spreading resistance measurements, first the NWs were embedded in SiO_2 (~ 400 nm) grown by plasma enhanced chemical vapor deposition (PECVD). Subsequently the samples were glued with the same epoxy adhesive (M-Bond 610, Vishay Micro-Measurement, USA) used for cross-sectional TEM sample preparations to a dummy (a bare Si), and cut into 3mm x 1mm pieces. These pieces were lapped and ground first with SiC powder, and then polished with diamond powder. This reduced the thickness of the samples from around 625μm (~ thickness of the wafer on which the NWs were grown) down to around 100μm. An SEM image of a finished sample is shown in Chapter 4 where the NWs, the oxide matrix, the substrate and the dummy are indicated. The average roughness of the polished samples varied from 2nm to 10 nm which is illustrated with AFM topography images in Appendix 3. The SSRM measurements were performed using a conductive AFM system (Multimode Scanning Probe Microscope, Veeco Instruments) equipped with a conductive diamond coated Si tip (CDT-CONTR, NANOSENSORS) at Forschungszentrum Dresden-Rossendorf. An image of the measurement setup is shown in Figure 3.7.

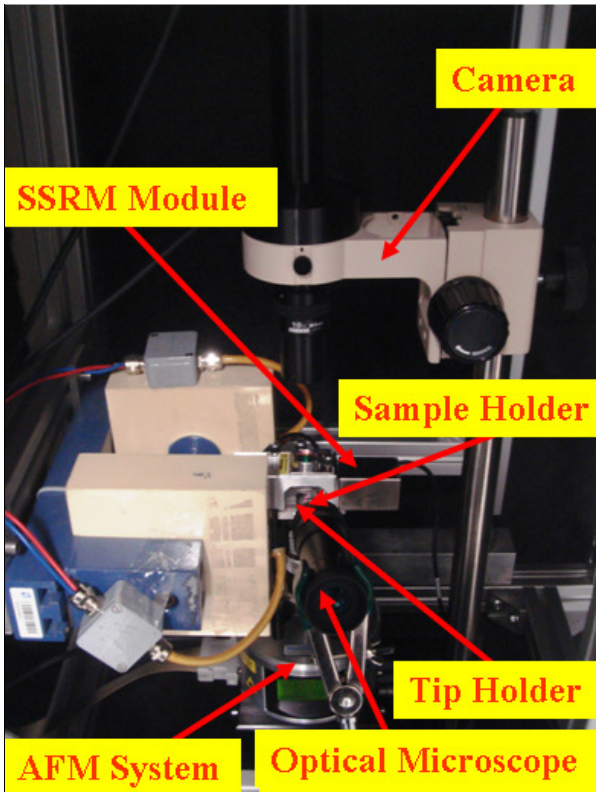

Figure 3.7 An image of the actual SSRM measurement setup using the conductive AFM system

As shown in the scheme in Figure 2.9, the electrical circuit consists of the AFM tip, the specimen including the NW embedded in the oxide matrix and the bulk substrate, and a logarithmic current amplifier in the SSRM module of Figure 3.7 to read out the signal. The measured current was in the range of 10pA to 0.1mA. For two-dimensional image scans a constant bias voltage of -2.5 V was applied between the tip and the specimen to achieve a reasonable signal to noise ratio. For indenting the sample surface and moving deeper into the volume by abrading material from the NW, a deflection voltage between 0.2 and 1.5 V was used to generate a higher force. During the measurements, the tip was always scanned perpendicular to the Si/SiO_2 interface (shown in Chapter 4) in the axial direction of the NW. The output of the SSRM measurement is the local spreading resistance values across the cross-section of the sample which can be duly converted to carrier concentration profiles and are discussed in Chapter 4.

Chapter 4

Results and Discussions

4.1 Morphology of the In-situ B-Doped NWs

Morphology of the in-situ B-doped Si NWs was investigated by a field emission SEM (JSM 6701F, JEOL) and are shown in Figure 4.1. Figure 4.1(a) and (b) show a plan view image of an ensemble of in-situ B-doped Si NWs (taken from sample NWB5 in Table 3.2) and a 45°-tilted image of the same (in a higher magnification) respectively. The intended B-doping was 10^{19} cm^{-3}. However, as mentioned above, this intended doping level only corresponds to the calibration curve in Figure 3.3 obtained from SIMS measurements on B-doped Si layers and will be verified with electrical measurements latter. The dark hemispherical cap on top of the NW is the solidified Au that initiated the NW growth when it was an Au/Si Eutectic droplet. As can be seen in Figure 4.1(b), unlike the CVD-grown in-situ doped NWs [1.58, 1.103], no significant tapering was observed in the MBE-grown in-situ B-doped NWs. This implies that in-situ doping mechanism as outlined in Section 2.3 did not increase the lateral growth rate of the NWs in comparison to the axial growth rate which is the case for the CVD-grown NWs. This reasonable uniformity in the shape of the B-doped NWs can be an added advantage for estimating their electrical properties where the geometry has to be taken into consideration. The morphology did not change with the doping levels as well. This further confirms that the boron flux did not influence the Si deposition and the NW growth rate.

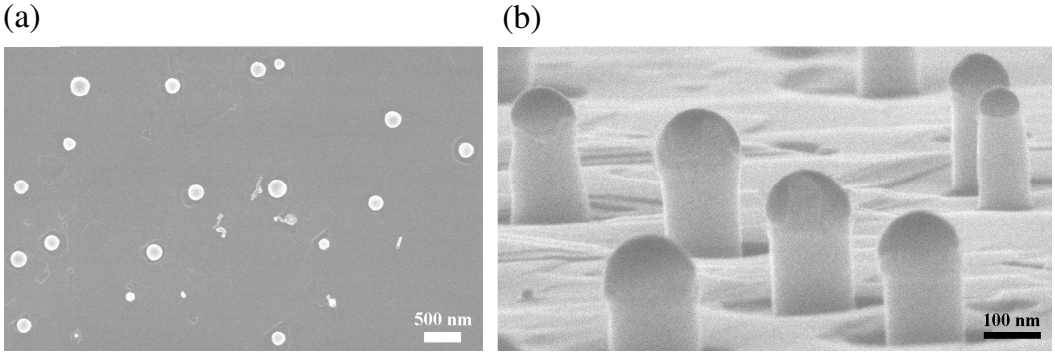

Figure 4.1 SEM image of (a) Plan view (b) 45°-tilted view of in-situ B-doped Si NWs. The intended B-doping level for these NWs was 10^{19} cm^{-3}.

From the top view images, the average diameter of the NWs for all doping levels (see Table 3.2) was calculated to be around 155nm (see Figure A4.1 in Appendix 4), and from the 45°-tilted images the average length amounted to around 350nm including the dark Au cap on top. For implantation and electrical measurements, the Au cap was removed which resulted in a decrease in the average height to around 300 nm.

4.2 Gold in Si NW

Like the undoped Si NWs grown by MBE (see Figure 2.2(c)), cross-sectional TEM (CM20 Twin, Philips) images of the in-situ B-doped Si NWs revealed Au existing on the grown Si NWs. The TEM image in Figure 4.2(a), taken from sample NWB5 in Table 3.2, shows the Au cap on top and the Au decoration on the sidewalls of an as-grown NW. The TEM image in Figure 4.2(b) shows a NW with the Au cap removed by wet etching described in Chapter 3.

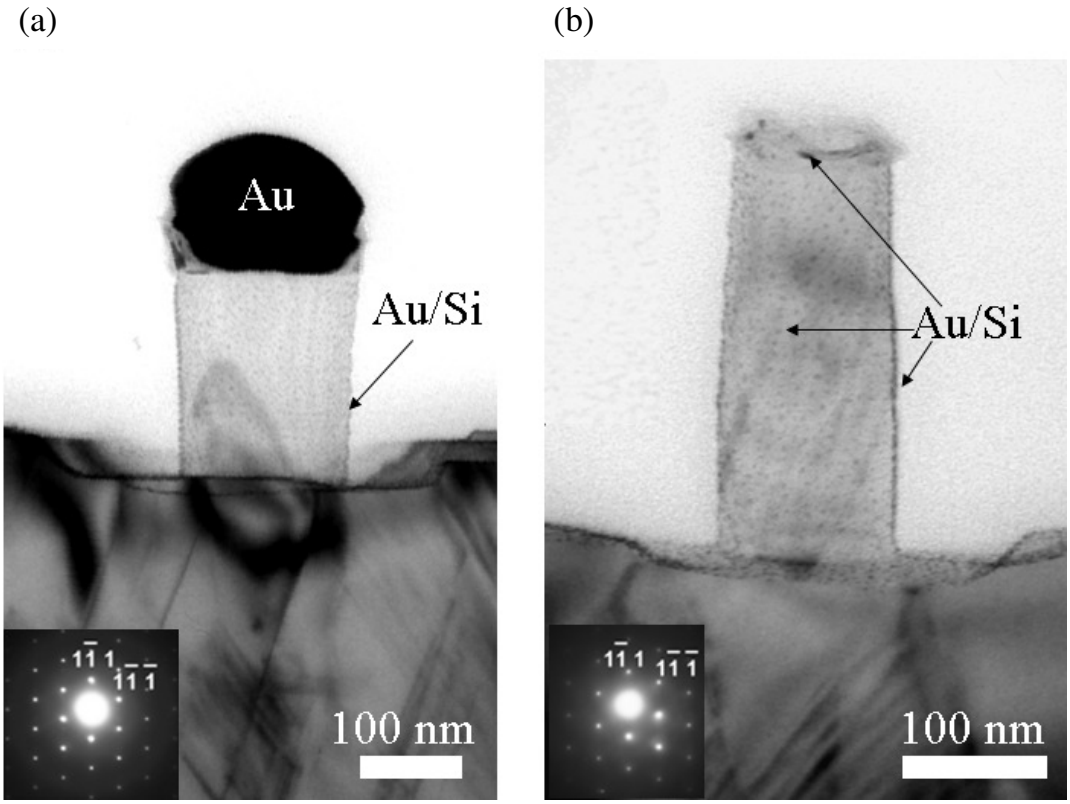

Figure 4.2 Cross-sectional TEM images of in-situ B-doped (intended doping ~ 10^{19} cm^{-3}) Si NWs. (a) An as-grown NW with both the Au cap on top and Au/Si nanoparticles on the sidewalls (b) A NW with the Au cap removed. The Au/Si nanoparticles remain. Insets of the images show SAED patterns confirming their crystallinity.

However, the decoration of Au/Si nanoparticles was not removed by this process. They are visible as tiny dark spots on the NW surface in Figure 4.2(b). As mentioned before, Au can form mid-gap levels (acceptor level at 0.35eV, donor level at 0.54eV) in the Si energy band [3.2, 4.1, 4.2] and thus can act as a carrier trap or recombination center reducing the free carrier concentration in the volume of the NW. Therefore, it is important to know whether any Au diffused into the volume of the NW during growth.

In order to probe if Au diffused into the Si NW during growth, TEM EDX (CM20 FEG, Philips) was performed on the plan-view Si NW samples prepared by FIB (Figure 4.3). Inset of Figure 4.3(a) shows the plan view TEM image of the top of the NW embedded in carbon with the red line (1-9) indicating the path of the EDX line-scan. An EDX spectrum was acquired at each of the equally spaced (~3nm) 9 points. The spectrum shown in Figure 4.3(a) is acquired at the point 4 which sits right at the periphery and falls on the outer surface of the NW. Along the entire line-scan a detectable AuLα peak (see Figure 4.3(a)) could be seen only at the point 4. No Au signal could be detected inside or outside of the NW (at the point 1 or 9 for example). This is clear from the intensity plot of the AuLα line in Figure 4.3(b). The Si Kα line is included in Figure 4.3(b) for reference. However, the detection limit of EDX is around 1% (atomic) which amounts to an Au concentration of 10^{20} cm^{-3}. At the Si NW growth temperature of 525°C the Au solubility in Si is only around 10^{14} cm^{-3} [4.1, 4.3]. Even at the annealing temperature of the ion-implanted Si NWs (850°C - 1100°C), the maximum solubility of Au in Si is around 10^{16} cm^{-3} [4.1, 4.3]. Therefore, a chemical detection of Au inside Si NWs by EDX is almost impossible. It must be mentioned that Perea et al. [1.71] could not detect Au in the CVD-grown Ge NWs using atom probe tomography. Putnam et al. [4.4] reported a maximum Au concentration of $1.7x10^{16}$ cm^{-3} in the CVD-grown Si NWs using Nano-SIMS. Using scanning transmission electron microscopy (STEM) Oh et al. [4.5] reported an Au concentration of ~ 10^{18} cm^{-3} inside MBE-grown Si NWs which is way above the solubility limit of Au in Si at 525°C mentioned above. However they mentioned that the probing electron beam could have influenced the measured value.

From the simulations (see Figure 3.4, 3.5), most of the ion implanted and annealed NWs in this work (see Table 3.4, 3.5) are expected to have a high doping level (>10^{18} cm^{-3}) which is orders of magnitude higher than the Au solubility at the annealing temperature (~10^{16} cm^{-3}). As a result, full compensation of free carriers by mid-gap Au traps can be neglected. For the in-situ B-doped Si NWs in this work (see Table 3.2), a variety of doping levels from 10^{15} cm^{-3} to 10^{19} cm^{-3} were used. However, as mentioned above, the maximum Au solubility at the growth temperature of 525°C is only around 10^{14} cm^{-3} which is not high enough to compensate all the activated dopants. Therefore, the effect of in-diffused Au (if any) on the electrical properties of

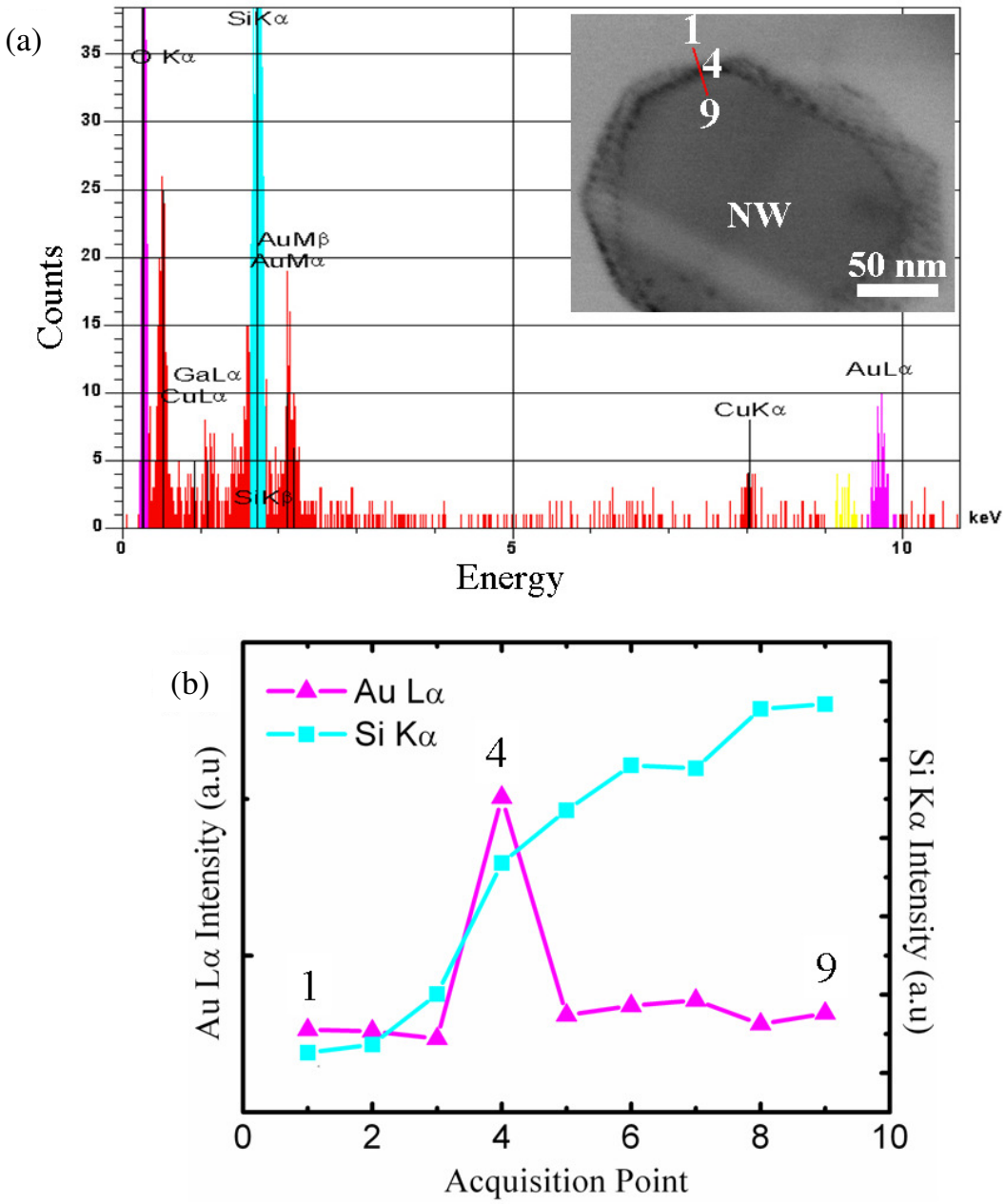

Figure 4.3 EDX analysis of a plan view in-situ B-doped (intended doping ~ 10^{19} cm^{-3}) Si NW. (a) The spectrum acquired at point 4 on the line-scan (1-9) shown at the inset. The black dots on the periphery of the NW at the inset are Au/Si nanoparticles, same as the ones seen in Figure 4.2(a). (b) Intensity variation of the AuLα peak along the EDX line-scan 1-9. Points 1, 4 and 9 are marked on the figure. Intensity variation of the SiKα line is included for reference.

the Si NWs is neglected for the analysis here. It should be noted that the Au/Si nanoparticles on the sidewalls of the NWs (Figure 4.2), may modify the local conductivity [4.6] at the surface of

the NWs as suggested by Bauer et al. [1.108]. A detailed investigation on these Au-Si nano-contacts is underway.

4.3. Microstructure of the In-situ B-Doped NWs

From the representative cross-sectional TEM images of Figure 4.2 it can be seen that the in-situ B-doped Si NWs grown in this work are free of any extended defect such as dislocation or stacking fault. The selected area electron diffraction pattern (SAED) shown at the inset of both Figure 4.2(a) and (b) prove that they are single-crystalline, oriented along the <111> direction, i.e. they are epitaxially grown. This is a significant difference from the in-situ B-doped CVD-grown NWs [1.58, 1.103] which often consist of a crystalline core and an amorphous shell.

It has been suggested [1.58] that the introduction of diborane (B_2H_6) as a precursor for B, enhances the rate of dissociation of silane (SiH_4), the precursor for Si, at the Au droplet. This leads to the deposition of amorphous Si. No such amorphization was observed for the MBE-growth Si NWs in this work at all B-doping levels. Unlike CVD, there is no cracking of the precursor involved either in growth or in doping of Si NWs in MBE. This further corroborates the fact that the Si incorporation rate was not significantly altered by the introduction of the B flux in MBE.

4.4 Hall Mobility in Doped Si Films

The measured Hall mobility for each in-situ B-doped Si layers (see Table 3.3) as well as for the implanted and annealed Si wafers (see Table 3.4/3.5) are listed in listed in Table 4.1. Along with the mobility, carrier concentration and resistivity of the layers were also measured to get an estimate of the electrical activation in the Si film/wafer and are reported in Table 4.1 as well.

The measured mobility values are substituted Equation 4.2 to calculate carrier concentrations. From Table 4.1 it can be clearly seen that the electrical activation is almost 100% for both in-situ and ex-situ doped Si thin films at all doping levels. The measured resistivity and mobility values match very well with the expected ones. These control experiments, therefore, show that both the in-situ and ex-situ doping techniques used here are quite effective in terms of dopant incorporation and activation in silicon films. Whether they are equally effective in doping Si NWs will be assessed in the next sections.

Sample Number	Dopant Specie	Expected Doping (cm^{-3})	Measured Doping (cm^{-3})	Expected Resistivity (Ω-cm)	Measured Resistivity (Ω-cm)	Expected Mobility ($cm^2V^{-1}s^{-1}$)	Measured Mobility ($cm^2V^{-1}s^{-1}$)
HB1	B	10^{15}	$7x10^{14}$	13.5	20	462	465
HB2	B	$3x10^{16}$	$1x10^{16}$	0.53	1.5	389	390
HB3	B	10^{17}	$9x10^{16}$	0.2	0.3	317	325
HB4	B	10^{18}	10^{18}	0.04	0.04	153	150
HB5	B	10^{19}	10^{19}	0.008	0.009	71	70
WafAs	B	10^{18}	10^{18}	0.04	0.04	153	150
WafB1	P	10^{19}	$5x10^{18}$	0.005	0.008	115	138
WafB2	As	10^{18}	$8x10^{17}$	0.02	0.02	284	311

Table 4.1 Expected and measured Hall mobility, doping (carrier concentration), and resistivity of differently doped Si layers/wafers. HB1-5 are in-situ B-doped Si layers while WafAs, WafB1 and WafB2 are implanted Si wafers

4.5 Electrical Property of the In-situ B-Doped NWs

This section is further subdivided according to the two different electrical characterizations pursued for this work.

4.5.1 Resistance of the B-Doped NWs

The resistance of the in-situ B-doped Si NWs listed in Table 3.2 were extracted from the current-voltage (I-V) characteristics measured by the technique described and illustrated in Chapter 2 and 3. An SEM image of a NW contacted with the Pt/Ir tip is shown in Figure 4.4. The measured I-V curves in the range of -0.5V to 0.5V for the NWs corresponding to different intended B-doping levels (N_{int}) are shown in Figure 4.5. N_{int} simply means the doping level that can be expected for a particular B source temperature from the B source calibration curve in Figure 3.3 during in-situ doping (see Table 3.2). A typical NW of comparable diameter (~ 155nm) and length (~270nm) was chosen for each N_{int} value. Broadly, the expected doping levels are divided into three categories – 1. nominally undoped and low-doped ($N_{int} = 10^{15}cm^{-3}$) (see Figure 4.5(a), (b)), 2. medium-doped ($N_{int} = 3x10^{16}$ and 10^{17} cm^{-3}) (see Figure 4.5(c)) and 3. high-doped ($N_{int} = 10^{18}$ and 10^{19} cm^{-3}) (see Figure 4.5(d)). As seen in Figure 4.5(a), the I-V curves of both the low-doped and nominally undoped NW look similar. Both of them show highly rectifying characteristics. This is explained latter. Both the medium-doped and high-doped Si NWs showed Ohmic or quasi-Ohmic I-V curves. However, the order of magnitude of the current changed from hundreds of nA for the medium-doped to hundreds of μA for the high-doped NWs in the same voltage range (-0.5V – 0.5V) implying an obvious increase of the electrical conductivity. The s-shaped I-V curve of the highest-doped NW ($N_{int} = 10^{19}$ cm^{-3}) results from self-heating as the current flowing through it is quite high (>300μA) at higher biases. In fact some of the NWs melted on applying a bias of 1V (see Figure A4.2 in Appendix 4). The Ohmic I-V curves result from an Ohmic contact between the Pt/Ir tip and the p-Si NW. The tip resistance was measured to be around 10Ω. The contact resistance between the tip and the NW can not be measured from a two-point measurement. The theoretical Schottky barrier height of this junction should be around -0.15V [1.52]. A negative barrier height is never measured in reality due to the unavoidable surface states at the metal-silicon interface [1.52, 3.3]. However, in order to estimate the contact resistance for the medium-doped NWs, this theoretical value was used which gave a contact resistance of around 350kΩ according to Equation 2.13 and 2.14, assuming the contact is formed across the entire cross section of a NW of diameter 155nm. This value of contact resistance can provide reasonable estimate for the medium-doped NWs (Figure 4.5(c)). The resistance (R) calculated from the slopes of the medium-doped NWs (Figure 4.5(c)), are 20MΩ for $N_{int} = 3x10^{16}$ cm^{-3} and 4MΩ for $N_{int} = 10^{17}$

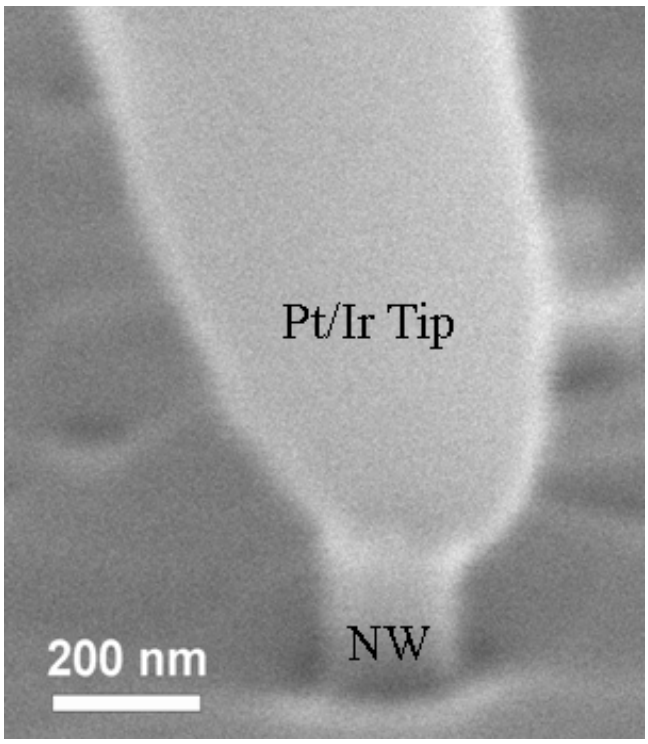

Figure 4.4 A B-doped Si NW contacted with a Pt/Ir tip for current-voltage measurement

cm^{-3} respectively, both of which are significantly higher than the theoretical value of the contact resistance (350kΩ). For the high-doped NWs (Figure 4.5(d)), tunneling of charge carriers will result in an exponential decrease of the contact resistance [1.52, 2.30, 3.3] with N_{int} as mentioned in Chapter 2. Most definitely the contact resistance is lowered by several orders of magnitude since the measured resistance from the slopes of the I-V curves in Figure 4.5(d) is 5kΩ for $N_{int} = 1x10^{18}$ cm^{-3} and 2kΩ for $N_{int} = 1x10^{19}$ cm^{-3}. In these cases, the theoretical specific contact resistance (ρ_C) should be lower than 10^{-7} Ω-cm^{-2} [4.7]. Assuming a limiting value of 10^{-7} Ω-cm^2, the contact resistance can be estimated as 0.5kΩ for $N_{int} = 10^{18}$ cm^{-3} and it should be even lower for for $N_{int} = 10^{19}$ cm^{-3}. Both of them are significantly lower than the corresponding NW resistances. The resistivity (ρ) of the NWs was calculated making use of Equation 2.15, i.e.

$$\rho = \frac{\pi D^2 R}{4l} \qquad [4.1]$$

where l is the length and D the diameter of the NW, measured from the SEM images (such as Figure 4.4) before measuring the I-V curves.

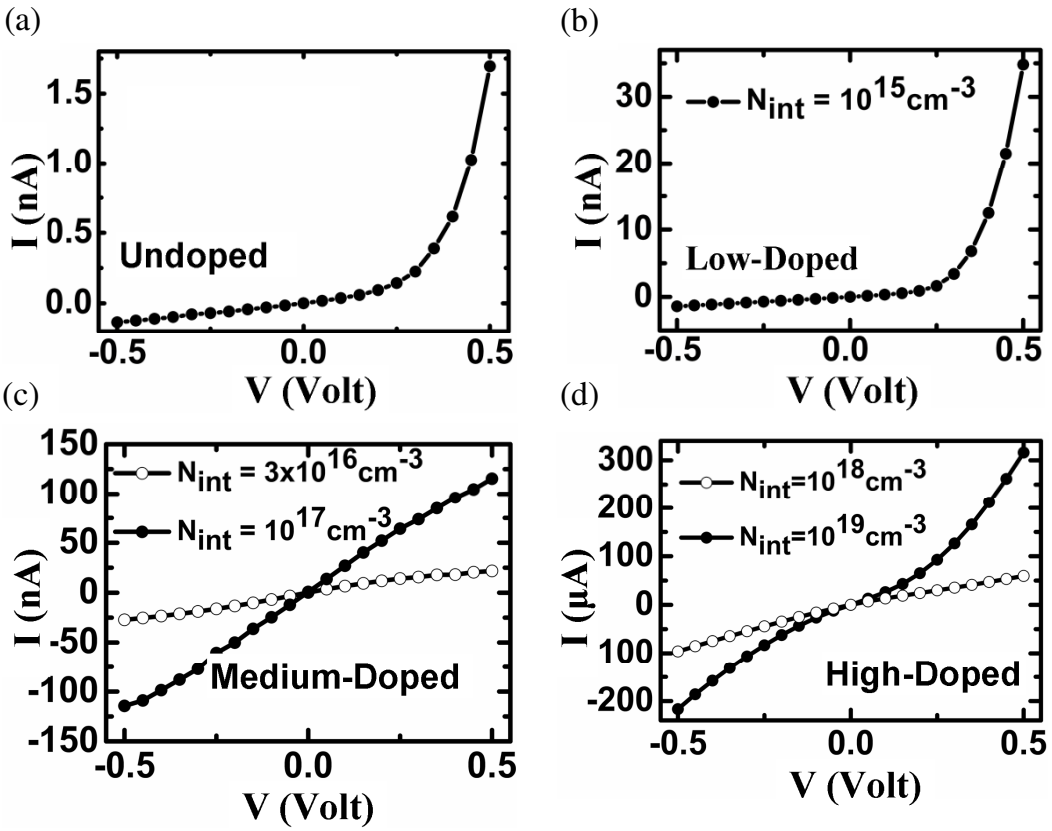

Figure 4.5 Current-Voltage (I-V) curves of (a) An undoped NW (b) A low-doped NW. (c) Two medium-doped NWs. (d) Two high-doped NWs. The intended doping levels are shown in the respective figures.

From the calculated resistivity, an apparent free carrier concentration (N_{app}) was calculated using Equation 2.5, i.e.

$$N_{app} = \frac{1}{e\rho\mu_p} \qquad [4.2]$$

It was termed the 'apparent concentration' since they were calculated assuming the whole NW is a cylindrical resistor without taking into account the surface depletion effects [1.76, 1.77]. Using the mobility (μ_p) values from Table 4.1, N_{app} values were calculated from Equation 4.2 and plotted against the intended doping levels in Figure 4.6. It can easily be seen in Figure 4.6 that for the medium-doped NWs, N_{app} falls orders of magnitude short of N_{int}. For $N_{int} = 3x10^{16}$ cm^{-3}, $N_{app} = 10^{14}$ cm^{-3}, and for $N_{int} = 10^{17}$ cm^{-3}, $N_{app} = 10^{15}$ cm^{-3}. For the high-doped NWs, the difference between N_{int} and N_{app} is less than an order of magnitude. For $N_{int} = 10^{18}$ cm^{-3}, $N_{app} = 4x10^{17}$ cm^{-3}, and for $N_{int} = 10^{19}$ cm^{-3}, $N_{app} = 7x10^{18}$ cm^{-3}. To explain this trend, the surface

depletion effect [1.76, 1.77] must be explicitly taken into account which is explained in the next section.

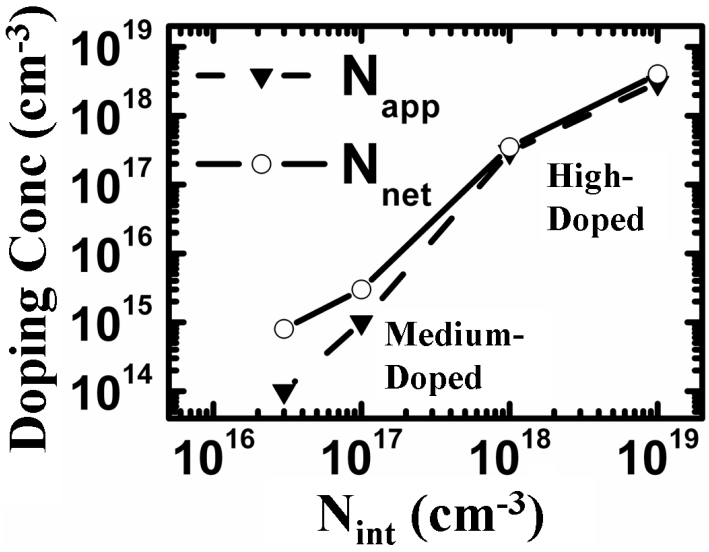

Figure 4.6 Apparent (N_{app}) and net (N_{net}) carrier concentrations of the NWs against the intended doping level. This serves as a calibration curve for in-situ B-doping of Si NWs in MBE. The error in N_{app} from the linear fitting (not shown) of the I-V curves in Figure 4.5 was 2.5%, 1%, 3% and 5% corresponding to N_{int} values of $3x10^{16}$, 10^{17}, 10^{18} and 10^{19} cm^{-3} respectively. The error in N_{net} obtained from the fittings in Figure 4.8 was 2% in all cases.

4.5.2 Surface Depletion in the NWs

It is well known that as soon as a 'fresh' Si wafer is exposed to air under ambient conditions, the Si surface starts to get oxidized at a very slow rate [4.8, 4.9]. This oxide, known as native silicon oxide, grows to around 1-2nm of thickness within a few hours [4.8, 4.9]. In the case of Si NWs, as soon as they are taken out of the MBE chamber, the native oxide starts to form on the outer surface of the NWs. As mentioned in Chapter 1, the Si/native oxide interface is characterized by unsatisfied or dangling bonds that give rise to electronic defects known as surface states with energy levels within the bandgap of silicon [1.52]. These surface states can effectively act as electron/hole trap by capturing the free electrons from the volume of the Si NWs, and thus deactivating them for current conduction through the volume. This creates an excess of charges on the surface which is balanced by bending of the conduction and valence energy bands of the NW even without the application of an external bias. This is called surface pinning of the Fermi level. A schematic illustration of surface depletion and Fermi level pinning for a p-type Si NW is shown in Figure 4.7(a) and (b) respectively. Due to the loss of free

carriers from the volume of the NW, the effective conductive cross-section of the NW reduces. Seo et al. [1.77] proposed a model to explain the surface depletion in Si NWs. This model is applied to explain the electrical properties of the NWs presented here. It is assumed that a uniform surface charge density of N_s exists at the outer surface of a NW at the interface between Si and the native oxide. It is also assumed that for a cylindrical NW of physical diameter D (determined from the SEM image before measurement), the surface depletion reduces the effective conductive region to a uniform cylindrical core of diameter d. In order to have an electrostatic balance of the total charges, the total charge contained in the shell of thickness (D-d)

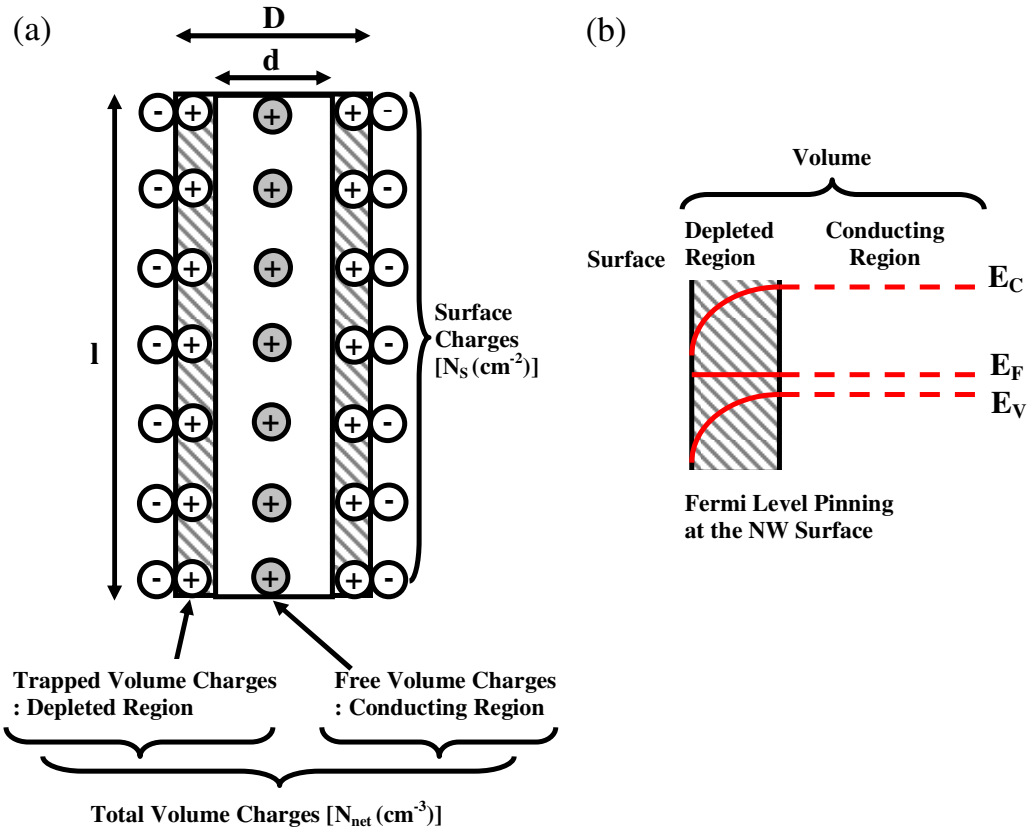

Figure 4.7 (a) Schematic illustration of surface depletion in a p-type NW by the surface charges. With a charge density of N_S cm^{-2}, the surface charges (negative in this case) uniformly deplete the NW of free carriers. If l is the length and D the physical diameter of the NW, it's real conductive diameter is reduced to d. The net free carrier concentration averaged over the entire NW volume is N_{net} cm^{-3}. (b) Fermi level pinning of the surface depleted NW. E_C, E_V and E_F refer to the conduction, valence and Fermi energy levels respectively.

surrounding the core should be equal to total surface charges, i.e.

$$\frac{\pi}{4}(D^2 - d^2)lN_{net} = \pi DlN_s \qquad [4.3]$$

where N_{net} is the net or average free carrier density in the total volume of the NW including both the core and the shell. Combining Equation 4.1 and 4.3

$$\frac{R}{l} = \frac{\frac{4\rho}{\pi}}{D^2 - \frac{4N_S}{N_{net}}D} \qquad [4.4]$$

The resistance per unit length can be measured for NWs of different diameters (D) and lengths, and the data can be fitted against D. Figure 4.8 shows the measured data and the fitted curves of resistance per unit length for different doping levels. It can clearly be seen that the resistance per unit length increases according to Equation 4.4 as the diameter of the NW decreases. Physically it means that for the same surface charge density, thinner NWs get more strongly depleted by than the thicker ones since the carrier-depleted shell region (see Figure 4.7(a)) extends more into the core of the NW. It can also be seen that as the intended doping level is increased, the decrease of resistance per unit length becomes less abrupt with the increase of NW diameter. For an intended doping level of $3x10^{16}$ cm^{-3} (Figure 4.8(a)) the resistance per unit length falls much more steeply than for an intended doping level of 10^{19} cm^{-3} (Figure 4.8(d)). This is due to the fact that as the doping level increases, the surface depletion effect subsides. For the same surface charge density, the ratio N_s/N_{net} decreases with the increase of N_{net}, rendering the second term in the denominator of Equation 4.4 less significant. As a result, the diameter dependence of R/l becomes more inverse parabolic like a uniformly charged solid cylinder. The average value of surface charge density extracted from the fits was $2x10^{10}$ cm^{-2} which is lower the standard value for Si thin films, i.e. ~ 10^{12} cm^{-2} [1.52]. N_{net} was also extracted from the fitted curves for each doping level and plotted against the doping level in Figure 4.6 along with N_{app} values extracted earlier. It can easily be seen that the N_{net} values are always higher than the N_{app} values for medium doping levels. For higher doping levels, the difference between N_{app} and N_{net} is significantly reduced since the surface depletion itself is not as strong as the medium-doped ones.

Using the extracted value for N_S, i.e. $2x10$ cm^{-2}, it can also be shown by using Equation 4.4, that both the undoped and the low-doped NW will be fully depleted, i.e. devoid of any free carriers. The rectifying I-V curves for these two (see Figure 4.7(a) and (b)), as verified by Bauer et al. [1.108] using electron beam induced current (EBIC) measurements, comes from the junction at

the base of the NW between the fully depleted NW and the undepleted epi-layer (see Figure A4.4 in Appendix 4).

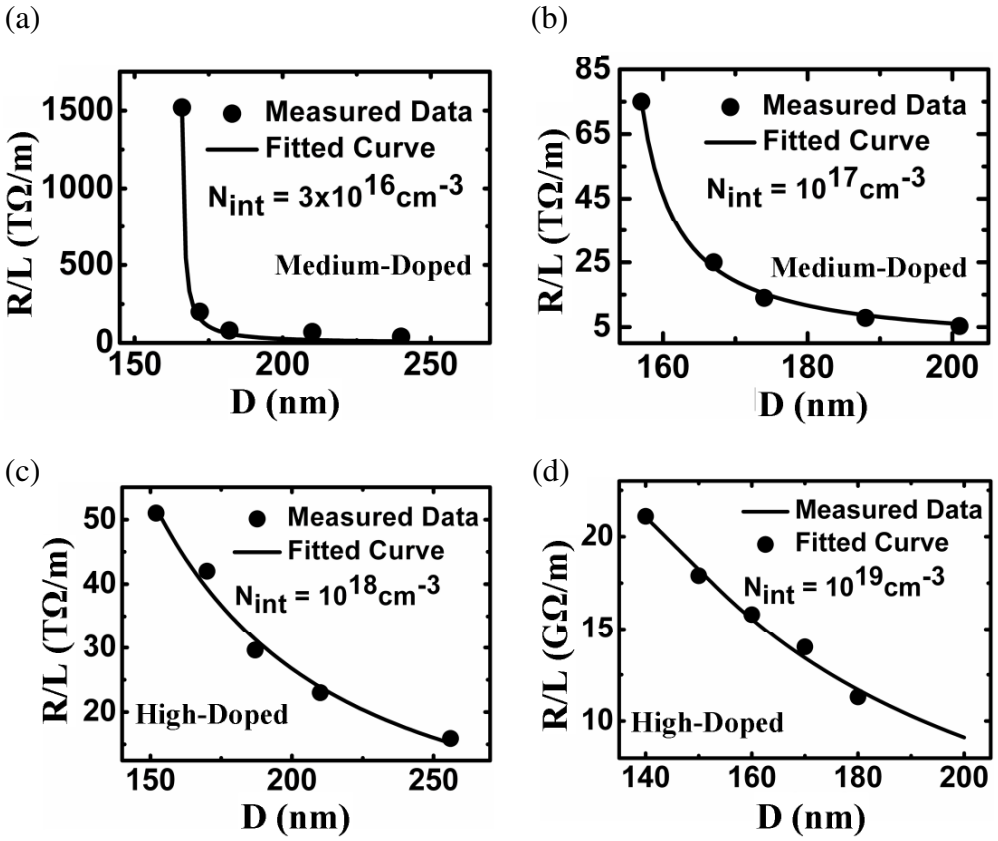

Figure 4.8 Variation of resistance per unit length (R/L) with diameter and intended doping (N_{int}) levels of NWs (a), (b) Medium-doped NWs and (c), (d) High-doped NWs. Both the measured data and the fitted curves using Equation 4.4 are shown in each case.

It is clear from the above discussion that surface charges heavily curtail the electrical conductivity of the in-situ B-doped Si NWs investigated here unless the doping level is significantly high (>10^{18} cm^{-3}).

4.5.3 Error Analysis I

There are a few sources of error in the NW resistance measurements performed with the micro-manipulator. Subsequently, these errors affect the quantification of N_{app} and N_{net}.

Firstly, a stable contact between the NW and the tip is a necessity so that the contact pressure does not change during measurements. The contact pressure can be changed by pressing the tip

harder on top of the NW. It was observed that the contact pressure variation can change the measured current by almost three orders of magnitude (see Figure A4.3 in Appendix 4). Too high contact pressure, however, damaged the Pt/Ir tip. It is difficult to quantify this variation as the contact force/pressure can not be measured. Therefore, all the measurements were obtained for maximum current flow without damaging the tip or the NW.

Secondly, the actual tip-NW contact area is assumed to be the entire radial cross-section of the NW which may not be the case always. The NW top is not completely flat, and therefore it is possible that the tip does not contact the entire radial cross section of the NW on top. In addition, there exists an interfacial native silicon oxide layer all around the NW which can strongly modify the contact properties.

Thirdly, the contact resistance, although theoretically much smaller than the measured resistance as discussed above, is completely disregarded for all calculations. This may influence the N_{app} and N_{net} values as well.

From the linear I-V curves of Figure 4.5, a fitting error of 2.5%, 1%, 3% and 5% for N_{app} values $9x10^{14}$, $5x10^{15}$, $3x10^{17}$ and $3x10^{18}$ cm^{-3} (see Figure 4.6) was calculated. The error from fittings in Figure 4.8 in the extracted values of N_{net} was around 2% in all cases.

4.5.4 Carrier Profile in a Single B-doped Si NW

As explained in Chapter 2 and 3, SSRM was used to measure the carrier profile in a single NW. In order to obtain the highest resolution [2.33], a NW from the high-doped (10^{18} cm^{-3}) sample was used. Figure 4.9(a) and (b) shows SEM images of a plan view and a cross-sectional SSRM sample respectively. The NWs are indicated along with the substrate, the embedding oxide matrix and the dummy wafer used (for cross-section).

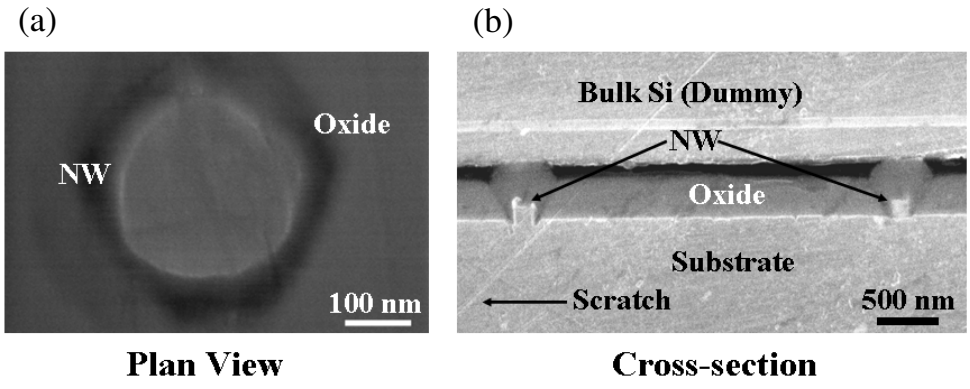

Figure 4.9 An SEM image of a (a) Plan view (b) Cross-sectional SSRM sample.

Also noticeable in Figure 4.9(b) is a long scratch line that resulted from polishing of the sample. Figure 4.10(a) and (b) show the SSRM images of a NW in a plan-view and axial cross-section respectively. A brighter contrast in the image signifies lower spreading resistance, i.e. higher conductivity while a darker contrast signifies lower conductivity. It is clear from the plan view image that the conductivity of the NW is higher near the surface. The surrounding SiO_2 is uniformly dark owing to its high resistance. The axial cross-section in Figure 4.10(b) clearly exhibits a difference in contrast from the substrate (Sub) to the epi-layer (Epi) and the NW. This is due to lower doping level ($1.3x10^{15}$ cm^{-3} corresponding to the resistivity of 10 Ω-cm) of the substrate as compared to the expected doping level of 10^{18} cm^{-3} in the NW and epi-layer. The dark lines in the epi-layer result from similar scratches as indicated in Figure 4.9. It highlights the importance of a highly perfect specimen polishing without mechanical surface defects.

The measured average spreading resistance (R_S) values from Figure 4.10(b) in axial and radial directions are plotted in Figure 4.11(a) and (b) respectively. Figure 4.11 also shows the carrier concentrations (right Y-axis) that were extracted from the measured spreading resistance (R_S) values in the following way.

The resistivity of the substrate was known from the specification of the wafer, and the epi-layer was assumed to be doped to 10^{18} cm^{-3} (also confirmed by SIMS (see Figure 3.2(a)) and Hall measurements (see Table 4.1) on similarly doped layers). Therefore, the resistivity values of the NW were derived using linear scaling of R_S values as per Equation 2.16. It was assumed that the electrical radius (a) remains constant during an entire image scans. Since a higher carrier concentration is more desirable for calibration than a lower one [2.33], the ρ values in the NW were obtained from the epi-layer by scaling the corresponding R_S values. Since the data in the entire epi-layer is not noise-free owing to the scratches (see Figure 4.10(b)), R_S values from only a relatively noise-free small segment of the SSRM profile marked as AB in Figure 4.11(a) was used for calibration. The ρ values were then converted to carrier concentrations by using the standard carrier concentration vs. resistivity curve (see Figure A2.1 in Appendix 2) that takes into account the concentration dependent mobility of holes (majority carriers).

The extracted carrier concentrations in the NW (Figure 4.11(b)) are close to the expected doping level of 10^{18} cm^{-3} near the surface and dips to $6x10^{17}$ cm^{-3} near the center of the NW. This is consistent with the plan view SSRM image in Figure 4.10(a) that indicates higher conductivity near the surface. Such a 'core-shell' type of profile probably originates from the inherent inhomogeneity of the doping process of Si NWs. As indicated in Figure 2.3, dopant incorporation into the Si NW in MBE occurs both through the Au droplet on top and through the sidewalls of the NW. This way, the surface always accumulates more dopant than the bulk of the NW since both dopant fluxes I_{B1} and I_{B2} effectively add dopants to the surface while only

I_{B1} contributes to the bulk. Although an exact kinetics of doping can't be formulated from these profiles, the results confirm that in-situ doping of Si NWs in MBE do suffer from surface accumulation of dopants. It must be mentioned that surface depletion of carriers as illustrated in the previous section also occurs in this case. However, for the measured NW of diameter (D) 180nm, using $N_{net} = 10^{18}$ cm^{-3}, and $N_S = 2x10^{10}$ cm^{-2}, we get d = 179nm from Equation 4.3. This implies that the depletion width (D – d) is only 1nm. At present the SSRM measurement is limited to a resolution of around 10nm. This is why it is challenging to see a depleted shell of thickness 1nm just below the surface.

4.5.5 Error Analysis II

There are a few sources of error in an SSRM measurement. Firstly, as mentioned already, the polishing of the sample surface is extremely important since any surface defect such as a scratch (see Figure 4.10(b)) will drastically change the measured resistance. This noisy data introduces a high error in the extracted carrier concentration. The error in treating the epi-layer of constant doping (i.e. 10^{18} cm^{-3}) was around 25% which subsequently introduced a 25% error in the carrier concentration values in the NW shown in Figure 4.11(b).

In order to suppress the effect of the surface defects, a higher deflection voltage can be applied so that the AFM tip can press harder on the sample. However, drastic change in spreading resistance was observed with the deflection voltage. R_S changed by two orders of magnitude as the deflection voltage was increased from 0.2V to 1.5V (see Figure 4.5 and 4.6 in Appendix 4). Therefore the extracted carrier concentration values in Figure 4.11, measured at a deflection voltage of 0.8V, can be off by an order of magnitude.

Thirdly, the simple formula exhibiting a linear scaling between R_S and the local resistivity (ρ) as shown in Equation 2.16 is not very accurate. Wolf et al. [4.10] have shown that R_S depends on a barrier resistance ($R_{barrier}(\rho)$) related to the combined effect of the actual tip shape, surface states, contact force (related to the deflection voltage) etc. In that case,

$$R_S = \frac{\rho}{4a} + R_{barrier}(\rho) \qquad [4.5]$$

Therefore, it is important to measure a calibration curve by using a thin film sample with multiple 'known' doping levels. In this work, the calibration was done only with respect to a single 'known' doping level. The advantage of this procedure is that the calibration is done in the same sample as the NWs. However, at the same time it probably increases the margin of error in the measurements.

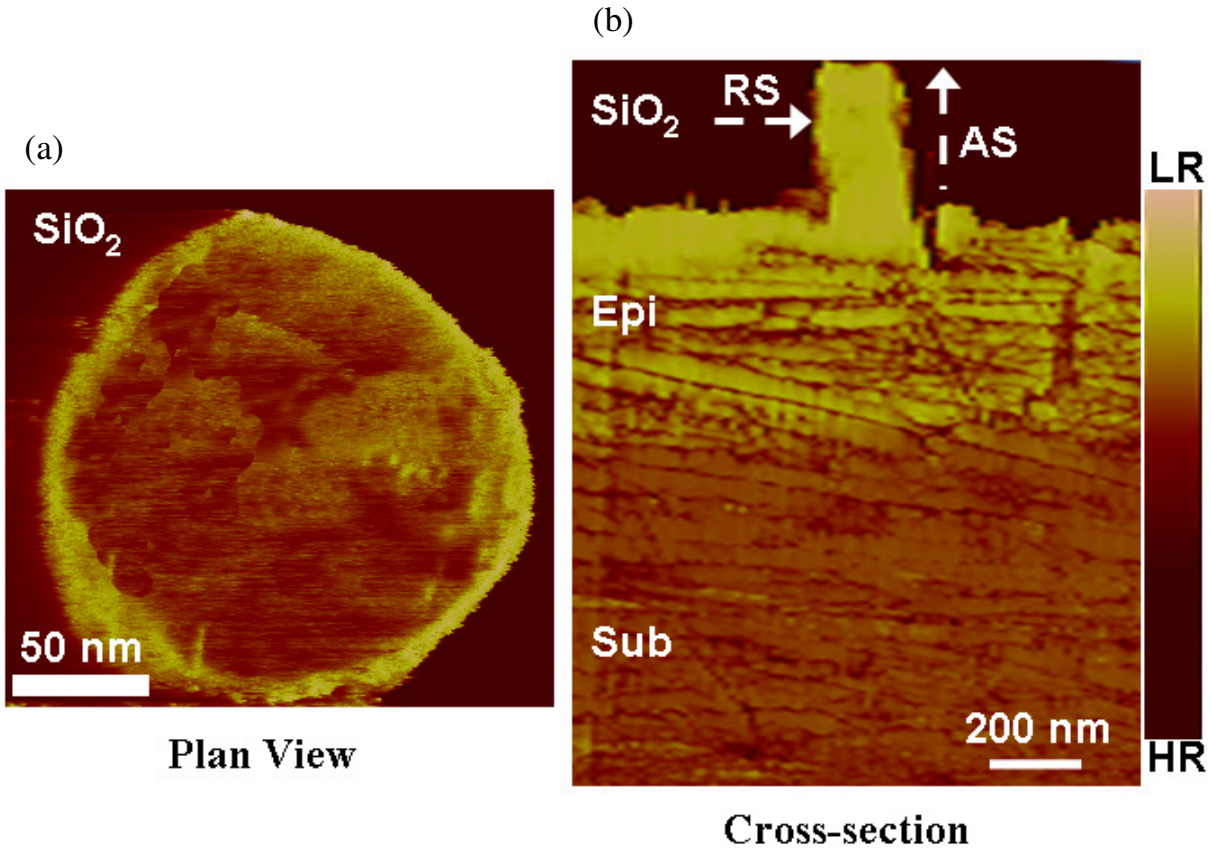

Figure 4.10 (a) Plan view (b) Cross-sectional SSRM image of an in-situ boron-doped NW. Note that the dark lines in (b) are scratches resulting from the mechanical polishing as explained in Figure 4.9. In the spreading resistance scale bar at the right, LR means low resistance and HR means high resistance implying that lighter areas in the images are more conductive than the darker ones.

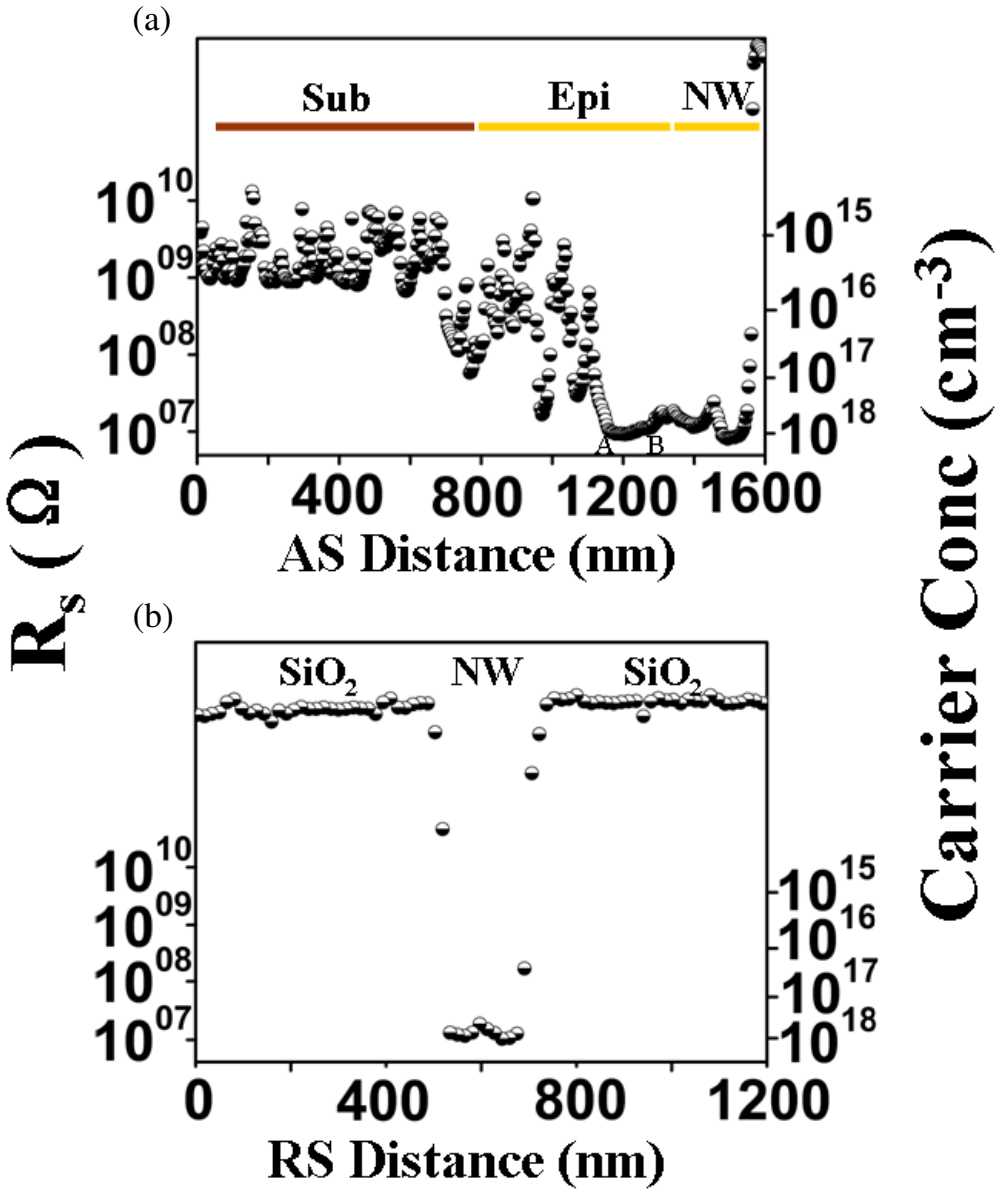

Figure 4.11 R_S (left) and carrier (right) profiles extracted from the SSRM image shown in Figure 4.10. (a) The average profiles in axial direction (AS). (b) The average profile in radial direction (RS). The estimated error in quantifying the carrier concentration was around 25%.

4.6 Uniformly Ion Implanted Si NWs

Since the uniformly ion-implanted Si NWs were originally undoped (sample UNWB, UNWAs, see Table 3.2) their morphology and crystal structure before implantation were the same as the in-situ doped NWs discussed in the previous section. In this section, the implantation-induced changes of structural and electrical properties of the NWs are discussed. Specific attentions are

paid to recrystallization of NWs that were fully amorphized by heavy As ion implantation, and dopant profile of a P implanted NW.

4.6.1 Microstructure of the Implanted NWs

Figure 4.12 shows the TEM images of as-implanted and annealed NWs for B (UNWB in Table 3.4/3.5), P (UNWAs1 in Table 3.4/3.5) and As (UNWAs2 in Table 3.4/3.5) implantations. It can clearly be seen that the all the NWs in Figure 4.12 (as-implanted as well as annealed) are single-crystalline like the as-grown NWs in Figure 4.2. No secondary defects such as dislocation loops were observed in the NWs. However, sometimes extended defects like stacking faults (Figure 4.12(c), (e)) and dislocation loops (Figure 4.12(f)) were observed in the epi-layer underneath the NWs.

These results are particularly interesting because they show that relatively high implantations can be performed without damaging vertical nanostructures. The actual doping levels, however, have to be assessed from electrical measurements.

4.6.2 Recrystallization of Fully Amorphized NWs

The high As implanted NW (UNWAs3 in Table 3.4) was fully amorphized. This is evident from the uniform grey contrast in the entire NW as well as in the epi-layer next to it in the TEM image of Figure 4.13(a). The SAED pattern (top left inset) taken from the NW shows the Debye-Scherrer rings typical for amorphous materials. Underneath the NW, a concave shaped amorphous-crystalline (a-c) interface is visible and is indicated with a dotted line in Figure 4.13(a). Such curvy interface was observed for all as-implanted NWs. However, for shorter NW (length ~ 200nm or less), the interface lied much below (>100nm) the base of the NW (see Figure A4.7 in Appendix 4). It is interesting to notice that the a-c interface in the epi-layer in Figure 4.13(a) is relatively much more flat than that in the NW. Figure 4.13(b) and (c) show high resolution TEM (JEM-4010, JEOL) image of the NW in Figure 4.13(a) taken from the bulk of the amosphous region (green box) and from the a-c interface (red box) respectively. It is clear from these two images that although some small crystalline pockets are present at the amorphous side of the a-c interface in Figure 4.13(c), no such pocket is present in the bulk of the amorphous region (Figure 4.13(b)). This signifies that the amrophization was complete.

Figure 4.14(a) and (b) show the result of one step annealing in a furnace at 600°C (UNWAs3b in Table 3.5) and in RTA at 900°C (UNWAs3a in Table 3.5) respectively. It is obvious that both figures look similar. As confirmed by the SAED pattern at the top inset Figure 4.14(a), the top

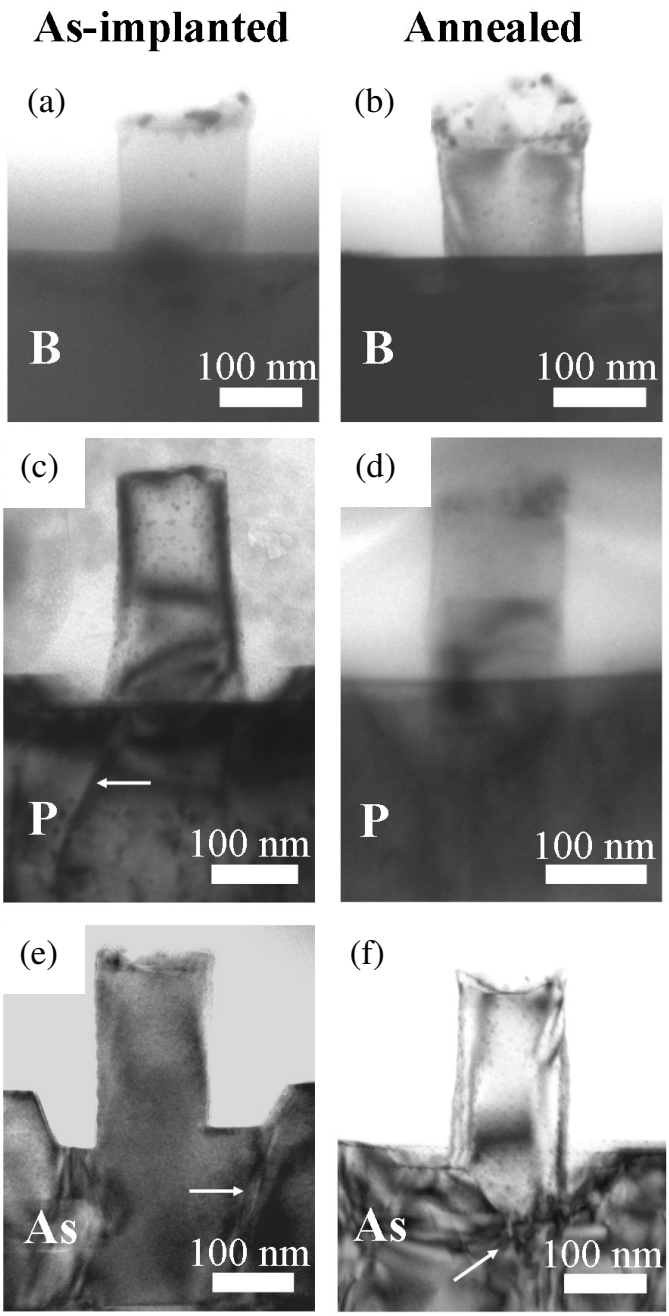

Figure 4.12 Cross-sectional TEM image of a (a), (b) B-implanted NW (UNWB) before and after annealing; (c), (d) P-implanted NW (UNWAs1) before and after annealing; (e), (f) As-implanted NW (UNWAs2) before and after annealing. In this case, annealing for the B-implanted NW was done at 850°C for 30s while that for both P and As-implanted ones was done at 1100°C for 30s. The arrows indicate defects, i.e. stacking faults in case of (c) and (e), and dislocation loops in case of (f).

part of the NW is polycrystalline. The small dark areas in the top part are single grains. They are more clearly visible in the HRTEM images of Figure 4.14(c). The grain diameter varied from 5 to 20nm. The bottom part of each of the NWs is single-crystalline with <111> orientation which is confirmed by the corresponding SAED pattern (bottom inset in Figure 4.14(a)).

If the annealing temperature is not above the silicon melting point, i.e. 1400°C, it enables recrystallization of the amorphous silicon (a-Si) via a mechanism called solid phase epitaxial regrowth (SPER) [4.11, 4.12] wherein the random network of a-Si arranges itself in the same crystal orientation as the substrate underneath starting from the a-c interface. The regrowth velocity of SPER in <111> direction amounts to only 1 nm/min at 573.5°C [4.13]. Assuming this rate, for a 5 hour anneal in a furnace, the regrown c-Si should be around 300nm. This is what can be seen in the regrown epi-layer where the end of range (EOR) defects appears at around 300nm from the surface, and the regrown part is fully single-crystalline. Even though some residual defects are observed in the epi-layers (Figure 4.14(a), (b)), no poly-Si could be found. This elaborates the difference between two-dimensional and three-dimensional recrystallization.

The poly-Si grains in the NW are formed by a process known as the random nucleation and growth (RNG) [4.14] wherein nucleation occurs in random directions seeding from small crystallites or even crystal defects. The surface of a NW is a sink of broken bonds that can serve as nucleation sites to initiate RNG. Since no pre-existing crystallite was found in the volume of the as-implanted NWs, it is assumed that the random grains formed are nucleated at the surface and proceeded laterally. Eventually they collided with the SPER growth front moving up from the bottom of the NW which led to the termination of SPER. RNG and SPER probably start simultaneously at the annealing temperatures used because both very short time (30 seconds) anneal in RTA and long time (5 hours) anneal in a furnace yield the same result. Unless RNG is suppressed, a recovery of the single-crystalline structure of the NW by SPER is nearly impossible.

It is difficult to measure the regrowth velocity in the NW due to the irregular shape of the a-c interface. However, the ratio between the average length of the single-crystalline bottom part ($L_{c\text{-}Si}$) and the total length of the NW (L_{NW}) for both a furnace anneal (600C°, 5 hours) and RTA (900°C, 30 seconds) increased with L_{NW} (see Figure A4.8 in Appendix 4). In both cases the ratio increased monotonously. As mentioned above, for shorter than average NWs the a-c interface lies much below the base of the NW (see Figure A4.7(a) in Appendix 4). Since the constrained amorphous volume in the NW is further away from the single-crystalline substrate, the probability of RNG increases. When such a short NW undergoes a single step anneal, almost the

whole of it turns polycrystalline (see Figure A4.7(b) in Appendix 4). The same phenomenon was observed for all the single step anneals listed in Table 3.5.

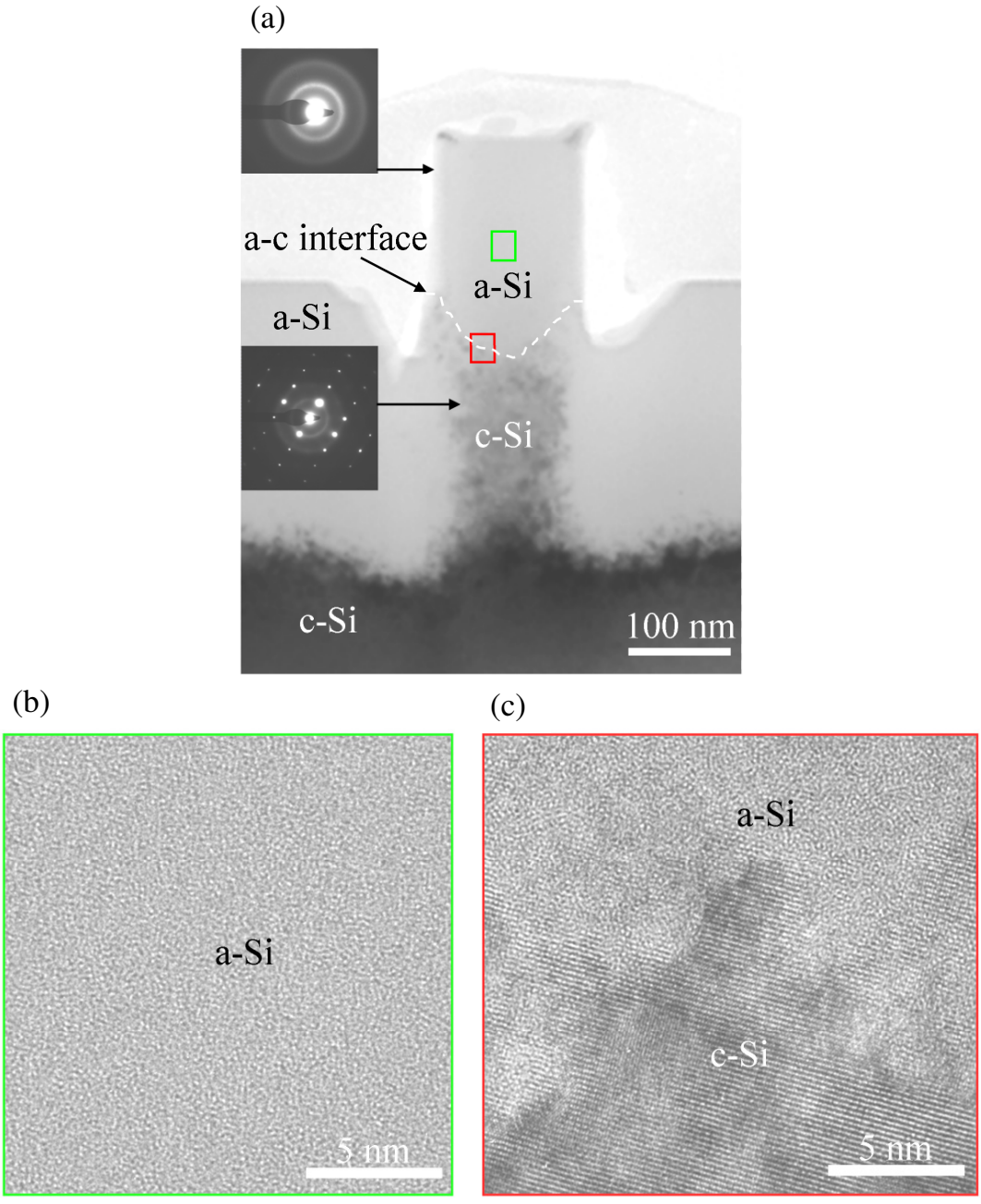

Figure 4.13 (a) A cross-sectional TEM image of an as-implanted NW. The SAED pattern at the top left was taken from the top of the NW, and the same at the bottom left was taken from underneath the NW, below the a-c interface as indicated. (b) An HRTEM image from the bulk of the amorphous region of the NW in (a) (green box). (c) An HRTEM image from the a-c interface in (a) (red box).

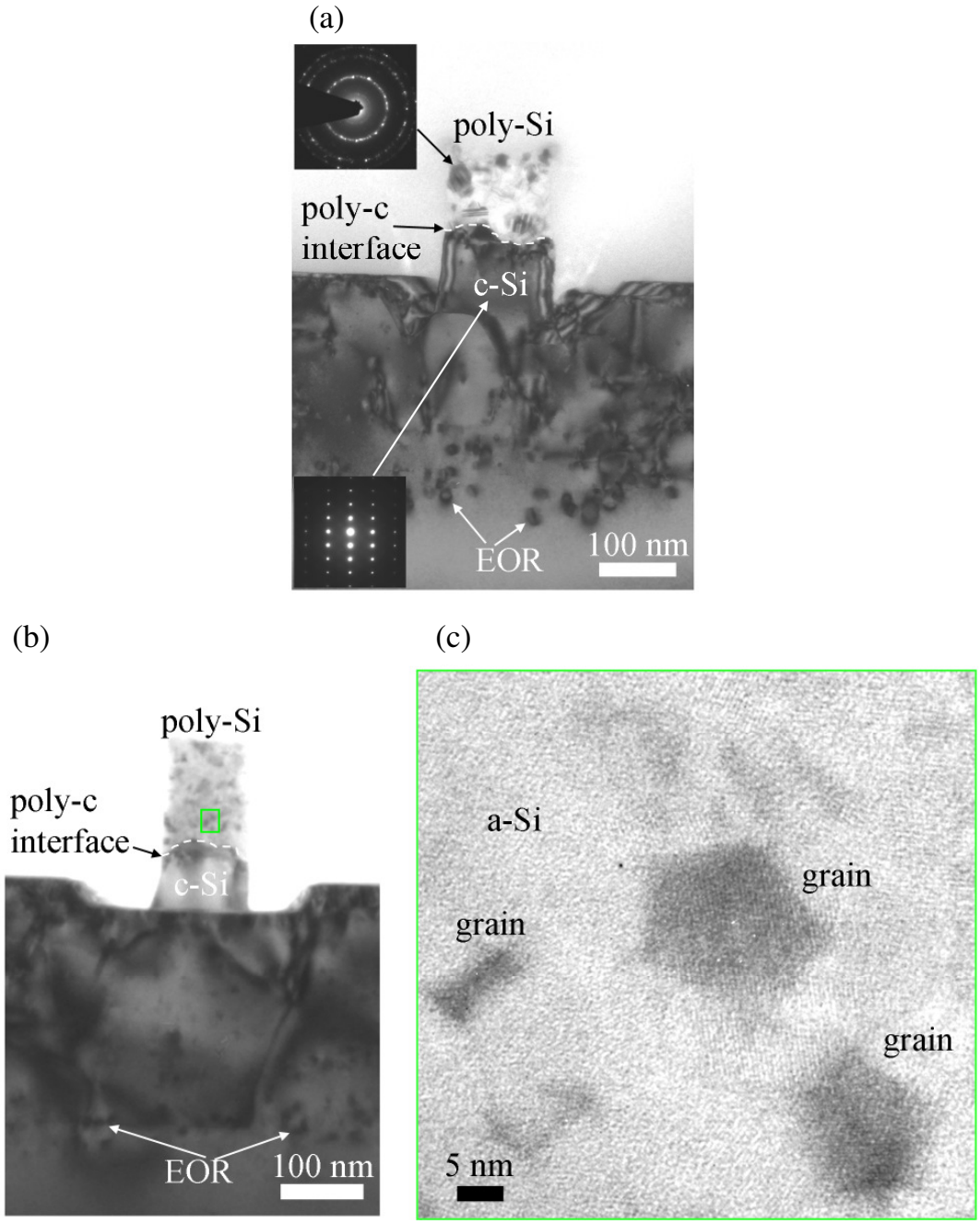

Figure 4.14 Cross-sectional TEM image of Si NW after a single step thermal anneal. (a) 600°C for 5 hours in a furnace, top and bottom inset shows the SAED pattern taken from above and below the poly-c interface respectively. (b) 900°C for 30 seconds by RTA. (c) An HRTEM image from the NW in (b) taken from the poly-Si part (green box).

However, the maximum of $L_{c\text{-}Si}/L_{NW}$ increased monotonously with the annealing temperature which is shown (see Figure A4.8 in Appendix 4). The maximum single-crystalline fraction achieved with a single step annealing was around 72% of the NW length.

The key to suppress RNG lies in the higher activation energy of it (4-5 eV [4.14]) with respect to SPER (2.7 eV [4.11, 4.12]). This implies that nucleation rate of RNG is negligible at low temperatures (<550°C) whereas SPER can start and proceed (although at a relatively slower rate). This concept was first suggested by Csepregi et al. [4.15].

This was utilized in this work with the sequential anneals (UNWAs3c and UNWAs3d in Table 3.5). The TEM image of a NW from the sample UNWAs3c in Table 3.5 after the first anneal at 550°C is shown in Figure 4.15(a). From Figure 4.15(a) and the diffractograms at its inset, it is clear that no poly-Si was formed after the first anneal. The entire NW turned single-crystalline except for a small amorphous pocket at the top left corner (see the diffractogram at the top inset). This bears testimony to the fact that the first anneal at a low temperature indeed suppressed RNG, and SPER from the bottom of the NW proceeded uninterrupted towards the top. The a-c interface (indicated by a dotted line in Figure 4.15(a)) moved much higher in the NW as compared to the cases of single step anneals. The diffractogram taken from the single-crystalline part of the NW (lower inset in Figure 4.15(a)) indicated the presence of micro-twins. This is verified by the HRTEM image in Figure 4.15(b) where the twin-planes are indicated. Formation of micro-twins during SPER is typical for Si (111) [2.21, 4.16] because for recrystallization along <111> direction, a simultaneous attachment of three adjacent atoms from amorphous to a crystalline part is required in order to initiate the nucleation. These three atoms can either add in the desired <111> direction or in a twin orientation.

The second anneal rendered the NWs completely single-crystalline. This is shown in Figure 4.16(a) and (b) for the furnace anneal and RTA respectively. The diffractogram in Figure 4.16(a) confirms a twin-free <111> orientation of the NWs. It shows that unlike the polycrystalline grains, the micro-twins in a NW can be annealed out and the leftover amorphous silicon from the first anneal can be fully converted to single-crystalline silicon. Both in Figure 4.16(a) and (b) a few dark colored triangle-shaped regions are visible. They are probably defects that formed on the thermal evolution of the micro-twins. However, the exact nature of these defects is not clear yet. A detailed characterization of these defects is under way.

To conclude, it was shown here that SPER of amorphous Si NWs is not trivial. It requires a sequential annealing that effectively suppresses the polycrystalline grain formation at the first low temperature anneal, and subsequently aligns the NW to its epitaxial orientation.

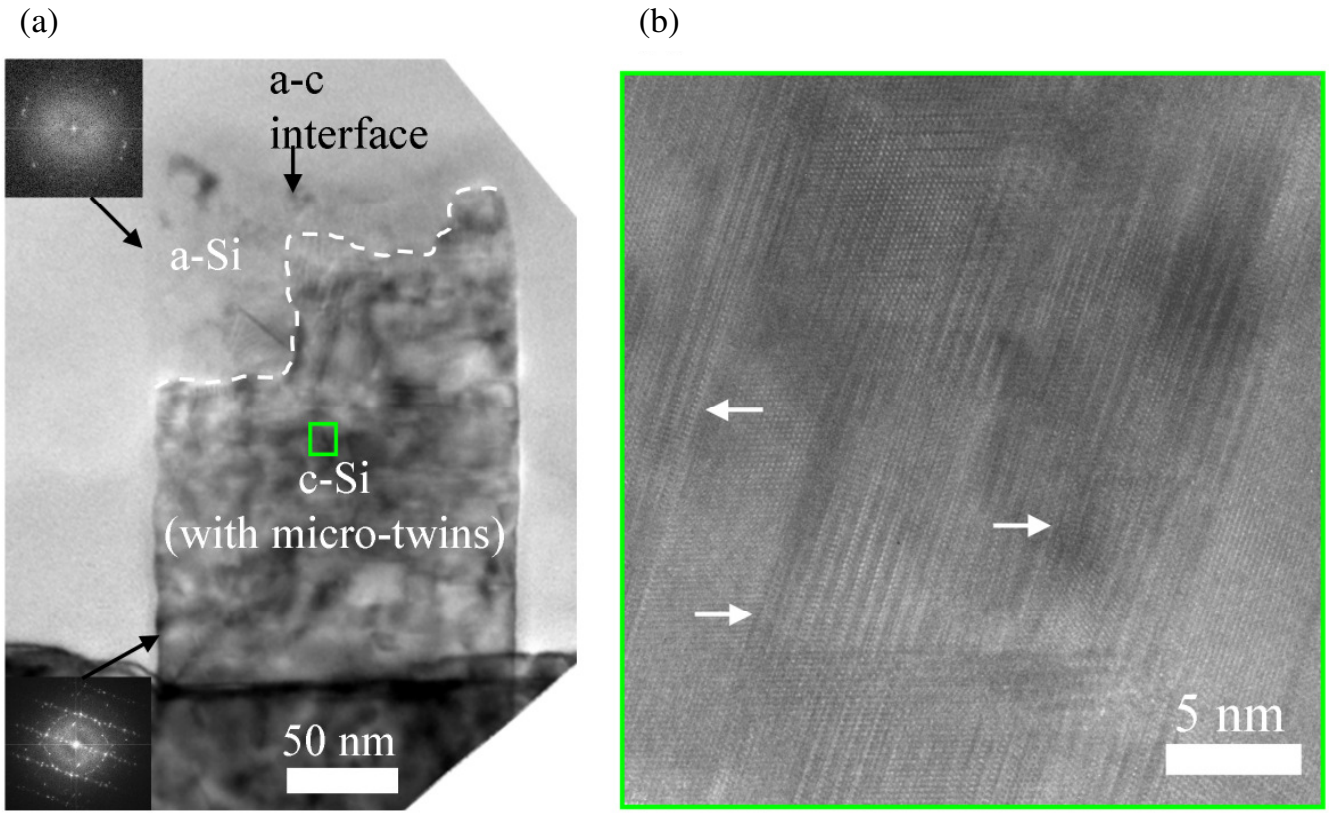

Figure 4.15 (a) A cross-sectional TEM image of a NW after the first step (550°C for 1 hour) of the two-step sequential anneal. The diffractogram at the top and bottom left was taken from above and below the a-c interface respectively. (b) An HRTEM image taken from the micro-twinned c-Si part in (a) (green box). The twins are indicated with arrows.

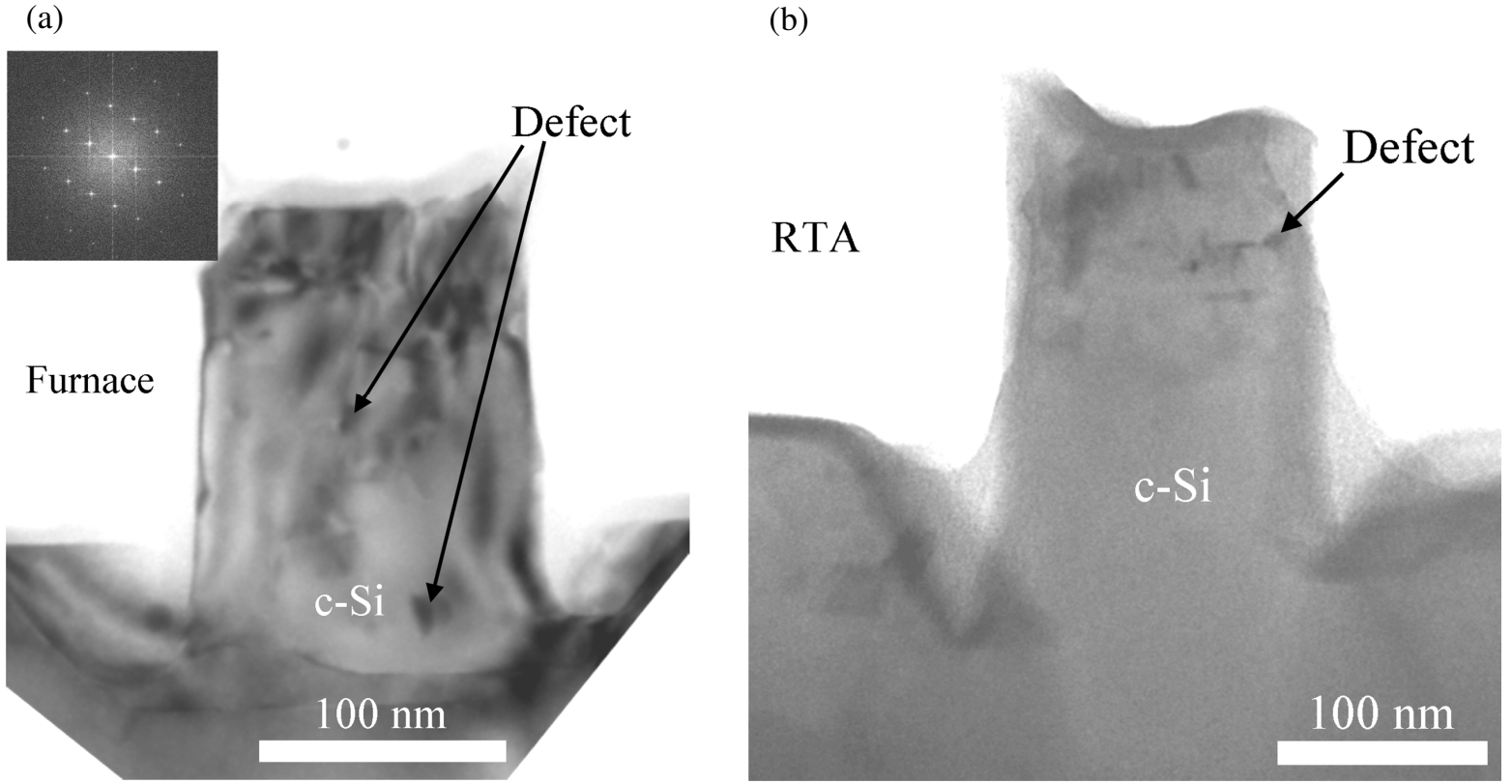

Figure 4.16 A cross-sectional TEM image of a NW after the second step of the two steps sequential anneal. (a) 950°C for 30 min in furnace anneal. The diffractogram at the top left was taken from the middle of the NW. (b) 950°C for 30 seconds by RTA. The NW is fully single-crystalline; however some triangular shaped defects are visible as indicated in the images.

4.6.3 Resistance of the Uniformly Implanted NWs

The I-V curves of individual implanted Si NWs were measured in the same way as the in-situ B-doped NWs and are shown in Figure 4.14. Figure 4.17 (a), (c) and (e) show the semi-logarithmic I-V curves of an unimplanted, an as-implanted and an annealed NW for B implantation (UNWB in Table 3.4/3.5), two implanted and annealed NWs each for P (UNWAs1 in Table 3.4/3.5) and As (UNWAs2 in table 3.4/3.5) implantation at different annealing temperatures respectively. Clearly it can be seen that the current increases by orders of magnitude from the unimplanted to as-implanted, and from the as-implanted to the annealed NWs. In case of P and As implantation, the current increased significantly with the increase of the annealing temperature. This is because of the fact that for P and As, higher electrical activation is achieved by increasing the annealing temperature beyond 1000°C while for B, the electrical activation saturates at 850°C [2.21, 2.22]. Figure 4.17 (b), (d), (f) show the I-V curves of three B, P and As-implanted NWs respectively in a linear scale. For comparison, the I-V curve of an unimplanted NW is also shown in each case. The NW resistance (R) was calculated from the slope of these Ohmic curves. Assuming the measured resistance is coming only from the bulk of the NW, the resistivity (ρ_{meas}) was calculated using Equation 4.1 and listed in Table 4.2 for all the measured NWs. To compare the measured resistivity with that expected from the intended doping level, the expected resistivity (ρ_{exp}) values were also calculated using Equation 4.2 and listed in Table 4.2. The mobility values used for evaluating Equation 4.2 were those measured for similarly implanted Si wafers (WafAs, WafB1, WafB2 in Table 3.4) and reported in Table 4.1.

From Table 4.2, it can be seen that in case of the B-implanted NWs, ρ_{meas} is of the same order of magnitude as ρ_{exp}. For the P-implanted NW, ρ_{meas} is 43 to 166 times higher than ρ_{exp}. For the As-implanted NWs ρ_{meas} is 16 to 26 times higher than ρ_{exp}. Possible reasons behind this are briefly discussed below.

4.6.4 Origin of Discrepancies in the NW Resistivity

Along with normal diffusion according to Fick's law [2.22], implanted dopants, mainly boron and phosphorus, often exhibit an anomalous diffusion known as transient enhanced diffusion (TED) [4.17 – 4.21] that arises out of coupling between Si self-interstitials generated by the implantation and the dopants. This coupling results in mobile dopant complexes that diffuse much faster than the dopants themselves. This effectively enhances the dopant diffusion which is measured by an enhanced diffusivity directly proportional to the concentration of Si self-interstitial. The enhanced diffusivity can be orders of magnitude higher than the diffusivity of the dopant under equilibrium. This leads to a significant smearing out of the as-implanted

dopant profiles, i.e. the dopants diffuse out and eventually segregate at the surface. This effect, however, is mainly observed for heavy doping that requires high implantation energy and dose.

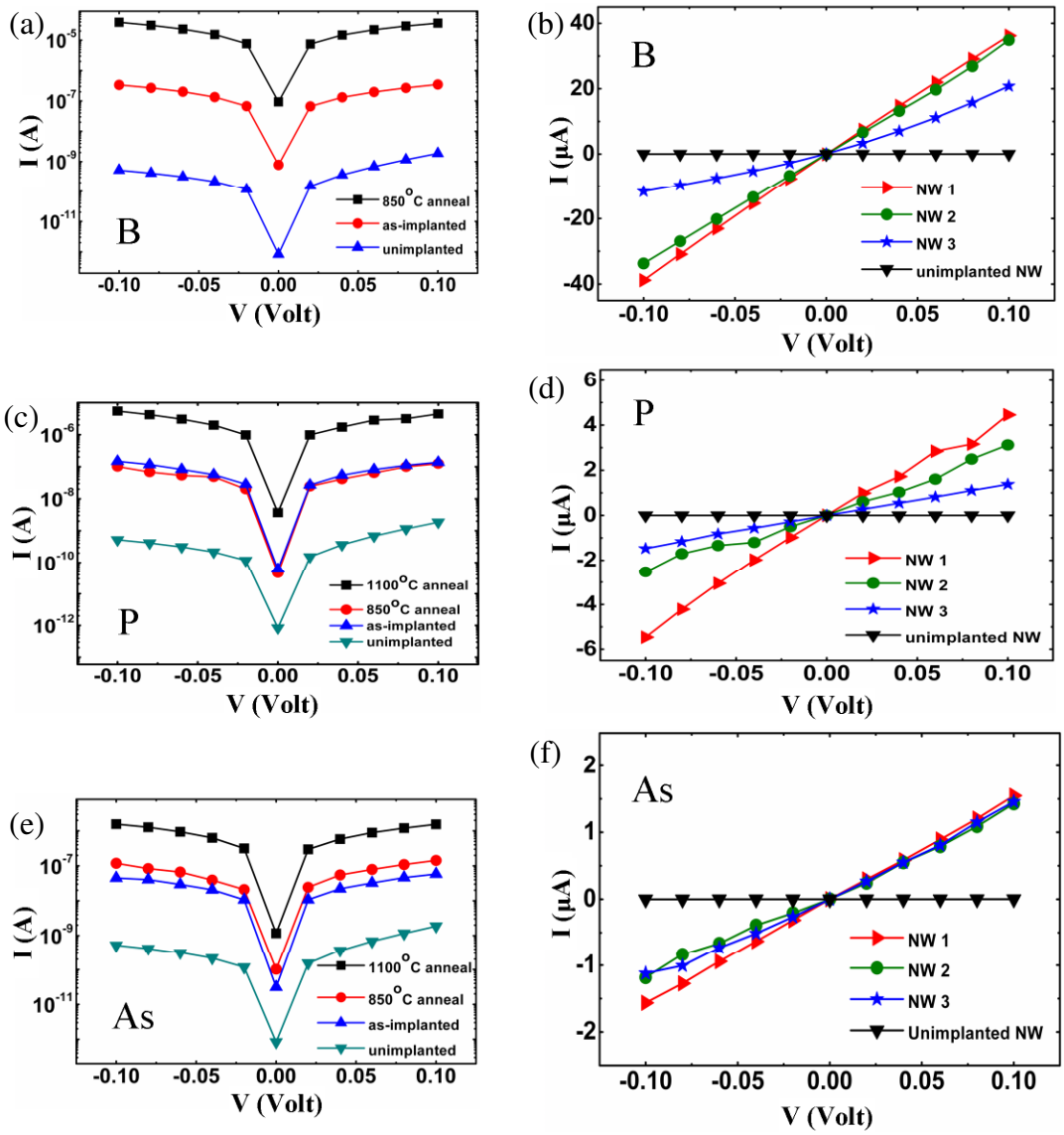

Figure 4.17 Current-Voltage (I-V) characteristics of unimplanted, as-implanted, and implanted and annealed NWs in semilog scale for (a) B (c) P and (e) As implantations, in linear scale for three NWs implanted (b) with B and annealed at 850°C for 30 seconds, (d) with P and annealed at 1100°C for 30 seconds and (f) with As and annealed at 1100°C for 30 seconds. The error from linear fits (not shown) in Figure (b), (d) and (f) was around 2%, 5% and 2% respectively.

Implant Specie	**N_{int} (cm^{-3})**	**NW number**	**D (nm)**	**L (nm)**	**R (Ω)**	**ρ_{meas} (Ω-cm)**	**ρ_{exp} (Ω-cm)**
B	$3x10^{18}$	NW 1	160	240	3.0k	0.02	0.02
		NW 2	176	308	2.6k	0.02	
		NW 3	191	255	6.8k	0.07	
		Unimplanted NW	160	280	1.0G	7180	
P	$1x10^{19}$	NW 1	150	270	21k	0.13	0.003
		NW 2	140	270	37k	0.20	
		NW 3	160	240	71k	0.50	
		Unimplanted NW	165	295	980M	7103	
As	$1x10^{18}$	NW 1	166	240	65k	0.50	0.03
		NW 2	175	235	77k	0.70	
		NW 3	180	260	80k	0.80	
		Unimplanted NW	165	295	980M	7103	

Table 4.2 Measured resistance (R) and resistivity (ρ_{meas}) of B, P, and As-implanted and annealed NWs. The I-V curves of these NWs are shown in Figure 4.14 (b), (d) and (f) and the resistivity calculated using Equation 4.2 with the diameters (D) and lengths (L) listed here. The expected resistivity (ρ_{exp}) calculated using Equation 4.3 with mobility values from Table 4.1 are included for comparison.

Since the measured B-doped Si NWs showed the expected resistivity, TED is probably not active in this case. In fact, most examples of TED in the literature are found for an expected boron concentration of $10^{19}cm^{-3}$ or more [4.17] which is more than an order of magnitude higher than the boron implantation used for this work, i.e. 10^{18} cm^{-3}. The Implanted boron, therefore, is expected to diffuse through interstitials and vacancies (interstitialcy) [4.16] which is the normal diffusion mechanism for it and is fully electrically active at the annealing temperature of 850°C. Besides, surface depletion effect at this B concentration plays an insignificant role as demonstrated with the in-situ B-doped NWs (see Figure 4.6). Like in the case of the in-situ B-doped Si NWs, the high doping also reduces the contact resistance at the p-Si NW - Pt/Ir tip which adds to the measurement accuracy.

In case of phosphorus, the implantation doses and energies were much higher than that for boron to result in a concentration of 10^{19} cm^{-3}. This however, can easily enable TED which may lead to an enhanced diffusion constant (D_{enh}) of $1.2x10^{12}$ cm^2 s^{-1} at 1100°C [4.21]. This can lead to a diffusion length ($2\sqrt{D_{enh}t}$, where t = annealing time) of 120nm for a 30 seconds of RTA. This diffusion length is close to the average NW diameter of 155nm implying that it is highly likely that the phosphorus atoms are diffused out and reach the surface of a NW. It has been observed that P atoms generally segregate at the Si/SiO_2 interface during a thermal oxidation [4.22 – 4.26] which generates the SiO_2 layer, as well as during a thermal anneal when a Si/native oxide interface is already present as in the case of the Si NWs measured here. The segregated dopants can get deactivated by the surface states as discussed in Chapter 1 and in Section 4.5. However, this has to be verified with carrier profiling.

In case of the As-implanted NWs, TED is probably not as pronounced as arsenic is not known for exhibiting significant TED [4.17]. However, As segregation at the Si/SiO_2 interface has been predicted [4.27], as well as observed [4.28, 4.29] even for low doses (~10^{13} cm^{-2}). Clement et al. [4.30] have reported an increase in resistivity by a factor of 14 for As-implanted horizontal NWs, i.e. ρ_{meas} was 14 times higher than ρ_{exp}. This agrees well with the results presented here.

4.6.5 Error Analysis III

The error from linear fits (not shown) in Figure 4.17(b), (d) and (f) is 2%, 5% and 2% for B-, P- and As-implanted NWs.

However, a significant difference of error between B-implanted and P/As-implanted NWs can come from the contact resistance. The contact resistance of the P/As-implanted n-Si NW – Pt/Ir contact can be significantly higher than the B-implanted p-Si NW – Pt/Ir contact as the theoretical Schottky barrier height is 0.85eV in case of the former and -0.15eV in case of the

latter [1.52]. This implies a higher contact resistance for the P/As-implanted NW which probably affected the accuracy of the measurements.

4.6.6 Carrier Profile in a Single P Implanted NW

Figure 4.18(a) presents the SEM image and 4.18(b) the SSRM images of a P-implanted NW. Figure 4.18(c) is the SEM image of the same NW after SSRM measurements. Like the SSRM image of the in-situ B-doped NW (Figure 4.10) the dark area surrounding the NW indicates the SiO_2 layer with high resistance (HR), and the brighter color shown in the substrate indicates a lower resistance (LR) there due to the high carrier concentration of 7.4×10^{19} cm^{-3} corresponding to its resistivity of 0.001 Ω-cm. The uniform medium dark color shown both in the epi-layer and in the bulk of the NW demonstrate their homogeneous doping to the same level. This is in agreement with the expected carrier concentration (~10^{19} cm^{-3}) simulated by the TRIM code (see Figure 3.4(b)). Evidently, there is a brighter colored band at the side wall of the NW shown in Figure 4.18(b). This indicates a lower resistance or higher conductivity there as compared to the bulk of the NW.

Averaged profiles of the spreading resistance (R_S) and carrier concentration in axial (AS) and radial (RS) directions are shown in Figures 4.19(a) and (b). R_S was converted to carrier concentration by the same scaling procedure as used for the in-situ B-doped NW. However, in this case the calibration was done with the known resistivity of the highly doped substrate (from the segment AB in Figure 4.19(a)). The carrier concentrations along the axial and radial directions to the NW are shown at the right Y axis of Figure 4.19(a) and (b) respectively. Figure 4.19(a) indicates, as expected, that the epi-layer and the bulk of NW are more than one order of magnitude less highly doped than the substrate. Figure 4.19(b) confirms a higher doping level close to the surface in comparison to the core region of the NW. The more highly doped region extends from the surface to about 30nm inside the NW, and the difference between the maximum doping level of this outer shell and the minimum doping level of the inner core is about a factor of 6-7. The average carrier concentrations of 2.5×10^{18} cm^{-3} in the NW bulk (Figure 4.18) is off by a factor of 4 from the expected average doping level of 10^{19} cm^{-3}. The lower discrepancy compared to the values measured from NW resistance in the previous section (the measured resistivity was off from the expected resistivity by a factor of 40-50) is probably due to a better electrical contact between the tip and the sample since the conductive AFM tip for SSRM measurements presses the sample much harder than the metal tip for NW resistance measurements. However, as mentioned in section 4.5.5, the extracted carrier concentrations can be off by an order of magnitude due to the significant change of R_S with the deflection voltage (see Figure A4.5 and A4.6 in Appendix 4).

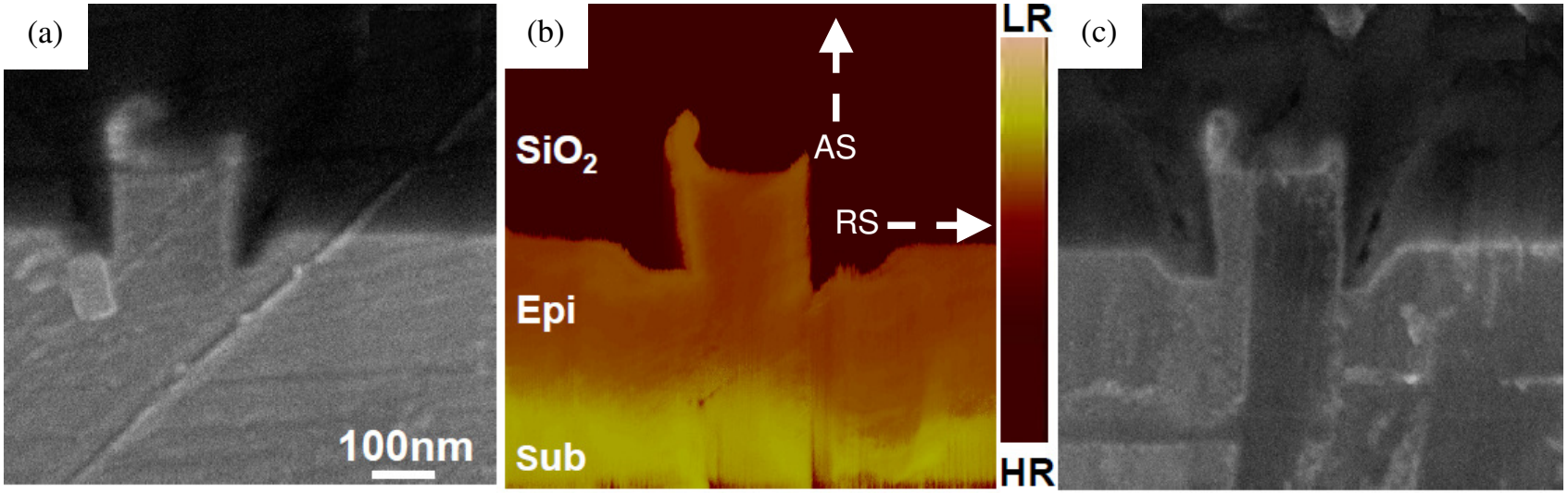

Figure 4.18 (a) SEM image of a P-implanted NW prepared for SSRM measurement (b) SSRM image of the same NW (c) SEM image of the same NW after SSRM measurement.

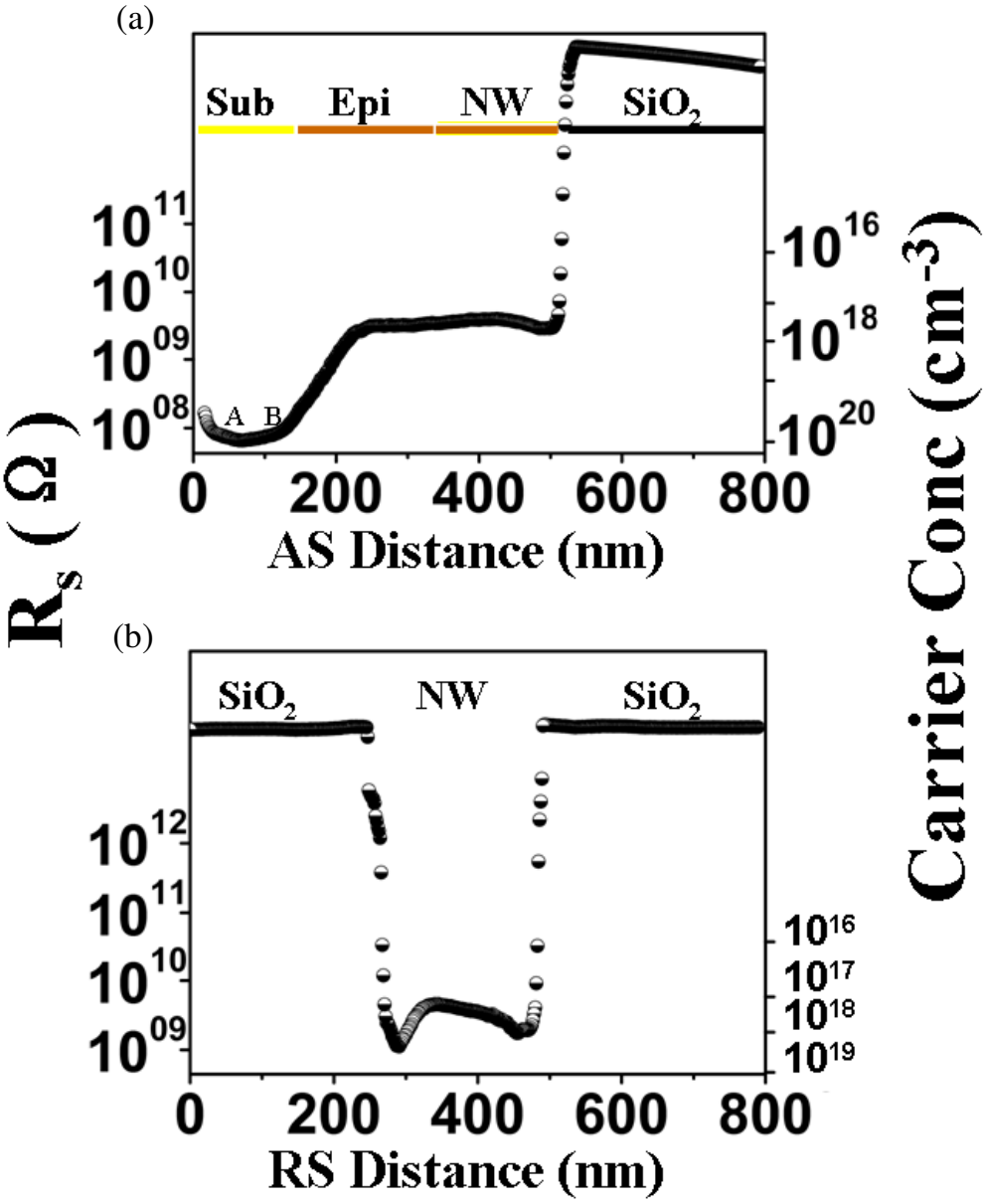

Figure 4.19 R_S (left) and carrier (right) profiles extracted from the SSRM image shown in Figure 4.18. The profiles in axial direction (AS) and in radial direction (RS) are averaged over the whole NW.

Thus, the SSRM image and carrier profile confirmed the piling up of P at the Si NW surface. This probably happened during the RTA and the higher number of P atoms might have reached the NW surface owing to TED as discussed in section 4.6.4. However, it is interesting to notice from this profile that the high amount of P atoms detected near the surface are not electrically deactivated.

The deactivated dopants at the surface could not be observed. For the measured NW of diameter (D) 175nm, using $N_{net} = 10^{19}$ cm^{-3}, and $N_S = 2x10^{10}$ cm^{-2}, we get d = 173nm from Equation 4.3. This implies that the depletion width (D – d) is only 2nm. As mentioned previously, this thickness can not be resolved by the present SSRM measurement since the distance between the neighbouring data points is 1.6nm and the spatial resolution is evaluated to be 10nm by the measured width of a sharp thermally grown Si/SiO_2 interface.

Another important factor that can influence the dopant profiles in the Si NWs is the existence of the Au remaining from the growth-initiating phase on the sidewalls of the NWs. It has been already discussed that any Au diffused into the NW is limited to a maximum solubility of 2×10^{16} cm^{-3} [4.4] at the annealing temperature. This can not compensate the high P concentration. However, the Au/Si nanoparticles on the side-walls may contribute to the surface conductivity which may be reflected on the SSRM profile. Since the average size of the Au particles is around 2nm, it is challenging to resolve the contribution coming from them with the current setup.

4.6.7 Error Analysis IV

The error in treating the substrate of uniform resistivity was around 15%, i.e. the spreading resistance varied by 15% in the segment AB of Figure 4.19(a). Therefore, the error in the measured carrier concentration is roughly around 15% disregarding the error from contact pressure (see Figure A4.5 and A4.6).

4.7 Intra-NW p-n Junction

In this section, first the implication of an intra-NW p-n junction on its electrostatic properties is illustrated which is followed by the results of its current-voltage characteristics.

4.7.1 The p-n Junction Formation

Figure 4.20 shows the p-n junction formation in the NW. Figure 4.20(a) shows an SEM image of a NW (tilted by 90°) for which the top half is expected to be n-type and bottom half p-type. Figure 4.20(b) is an energy band diagram of this NW simulated with Sim Windows™ [4.31]. For simulation, 100% electrical activation of both dopants from the doping profile in Figure 3.5(b) was assumed, i.e. the electron concentration was assumed to be fixed at $2x10^{19}$ cm^{-3} from 0 (NW top) to 135nm, and hole concentration from 135nm to 270nm. The average length of these NWs was found to be around 270nm which is slightly shorter than the average length of the uniformly implanted NWs. The p-n junction was assumed to be abrupt. The simulation

showed a built-in voltage of 1.04eV and a depletion width (w), i.e. the width of the space charge region of the p-n junction [1.52], of 40nm. This implies that ideally the p-n junction should be confined within the length of the NW. Indeed, preliminary results of the cross-sectional SSRM

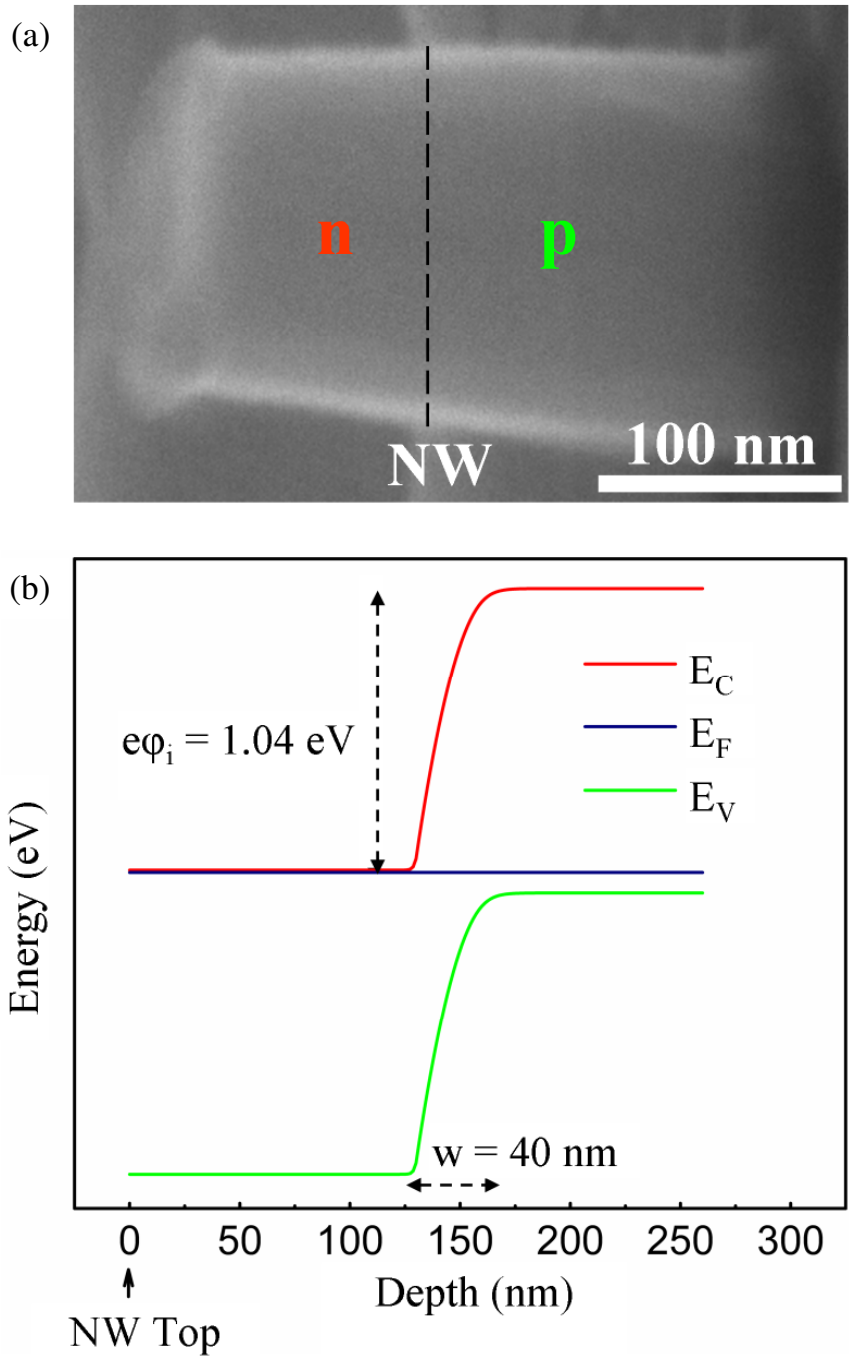

Figure 4.20 (a) SEM image of a p-n junction NW (b) Band diagram of a p-n junction NW assuming the dopant profile shown in Figure 3.5(b) and 100% electrical activation of the dopants.

profile of an unimplanted, i.e. p-i junction NW indicated this as well. Figure 4.21(a) shows an back scattered electron (BSE) SEM image of a cross-sectional SSRM sample, and Figure 4.21(b) shows the SSRM image of the same. It is obvious from Figure 4.21(b) that the B-doped lower segment is more conductive (lighter) than the undoped upper segment (darker). This confirmed that the modulation doping (MNWB in Table 3.2) worked. SSRM profiling of a p-n junction NW is underway.

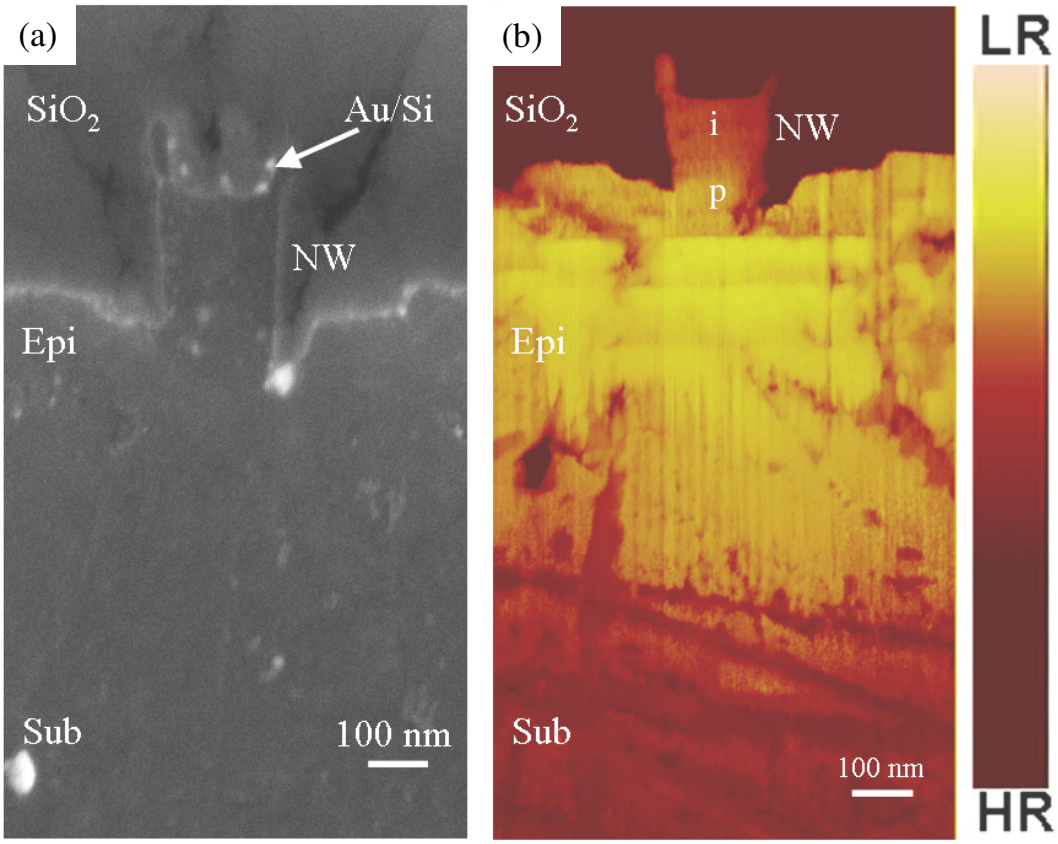

Figure 4.21 (a) BSE SEM image of a cross-sectional SSRM sample of unimplanted p-i junction NW. (b) SSRM image of the same sample

4.7.2 The NW Diode

The measured I-V curves of three different p-n junction NWs along with an unimplanted p-i NW are shown in Figure 4.22(a). Details of these NWs are listed in Table 4.3. The inset of Figure 22(a) shows the I-V curve of the substrate of the NW. This was measured by contacting the epi-layer just next to the base of the NW with the Pt/Ir tip. As can be seen from Figure

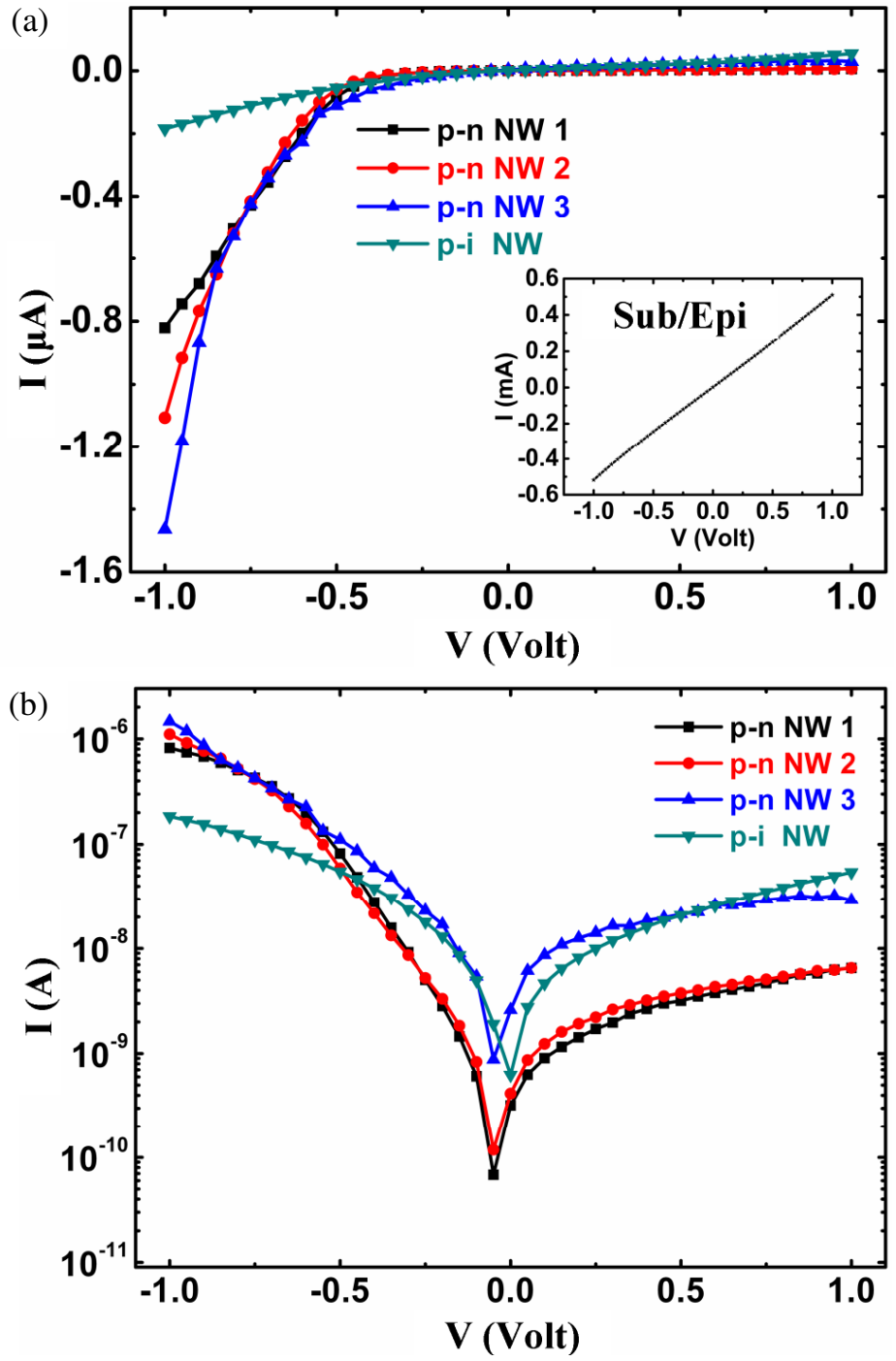

Figure 4.22 The measured current-voltage (I-V) characteristics from the NWs. (a) I-V curves of three p-n NWs, and a p-i (unimplanted) NW. Refer to Table 4.3 for details of the NWs. Inset of Figure (a) shows the I-V curve of the substrate in the same voltage range. (b) Semi-log plot of the I-V curves in Figure (a). For extracting the ideality factors of the p-n junctions, the linear regions of the curves of the p-n NWs in forward bias (-0.2 - -0.6 volt) were used.

4.22(a), all the p-n junction NWs show excellent rectifying characteristics with an ON/OFF current ratio of 168, 120, and 50 respectively at ±1 volt (see Table 4.3). In comparison, the unimplanted p-i NW shows a quasi-Ohmic behavior implying the lack of a significantly rectifying junction. The p-type substrate of the implanted NWs (inset of Figure 4.22(a)) showed an Ohmic (linear) behavior. This confirmed that the P implantation is indeed forming a p-n junction within the NWs as illustrated in Figure 3.5(b) and 4.20(b) and it did not extend to the substrate. The protection of the substrate with the SOG was successful.

In forward bias, the diode current (I) in the lower voltage range can be written as [1.52]

$$I = I_s \exp[\frac{eV}{nkT} - 1] \qquad [4.6]$$

where I_S is the saturation current, V the applied voltage, k the Boltzmann constant, T the temperature and n the ideality factor of the diode. The ideality factor of a diode is a measure of the influence of the electrical defects present in the device on its current rectification ability. For an ideal diode, the carrier transport is determined by diffusion current which leads to an ideality factor of 1. In order to extract n, the I-V curves of Figure 4.22(a) are plotted in a semi-log scale in Figure 4.22(b). From the slope (S) of the linear parts of these curves in the lower voltage range (-0.2 - -0.6 volt) n was extracted by using

$$n = \frac{e}{(\ln 10) SkT} \qquad [4.7]$$

The values of n for the three p-n junction NWs were 2.0, 1.8, and 1.7 respectively (see Table 4.3). This indicates presence of defects in or around the depletion/space-charge region of the p-n junction.

Type	**Number**	**Diameter (nm)**	**Length (nm)**	**ON/OFF Current Ratio**	**Ideality Factor (n)**
p-n	1	160	250	168	1.8
p-n	2	155	290	125	1.7
p-n	3	230	277	50	2.0
p-i	-	145	280	_	_

Table 4.3 Dimensions (diameter and length), ON/OFF ratio, and the ideality factor for the three NW p-n junctions plotted in Figure 4.22.

In addition to diffusion that leads to an ideality factor of 1, the carriers also recombine both in the bulk as well as on the surface of the NW. Sah et al. [4.32] have found that the ideality factor of a p-n diode can vary from 1 to 4 (or even higher in special cases) depending on what kind of carrier recombination mechanism is dominating. A value close to 2 (as in the case of NW p-n junctions discussed here) indicates that recombination across the p-n junction through the surface states is dominant in the carrier transport mechanism [4.32]. Previous discussions have already demonstrated that the MBE-grown Si NWs are indeed covered with a thin (~2nm) native oxide with an estimated surface state density in the order of 10^{10} cm^{-2}. These surface states are in direct contact with the space charge region of the p-n junction and therefore they can play a major role in carrier recombination. Surface recombination drastically reduces the lifetimes of minority carriers which adversely affect the diode current. In fact, surface recombination is identified as a stumbling block for using the NW p-n junctions as effective solar cells [4.33, 4.34]. An effective surface passivation by thermal oxidation [2.22] or long lasting hydrogen termination [4.35] will be important to reduce the surface recombination and use the NW p-n junctions for photovoltaics. It is worth noting that NW p-n junctions fabricated by pure in-situ doping [1.89] or by pure ion implantation [1.67] are reported to show even higher ideality factors than 2 which indicates even stronger surface recombination in them.

In conclusion, the p-n junction Si NWs worked as functioning nano-diodes showing significant current rectification. However, they are probably strongly affected by surface recombination.

Chapter 5

Conclusions and Outlook

This chapter is intended to highlight the coherent connections between the previous chapters from where a number of significant conclusions can be drawn and an outlook for future work can be identified.

5.1 Conclusions

In brief, a number of phenomena related to doping of Si NWs were investigated in details and the results were explained with relevant physical explanations.

Firstly, in-situ doping of Si NWs with boron was demonstrated using MBE [5.1]. A wide range of doping levels from 10^{15} cm^{-3} to 10^{19} cm^{-3} were achieved. Unlike CVD, the dopants were introduced following a calibration curve based on doped Si layers, and with electrical measurements the actual doping levels were assessed. TEM investigations revealed defect free single crystalline structure for all doping levels which is desirable for superior electrical properties. The effect of surface depletion was extensively investigated as a function of NW diameter and doping density. It was observed that thinner NWs are more depleted than the thicker ones, and the depletion width diminishes as the doping density increases. A direct visualization and simple quantification of the carrier profile of a highly doped NW revealed that surface accumulation of active dopants [5.2] may be related to inherent inhomogeneity of in-situ doping.

Another part of the motivation was to fully exploit ion implantation as an ex-situ doping technique for the MBE-grown NWs. This was successfully achieved by uniformly implanting the undoped NWs with boron, phosphorus and arsenic separately. The electrical activation of the dopants was achieved by a rapid thermal annealing. The measured resistivity for the B-implanted NWs [5.3] corresponded to that expected from the implantation assuming full electrical activation. However, the resistivity of both P, and As-implanted NWs was 1-2 orders of magnitude higher than expected even after annealing at a higher temperature [5.3]. In order to investigate if this is specific to n-type NWs, carrier profiling of a single P-implanted NW was performed [5.2] which revealed a significant accumulation of the active dopants at the Si/native oxide interface at the surface.

Another unique phenomenon investigated in connection with implantation was recrystallization of fully amorphized NWs. It was observed that solid phase epitaxial regrowth, the classical mechanism of recrystallization, is incomplete in case of NWs and is greatly hindered by

polycrystalline grain formation. A sequential annealing technique was successfully optimized to completely recrystallize the amorphized NWs.

A novel method to form an intra-NW p-n junction by combining in-situ and ex-situ doping was demonstrated [5.4]. The NW p-n junctions showed reasonably good diode characteristics and evidences of surface recombination in the current conduction mechanism.

5.2 Outlook

In order to carry forward the knowledge and understanding generated from this work, a number of future directions can be identified.

From the point of view of basic physics, the concerted effort in the NW community now is to relate the properties of the NWs to their atomic structures. In this respect, a combination of atom probe tomography and scanning spreading resistance microscopy will provide valuable information about dopant activation from an atomistic point of view. However, since both the techniques are destructive, a qualitative rather than a quantitative trend can be measured by comparing different NWs grown and doped during the same experimental run. As an alternative, a three-dimensional SSRM [5.5] can be performed to map the active dopants in the volume of the NW. By repeated scanning of the same NW with a controlled force the tip can abrade some material from the surface of the measured NW cross section. In Figure 4.18(c) the change of the surface after the SSRM investigation is clearly visible. In this way, the tip gradually moves deeper through the volume of the NW. By measuring the cross sections at different depths of the same NW in succession, a three-dimensional (3D) carrier profiling of the NW can potentially be obtained by using an appropriate projection of the two-dimensional profiles along the depth scale. Further investigations regarding 3D SSRM are in progress [5.5].

To probe the conduction mechanism in depth, a temperature dependent electrical transport measurement will be helpful. From an Arrhenius plot of the measured electrical conductivity vs temperature, the activation energy of the dopants can be extracted and the dominant current conduction mechanism can be identified. In this respect, surface passivation of NWs was another important factor that was not explored in this work. The unpassivated surface curtailed the electrical properties of the NWs measured, as explained in Chapter 4. Surface passivation either by thermal oxidation, atomic layer deposition of a dielectric or spin-coating organic molecules can be investigated. A strong surface passivation will be the key to use the NWs in photovoltaics where surface recombination of carriers on the NW surface offsets the gain achieved by their superior light absorption compared to Si wafers.

In addition, the effect of the Au/Si nanoparticles decorating the sidewalls of the NWs on the electrical properties of the NWs needs to be investigated in details. Since the spatial resolution

of the SSRM measurements used for this work was around 10nm, it was challenging to resolve the Au/Si nano-contacts on the NW sidewalls. However, a more precise conductive AFM measurement to study these nano-contacts is under progress.

To conclude, this work has touched and can be further extended to probe many different aspects of NW doping that are extremely important for Si NW based future nanotechnology.

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Chapter 1

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Chapter 5

5.1. P. Das Kanungo, N. Zakharov, J. Bauer, O. Breitenstein, P. Werner, U. Gösele, *Controlled In-Situ Boron Doping of Short Silicon Nanowires Grown by Molecular Beam Epitaxy*, Appl. Phys. Lett., 2008, 92, 263107
5.2. X. Ou, P. Das Kanungo, R. Koegler, P. Werner, U. Gösele, W. Skorupa, X. Wang, *Carrier Profiling of Individual Si Nanowires by Scanning Spreading Resistance Microscopy*, Nano Lett., 2010, 10, 171
5.3. P. Das Kanungo, R. Koegler, K. Nguyen-Duc, N. Zakharov, P. Werner, U. Gösele, *Ex-Situ n and p Doping of Vertical Epitaxial Short Silicon Nanowires by Ion Implantation*, Nanotechnology, 2009, 20, 165706
5.4. P. Das Kanungo, R. Koegler, P. Werner, U. Gösele and W. Skorupa, *A Novel Method to Fabricate Silicon Nanowire p–n Junctions by a Combination of Ion Implantation and in-situ Doping*, Nanoscale Res. Lett., 2010, 5, 243
5.5. X. Ou, P. Das Kanungo, R. Koegler, P. Werner, U. Gösele, W. Skorupa, X. Wang *Three-Dimensional Carrier Profiling of Individual Si Nanowires by Scanning Spreading Resistance Microscopy*, Adv. Mater., (accepted)

Appendix 1

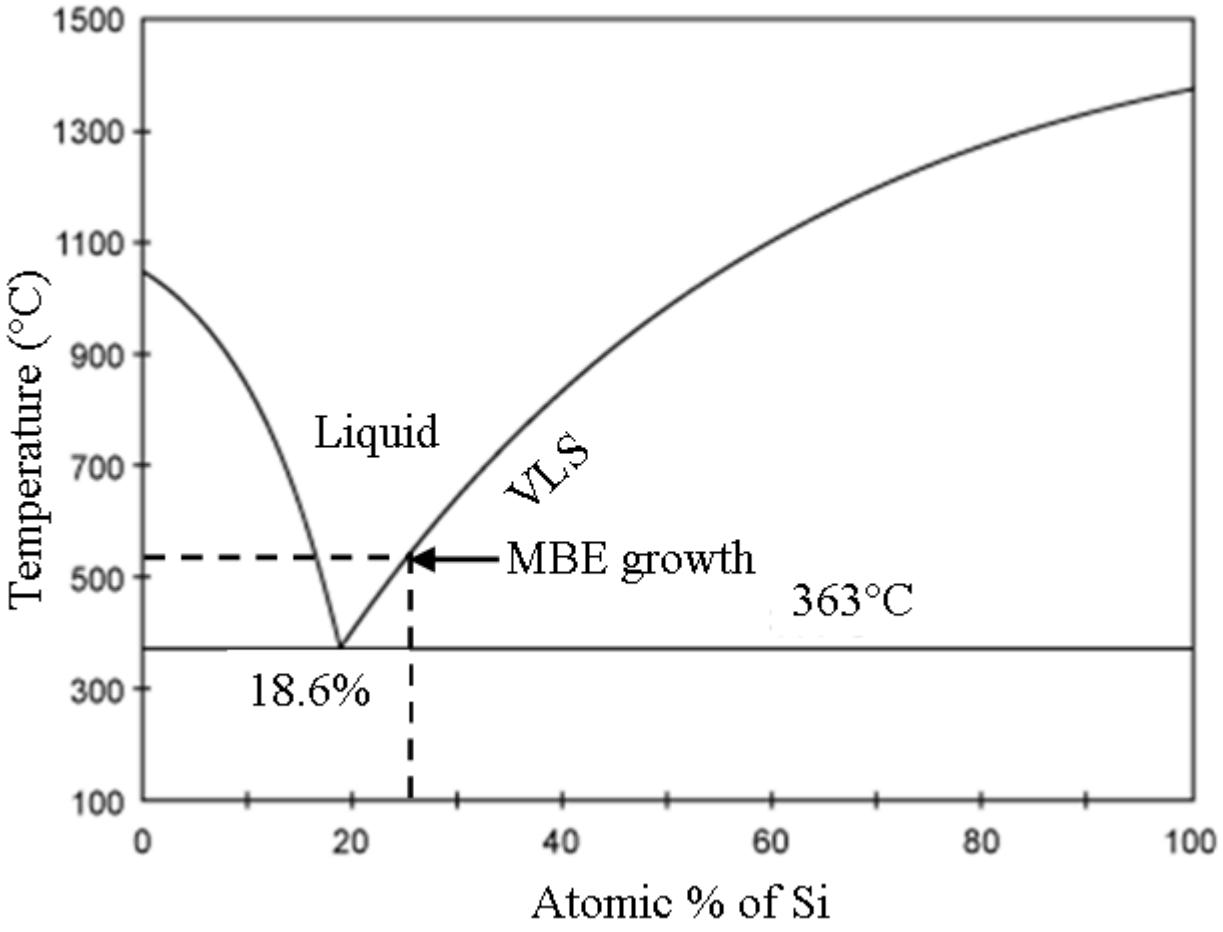


Figure A1.1: The Gold-Silicon phase diagram. The Eutectic point occurs at 363°C at 18.6% of silicon. The Si NWs for this work were grown at 525°C which is indicated in the image.

Appendix 2

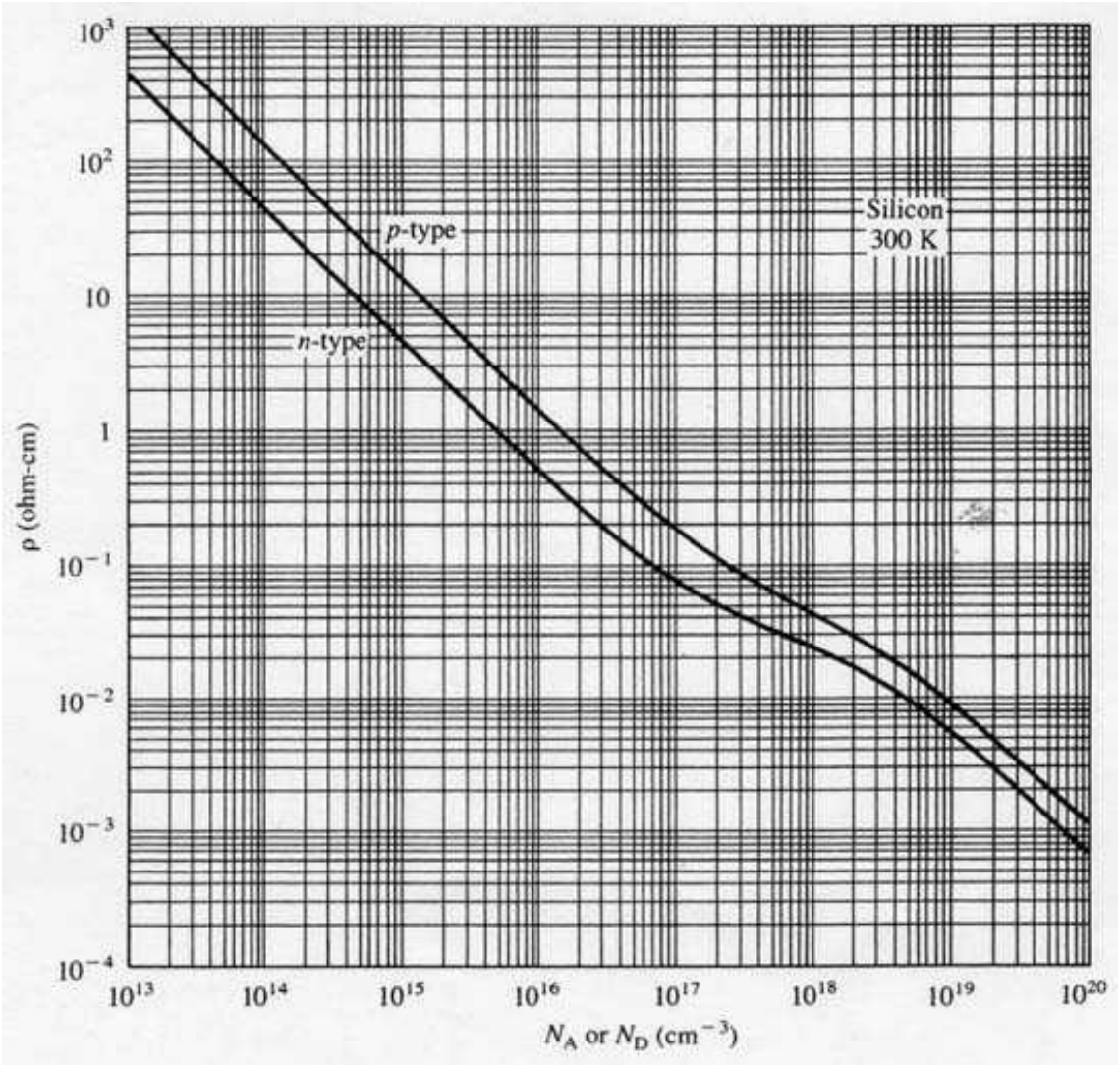


Figure A2.1: Resistivity vs carrier concentration in p- and n-type silicon.

Appendix 3

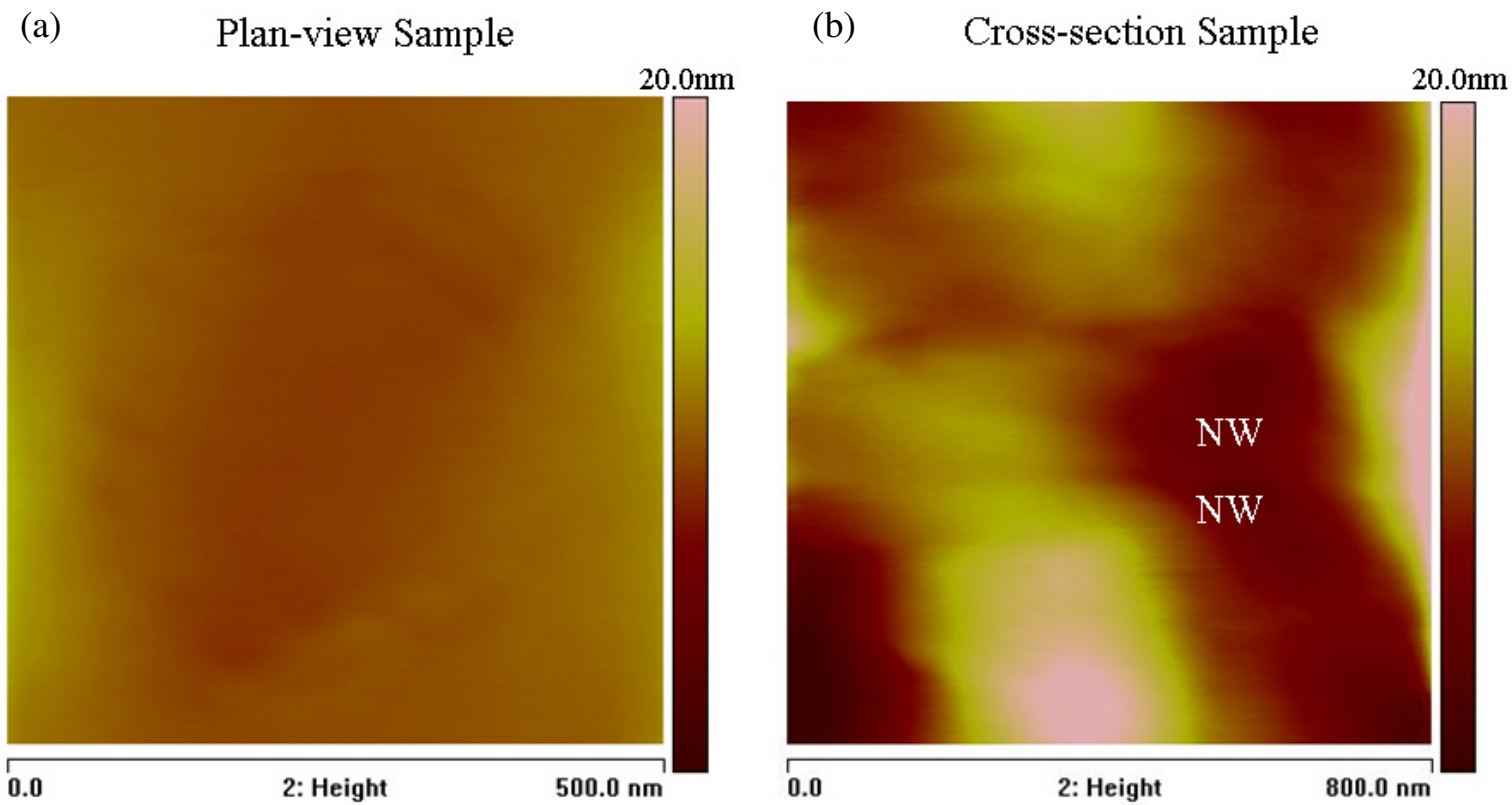


Figure A3.1 Contact mode AFM topography scan to asses the average roughness of the SSRM samples. (a) Plan view sample of Figure 4.10(a), average roughness across the NW ~ 5nm. (b) Cross-section sample of Figure 4.18(b), average roughness across the NW ~ 7nm.

Appendix 4

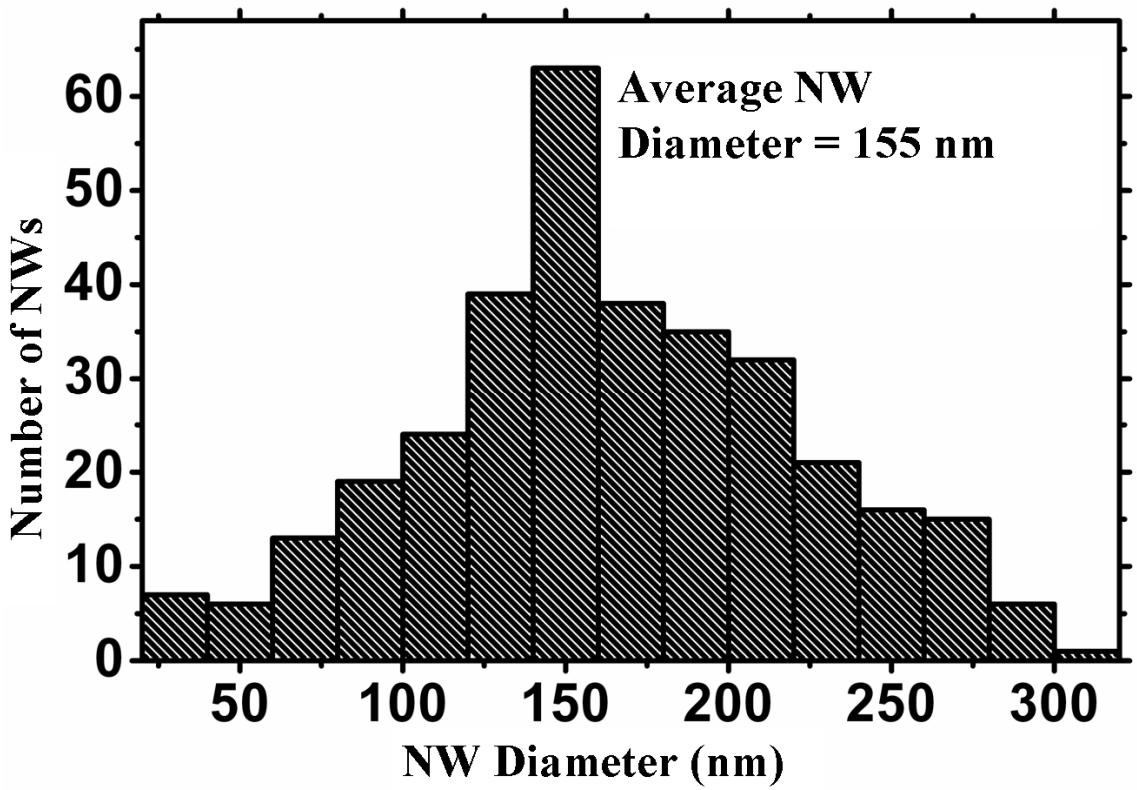
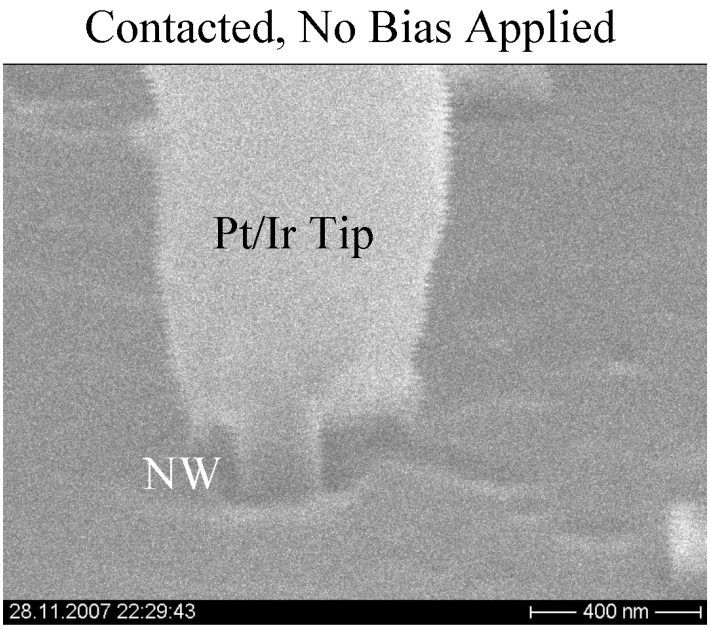


Figure A4.1 Diameter distribution of in-situ B-doped Si NWs. A total of 400 NWs were sampled for the expected B doping of 10^{19} cm^{-3} in this case. The average diameter for all doping levels was in the same range.

(a)



(b)

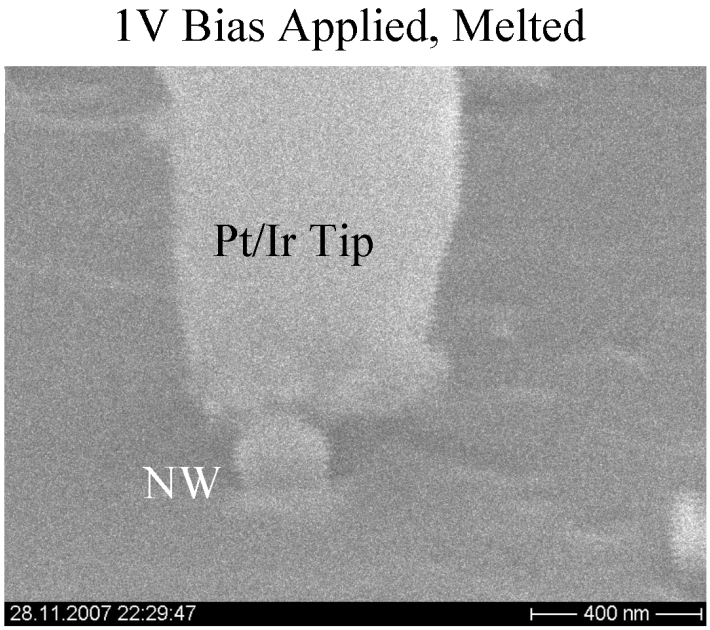


Figure A4.2 SEM images to illustrate the melting of high-doped NWs upon application of a high external bias. (a) NW contacted with the Pt/Ir tip, but no bias applied. (b) 1V Bias applied to the Pt/Ir tip resulting in immediate melting of the NW and loss of contact.

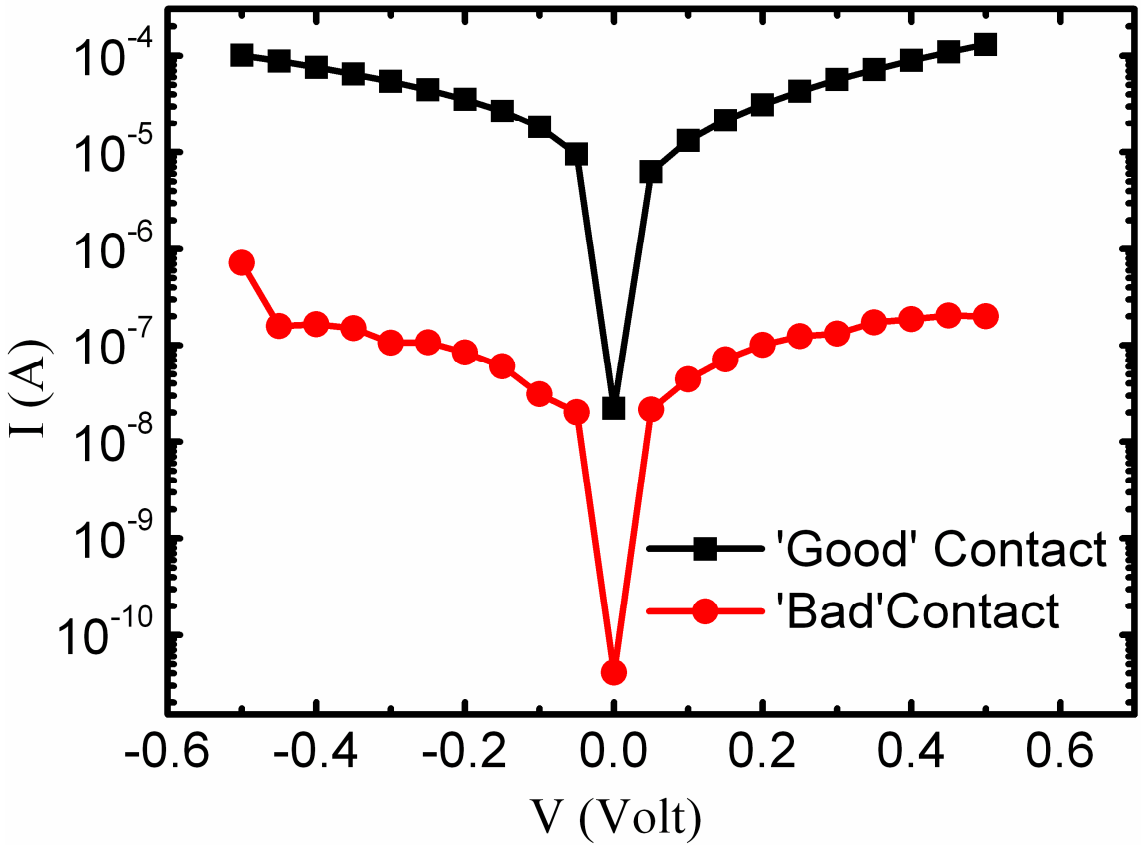


Figure A4.3 I-V curves illustrating a ‘good’ and a ‘bad’ contact between the Pt/Ir tip and a B-doped Si NW. The current drops nearly three orders of magnitude for a ‘bad’ contact.

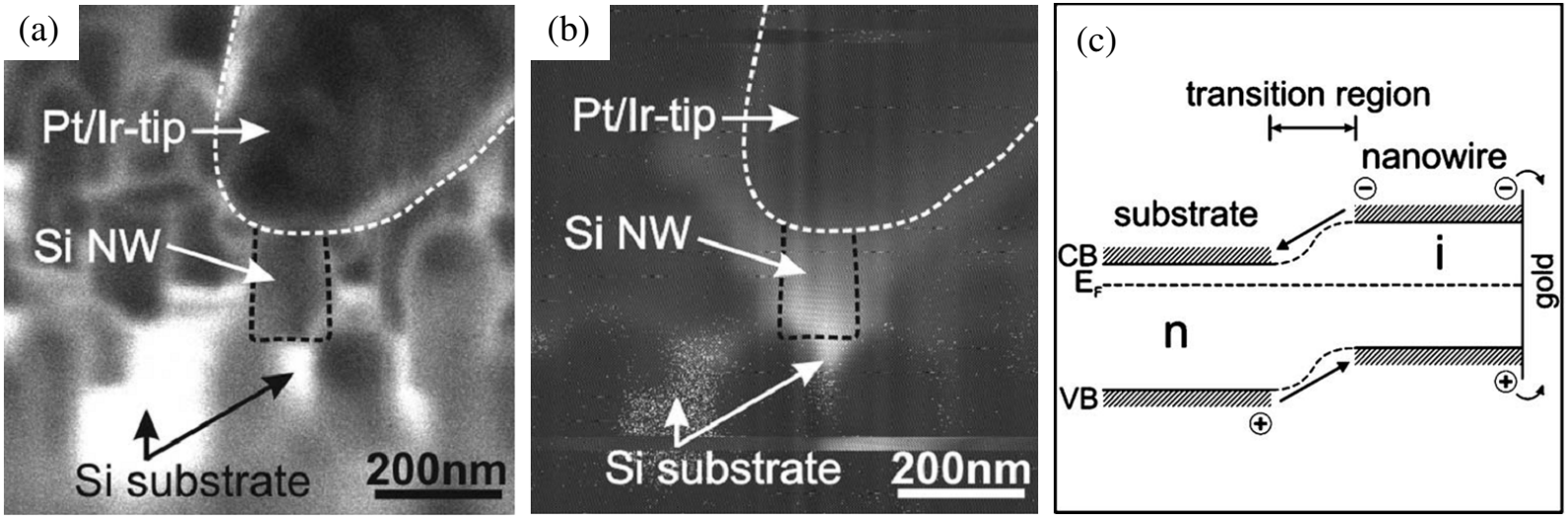


Figure A4.4 (a) SEM image of an undoped Si NW contacted with the Pt/Ir tip. (b) Electron beam induced current (EBIC) image of the NW in (a) The dotted lines frame the NW and the tip. The EBIC signal is generated at the base of the NW at its interface with the substrate, and not at the top where the tip contacts the Au cap of the NW (they were not removed in this measurement). (c) The energy band diagram of the metal (Au in this case which contacts the Pt/Ir tip) – i-Si NW- n-Si substrate that is consistent with the EBIC measurement. CB and VB are the conduction and valence bands, and E_F is the Fermi level. The band bending occurs between n-Si substrate and i-Si NW. (Reprinted form Ref. 1.108)

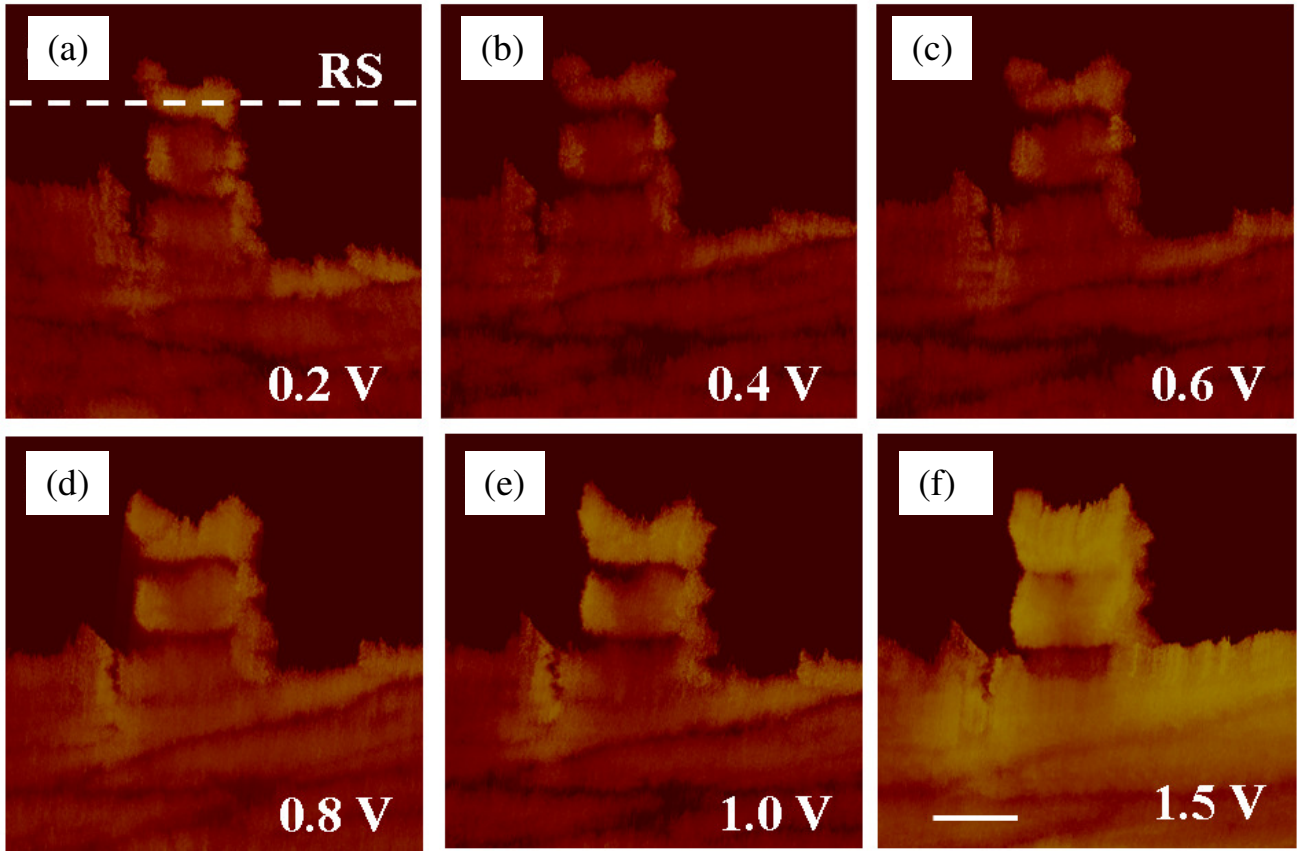


Figure A4.5 Variation of contrast in the SSRM image scans with the deflection voltage. As the deflection voltage (indicated in each figure) is increased from 0.2V in (a) to 1.5V in (f), the AFM tip presses with an increasing force on the sample surface. This increases the contrast by suppressing the effects of surface defects such as scratches. The scale bar is 100 nm.

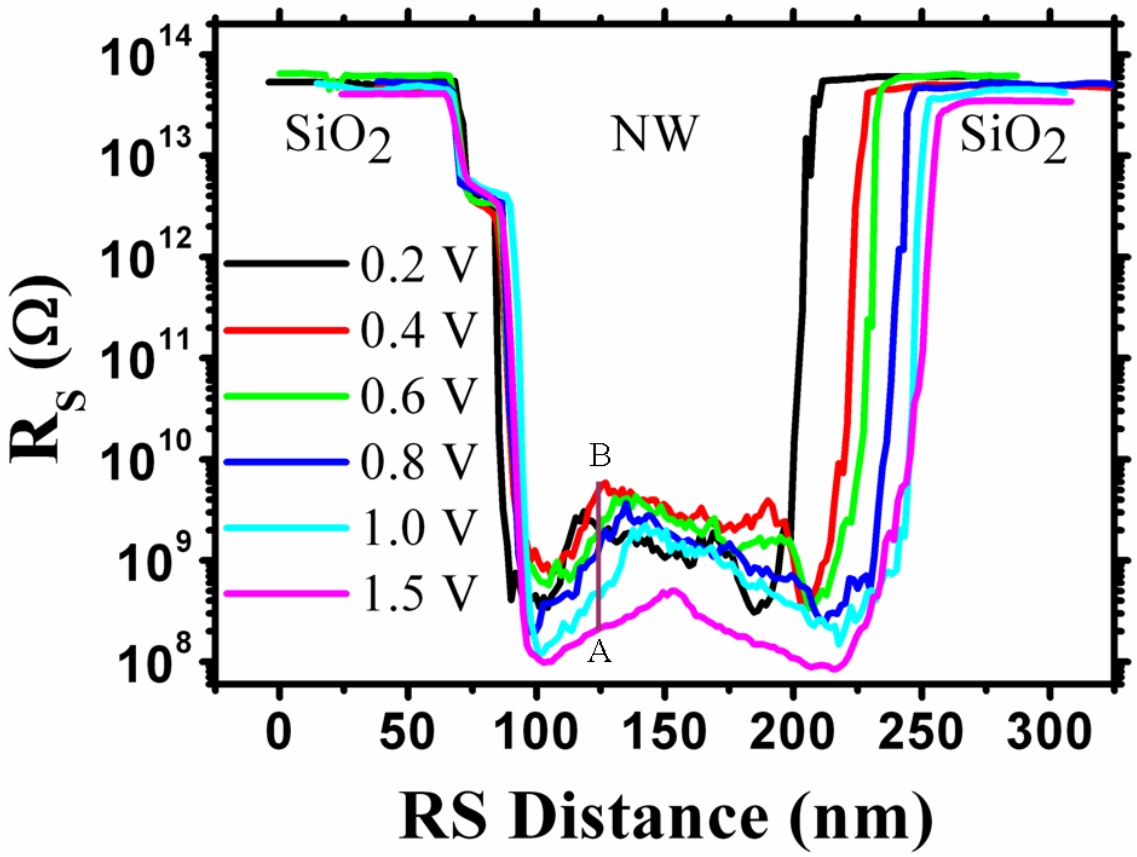


Figure A4.6 Average spreading resistance (R_S) values extracted from the SSRM images in Figure A4.5 along the direction R_S (see Figure A4.6(a)) at different deflection voltages (shown in the figure). R_S decreases consistently (from A to B) by two orders of magnitude with the increase of the deflection voltage as the AFM tip presses harder on the sample surface allowing higher current flow.

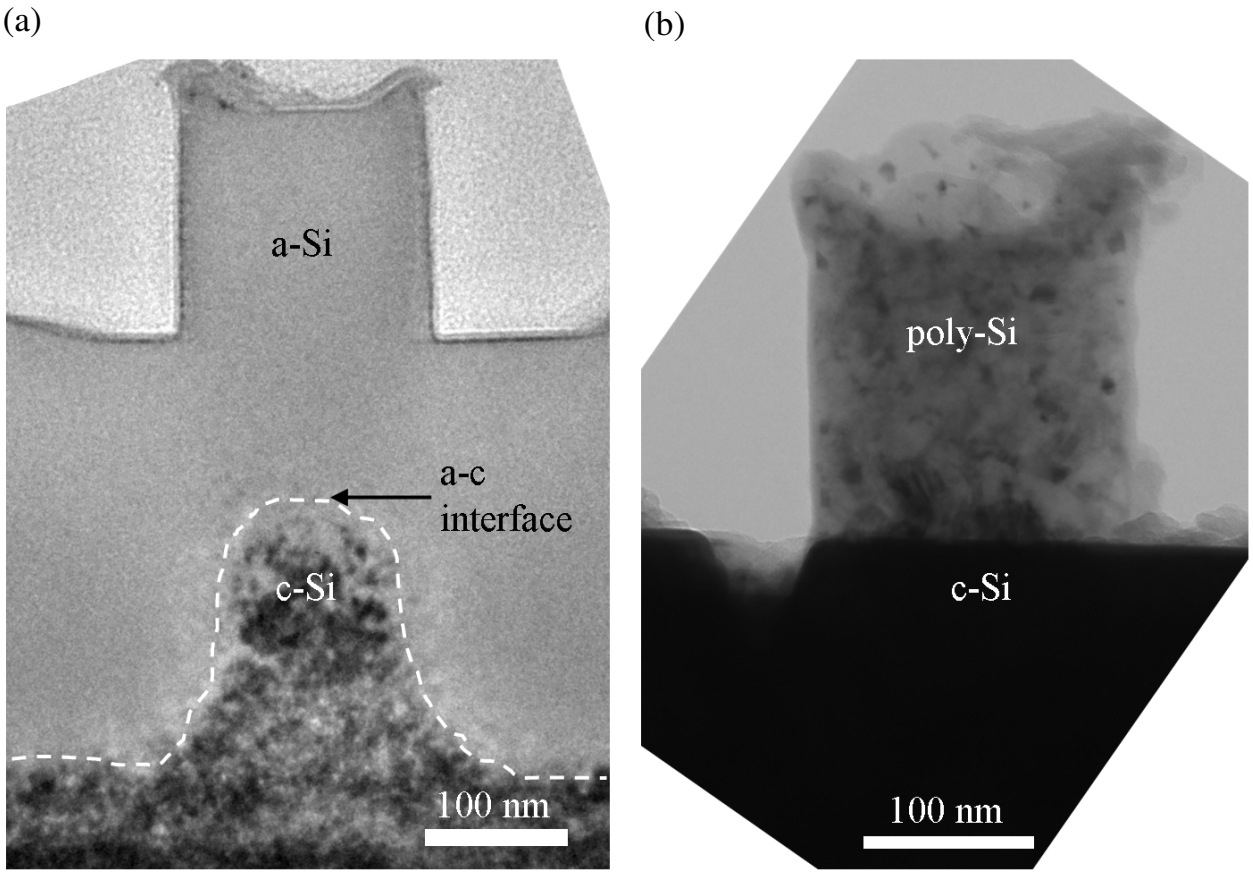


Figure A4.7 TEM images of shorter than average Si NWs. (a) A NW of length ~ 220nm with the amorphous-crystalline (a-c) interace around 120nm below the NW base. (b) A NW of equal length as the one in (a) after a single step thermal anneal at 900°C for 30 seconds by RTA. The entire NW turns poly-crystalline as the a-c interface too far below the NW base to recrystallize the NW by solid phase epitaxial regrowth (SPER).

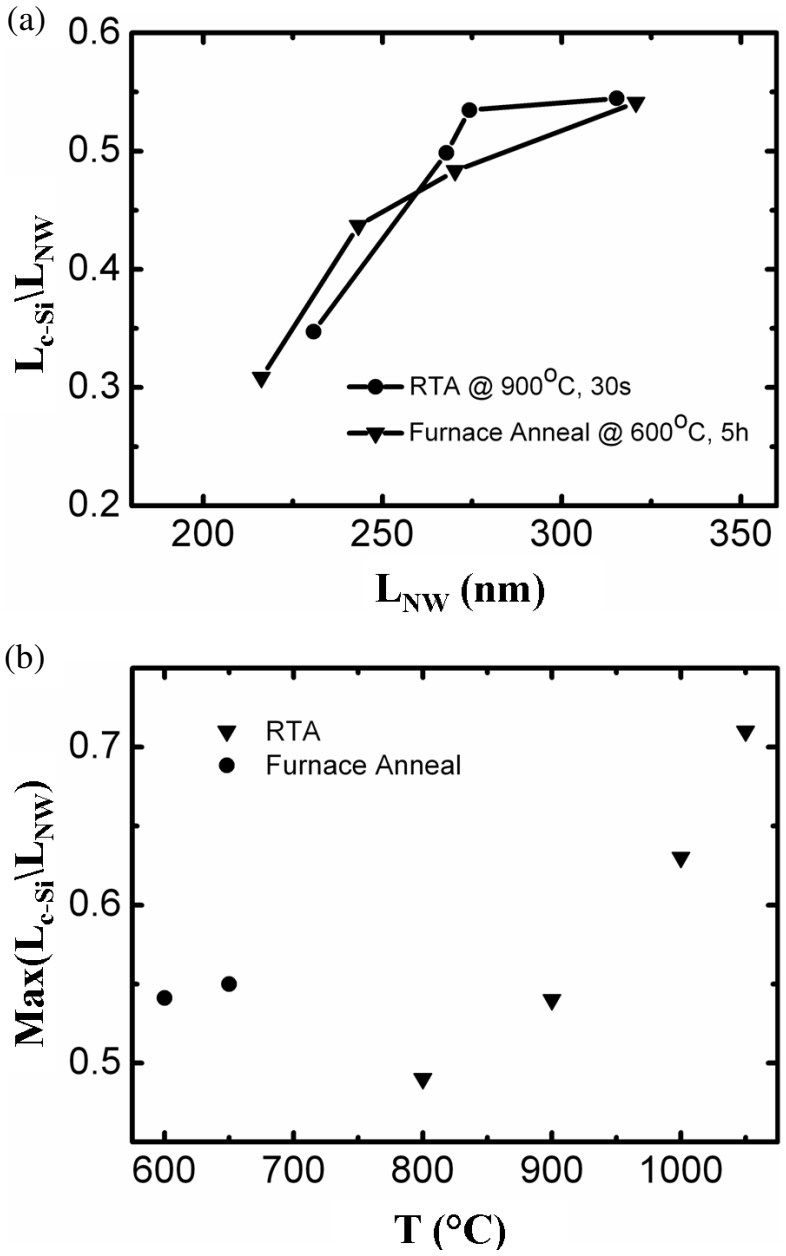


Figure A4.8 Dependence of the recrystallization on the NW length. (a) The fraction of single crystalline (c-Si) length ($L_{c\text{-}Si}$) w.r.t to the total length (L_{NW}) vs the total length (L_{NW}) for an RTA and furnace anneal. (b) The maximum fraction of the single-crystalline length vs annealing temperature (T) for both RTA and furnace anneal.

Erklärung an Eides statt (I)

Hiermit erkläre ich, dass ich die vorliegende Arbeit selbstständig und ohne fremde Hilfe verfasst, andere als die von mir angegebenen Quellen und Hilfsmittel nicht benutzt und die den benutzten Werken wörtlich oder inhaltlich entnommenen Stellen als solche kenntlich gemacht habe.
Eine Anmeldung der Promotionsabsicht habe ich an keiner anderen Fakultät einer Universität oder Hochschule beantragt.

Pratyush Das Kanungo
Halle (Saale), 28th April, 2011

Erklärung an Eides statt (II)

Hiermit erkläre ich, dass ich die vorliegende Arbeit selbstständig und ohne fremde Hilfe verfasst, andere als die von mir angegebenen Quellen und Hilfsmittel nicht benutzt und die den benutzten Werken wörtlich oder inhaltlich entnommenen Stellen als solche kenntlich gemacht habe.
Eine Anmeldung der Promotionsabsicht habe ich an keiner anderen Fakultät einer Universität oder Hochschule beantragt.

Pratyush Das Kanungo
Halle (Saale), 28th April, 2011

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EDUCATION			
Degree	**Year Received**	**Institute/University**	**Thesis**
Doctor rerum naturalium (Dr. rer. nat) in Physics	July, 2010 (Expected)	Max Planck Institute of Microstructure Physics & Martin Luther University, Halle, Germany	'On the doping of silicon nanowires' with Prof. Ulrich Gösele (recently passed away) & Dr. Hartmut Leipner
Master of Science in Electrical Engineering (MSEE)	January, 2005	University of Notre Dame, Indiana, USA	'Gated Hybrid Hall Effect Devices on Silicon' with Prof. Wolfgang Porod
Bachelor of Science (BS) in Physics	May, 2003	Indian Institute of Technology, Kharagpur, India	_

REASEARCH EXPERIENCE			
Institute/University	**Time Frame**	**Position**	**Project**
Max Planck Institute of Microstructure Physics	March, 2007 - Present	Graduate Research Assistant in the group of silicon/germanium molecular beam epitaxy (MBE)	MBE growth, in-situ and ex-situ doping, device fabrication, structural and electrical characterization of individual silicon and silicon-germanium nanowires
University of Notre Dame	August, 2003 – November, 2005	Graduate Research Assistant in the Center for Nanoscience and Technology	Design and fabrication of silicon metal-oxide-semiconductor-field-effect-transistor (MOSFET) based Hall effect devices
Indian Association for the Cultivation of Science	May – July, 2003	Undergraduate Summer Student Research Assistant in the group of ZnO thin films	Sol-gel growth and structural characterization of nickel and manganese doped ZnO thin films as a dilute magnetic semiconductor

TEACHING EXPERIENCE			
Institute/University	**Time Frame**	**Position**	**Class**
University of Notre Dame	January – April, 2004	Graduate Teaching Assistant	Electronics II Laboratory for Juniors majoring in Electrical Engineering

INDUSTRY EXPERIENCE			
Employer	**Time Frame**	**Position**	**Tasks**
KLA-TENCOR Corporation	March, 2006 – March, 2007	Application Development Engineer in the Electron Beam Defect Review division	**1.** Scanning electron imaging and review of material defects in silicon integrated circuits at different process steps **2.** Training Yield Engineers at United Microelectronics (Taiwan), and Chartered Semiconductors (Singapore)

PEER-REVIEWING EXPERIENCE

- Assisted supervisors in reviewing manuscripts from ACS Nano (ACS), Applied Physics A (Springer), and Journal of Crystal Growth (Elsevier)
- Assisted supervisors in reviewing project proposals from German Research Foundation, European Research Council and Israel Science Foundation

TECHNICAL SKILLS

Semiconductor Processing and Characterization

- Thin film deposition and epitaxial growth – Molecular Beam Epitaxy (MBE), Physical Vapor Deposition (PVD)
- Morphological characterization – Reflection High Energy Electron Diffraction (RHEED), Atomic Force Microscopy (AFM)
- Structural characterization – Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM)
- Device fabrication – Reactive Ion Etching (RIE), Sputtering, Oxidation, Annealing, Electron Beam Deposition, Optical and Electron Beam Lithography, Focused Ion Beam (FIB) Lithography in Class 1 – Class 1000 cleanrooms
- Electrical Transport – Current-Voltage, Capacitance-Voltage Measurements etc. in a Probe Station, inside a Cryostat, and inside an SEM using Nano-Manipulators

Computation

- Data Analysis – Origin, Matlab
- Simulation – SRIM, Silvaco TCADs
- Documentation – Microsoft Office, Open Office
- Image Processing - Adobe Photoshop, Paint-Net, Image-J
- Physical Layout Design – L-Edit

AWARDS

- Graduate Fellow, Department of Electrical Engineering, University of Notre Dame, Fall 2003
- National (India) Top 1% in Physics Olympiad, 1999

LANGUAGE PROFICIENCY

- English – Native Fluency
- German – Intermediate Fluency

OTHER ACTIVITES

- Member – IEEE, MRS, German Physical Society (DPG)
- Organizer – Max-Planck-Halle 'Movie-Nights'
- Former President – Phy Society and India Association at Notre Dame, a student club in the Physics department of IIT-Kharagpur and University of Notre Dame respectively

REFERENCES

Available on request

Publication List

Journals

1. 'Three-dimensional carrier profiling of individual Si nanowires by scanning spreading resistance microscopy', X. Ou, **P. Das Kanungo**, R. Koegler, P. Werner, U. Gösele and W. Skorupa (accepted in **Adv. Mater.**, Manuscript ID: adma.201001086)

2. 'Carrier profiling of individual Si nanowires by scanning spreading resistance microscopy', X. Ou, **P. Das Kanungo**, R. Koegler, P. Werner, U. Gösele, W. Skorupa and X. Wang, **Nano Lett.** 2010, 10, 171

3. 'A Novel Method to Fabricate Silicon Nanowire p–n Junctions by a Combination of Ion Implantation and in-situ Doping', **P. Das Kanungo**, R. Koegler, P. Werner, U. Gösele and W. Skorupa, **Nanoscale Res. Lett.** 2010, 5, 243

4. 'Comparison of the Top-Down and Bottom-Up Approach to Fabricate Nanowire-based Silicon/Germanium Heterostructures', A. Wolfsteller, N. Geyer, T.-K. Nguyen-Duc, **P. Das Kanungo**, N.D. Zakharov, M. Reiche, W. Erfurth,H. Blumtritt, P. Werner and U. Gösele, **Thin Solid Films** (in press), DOI:10.1016/j.tsf.2009.08.021

5. 'Enhanced electrical properties of nominally undoped Si/SiGe heterostructure nanowires grown by molecular beam epitaxy', **P. Das Kanungo**, A. Wolfsteller, N. D. Zakharov, P. Werner and U. Gösele, **Microelectron. J.** 2009, 40, 452

6. 'Ex-situ n and p doping of vertical epitaxial short silicon nanowires by ion implantation', **P. Das Kanungo**, R. Koegler, K. Nguyen-Duc, N. Zakharov, P. Werner and U. Gösele, **Nanotechnology.** 2009, 20, 165706

7. 'Controlled in-situ boron doping of short silicon nanowires grown by molecular beam epitaxy', **P. Das Kanungo**, N. Zakharov, J. Bauer, O. Breitenstein, P. Werner and U. Gösele, **Appl. Phys. Lett.** 2008, 92, 263107

8. 'Gated Hybrid Hall Effect Devices on Silicon', **P. Das Kanungo**, A. Imre, W. Bin, A. Orlov, G. Snider, W. Porod, N. P. carter, **Microelectron. J**. 2005, 36, 294297

Conference Presentations

1. 'Doping and electrical characterization of individual silicon nanowires' – Poster Presentation, **P. Das Kanungo**, X. Ou, R. Kögler, N. Zakharov, P. Werner, W. Skorupa and U. Gösele, **Spring Meeting of the Material Research Society (MRS)**, April 5 – 9, 2010, San Fransisco, USA

2. 'Ex situ n and p doping of vertical Si nanowires by ion implantation' – X. Ou, **P. Das Kanungo** and M. Zier, **Workshop Ion Beam Physics**, March 29 – 31, 2010, Forschungszentrum Dresden, Dresden, Germany

3. 'On the in-situ and ex-situ doping of silicon nanowires' – Oral Presentation, **P. Das Kanungo**, R. Koegler, N. Zakharov, P. Werner and U. Gösele, **12th International Conference on the Formation of Semiconductor Interfaces (ICFSI-12)**, July 5 – 10, 2009, Weimar, Germany

4. 'Doping of vertical silicon nanowires by ion implantation' – Oral Presentation, **P. Das Kanungo**, R. Koegler, N. Zakharov, P. Werner and U. Gösele, **Spring Meeting of the German Physical Society (DPG)**, March 22 - 27, 2009, Dresden, Germany

5. 'Optical and electrical characterization of silicon nanowires etched from highly doped silicon wafers', **P. Das Kanungo**, N. Geyer, O. Moutanabbir, M. Alexe, W. Erfurth, P. Werner, U. Gösele – poster, **Spring Meeting of the German Physical Society (DPG)**, March 22 – 27, 2009, Dresden, Germany

6. 'In-situ and ex-situ doping of silicon nanowires grown by molecular beam epitaxy – Oral Presentation, **P. Das Kanungo**, R. Koegler, N. Zakharov, P. Werner and U. Gösele, Summer **School on Nanowire based One-Dimensional Electronics (NODE)**, July 1 – 5, 2008, Cortona, Italy

7. 'Enhanced electrical properties of nominally undoped Si/SiGe heterostructure nanowires grown by molecular beam epitaxy' – Poster, **P. Das Kanungo**, A. Wolfsteller, N. D. Zakharov, P. Werner and U. Gösele, **Workshop of Recent Advances in Low Dimensional Structures and Devices (WRALDSD)**, April 7 – 9, Nottingham, England

8. 'Controlled boron doping of silicon nanowires grown by molecular beam epitaxy' - Poster, **P. Das Kanungo**, A. Wolfsteller, J. Bauer, O. Breitenstein, N. Zakharov, P. Werner and U Gösele, (Presented by A. Wolfsteller), **Spring Meeting of the Material Research Society (MRS)**, March 24 – 28, 2008, San Fransisco, USA

9. 'Electrical and optical characterization of boron doped silicon nanowires grown by molecular-beam epitaxy' – Poster, **P. Das Kanungo**, A. Wolfsteller, J. W. Chou1, O. Breitenstein, P. Werner and U. Gösele, Spring **Meeting of the German Physical Society (DPG)**, February 25 – 29, 2008, Berlin, Germany

10. 'Effect of gold on the electrical properties of silicon nanowhiskers grown by molecular beam epitaxy' - Poster, **P. Das Kanungo**, C. Büttner, J. Bauer, O. Breitenstein, N. Zakharov, P. Werner and U. Gösele, **397th Wilhelm and Else Heraeus Seminar - Semiconducting Nanowires**, October 14 – 17, 2007, Bad Honnef, Germany

Science Journalism

1. Prepared the following press-release on his collaborative paper
   'High, Not Flat: Nanowires for a New Chip Architecture'
   http://www.sciencedaily.com/releases/2010/02/100202103625.htm
2. Contributed to the reports in the MRS Spring 2010 Meeting Scene
   http://www.mrs.org/s_mrs/doc.asp?TrackID=ZTEVTP6BUN5G7M6QERQDLUBMTEBEWD6Z&CID=26519&DID=320537