Patterned Silicon Nanowires *p*-doped by Al-induced Crystallization for Photovoltaic Applications

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Gutachter:

1. Prof. Dr. Ralph Wehrspohn

2. Prof. Dr. Carsten Ronning

3. Dr. Jörg Schilling

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Chapter 1

Introduction: state of the art and motivation

The research on now-a-days called silicon nanowires (Si NWs) basically started with the first observation of an artificial silicon fiber in 1957 [Tre57] and with the explanation of the silicon wire growth mechanism in 1964 [Wag64]. In the last years metal-catalyzed NWs found applications in the most different fields, e.g. electronics, photonics, and sensorics [Sch06, Pea07, Jav07, Bec07, Li07, Yan09]. Research is driven by application requirements: possible catalyst materials, their deposition techniques, use of cheap substrates, and inexpensive methods which can be implemented on large scale. Moreover, depending on the application, either the in-place growth of single nanowires [Bec08], a large scale NW array [Kay07], or unorganized densely-packed NW forests [Ste08, Siv09a] may be preferred. Having the various applications in mind, the characterization of nanowires now investigates not only their crystallinity and reproducible synthesis, but also electrical properties like mobility and conductivity, as well as size-dependent effects. Of course, basic research drives these further developments, as only a thorough understanding of the mechanism of NW formation, crystallization, patterning, doping, etc., can lead to a high control of the synthesis process, allowing predictable and reproducible results.

Numerous publications focus on the use of new catalyst materials, in view of the substitution of the pioneer catalyst, gold. Although excellent results have been achieved with many other metals (see for example [Wan06, Kay07, Ke09] or the review paper [Sch10]), the use of gold is still preferred for testing other aspects. Gold-catalyzed nanowires can be used as a base for exploring new methods or applications, as the process conditions which lead to monocrystalline Si NWs are well known for different deposition techniques and precursors (see for instance [Mor98, Ste06, Kay06]). Also from a more theoretical point of view, the growth mechanism of Si NWs catalyzed by gold has been thoroughly investigated. The seminal publication which first nominated the Vapor-Liquid-Solid mechanism [Wag64] explained how the catalyst droplet incorporates silicon atoms during the process and supersaturates, causing the deposition of silicon at the Au/Si interface and consequently the formation of the nanowire. Later publications added more details to this model [Giv75, Han06, Sch08], which remains widely accepted.

Knowing the growth mechanism and the successful experimental parameters, research can now focus on other aspects. It is crucial for most applications, for instance, to control the NW diameter and position, where the latter refers to both the growth of patterned nanowire arrays and to the in-place selective growth of single nanowires. This control is achieved by controlling diameter and position of the catalyst particle. Different solutions have been proposed and successfully tested. They either rely on some type of lithographic process [Cro00, Fan06, Kay07, Lug10] or on the localized deposition by Focused Electron Beam (FEB) or Focused Ion Beam (FIB), as for instance in [Utk08, Mur09]. Nevertheless, such methods are characterized by laborious multi-step procedures (standard lithography) or they result in nanowires of poorer quality (FEB).

In this regard, two scalable solutions for patterning nanowires on various types of substrate are offered in this thesis. The selective in-place growth of single nanowires is obtained by combining FIB milling, FEB induced deposition (FEBID), and Chemical Vapor Deposition (CVD) [Ler10b]. For the proof-of-concept experiments, gold has been used as a catalyst, deposited by FEB using a gas precursor. Nevertheless, the method can be applied also to other selected catalyst materials, growth mechanisms, and deposition techniques. Concerning the growth of nanowire arrays uniformly covering large areas, the patterning has been performed by nanosphere lithography (NSL) combined with sputtering and annealing [Ler10a]. NSL is considered one of the inexpensive alternatives to e-beam lithography. The NSL mask is constituted by polysterene spheres uniformly spin-coated over large areas of the sample ($> 50\ \mu\text{m}^2$). The following steps of gold deposition, sphere removal, and annealing result in a gold dot array with a narrow diameter distribution which mainly depends on the annealing conditions [Bec10]. The Si NWs catalyzed by these dots and grown by CVD are orderly positioned and characterized by a similar diameter. Such an array of nanowires with a sharp diameter distribution is of crucial importance when dealing with applications in the photovoltaics, e.g. a nanowire-based solar cell. In fact, the NW diameter influences the effective doping of the nanostructures [Sch10] and their doping determines the technical properties of the solar cell.

The NSL-patterned NWs have been used for realizing a nanowire-based solar cell where this control can be achieved. Generally, a solar cell is composed by an *n*- and a *p*-doped region. The NWs have been *n*-doped during the growth process. The *p*-doping has been achieved by a technique, the Al-induced crystallization (AIC) of silicon, which has not been tested on NWs so far.

The AIC of Si is a solid phase transition where a layer of amorphous silicon (a-Si) and one of Al, deposited on a substrate, interchange their positions when annealed. During the annealing the *p*-doping and the crystallization of the Si layer take place as well. The silicon layer grows epitaxially to the substrate, if it is monocrystalline. The AIC process has been investigated since 1972 [Her72], but only in the past decade the exact process dynamics and influent parameters were studied in detail [Nas00b, Nas00c, Nas00a, Nas01, Zha04, He05a, He05b, He06, Civ09]. Despite of these reports, some aspects are still not clear, like the overall process driving force and the role of an oxide interface layer between the Al and Si layers. In this work the thermodynamics of the AIC process is evaluated, clarifying the impact of the oxide layer and explaining the observed experimental results: the AIC process has been applied on planar geometries, also for the synthesis of nanostructures, as well as on nanowires, for the doping of epitaxial Si-shells around them. In particular, *p*-doped epitaxial Si layers have been formed around *n*-doped NSL-patterned Si NWs, obtaining a radial *p*-*n* junction in each nanowire. A nanowire-based solar cell has been realized combining the two physical phenomena studied in this work: AIC and NW growth, where NSL patterning allows a narrow diameter distribution and, consequently, control of the nanowire doping.

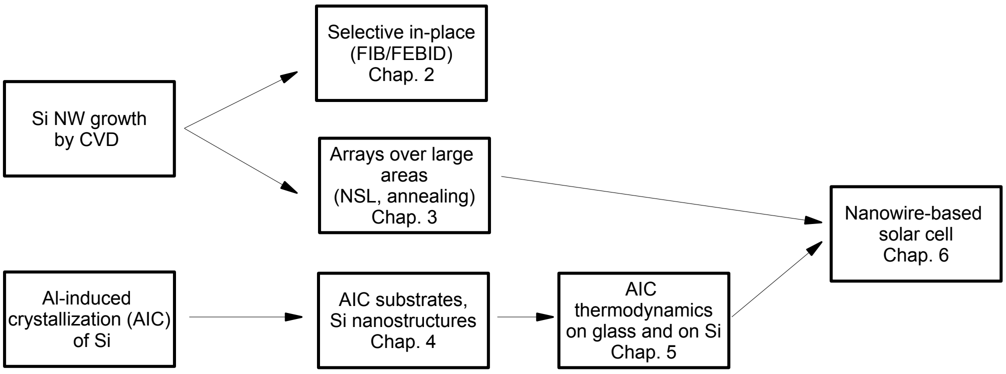

Figure 1.1: *Scheme of the structure of this thesis.*

This thesis is structured as follows (see Fig. 1.1). The first two chapters focus on the synthesis of Si NWs. Chap. 2 offers first a brief introduction of the published results and the technical parameters typical of FIB and FEBID. Subsequently, our FEBID structures are shown and characterized before and after an annealing step. By using a sacrificial layer, such structures have been used as a catalyst for selective in-place growth of Si NWs by CVD. Single monocrystalline NWs could be synthesized on both wafer substrates and AFM tips. Chap. 3 describes the use of nanosphere lithography for achieving NW arrays over large areas. After summarizing the state of the art, the gold dot arrays obtained by NSL are studied for different annealing parameters, namely temperature and time. Such arrays catalyze patterned epitaxial Si NWs by CVD.

The two following chapters focus on the AIC process, introduced in Chap. 4. The experimental results are presented, which include the synthesis of Si nanostructures by different techniques on substrates formed by Al and Si layers on glass. Different morphologies could be realized, from “nanoballoons” to nanowires. Possible growth mechanisms are suggested based on diffusion-limited aggregation and reaction-limited growth, respectively. The reactants present in the process chamber which could contribute to the growth process by chemical vapor deposition are discussed in Appendix A. Subsequently, in Chap. 5, the AIC process is discussed from a thermodynamical point of view. Based on the “macroscopic atom” model, we calculated the Gibbs energy differences of five layer configurations, with and without oxides, on glass and on silicon. The results explain the experimental findings and the role of the oxide layer, allowing to control and predict the layer configuration after annealing. The calculations for the basic case without oxide have been derived from results presented in literature and are reported in Appendix B.

These findings are then employed in Chap. 6 for achieving epitaxial *p*-Si shells around *n*-doped NSL-patterned nanowires. The so-obtained radial *p*-*n* junction is used for the realization of a nanowire-based solar cell prototype. The measured I-V characteristic is discussed and compared with published solar cell performances.

Finally, the conclusions (Chap. 7) summarize the results achieved in this thesis and suggest possible future work.

Chapter 2

Selective in-place growth of Si nanowires (Si NWs)

The subject of this chapter is the in-place growth of Si nanowires selectively where a gold precursor had been deposited. The procedure combines Focused Ion Beam (FIB) milling, Focused Electron Beam Induced Deposition (FEBID), and Chemical Vapor Deposition (CVD) for performing Vapor-Liquid-Solid (VLS) growth. Nanowires were successfully synthesized on both silicon wafer and Atomic Force Microscope (AFM) tips.

The results have been achieved in collaboration with the EMPA in Thun, particularly with Dr. M. Jenke of the group of Dr. I. Utke / Dr. J. Michler. Part of these results is being published [Ler10b].

In the next section, the motivation for the studied method is given, together with the comparison to related publications. A brief description of the FIB, FEBID, and VLS characteristics relevant to the investigated samples is offered in the subsequent section. Successively, the experimental parameters are listed, followed by the achieved results. The chapter is closed by conclusions and suggestions for future work.

2.1 Introduction

In the past 20 years, the mechanism which allows a controlled growth of high-quality Si nanowires has been investigated. Now, mono- or polycrystalline Si nanowires are achieved by standard procedures at least for common growth conditions and catalyst materials. The contemporary research in the field is challenged by the NW synthesis in view of various applications, e.g. in nanoelectronics, nanophotonics and nanomechanics [Sch06, Pea07, Jav07, Bec07, Li07]. This includes (i) the synthesis of high quality monocrystalline NWs uniformly organized on large areas, which will be addressed in the next chapter; and (ii) the growth of single nanowires, selectively localized with high spatial resolution.

So far, the in-place growth of nanowires or nanostructures has been generally achieved with two different methods: (i) a large-area lithographic process [Kay07] or (ii) a localized deposition by a focused beam using a gas precursor (see below). The use of lithography implies a multistep procedure, a high cost, and possibly tedious alignment issues. It can be used for single-nanowire synthesis [Lug10], but it is laborious, while the etching steps included in the lithographic process might damage other important regions of the sample surface. When the in-place growth could not be achieved, the nanowires have been removed from their original substrate and transferred to the desired location by nanomanipulation [Bec08]. This allows full control on the NW position, but includes long processing time, tedious nanomanipulation tasks, high risk of breaking the nanodevice and no possibility of large scale implementation.

The deposition induced by focused electron or ion beam enables to realize nanostructures selectively in-place in one single step and without affecting the substrate. The nanostructures realized by FEBID have been investigated in literature concerning, for instance, Si nanodots [Syc10], tungsten nanowires [Kle08, Che10], platinum nanowires [Fra06, Mur09], gold nanodots and nanopillars [Dha09], iron and iron oxide nanowires and antennas [Fur07, Shi07], or even in absence of precursor gas using only gas residuals on different substrates [Mat88, Ued04]. These structures have been characterized from a crystallographic perspective and sometimes their electric or magnetic properties have been measured as well [Utk00b, Li06, Fur07, Gaz08], also in dependence on the temperature of a successive annealing [Erv07]. They are affected by at least one of the following drawbacks: high carbon content, nanocrystallinity, high surface roughness, sensitivity to even low-temperature annealing steps. In addition to this, the generally high costs of the gas precursor and the long deposition time required for realizing such structures have to be considered. Despite these disadvantages, the FEBID represents a remarkable option for a damage-free patterning of any substrate with absolut freedom in the feature shape and size.

Ideally, one should use the damage-free one-step patterning typical of the FEBID for structuring surfaces used as a template by other methods for the synthesis of high-quality nanostructures. In the case of Si nanowires synthesized via the Vapor-Liquid-Solid (VLS) mechanism, this means that the catalyst particles are deposited with high spatial resolution by the focused electron beam; subsequently, they are used for growing monocrystalline silicon nanowires by a bottom-up approach, like e.g. Chemical Vapor Deposition (CVD). The grown nanowires preserve all their typical mechanical and material properties. For instance, they do not present a high carbon content and, consequently, they do not shrink like the FEBID realized nanowires when annealed [Erv07, Utk08]. In addition to this, the amount of precursor used for the deposition of the catalyst particle is significantly less than the one needed for realizing a whole nanostructure, so that the costs and the processing duration are reduced. But contrary to the nanowire arrays obtained by other patterning methods, the wires catalyzed by FEB-deposited materials can be synthesized singularly in-place, even on pre-structured surfaces, without affecting other areas of the sample.

This is shown in this chapter. We patterned the gold catalyst particles combining FIB milling and FEBID; subsequently, we grew the nanowires by Chemical Vapor Deposition (CVD). It is worth mentioning that the precursor gas for the CVD process is silane diluted in argon: no high-temperatures due to $SiCl_4$ nor expensive helium are needed for the overall process. Monocrystalline Si nanowires have been obtained both on Si wafer as well as on AFM tips, as an example for the possibility of selectively growing NWs on any type of surface, also pre-structured. The pattern has flexible feature size and shape and high control of the NW diameter is achieved.

To the best of the author's knowledge, this is the first time that both top-down techniques, FIB and FEBID, are combined with a bottom-up growth mechanism (CVD) for achieving selective in-place NW synthesis. The use of FEBID for patterning nanowires has already been reported combined with Reactive Ion Etching [Gua08]. Nevertheless, this approach might be destructive for most types of structures and materials. The combination of FEBID with a VLS-based growth process allows a high control on the wire location without damages. Such combination has been tested by Wanzenboeck et al. [Wan08], who could confine the Si NW synthesis to previously FEB-deposited gold structures, though without achieving highly selective growth of single nanowires, e.g. control of their position and of their diameter.

It is noteworthy that this method can be easily used with other materials: a wide range of gas precursors is available for FEBID and for CVD. In addition to this, other bottom-up techniques can be chosen, where the material is evaporated from a crucible and no gas precursor is used (e.g. Molecular Beam Epitaxy, Electron Beam Evaporation). In this view, the range of semiconductors and metals which can be grown catalyzed by FEBID-patterns is even wider.

2.2 Used techniques and mechanisms

This section briefly explains the experimental methods used in this chapter and highlights the aspects which are important to the realization of the samples and for the interpretation of the results. It does not want to offer an exhaustive review of the technical and theoretical studies in this matter.

First, the implications of the milling by Focused Ion Beam are summarized. Then, the Focused Electron Beam Induced Deposition is presented, without discussing any type of modeling of its principles and of the concurring physical processes which take place during deposition; the modeling is discussed in the cited references. The last part briefly describes the Vapor-Liquid-Solid mechanism, which will also be used for the synthesis of the samples in the next chapter.

2.2.1 Focused Ion Beam (FIB)

The focused ion beam (FIB) was first applied in the field of micro- and nanofabrication in 1973 [Sel73]. The ion beam can mill, implant or damage materials directly; in presence of a gas ambient, it can deposit or etch. Its first applications included photomask repair and sample preparation for transmission electron microscopy (TEM). The main drawbacks consist in the unavoidable ion implantation with consequent surface damages, the degree of contamination depending on the used ion source. Commonly, a liquid metal ion source is used. The metal ions need to have a low enough vapor pressure in order to operate in vacuum, a low-temperature melting point, and little chemical reaction but high wet-ability with the system. Prevalently Ga^+ sources are used, although alloys can be used as well, e.g. Au/Si. In case less contamination is desired, species such as hydrogen should be employed, i.e. a gas field ion source or a gaseous plasma source.

In this work the FIB system, equipped with a Ga^+ source, has been used without the presence of gas and exclusively for site-specific milling. The FIB milling is stress-free, non-thermal, and directional [Ish08]. It is based on ion-solid interactions. More in detail, the FIB system is formed by the liquid metal ion source, the lenses, the apertures, and the beam deflector. The ion source ends in a tungsten needle, which is located in the middle of the extractor electrode. When the needle has a voltage more positive than the extractor, a high electric field forms at the Ga-wetted needle tip. This causes the liquid Ga to form a point source. Under high electric field, the source material is extracted as ions, while liquid Ga from the reservoir flows to the needle for replacing the evaporated particles.

With an atomic mass of circa 70 amu, the Ga ions are heavy enough to sputter the target atoms when the energy transferred to them from the incident particle is bigger than the atom displacement energy. In this case, the target atoms are knocked out from their lattice positions and secondary ions and electrons are generated, which are mainly used for imaging. In addition, some of the ions are implanted and retained in the target. The implanted ion depth-profile is characterized by a Gaussian-like curve. Increasing the ion dose, the target surface is eroded by sputtering and the implanted ions accumulate below the sputtered layer [Ish08]. Under certain ion bombardment conditions, a steady state between ion implantation and ion removal can be reached. For a Si cross sections and at an acceleration voltage of 30 keV, the implanted Ga ions are located within 10 nm from the target surface and their calculated surface concentrations is about 4 at% [Ish08].

The ion bombardment also causes a collision cascade which results in damages to crystalline samples. The thickness of the damaged layer, which becomes amorphous, depends on the acceleration voltage, as plotted in Fig. 2.1a. At 30 keV the amorphous layer is approximately 20 nm thick. Such damage depth can be reduced by lowering the beam energy, by using broad ion beam (BIB) milling, or by milling at grazing incidence. Nevertheless, a lower beam energy reduces the milling rate, prolonging the processing time, and increases the beam size, losing in site-specificity, as also in the case of the use of a BIB.

All the implications resulting by the use of a focused ion beam on a target are schematically sketched in Fig. 2.1b.

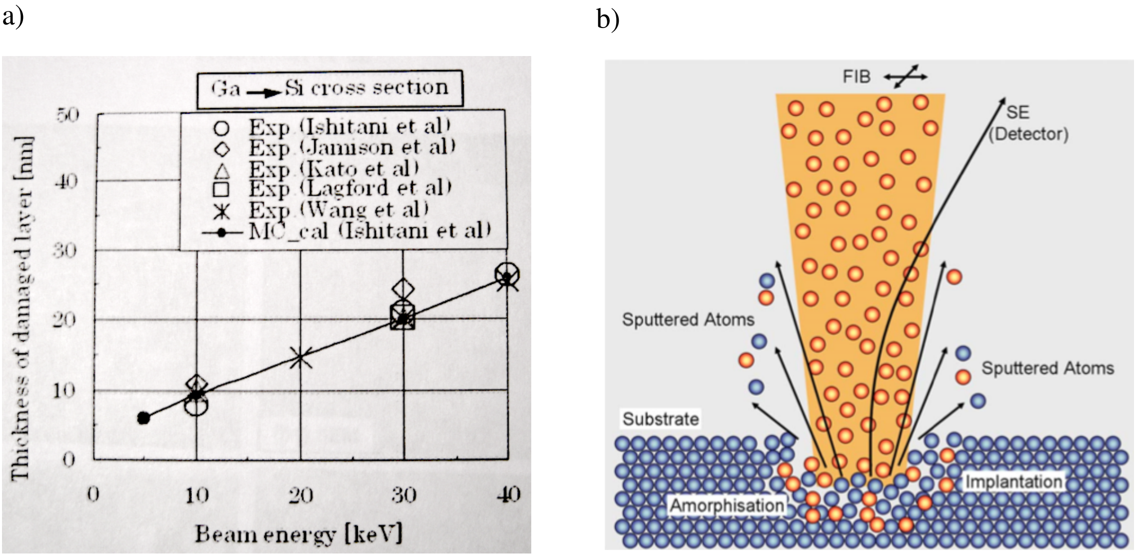

Figure 2.1: ***a)**: Plot of the thickness of the FIB-generated amorphous layer on a crystalline Si target as a function of the acceleration voltage. All the points are experimental values with exception of the filled circles, which are obtained from Monte-Carlo calculations. Reproduced with permission from [Ish08]. **b)**: Schematic drawing of the principles of FIB milling. When an ion beam bombards the target and sufficient energy is transferred to the target atoms, the target atoms are sputtered, while also secondary ions and electrons are generated. In addition to this, Ga^{+} is implanted in the sample and an amorphous layer is formed on the target. Reproduced with permission from [Utk08]. Copyright 2008, American Vacuum Society.*

2.2.2 Focused Electron Beam Induced Deposition (FEBID)

The fabrication of features by focused electron beam (FEB) was first demonstrated in 1934 [Ste34] using carbon contamination. Recently, it is becoming more widely employed and preferred to the focused ion beam because it does neither implant ions nor damage the processed surface. "The electron-beam induced deposition is a nanofabrication technique in which a precursor gas is introduced to a sample, where it is decomposed by a focused electron beam, so that a nanosize structure is fabricated" [Mit08]. The precursor gas molecules are composed of a volatile and a non-volatile part. When the molecules enters the electron beam, it becomes unstable, separating into its volatile and non-volatile components. The volatile parts are pumped away. The non-volatile components deposit on the sample surface.

The resolution of the FEB induced deposition (FEBID) is controlled by the electron beam characteristics and by the interactions of the electrons with the precursor and with the substrate. The ideal electron beam for FEBID is small and intense. Nevertheless, in typical conditions the current distribution presents a central maximum and a more extended tail with maxima and minima [Cro10]; even a bimodal deposition distribution has been reported [Utk08]. This implies that non-local deposition in nanofabrication is intrinsic in FEBID, as some fraction of the electron intensity is present in the tail of the current distribution.

Other factors increase the possibility of non-local deposition. It is still not clear whether the dissociation process of the precursor molecules is dominated by the primary or by the secondary electrons [Cro10, Utk08]. In case the secondary electrons drive the dissociation process, the range in which the non-volatile components of the adsorbed molecules can deposit might be wider than the region irradiated by the electron beam (see Fig. 2.2a). Only secondary electrons traveling parallel to the surface might participate in the dissociation process. They are likely to cover up to one mean free path from the primary beam before being scattered out of the surface. Their mean free path upper limit ranges from a few nanometers [Cro10] to some micrometers [Utk08], depending on the chamber pressure and other parameters. In addition to this, the geometry of the precursor injection needle and the electron beam can spread the adsorbed molecules quite far from the primary electrons, as shown in Figure 2.2b. Backscattered electrons or primary electrons scattered in the gas can crash precursor molecules far from the irradiated regions.

It is worth mentioning that a significant carbon content has been found in the deposits even when it is not present in the used precursors. This carbon derives from hydrocarbon species present in the vacuum system and on the sample surface [Cro10]. They practically provide a second precursor. A lower carbon concentration can be achieved using clean substrates (heated in vacuum or etched by plasma), using ultra-high vacuum conditions, or performing the deposition on a heated substrate (for instance, 150°C). The carbon content might determine the material composition of the deposit. The analysis often revealed that it was formed by the material of the precursor (gold, platinum) embedded in a carbon matrix [Utk08]. In addition to this, deposits result in most cases to be an aggregation of nanocrystallites.

Contrarily to FIB, during FEBID the electrons entering the sample transfer relatively small energy to the target atoms, because of the large mass difference. Therefore, no sputtering nor amorphization occurs, but rather electron diffraction, phonon scattering, and backscattering. These effects are not crucial for the samples studied in this work, if not for decreasing the selectivity of the deposition, as mentioned earlier. They are therefore not further considered.

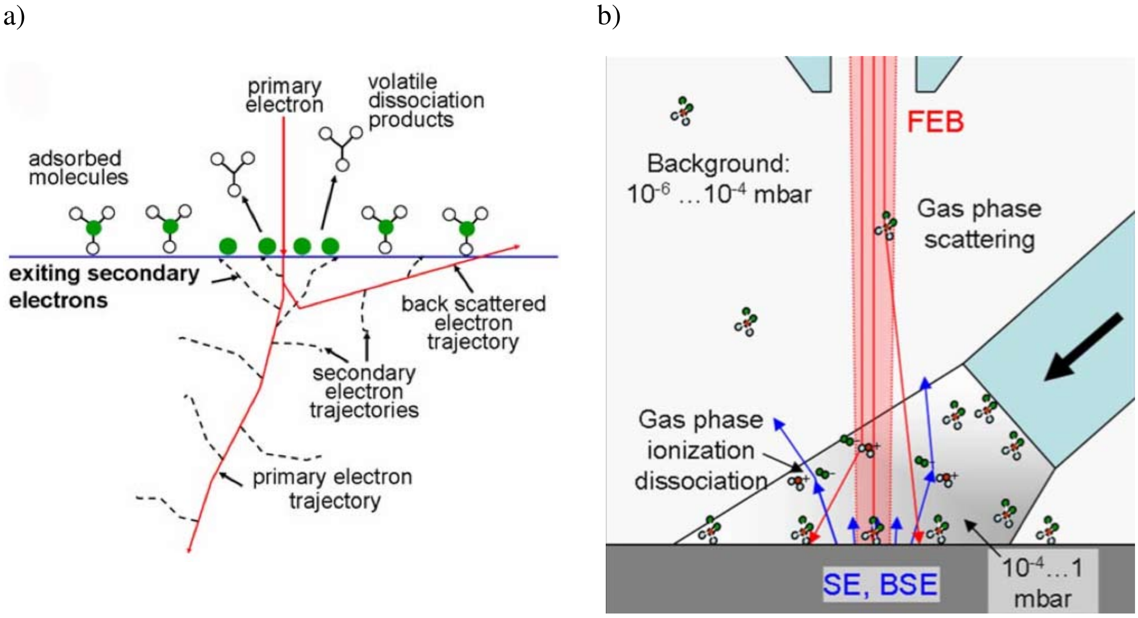

Figure 2.2: ***a)**: Sketch of the path of a primary electron and the correlated processes. The primary electron might create secondary and back-scattered electrons, which can both dissociate precursor molecules deposited on the sample surface, even if quite far from the primary electron trajectory. **b)**: Schematic representation of the focused electron beam and the precursor needle inside the microscope chamber. Because of the geometry of the system, gas precursor molecules can be dissociated by secondary and back-scattered electrons also far from the irradiated region. Both images are reproduced with permission from [Utk08]. Copyright 2008, American Vacuum Society.*

Finally, it has to be highlighted that FEBID is a direct writing technique and therefore characterized by a one-step processing, e.g. contrarily to lithography.

2.2.3 The Vapor-Liquid-Solid (VLS) growth mechanism

The Vapor-Liquid-Solid mechanism [Wag64] is based on a catalyst particle, which strongly enhances the growth of Si NWs. As discussed in [Sch10], the catalyst can be represented by various materials. Here, the case of gold is considered for growth by Chemical Vapor Deposition (CVD). The gold is the standard catalyst for the VLS growth because of the Au/Si phase diagram (see Fig. 2.3), characterized by a low eutectic temperature $T_E = 363°C$. At temperatures higher than T_E, gold and silicon form a Si-rich liquid alloy.

The name of the VLS mechanism summarizes the three steps which lead to the synthesis of the nanowire: (i) vapor: during the CVD process, a gaseous silicon precursor is supplied, e.g. silane. Its molecules are cracked on the catalyst droplet surface into hydrogen and silicon: $SiH_4 \rightarrow Si + 2H_2$. (ii) liquid: the silicon is incorporated in the liquid alloy droplet and diffuses through the droplet to the liquid/solid interface. (iii) solid: the droplet supersaturates, causing silicon to deposit and condensate at the droplet/substrate interface, forming the nanowire.

Some very similar mechanisms are called Solid-Liquid-Solid or Vapor-Solid-Solid mechanisms, depending on the state of the supplied silicon or of the catalyst droplet. Nevertheless, the dynamic is absolutely comparable.

The VLS mechanism has been extensively studied from both an experimental and a theoretical

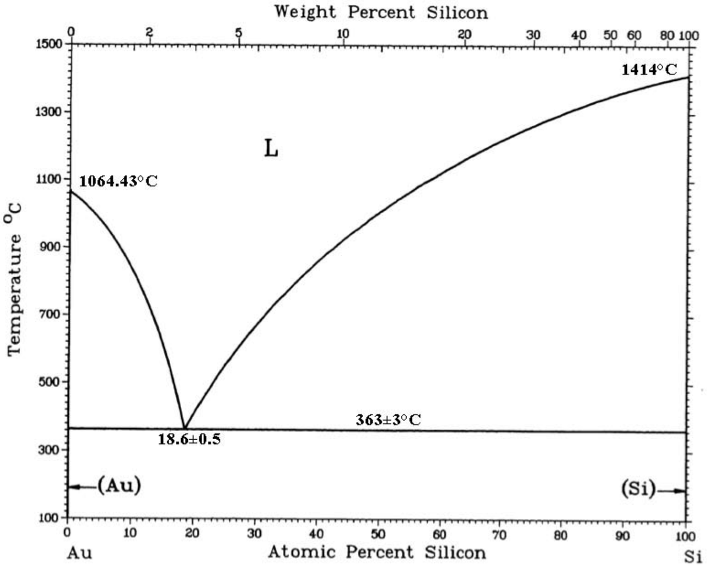

Figure 2.3: *Phase diagram of the Au/Si system. Note the eutecticum at* $363°C$*. From [Mas90]*

point of view [Sch10], as it has many implications for Si nanowire growth. Its effects on the results reported in this work are discussed in the single chapters, when relevant.

2.3 Experimental parameters

The substrate is represented by either an AFM tip or a (111) Si wafer previously cleaned in acetone and ethanol. The sample has then been oxidized by annealing in a furnace at 1000°C in air for 27 minutes, the resulting oxide thickness being 50 nm. The oxidized sample is loaded into the microscope, a dual beam Lyra FIB-SEM from TESCAN s.r.o. equipped with a gas injection system of the company alemnis GmbH. The FIB has a Ga^+ ion source. Its theoretical resolution limit is 5 nm at an acceleration voltage of 30 kV and a probe current of 10 pA. The resulting nominal full width at half maximum of the beam diameter is 10 nm. The silicon oxide layer is patterned by FIB milling, forming holes. The milling rate in the oxidized SiO_2 has been measured and results to be approximately 0.5 $\mu m^3/(nA \cdot s)$ [Ler10b], while it is higher if also the underlying Si wafer is milled, namely 0.6 $\mu m^3/(nA \cdot s)$ [Ler10b]. The hole diameters range between 40 and 800 nm and the hole depth between 50 and 150 nm.

Gold is deposited inside the holes by FEBID using either Dimethyl(trifluoroacetylacetonate)-gold(III) ($Me_2Au(tfac)$) (CAS 63470-53-1) or Dimethyl(acetylacetonate)gold(III) ($Me_2Au(acac)$) (CAS 14951-50-9) as precursors. The parameters for the gold deposition are: electron acceleration voltage 30 kV, electron probe current 9 to 30 pA, beam diameter 17 to 30 nm, deposition time 10 to 300 s.

Some of the samples have been purified by oxygen plasma (200 W, 40 kHz, 320 cm^3/min, 99.9% O_2, process time 45 min). In the case of AFM tips, the sample has been mounted mechanically on a clean Si holder. Just before loading the samples into the CVD process chamber, they have all been etched in 5% HF for 3 minutes. The CVD base pressure is approximately 10^{-7} mbar. Process temperature and pressure are approximately 525°C and 0.5 mbar, respectively. The

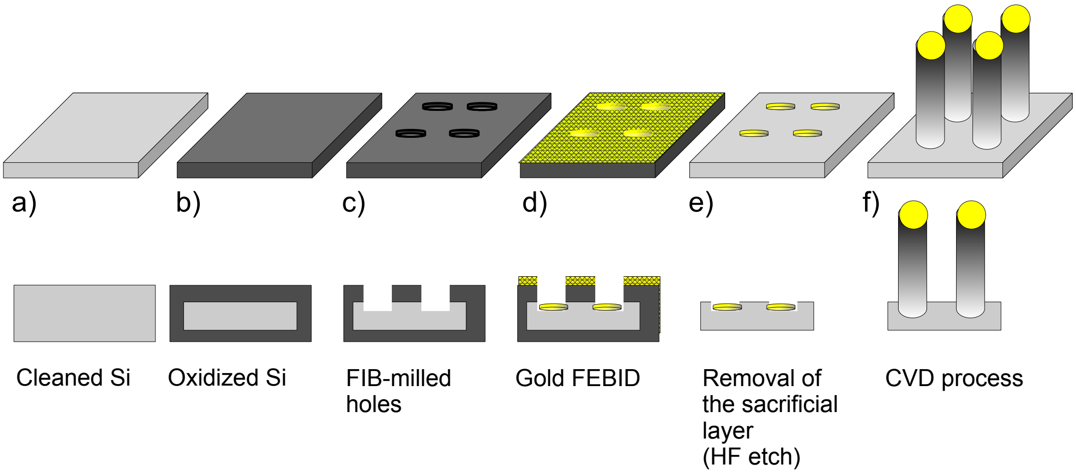

Figure 2.4: *Schematic representation (top line: tilted view, bottom line: cross section) of the combined FIB/FEBID/CVD process for the realization of in-place grown nanowires.* ***a)****: cleaned substrate, here a Si wafer.* ***b)****: formation of a sacrificial layer on the substrate surface. Here, oxidation in air. The sacrificial layer is therefore all around the substrate, but this has no influence on the overall process.* ***c)****: FIB-milling of holes. The holes have to be deep enough to reach the substrate below the sacrificial layer.* ***d)****: gold FEBID. The electron beam allows to deposit the non-volatile part of the precursor molecule in the hole. Nevertheless, as explained in Sect. 2.2.2, the gold particles could deposit also on neighboring regions.* ***e)****: removal of the sacrificial layer, e.g. here, etch in HF.* ***f)****: CVD process and nanowire synthesis.*

process takes place in a flow of 5 sccm Ar and 4 sccm SiH_4 for 15 minutes. In some cases, the Ar has been substituted by He, keeping the other parameters constant.

When the CVD chamber cools down to room temperature, the samples are unloaded. Their characterization has been performed with an Scanning Electron Microscope (SEM, Hitachi S-4800) equipped with a detector for electron back-scattered diffraction (EBSD) and for scanning transmission electron microscopy (STEM) with an acceleration voltage up to 30 kV. Additionally, energy-dispersive X-ray spectroscopy (EDX, Hitachi S4800 136-10, voltage: 5kV) analyses have been achieved. Atomic force microscope (AFM) scans have been performed with a M4 of Park Scientific Instruments using a silicon tip with a radius equal to 3 nm.

The whole process is sketched in Figure 2.4.

2.3.1 The gold precursor

In this work, two gold precursors have been used for FEBID deposition and consequently for catalyzing the Si NWs. No differences could be detected among the wires grown with different precursors. Both precursors are characterized by a high carbon content. Nevertheless, the Me_2Au(tfac) percent of carbon is far less than the amount of most precursors, which is generally around 80% [Utk08]. Their chemical composition, obtained by EDX, is reported in Tab. 2.1. More information about the properties, composition and use of the Me_2Au(tfac) can be found, for instance, in [Utk00a, Utk08], while the Me_2Au(acac) precursor is studied in [Rüb89, Vic03, Wnu10].

	$Me_2Au(acac)$ [At%]	$Me_2Au(tfac)$ [At%]
C K	88.2	49.3
Au M	11.8	50.7

Table 2.1: *EDX measurement regarding the composition of the two gold precursors used in this work for catalyzing Si NWs.*

2.4 Localized Si NWs on wafer

The idea of using the gold particles deposited by FEBID for catalyzing Si NWs is not completely new. Nevertheless, first trials show no selectivity in the exact position of the grown nanowires [Wan08]. This is due to the mechanism itself on which FEBID is based: the precursor gas containing the gold molecules is cracked by the electron beam. The broken molecules present some volatile parts, which are pumped away, and some heavier parts, which deposit. The range within which such non-volatile components deposit exceeds the electron beam diameter, as explained in Sect. 2.2.2. Every tiny amount of gold can lead to the growth of a Si nanowire, independently on the amount of gold deposited. This is shown in Figure 2.5, where the array of gold dots deposited by FEBID is almost barely recognizable in the NW forest. In order to obtain a nanowire pattern, one has to prevent the deposition of gold outside the array, that is, far from the electron beam focus. With this goal a structured sacrificial layer is introduced: the gold deposits on such layer, but is removed prior to the CVD process, unless the gold is located inside the milled holes of the sacrificial layer. More in detail, the sacrificial layer is represented here by a silicon oxide layer grown by oxidation in air all around the sample. It has to be noted that it can be synthesized by any method, as it is a sacrificial layer. The oxidation in air has been chosen because of the available equipment. Some other materials could be used as well, but the silicon oxide has the advantages that it is cheap, easy to form and easy to etch without damaging the other materials (silicon, gold). For the selective growth of nanowires, the sacrificial layer must be characterized by holes in which the catalyst can be deposited. The holes must be deep enough to reach the silicon surface, so that

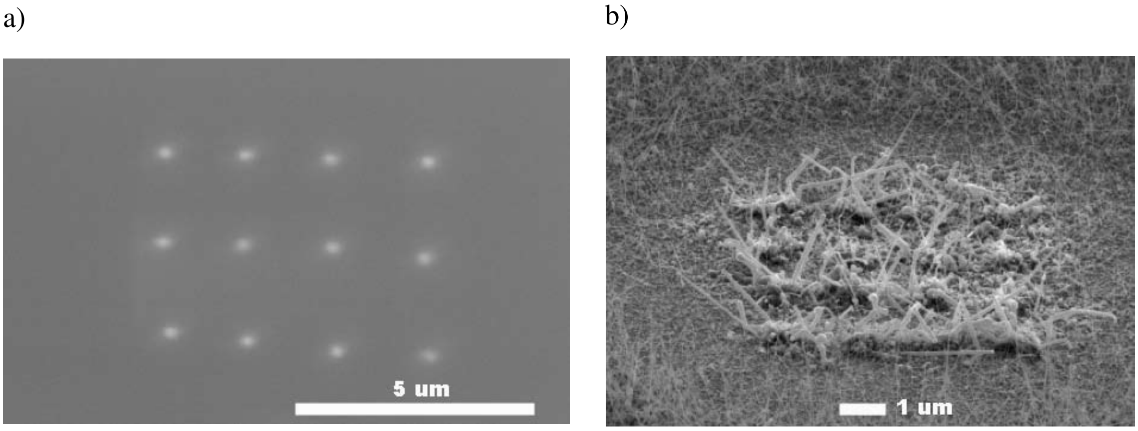

Figure 2.5: *Results obtained by first trials of FEBID deposition on a Si wafer (a) and subsequent CVD growth (b) without the FIB-milling step nor the use of a sacrificial layer. The NW grow also outside the patterned region, with no control of the wire position. No control either is achieved on the nanowire diameter.*

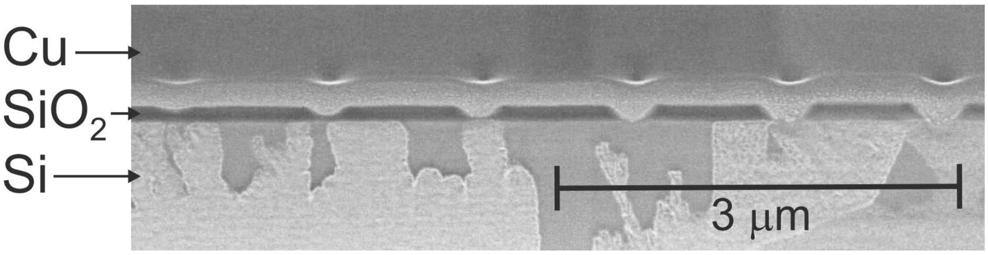

Figure 2.6: *Cross section SEM image of a patterned sacrificial layer on a silicon wafer. Copper has been deposited on the top of the sacrificial layer prior to cross section preparation for preserving the hole features. The cross section has been prepared by FIB. In this case the holes had different depth and the sacrificial layer was 175 nm thick. The conic shape of the holes is due to redeposition effects. From [Ler10b]*

the gold deposits on silicon and not on silicon oxide. This is of fundamental importance for two reasons: (i) in the case the gold lies on the SiO_2, it would be etched away with the sacrificial layer and no gold-catalyzed growth of nanowires would be possible anymore; (ii) if the gold lies on the silicon wafer, the wires might grow epitaxially. The thickness of the sacrificial layer and the depth of the holes has been measured by cross-section SEM (Fig. 2.6). It has been found out that the oxide layer has to be thick enough to protect the underlying silicon but it should not be too thick in order to avoid difficulties and inhomogeneities in the FIB milling (for instance cause by redeposition effects) and in the removal step. In fact, a prolonged HF etch might result in damage to the gold array. A thickness of 50 nm gave the best results.

The FIB-milling of the holes and the gold deposition inside them is shown in Figure 2.7.

Other advantages characterize the sacrificial layer. For instance, the holes can be positioned

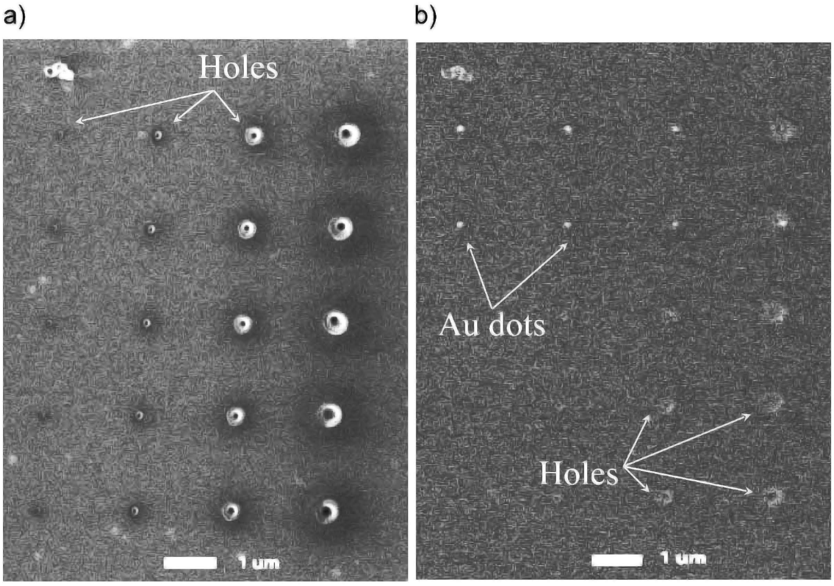

Figure 2.7: *SEM images of the same sample:* ***a)*** *after FIB milling of the hole pattern;* ***b)*** *after gold deposition within the FIB-milled holes. In this sample the hole diameter is constant in each column but changes along each row. In b) the gold has been deposited only in the first two rows.*

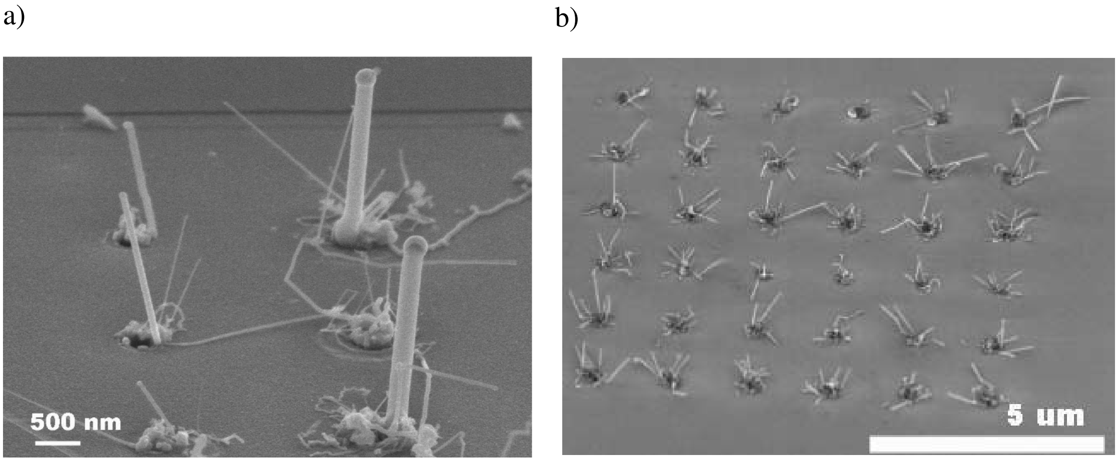

Figure 2.8: ***a):*** *60°-tilted SEM images of one of the first samples processed with the FIB/FEBID/CVD method. The holes have all the same depth, but the columns are characterized by different hole diameters, which influence the diameter of the grown Si nanowire, which are of approximately the same value.* ***b):*** *45°-tilted SEM image of a sample where the deposited amount of gold was not enough for agglomerating to a unique gold droplet and consequently catalyzing singles nanowires with a one-to-one correspondence with the patterned hole. Therefore, more gold droplets form during the annealing inside each hole and each gold dot catalyzes a NW. Nevertheless, the pattern is maintained, as the selectivity is given by the FIB/FEBID/CVD process.*

in any shape, thanks to the flexibility of the FIB milling. Moreover, the hole diameter determines the diameter of the deposited gold, and consequently of the grown nanowire. This can be seen in Figure 2.8a. The columns are characterized by different hole diameters, which is reflected in the diameters of the grown nanowires. Within each column, the diameter is constant. Note the gold droplet at the top end of each nanowires, which suggests that the growth is based on the VLS mechanism. It is worth mentioning that the gold deposited by FEBID is probably more similar to an agglomerate of small gold dots in a carbon matrix [Utk00b] than to a compact particle. Nevertheless, in the CVD process chamber, the temperature rises enough so that at least part of the carbon matrix oxidizes[1]. The so-formed carbon oxide evaporates and the gold becomes more compact, as it will be discussed in the next paragraph. When the eutectic temperature of the Si/Au system is reached, the alloyed droplet liquifies and catalyzes the Si nanowire. Noteworthy, this is possible only if enough gold is supplied. Otherwise, instead of a unique gold droplet, smaller gold clusters form inside the same hole during CVD. Each droplet catalyzes a nanowire, which results in more nanowires growing from the same hole (Fig. 2.8b), losing the one-to-one correspondence achieved with the best parameters.

The transformation of the deposited gold under annealing (300°C in air, 30 min) has been studied by AFM (Fig. 2.9). The Au deposits shrink when annealed: their height decreases to almost half of its as-prepared values, while their width reduces by approximately a factor 4. The reasons for this shrinkage can lie in the evaporation of the carbon content of the precursor, in agreement with the oxidative purification mentioned for the same gold precursor in [Utk08]: a comparable

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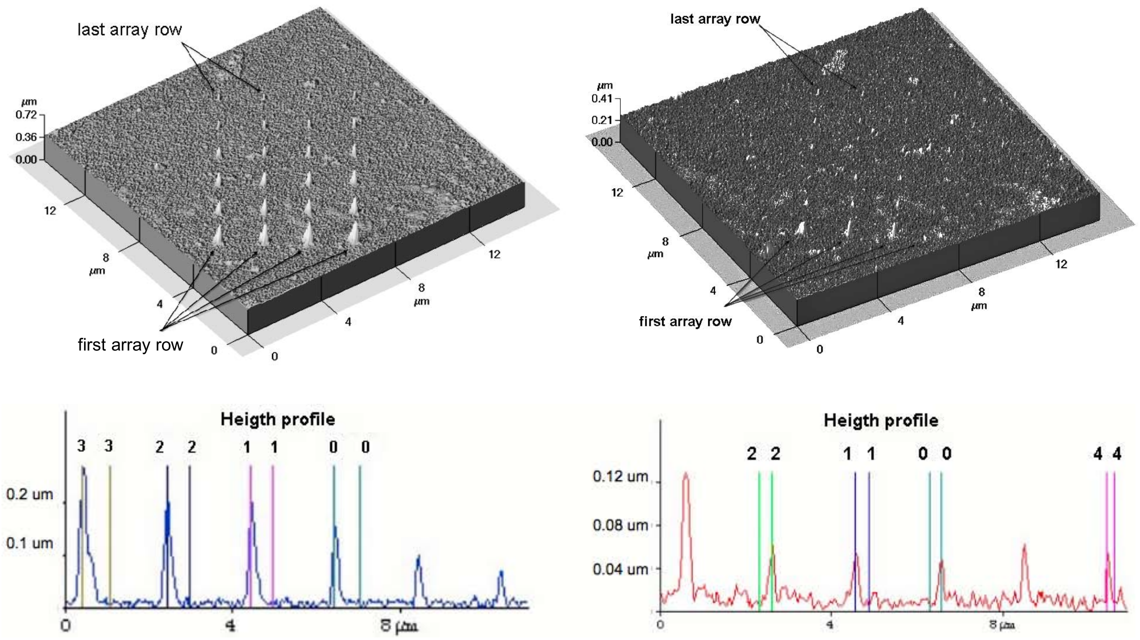
[1] Although the CVD process is performed in high vacuum (10^{-7} mbar), a rough calculation can show that at such pressure a few thousand of oxygen molecules are still present in the process chamber per 100 nm^2. They are enough for oxidizing the carbon in the sample.



a)-before annealing

b)-after annealing

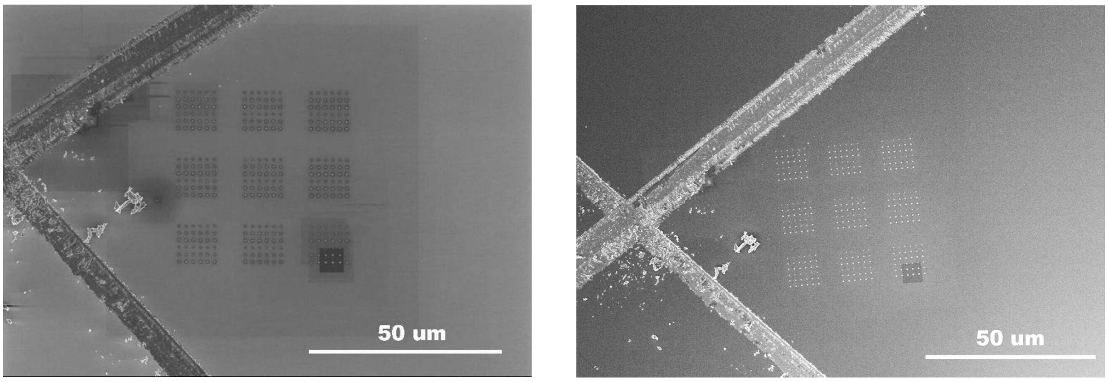
Before annealing	
Line identifier	Width [nm]
3	215
2	210
1	200
0	151

After annealing	
Line identifier	Width [nm]
4	44
2	55
1	48
0	46

Figure 2.9: *AFM scans and AFM line profile of the same sample before (a) and after (b) the annealing step (30 minutes at a temperature of 300°C in air). No FIB-milling has been performed. The dots have been deposited by FEB on the sample surface. Every line has a different deposition time, from 10 s to 200 s. It can be seen that the deposits, in particular the smaller ones, are detectable with difficulties after the annealing. The line scans have been performed along a column of dots. Note that the y-scale is different in the two scans, meaning that the annealed gold deposits are roughly half as high as the as-prepared ones. In both scans, the vertical lines identified by a number measure the width of the deposited gold, whose values are reported in the two corresponding tables. From the comparison (0-0, 1-1, 2-2), it results that by annealing the width reduces by approximately a factor three or four.*

annealing step resulted in a volume decrease for the removal of the carbon by oxidation. The diffusion of gold into the substrate as well as gold evaporation (see next chapter) are negligible at the annealing conditions of this sample.

While excellent growth can be achieved for some of the dots, namely the ones with bigger diameters, growth is rarely observed for smaller holes. This can be due to the CVD process conditions, but different Ar and SiH_4 ratio and various temperatures have been tested without achieving significant progress. Therefore, the cause of the problem must lie in the sample. Possible factors are the presence of residual oxide or, more probably, of organic contaminants left by the gas precursor on the sample surface or by the electron beam when scanning. In fact, a carbon layer could be seen in some samples after the FIB/FEBID process in correspondence of the patterned


a)-before plasma etch

b)-after plasma etch

Figure 2.10: *SEM images of the same sample patterned by the FIB/FEB process before (a) and after (b) the oxygen plasma cleaning. The darker regions in (a) represent carbon layers deposited during the processing, also simply while scanning the sample surface for acquiring an image. Almost no dark region is detected after the plasma etch step.*

region (see Fig. 2.10a). These organic impurities, although uniformly distributed on the whole array, might affect more significantly smaller gold deposits, on which they are present in higher percent, inversely proportional to their size. In order to clean the sample prior to CVD processing, different chemical etch recipes (RCA, HNO_3, Piranha) have been tested, yet without success, presumably because either the carbon layer was not removed or the gold was removed together with the layer. The solution has been found with an oxygen plasma cleaning. The plasma does neither affect the pattern, nor the deposited gold (Fig. 2.10b). Its only possible consequence might be a thicker oxide layer, which, however, can be removed just prior to CVD processing. Alternatively, some reports [Jen10] show that carbon does not affect the VLS growth when the nanowire synthesis is performed in He instead than in Ar. Also this possibility has been tested and the nanowires look similar to the ones grown in Ar after plasma cleaning. This last procedure has been preferred to the use of He because it results equally effective and much cheaper. The resulting wires are shown in Figure 2.11.

Interestingly enough, the nanowire orientation does not seem to depend on the substrate orientation. A possible explanation is given by the silicon on which the gold is deposited inside the hole. The superficial layer of the wafer is no more crystalline because of the amorphization caused by the FIB milling. When forming the holes in the sacrificial layer reaching the silicon surface, in fact, the Ga^+ ions not only remove some material, but also enter the surrounding silicon, which becomes amorphous [Utk08]. The thickness of this amorphous layer could not be determined, as a cross-section preparation would change its characteristics. Nevertheless, it can be estimated from Fig. 2.1a to be approximately 20 nm, which is enough for preventing epitaxial growth. It has been tested whether it is possible to remove the amorphous silicon layer prior to gold deposition without affecting the overall process, using a 1 HF : 3 HNO_3 solution. No epitaxy has been observed in these first experiments. Future work could investigate an optimal etching recipe for the complete removal of the amorphized silicon, also depending on the hole depth and diameter. Alternatively, the FIB milling might be substituted by FEB-induced etching, which would not cause amorphization of the target, still allowing the formation of patterned holes. Despite of this, it has

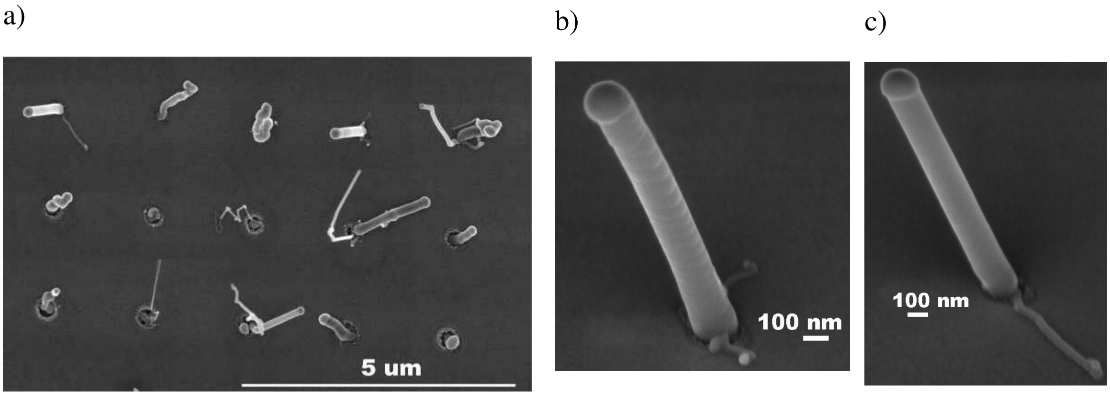


Figure 2.11: *SEM images of the grown nanowires.* ***a)****, top-view: array of wires patterned by FIB/FEBID and synthesized after plasma etch. Some wires are perpendicular to the viewing direction. Most wires are straight and monocrystalline. The growth is highly selective: the correspondence between the wires and the holes is very close to a one-to-one ratio, contrarily to Fig. 2.8b.* ***b)****, 45°-tilted view: single nanowire. The rippled sidewalls might be due to facetting.* ***c)****, 45°-tilted view: single nanowire, presumably monocrystalline.*

to be mentioned that the orientation of the wire is always within 50° with respect to the surface normal, possibly as a result of a guiding effect caused by the hole depth on the nanowire during its growth.

The crystalline quality of the grown nanowires has been checked by EBSD [Ler10b] and STEM measurements, transferring single wires on a tungsten tip using a nanomanipulator and FEBID. Most analyzed nanowires resulted to be monocrystalline (Fig. 2.12). In addition, EDX

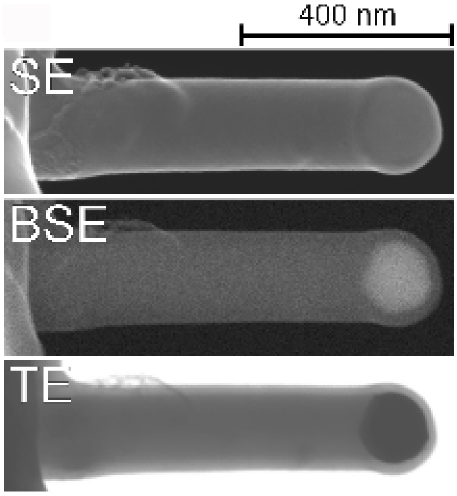


Figure 2.12: *Images taken in a scanning electron microscope with different detectors: secondary electrons (SE), back-scattered secondary electrons (BSE) and transmitted electrons (TE or STEM mode). In the SE scan it is possible to distinguish the nanowire from the substrate surface and some organic residuals left from the sample preparation. The BSE image highlights the location of the gold droplet at the end of the nanowire, probably surrounded by silicon oxide due to air exposure or by carbon deposited while scanning. The TE picture shows that the nanowire is monocrystalline, as it is transparent for a 30 kV electron beam. From [Ler10b].*

analysis on several nanowires have been performed for mapping the gold content. The EDX spectra show that most of the gold is located on top of the NWs, as expected.

2.5 In-place growth on AFM tip

Once the FIB/FEBID/CVD method had been successfully tested on a silicon wafer substrate, this procedure has been used for the in-place growth of Si NWs on an AFM tip keeping the same process parameters. The AFM tip has been only mechanically fixed to the sample holder for the CVD process, avoiding the use of high-vacuum carbon tape or silver paste, which might release organic residuals and prevent the growth of the nanowire. The resulting nanowire, presumably monocrystalline, is shown in Fig. 2.13, where high selectivity on the wire position could be achieved. Similar results had been obtained by removing a single nanowire from a planar substrate and, by nanomanipulation, attaching it on the tip of an AFM cantilever using carbon deposition [Bec08]. In that case, a tedious processing by nanomanipulation is needed in addition to the CVD process. This also includes the risk of damaging the nanowire or the AFM tip. Moreover, such method could not be implemented on an industrial scale, contrarily to the quick FIB/FEBID/CVD procedure.

2.6 Conclusions

A method for the in-place selective growth of Au-catalyzed Si nanowires on wafer and on AFM tip has been demonstrated. The method combines top-down approaches such as FIB milling and FEBID with a bottom-up synthesis process like the VLS growth mechanism by CVD processing: the gold deposited by FEBID in FIB-milled holes catalyzes the Si NWs by VLS mechanism. This combination allows to achieve patterned nanowires on pre-selected locations with freedom in the shape of the array and no damage on neighboring regions. Moreover, this quick procedure can be implemented on large scale, avoiding tedious alignment tasks characteristic of other patterning techniques (e.g. lithography) or risky transfers of the nanowires on the desired location by nanomanipulation.

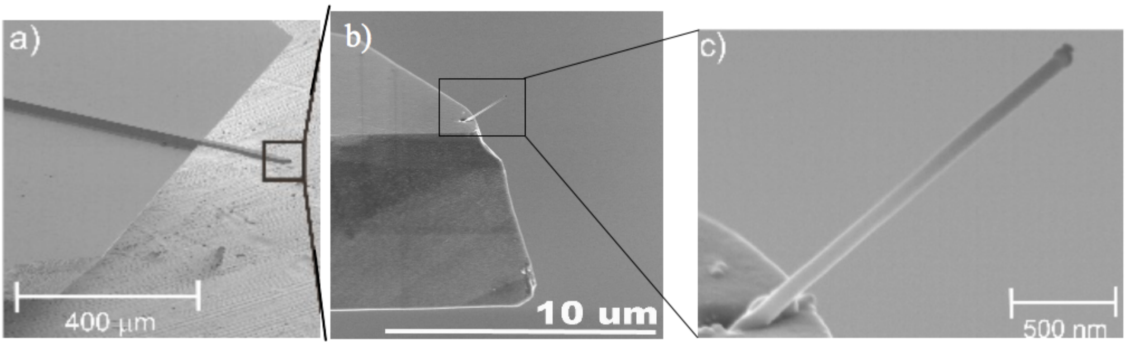


Figure 2.13: *SEM images of an AFM tip where a single NW has been grown.* ***a)****: overview of the AFM tip.* ***b)****: the single nanowire on the tip. Note that no other nanowires are present in the neighbor regions, e.g., the growth results to be highly selective.* ***c)****: the high-quality Si NW. Its straightness and surface smoothness suggest monocrystallinity. The gold droplet is visible on the top. From [Ler10b].*

The so-grown monocrystalline nanowires differ from the ones synthesized in-place by other methods (e.g. FEBID) for their high quality, smooth surface, low carbon content and resistance to annealing. A one-to-one correspondence between the nanowires and the holes has been obtained. Control of the NW diameter has been achieved but not yet of the NW orientation, although the NW growth direction is limited to a range of 50° with respect to the sample surface normal. The absence of epitaxial growth is probably due to the amorphous silicon layer formed during FIB milling. Future work will include the testing of selective etching recipes or the substitution of the FIB milling by a FEB-induced etching.

The method has been optimized characterizing the effect of annealing on the used gold precursor by AFM and testing different procedures for the sample cleaning. The best parameters have been found regarding the amount of deposited gold, the hole depth, the sacrificial layer thickness and the etching duration time. In addition to this, the synthesized nanowires have been characterized by SEM, STEM, and EBSD.

The combined FIB/FEBID/CVD procedure can be applied to any other material for which a gas precursor is available and on any type of substrate. Moreover, the CVD can be substituted by other bottom-up techniques.

Chapter 3

Epitaxial Si nanowires patterned by nanosphere lithography (NSL)

This chapter presents a procedure for synthesizing patterned gold-catalyzed Si NWs using nanosphere lithography (NSL) combined with gold sputtering, annealing in Ar and chemical vapor deposition (CVD) with silane. After an introduction which summarizes the state of the art in this matter, the experimental parameters are given. In the following section, the influence of the annealing temperature on the NSL-patterned Au arrays is discussed. Subsequently, it is explained how the arrays are used as a catalyst for the epitaxial growth of silicon nanowires. Finally, the results are summarized.

The content of this chapter has been partially published by the author [Bec10, Ler10a] in collaboration with the group of Dr. L. Philippe / Dr. J. Michler at the EMPA in Thun, and in particular with Dr. M. Bechelany.

3.1 Introduction

In the past years various processing methods and parameters have been tested to achieve high-quality Si nanowires (Si NWs). Nevertheless, for most applications (see for instance [The06, McA07, Gao07]) the quality is as important as the precise control of NW position, diameter, and length. While the NW length can be easily controlled by the process duration, nanowires with a predictable position and diameter are more difficult to achieve. Consider the VLS mechanism, described in Sect. 2.2.3, which is based on droplets of a catalyst. As the droplets determine the nanowire diameter and position, a NW array with a narrow NW diameter distribution can be obtained if the metal particles also possess a sharp size distribution and form an ordered pattern. In other words, it is necessary to pre-pattern the catalyst material.

There are different methods for patterning a metal, for example using an anodized aluminum oxide as a mask [Cro00, Fan06] or electron beam lithography. Alternative lithography procedures have been suggested for substituting the expensive e-beam lithography enabling similar resolution and maintaining some freedom in the feature shape and size [Sot03].

One alternative is nanosphere lithography (NSL), which allows to pattern a material on a substrate in an inexpensive, easy, flexible and quick way also on large scale. A further advantage is that NSL requires no special equipment. First reports of patterns in the sub-micrometer range obtained by using a mask of latex or polysterene spheres date back to the beginning of the '80s [Fis81, Dec82]. The interest for NSL significantly increased in the last years and many publications have characterized the optimal parameters for achieving good nanosphere masks [Hul95, Hul99]. Despite of these reports, the variety of procedures and technical equipment which can be used is far from being fully explored. This is also due to the wide range of suitable material and process parameters. The choice of the nanosphere composition and the deposited material, for instance, influences the shape of the metal pattern [Hul95]. Thermal evaporation results in triangular-shaped dots [Hay01], while sputtering leads to a honeycomb mask [Bec10].

Potential applications of NSL include optics [Hay01], carbon nanotube synthesis [Par05], plasmonics and/or sensing [Hic07, Ank08, Nag09], bio- and electrochemistry [Zha05, Val07]. Because of their well-defined geometrical properties, the patterns obtained by NSL have been studied for investigating the size dependence of material properties [Vol96]. Patterned metal dots have been used for the synthesis of nanowires, e.g. as an etching mask ([Kuo03, Che06] for Si nanopillars). In addition to this, NSL-patterned dots as catalysts have been reported for both silicon and other materials [Fan06, Kay06, Lin08]. The nanowires synthesized in this work differ from the already reported results in the deposition method of the gold (here, sputtering) and in the patterning method, which is a combination of nanosphere lithography and annealing. Both the deposition method and the annealing step influence the resulting pattern [Hul95, Lin08, Bec09, Bec10]. The work of Lindner et al. [Lin08] is particularly significant, as they patterned the metal catalyst dots by nanosphere lithography and synthesized silicon nanowires arrays by Chemical Vapor Deposition (CVD) with silane. However, they deposited the gold by electron beam evaporation (not sputtering) and annealed during the growth process, achieving limited control of the gold droplet size. In fact, Lindner affirms that the gold dots prior to CVD are smaller than the gold caps at the top of the grown nanowire. He suggests a coalescence mechanism which takes place on the sample surface during the CVD process. The understanding and control of the coalescence mechanism during the annealing step *prior* to the CVD process [Bec10] allows a good control of the size of the gold catalyst droplets. Thus, the synthesis of Si NWs with a predictable diameter is possible, as demonstrated in this chapter.

The nanowires synthesized in this work also differ from many reported results in the use of silane as a precursor gas for the CVD process. Kayes et al [Kay06] reported the use of silane on patterned substrates, but they used e-beam lithography for arraying the metal and an evaporation system for the gold deposition. It is additionally worth mentioning that no ultra-high vacuum equipment is used for our process, sometimes needed for preventing the formation of an oxide layer at the interface between the gold droplet and the silicon substrate [Fan06], as the oxide could prevent the wires to grow epitaxially. Finally, the CVD-performed growth process is substantially different from the one performed by Molecular Beam Epitaxy [Fuh05, Zak06]: the MBE is characterized by a uniform flux of Si atoms (not a gas precursor) which are absorbed in the same way by the Au droplets (no more acting as a catalyst cracking the precursor molecule) and by the substrate.

The ordered arrays of epitaxial Si NWs patterned by NSL combined with sputtered gold, annealing, and CVD with silane represent an improvement over other results in the use of inexpensive synthesis techniques and a predictable size. In addition to this, the grown nanowires are of high crystalline quality and can also be grown on cheap substrates, e.g. glass.

3.2 Process overview and experimental parameters

A schematic representation of the overall process combining nanosphere lithography, gold deposition, and CVD is shown in Figure 3.1. The process can be performed, with minor differences, on Si wafers as well as on glass substrates. With minor changes it is possibly applicable to other types of substrates and even other deposited materials.

Intrinsic (111) Si wafer pieces with a side length of about 15 mm are cleaned in acetone and ethanol to remove organic residuals and dipped in 2% HF for two minutes for etching the native oxide. Subsequently, these samples are heated in conventional RCA I cleaning solution (1 NH_4OH 25% : 1 H_2O_2 30% : 1 H_2O at 80°C for 20 minutes). The RCA cleaning step is not only important for the neatness of the sample surface, but also for turning it hydrophilic, which is a necessary condition for the uniform monolayer deposition of the polyspherene spheres (PS) by spin-coating. The used PS are a monodisperse suspension in water by Polysciences Inc with a diameter of 1 μm. Experiments using PS with a diameter of 200 nm have been performed and gave the same results after adjusting the spin-coating parameters. The best results with 1 μm spheres are achieved by a two-step spin-coating: 300 rpm for 10 seconds and 500 rpm for 30 seconds. Depending on the sample size, one or two drops of PS suspension are used. With these parameters, high areas of the sample surface are covered by a monolayer of PS (Fig. 3.2). The samples need to be dried in air at room temperature for at least one hour for allowing the PS to arrange themselves forming a closely packed structure due to attractive capillary forces. The two-dimensional ordered PS lattice is then used as a mask for the Au deposition. The sputtering is performed using an Edward's Sputter Coater S150B at a discharge current of 25 mA, a voltage of 800 V, a temperature of 20°C, and a pressure of 0.2 Torr. The typical sputtering time is 14 minutes. The deposited gold layer is about 200 nm thick. Afterwards, the samples are sonicated in toluene, ethanol, and finally distilled water for 5 minutes each in order to remove the PS mask. Subsequently, the samples are annealed in Ar atmosphere for one or two hours at different temperatures (400, 600, 800, 1000 and 1200°C

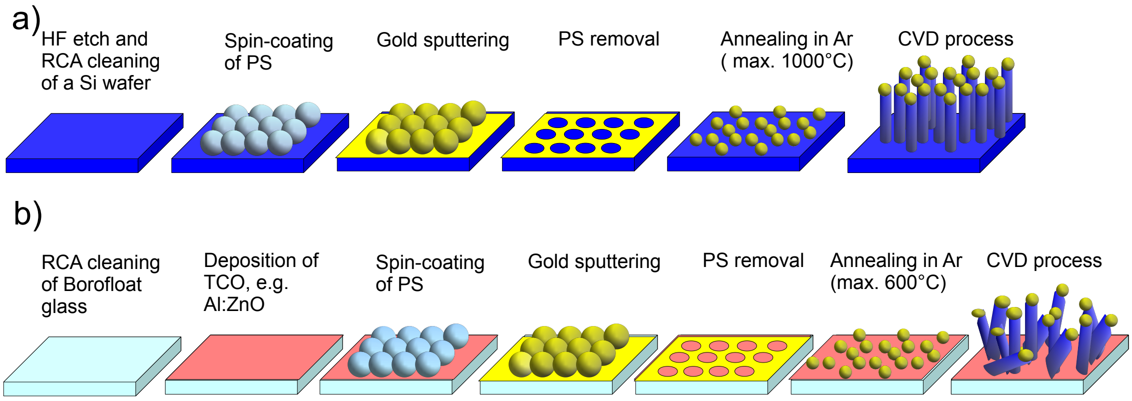


Figure 3.1: *Schematic representation of the process which combines nanosphere lithography, gold sputtering, annealing in Ar and Chemical Vapor Deposition. The procedure is shown for a* (111) *Si wafer substrate (a) and with minor differences for a glass substrate (b). The glass substrate might be covered by a deposited layer of thin conductive oxide (TCO). Note that the nanowires grown on glass can not be epitaxial. Nevertheless, they still present a sharp diameter and length distributions, as grown by dots with the same diameter.*

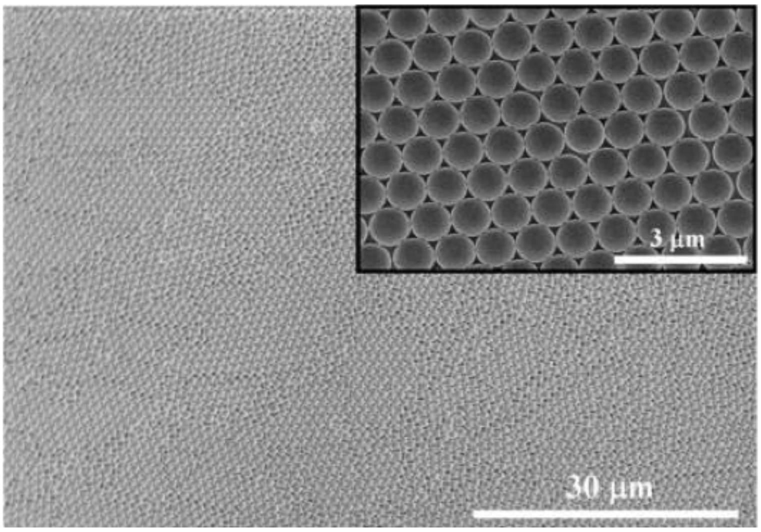


Figure 3.2: *SEM picture of the polysterene sphere mask self-arranged after drying in air at room temperature. The spin-coating conditions have been optimized in order to achieve uniform coverage of large areas of the sample surface by one monolayer of PS. In the inset, the same sample is shown with higher magnification. Reproduced with permission from [Bec10].*

at a heating rate of 10°C/min). Before unloading the samples, the tube furnace is cooled down to room temperature (RT). In order to study the mechanisms which led to the formation of the gold pattern, the samples have been characterized with a Scanning Electron Microscope (SEM; Hitachi S-4200, S-4800 at the EMPA in Thun and LYRA - Tescan at the IPHT, Jena), an Atomic Force Microscopy (AFM; TopoMetrix SPMLab version 4.0, EMPA), and by Glow Discharge Optical Emission Spectroscopy (GDOES; JY RF-5000, EMPA). The AFM data have been analyzed using the software WSxM by Nanotec. The samples analyzed by GDOES have been etched in KI/I_2 (1:10 in H_2O) for 5 minutes prior to the measurement, in order to achieve a planar surface for avoiding GDOES artifacts. The GDOES measurements have been performed with a 4 mm anode, at an Ar pressure of 650 Pa, and a power of 10 W. The measurement duration time is 120 seconds and 100 points are integrated per second. The raw data of the GDOES intensity as a function of the measuring time have been transformed to intensity as a function of sample depth using a plain Si sample calibrated by a laser-profilometer.

After the annealing step, samples processed at a temperature higher than 600 °C have been used for nanowire growth. Before loading them into the CVD chamber, the samples needed to be etched for 10 minutes in a solution produced by mixing 2 parts of sulfuric acid H_2SO_4 (96%) with one part of hydrogen peroxide H_2O_2 (30%). In this mixture, Caro's acid results from the reaction $H_2O_2 + H_2SO_4 \rightleftharpoons H_2SO_5 + H_2O$. This etch removes residual organic contaminants but oxidizes the sample, which needs therefore a subsequent etch in HF (5%, 1 minute). The sample is then transferred into the CVD system without further delay. The CVD chamber is pumped down to a base pressure of 10^{-7} mbar. The process pressure and nominal temperature are 0.5 mbar and 680°C, respectively. The process pressure is reached with a flow of 5 sccm of Ar and 2 sccm of SiH_4. Typical process duration is 20 minutes. The grown nanowires have been characterized by SEM. Some samples have been further processed for realizing a nanowire-based solar cell, as explained in Chapter 6.

If a glass substrate is used, the changes in the overall process are: (i) the annealing temperature is 600°C, not higher, because of the softening temperature of the glass; (ii) no further sample preparation before the CVD process, i.e. no etching step after the annealing; (iii) slightly different CVD process parameters: 10 sccm Ar, 5 sccm SiH_4, 2 mbar, but same nominal temperature and process time. In addition, the glass might be coated with a thin conductive oxide layer, like indium tin oxide or Al-doped zinc oxide.

3.3 Gold dot arrays by NSL and annealing in Ar

This section analyzes the patterns obtained by combining nanosphere lithography, gold sputtering, and annealing in argon. In particular, the influence of the annealing temperature on the patterns is investigated, also considering the amount of gold which diffuses into the silicon substrate or which evaporates.

During gold sputtering, Au atoms have a high mobility. When they are deposited through the PS mask, they may cover all the sample surface except the portions of the Si surface which are in direct contact with the PS spheres. Therefore, when the PS mask is removed in toluene, a honeycomb pattern is obtained (Fig. 3.3a). The honeycomb pattern, characterized by AFM, shows that the thickness of the sputtered layer is not uniform on the covered surface. This is presumably due to shadowing effects of the PS mask.

The honeycomb pattern is transformed in a well-defined array of gold dots by annealing at different temperatures. The characteristics of the obtained gold dot pattern critically depend on the annealing temperature, which determines the influence of the four pattern-shaping concomitant processes: coalescence, Ostwald ripening, gold evaporation, and diffusion of gold into the substrate [Bec10]. These mechanisms are discussed after the description of the experimental results, shown in Fig. 3.3.

The samples annealed at 400°C present big Au nanodots surrounded by smaller Au nanodots (Fig. 3.3b). The number of the smaller satellite nanodots decreases for higher temperatures, eventually disappearing at advantage of the bigger ones. At the same time, also the bigger droplets decrease in area, though increasing their height, as shown from the AFM line scan of Figure 3.4. The area occupied by the gold particles has its minimum at an annealing temperature of about 800°C and does not change for higher temperatures [Bec10]. Nevertheless, the height of the bigger droplets increases further for samples annealed at 1000°C, while the smaller particles rarefy (Fig. 3.3e). These nanodots have a diameter of approximately 100 nm and hemispherical shape. All smaller particles vanish when the annealing time is increased to 2 hours, as shown in Fig. 3.5a and the corresponding dot diameter distribution plotted in Fig. 3.5b. A higher temperature (1200°C), however, leads to a complete disappearing of the gold pattern, caused by either Au evaporation or Au diffusion into the Si substrate.

The Au particles align themselves in a hexagonal Au dot pattern. The regularity of the array has been checked also by its Fourier Transform (Fig. 3.6).

The mechanisms which determine the changes in the gold pattern are coalescence and Ostwald ripening; at higher temperature, gold evaporation and diffusion into the substrate have to be considered as well. Coalescence takes place when two nanoparticles merge to form one bigger nanoparticle, the driving force being the reduction of the total interfacial energy of the system.

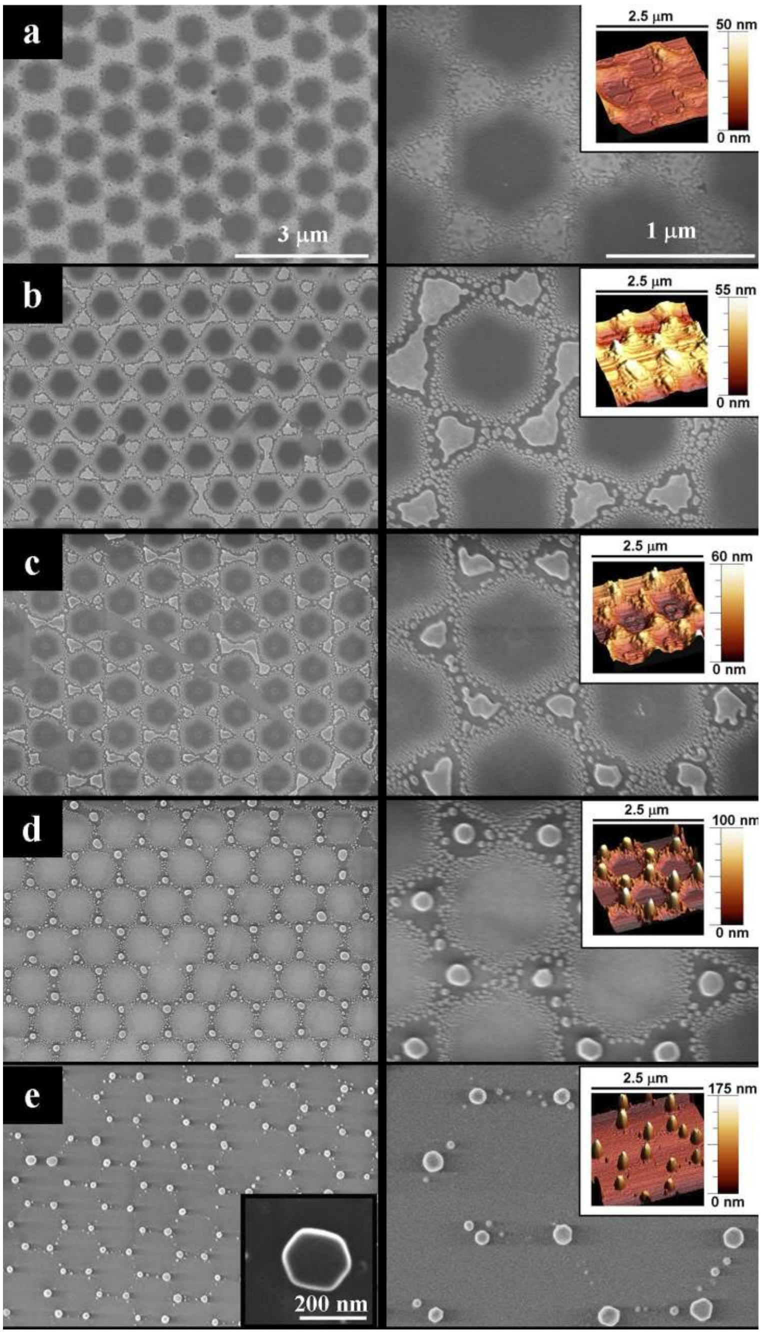


Figure 3.3: *SEM pictures and corresponding AFM images of the gold pattern on a silicon substrate obtained by nanosphere lithography prior to annealing (a) and after annealing for 1 hour in Ar atmosphere at different temperatures: b) 400°C; c) 600°C; d) 800°C; e) 1000°C. The inset in the SEM picture in e) zooms on a single gold dot. Reproduced with permission from [Bec10].*

Therefore, the coalescence mechanism typically leads to a majority of larger particles. In order to coalesce, the particles can migrate on the surface.

The Ostwald ripening mechanism is characterized by the transfer of atoms from one nanoparticle to another without contact between the exchanging nanoparticles. This mechanism is driven by

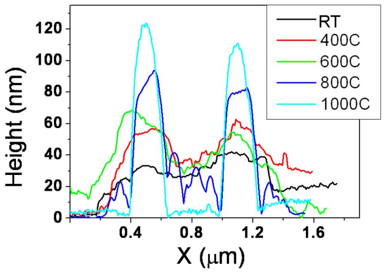


Figure 3.4: *AFM line scan of two dots forming the gold pattern on samples before (RT) or after the annealing in Ar at different temperatures. Reproduced with permission from [Bec10].*

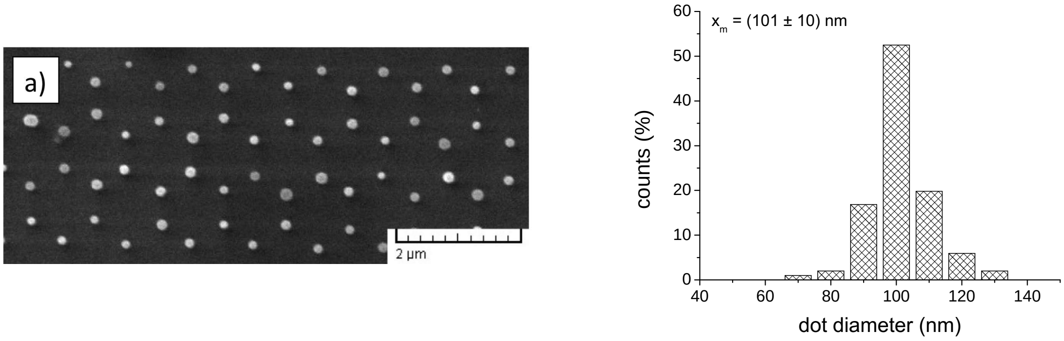


Figure 3.5: ***a)**: SEM picture of a gold dot pattern on silicon obtained after a 2-hours annealing in Ar at 1000°C. **b)**: experimental counts of the dot diameter size in a). The error of the mean value* x_m *is the standard deviation. Reprinted with permission from [Ler10a].*

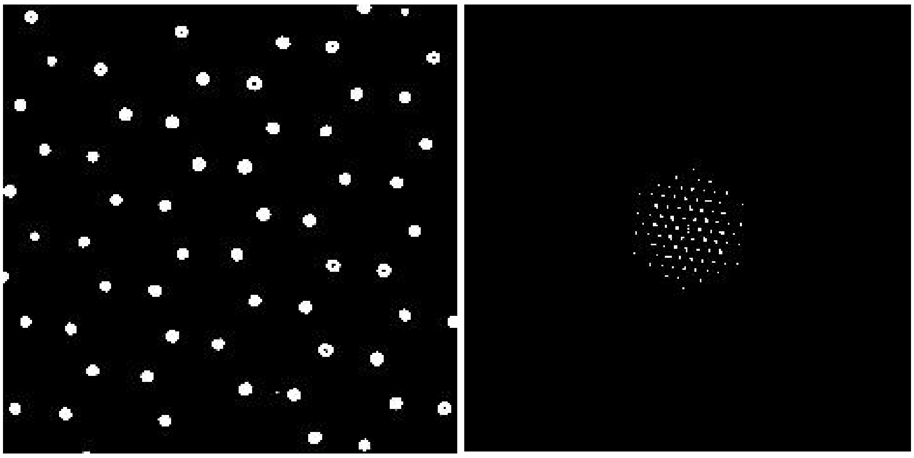

a) b)

Figure 3.6: ***a)**: SEM picture of a pattern obtained after annealing the sample for 2 hours at 1000°C. The image contrast has been selected to 100% for obtaining a black-white image, prerequisite for further image Fourier Transform (FT) processing. **b)**: Image FT of the black-white picture on the left. The FT has been obtained using the program ImageJ. The scale in a) is the same as in Fig. 3.5a, but it has been removed for calculating the FT.*

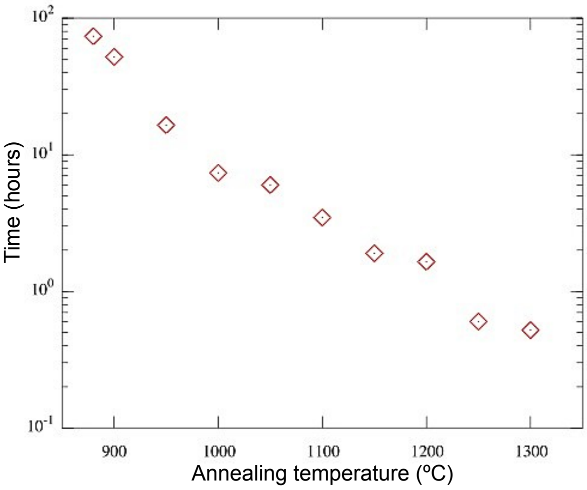


Figure 3.7: *Plot of the time needed for a complete evaporation of a gold layer at different temperatures. The vapor pressure values, which depend on temperature, have been taken from www.veeco.com . The area of the layer is 0.73 cm^2, obtained subtracting from the area covered by the PS mask (circa 1 cm^2) the area covered by the PS spheres.*

the reduction of surface energy. The theoretical distribution which describes Ostwald ripening has been first suggested by Lifshitz et al. and presents its maximum for bigger particles. Nevertheless, recent theories have proposed a more symmetrical distribution [Bal02].

As reported by Plante et al. [Pla06], Au islands can self-assemble driven by different and competing mechanisms. Both Ostwald ripening and coalescence play a role in transforming the honeycomb pattern into a dot array.

The other two mentioned mechanisms, namely gold evaporation and gold diffusion into the substrate, influence the pattern formation only at higher temperatures. Considering gold evaporation, the temperature influences the gold vapor pressures P. Using tabulated values of P, the time t_{ev} needed for the complete evaporation of the deposited gold layer at each annealing temperature could be calculated, considering bulk gold and neglecting size-dependent effects:

$$t_{ev} = \frac{1}{\sqrt{\frac{P}{d_{Au} \cdot A}}} \tag{3.1}$$

where d_{Au} is the gold density and A the layer surface area, which has been estimated subtracting from the approximate area covered by the PS mask (1 cm^2) the area covered by the spheres. The results are plotted in Fig. 3.7. It is clear that many hours are needed before a gold layer completely evaporates at a temperature of 850°C, while circa 30 minutes are sufficient at 1300°C. Regarding our samples annealed at 1200°C, the evaporation of gold definitely plays a significant role, but not all the gold could evaporate in the considered annealing time. At such temperature, part of the gold diffuses into the substrate, even through the Si oxide layer [Sch74] which is present on the sample surface after the NSL step. The diffusion of gold into the substrate has been checked by Glow Discharge Optical Emission Spectroscopy (GDOES) measurements.

The GDOES results reported in Figure 3.8 show the location of gold and oxygen within the

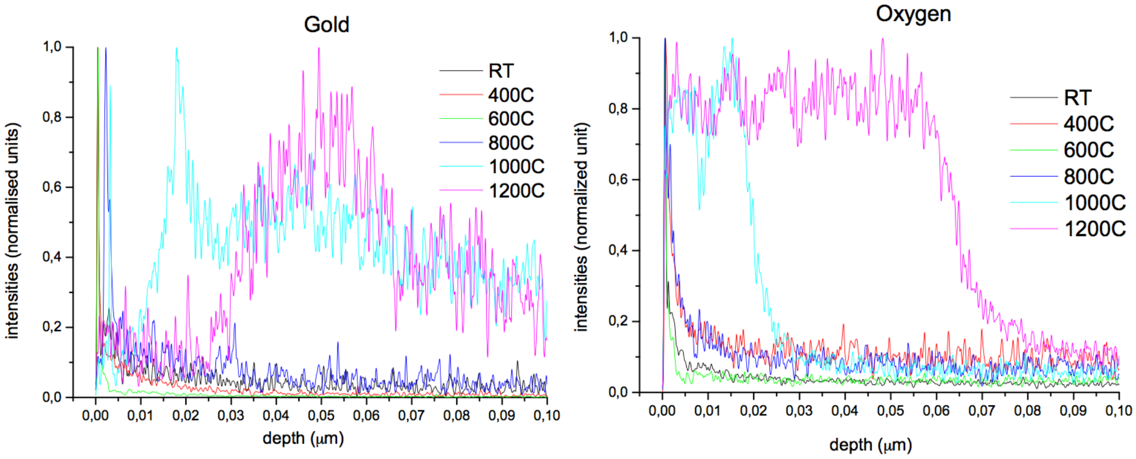


Figure 3.8: *GDOES measurements of the gold (left) and oxygen (right) diffusion in various silicon samples. "RT" indicates the samples measured prior to annealing. The other samples have been measured after annealing in Ar at different temperatures (400, 600, 800, 1000 and 1200°C). The spectra have been normalized to their maximum and shifted to a common depth zero value.*

silicon in samples not annealed or annealed at different temperatures. For comparison, the measurements have been normalized to the maximum intensity value for each sample and have been aligned with respect to the depth-axis. In the shown plots the sample surface corresponds to a depth equal to zero. Both the gold and oxygen diffusion into the silicon substrate clearly took place for annealing temperatures over 1000°C.

The depth profiles at the different temperatures are reported in Figure 3.9, where the GDOES results are shown for the diffusion of Si, O, and Au for the 7 considered temperatures and the non-annealed sample. The graphs have been normalized to the maximum like the previous ones, but have not been shifted. The GDOES spectra give a qualitative analysis of the depth profile, but can not offer a quantitative result, as the GDOES measurement technique is a comparative method.

The as-prepared sample, prior to annealing, shows a very thin Si oxide layer on the Si substrate and all the gold is located on the sample surface. Annealing at 400°C and 600°C does not significantly change the measurements: only the oxide thickness slightly increases (Fig. 3.9b and c). After the annealing at 800°C the gold moved from the surface (Fig. 3.9d). It is interesting to note that the gold is located below the silicon oxide, meaning that it diffused through the oxide reaching the silicon substrate. The same sequence of intensity peaks (from the surface: oxygen, then gold) can be observed in a sample annealed at 1000°C, where gold begins to diffuse also much deeper into the silicon substrate, but is still present near the sample surface (see inset of figure 3.9e). The oxide layer, on the contrary, is confined to the first 10-20 nm from the sample surface; and only in samples annealed at higher annealing temperature (Fig. 3.9f) a thicker oxide layer grew. In this last case gold completely disappeared from the sample surface.

It is not fully understood why oxygen is present in a significant amount in these samples, in particular for higher annealing temperatures, as the oven was filled with Ar. It is likely that the oven had an oxygen leak. This affected more the higher-temperature annealing steps, since the samples remained inside the oven for longer time: although the heating rate and the annealing duration was the same for all temperatures, the cooling time was longer for higher temperatures.

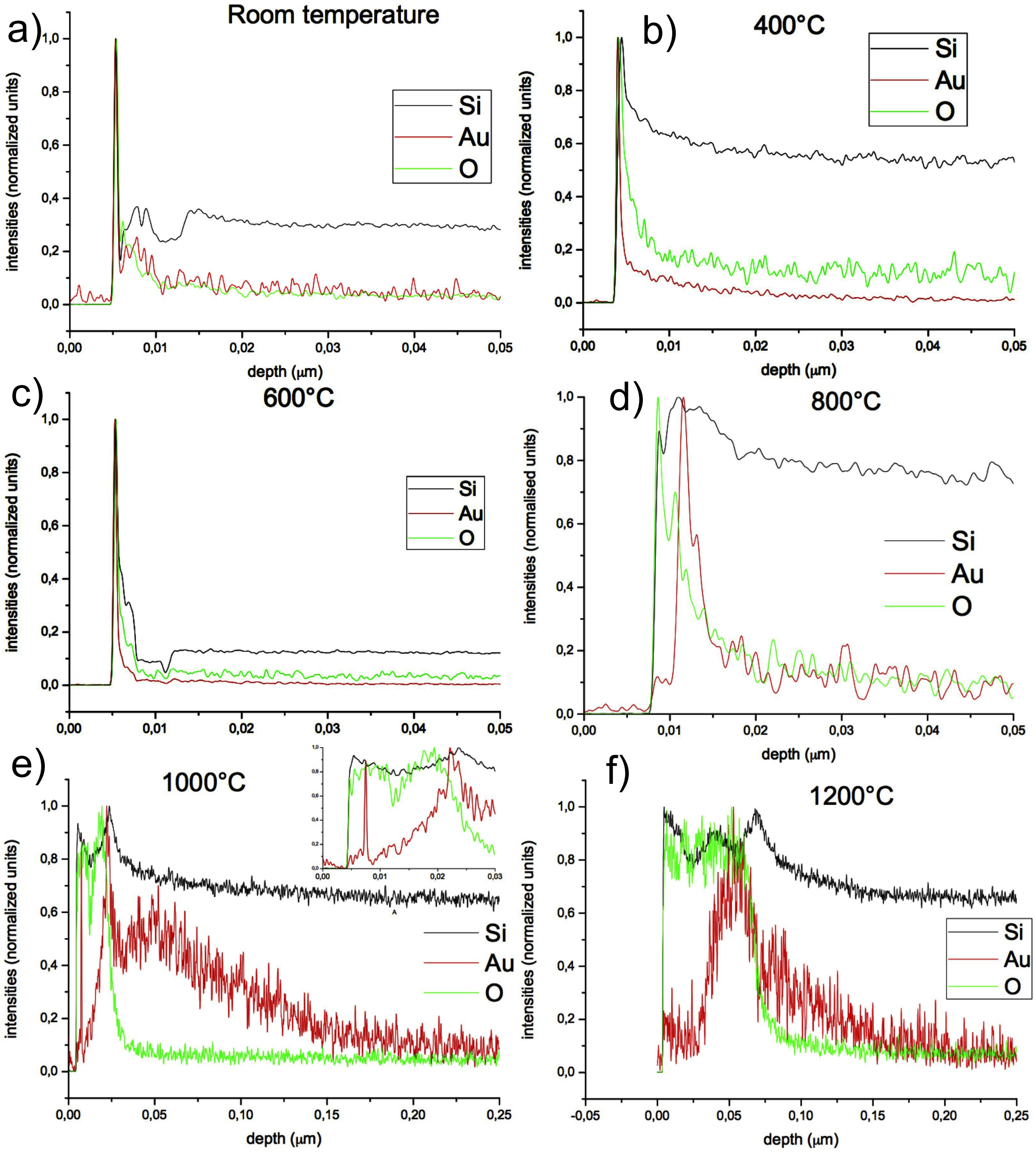


Figure 3.9: *GDOES-measured spectra of patterned samples prior to (RT) and after annealing at the indicated temperature. The samples have been etched in a KI/I_2 solution before measurement. Differences in the intensity values far from the sample surface for the same material in the various spectra are due to the normalization to the maximum value, which can be influenced by the noise, the position of the sample during measurement and some roughness on the sample surface. As GDOES is a comparative and not a quantitative method, the resulting values can be compared within one spectra, but not among different graphs. Note that the depth axis is the same for the spectra a)-d) and then again for the spectra e)-f). The inset of plot e) shows a close-up of the surface region demonstrating that part of the gold did not deeply diffuse into the silicon, but is still located near the sample surface.*

These results show that gold could reach the silicon substrate below the oxide layer. This is crucial for achieving epitaxial growth of silicon nanowires catalyzed by these gold dots, as shown in the next section.

In conclusion, these four mechanisms (coalescence, Ostwald ripening, gold evaporation, and

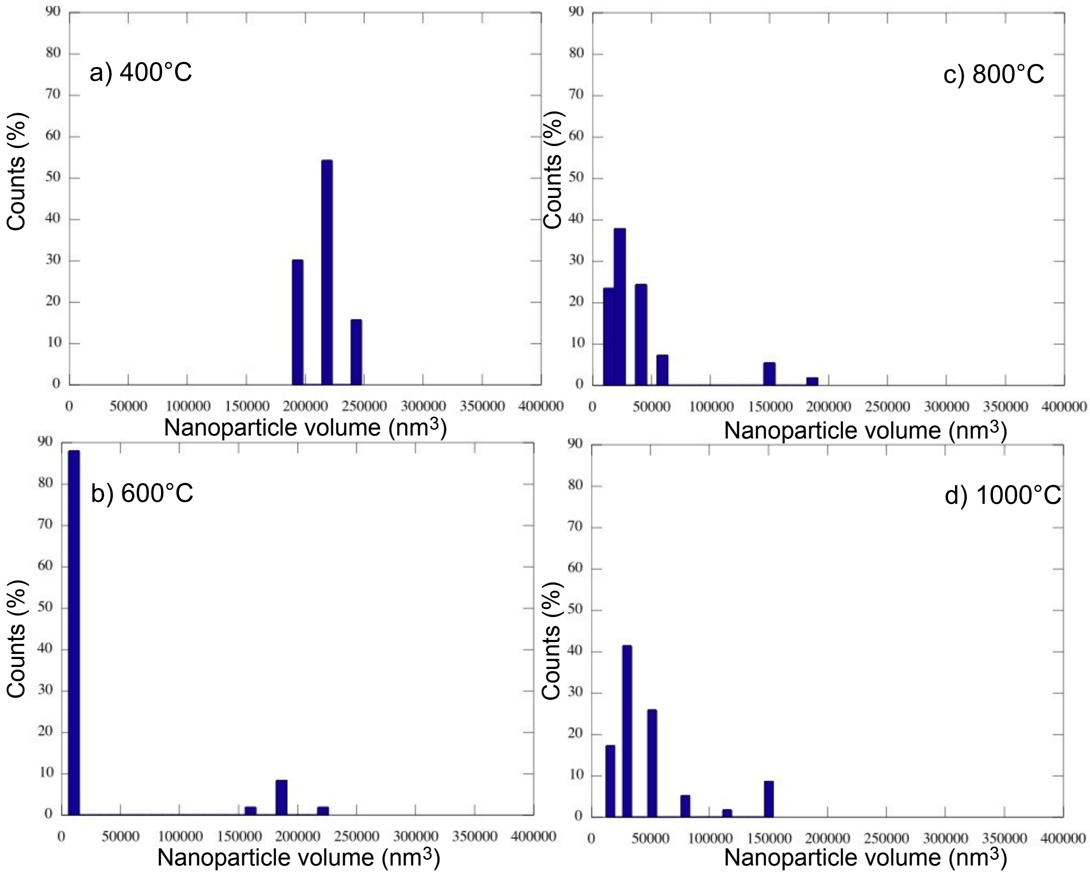


Figure 3.10: *Size distribution of the gold particles achieved at different annealing temperatures: a), 400°C; b), 600°C; c), 800°C; and d) 1000°C. The very tiny particles (diameter $<$ 30 nm) around the big droplets in samples annealed at 400°C are not considered, as difficult to measure. Both axes have the same scale in each plot.*

gold diffusion into the substrate) determine the appearance of the patterns at different temperatures. In order to describe the patterns more quantitatively, the size distribution for the different annealing temperatures is plotted in Fig. 3.10. We should now consider separately the small dots (with a volume $< 1.5 \cdot 10^5$ nm^3) and the big droplets (with a volume $> 1.5 \cdot 10^5$ nm^3). Small droplets can be measured only starting from 600°C, when the gold layer around the big droplets (Fig. 3.3b) is substituted by tiny particles (Fig. 3.3c), driven by coalescence. At 800°C (Fig. 3.10c) coalescence increases the amount of detectable small droplets, but, at the same time, Ostwald ripening favors the bigger ones of these newly formed particles. This causes the shift of the maximum of the distribution towards a volume of 2.5 $\cdot 10^5$ nm^3. These processes still take place at higher temperature, but the number of smaller droplets is decreased by evaporation and diffusion into the substrate. On the contrary, bigger droplets slightly shrink when annealed. Such decrease is possibly motivated by evaporation and diffusion into the substrate.

3.4 Gold dot arrays as catalysts for patterned epitaxial Si NWs

Although the growth of epitaxial Si NWs has been achieved using all types of substrates, the ones annealed at 1000°C have been preferred because of the narrower dot diameter distribution. The results shown in this chapter have used this type of substrates. The grown nanowires are shown after a summary on the necessary sample preparation prior to the CVD process.

3.4.1 The importance of sample preparation

The preparation of the sample surface is crucial for obtaining not only generic nanowire growth, but epitaxial growth. The sample surface is presumably highly contaminated with organic residuals after the removal of the PS spheres. These residuals affect nanowire growth in two ways: (i) they might contaminate the CVD process chamber causing a worse base pressure and thus negatively influence the overall process; (ii) they might change the chemical surface properties of the catalyst droplets, which might not be able to decompose the silane into silicon and hydrogen, so that no silicon is supplied for forming the nanowires. In addition to this, some silicon oxide might be present between the gold droplet and the silicon interface or around the gold droplet surface (Fig. 3.11a, d). The oxide can influence the growth process, leading to a decrease of the crystalline quality and the wire density on the sample surface, and in some cases preventing wires from growing. For avoiding these problems, different chemical etching combinations have been tested.

A traditional HF etch turned out not to be sufficient, as it does not remove the organic contaminants. Similarly, a second RCA cleaning is inadequate, as it does not etch the oxide, but on the

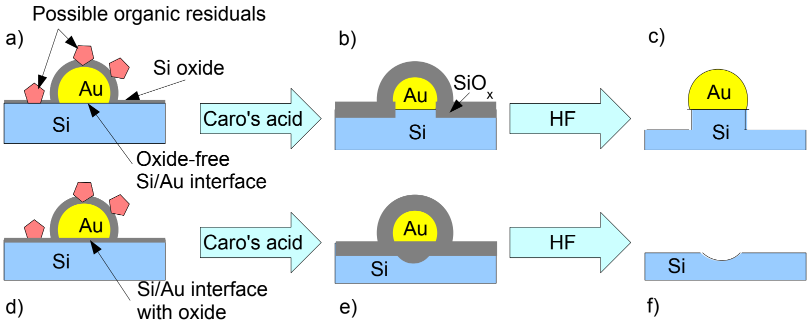


Figure 3.11: *Schematic representation of the effects of the two-steps etching process just prior to loading the sample in the CVD chamber.* ***a)****: the sample is covered with organic contaminants and Si oxide after the previous process steps. Nevertheless, the Si/Au interface is oxide-free.* ***b)****: the etch in* H_2SO_5 *removes the organic contaminants and increases the oxide thickness, although the Au/Si interface remains at least partially oxide-free.* ***c)****: after the dip in HF, the sample is clean and the gold pattern has been preserved.* ***d)****: in case of an annealing longer than 1 h, an oxide layer forms at the Au/Si interface. The sample is also covered in further oxide and organic residuals from the previous steps of processing.* ***e)****: the Caro's acid removes the organic residuals but increases the oxide thickness. The oxide grows faster at the Au/Si interface.* ***f)****: the HF removes the oxide layer and also the gold droplets laying on it. The gold pattern is no more present on the sample surface. In the region characterized by thicker oxide, where the droplets were situated, holes are formed. It has been found out that an oxide layer at the Au/Si interface can be formed also during a strong oxidizing etching, for instance RCA I. In this case, the path would be a)-e)-f).*

contrary might increase its thickness. In fact, a combined procedure of RCA I cleaning followed by HF etch resulted in the disappearing of the gold patterns, because the oxide increased its thickness to the whole contact interface between the gold and the silicon substrate. Therefore, the removing of the oxide implied also the removal of the gold dot (Fig. 3.11e,f).

For the same reason as for the RCA cleaning, a dip in Caro's acid alone did not allow nanowire growth. On the contrary, a two-step etch in diluted H_2SO_4/H_2SO_5 and in HF cleaned the samples from the organic contaminants removing the oxide but also saved the gold patterns. SEM pictures of the gold pattern before and after this combined etch do not present significant differences.

The success of the H_2SO_5/HF etch compared to the RCA/HF etch is probably due to the different oxidation rates of the Caro's acid and the RCA I cleaning, which can be roughly estimated to be 0.075 Å/min [Wes09] and 1 Å/min [Ale99], respectively. It is noteworthy that this combined etch is successful only when the gold/silicon interface is oxide-free (Fig. 3.11a). This is achieved when (i) the annealing process does not significantly increase the oxide layer thickness and (ii) the very first native oxide on the Si surface is removed prior to the RCA cleaning which prepares the samples for the spin-coating of the PS spheres. Such etching step does not affect in any way the patterning procedure, which gives the same results independent of the thickness or absence of the native silicon oxide.

Consider now the case in which an oxide layer embeds the gold droplet (Fig. 3.11d). During the etch the oxide layer becomes thicker where the substrate is in contact with the gold droplets (Fig. 3.11e), as the oxide grows faster at the gold/silicon interface [Siv09b]. Consequently, the gold is etched away in the HF dip prior to the CVD process together with the underlaying oxide, so that the catalyst dot array is removed and nanowire growth is impossible. When the oxide gets removed by the HF, holes indicate the locations where the gold dots were (Fig. 3.11f). This could be verified on samples annealed at 800°C for 10 hours (Fig. 3.12). The pattern is not

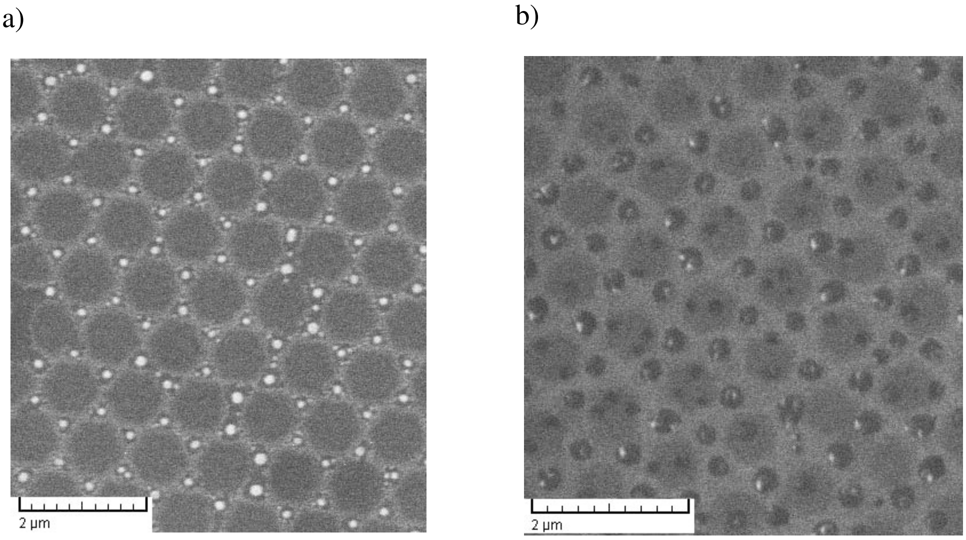


Figure 3.12: *SEM image of the gold pattern obtained by annealing a sample in Ar at 800°C for 10 hours before (a) and after (b) the etching in Caro's acid and HF. No gold pattern is detectable after the etching, although the bright spots might indicate gold residuals. Note that the gold pattern in a) does not present significant differences compared to the pattern obtained after an annealing at the same temperature for only one hour.*

significantly different from the one on samples annealed at the same temperature for only one hour. Nevertheless, the oxide layer is dramatically thicker, so that after the etch in Caro's acid and in HF only a "hole pattern" could be detected on the sample (Fig. 3.12b). In some of the holes a white spot can be seen, which can be an SEM artifact or a gold residual, although no CVD growth could be achieved.

In conclusion, the gold droplet must lie on Si for preserving the pattern after the etch in Caro's acid and HF. This is also a prerequisite for achieving epitaxial growth of high-quality monocrystalline nanowires. In fact, the nanowires can grow epitaxially during the CVD process exclusively when they are in contact with the crystalline Si substrate. The gold droplet might be covered by Si oxide, but this does not affect the NW growth, as the oxide is etched just prior to the CVD process (Fig. 3.11c).

3.4.2 Si nanowire growth

It is known that nanowires can grow only under particular process conditions. Within this window of temperature and pressure values, the preferred growth direction of the synthesized wires can be controlled by the CVD parameters [Yua09]. As for many applications it is crucial to obtain a high degree of vertical alignment, the case of the $[111]$ direction on a (111) Si substrate has been investigated, considering that the "normal to the (111) plane is favored [...] along other equivalent $< 111 >$ directions" [Yua09]. Nevertheless, the energy difference between the $< 111 >$ directions is very small. In order to grow NWs in the direction perpendicular to the substrate, a slow growth velocity has been chosen. This has been obtained performing the process with a low silane concentration and at a low pressure. The challenge is to find the parameters which allow preferential growth, but still enable nanowire growth.

The grown nanowires are shown in Figure 3.13. Although some growth in the other $< 111 >$ directions could not be completely prevented, a good percentage of NWs grow in the $< 111 >$ direction perpendicular to the sample surface, as clear from the cross-section SEM picture in Figure 3.13a. In Figures 3.13b and 3.13c the hexagonal pattern is recognizable, although some nanowires grew in the $< 111 >$ directions not perpendicular to the sample surface and appear to be in the wrong position. The growth directions are almost exclusively $< 111 >$, which is indicative of epitaxial growth.

TEM analyses have been performed on wires of non-patterned samples. These wires had been synthesized with similar growth parameters in the same CVD chamber and have a comparable appearance: straightness, smooth surface, Au droplet on the tip, diameter range, length. Therefore, it is believed that the results of those TEM analyses (see Fig. 3.14) can be applied also to the nanowires grown on NSL-patterned substrates, meaning monocrystallinity and low defect density.

Evidence regarding the sharpness of the nanowire diameter distribution can be obtained by measuring the diameters from the SEM pictures. The diameter distribution is given in Figure 3.15. The standard deviation is 12 nm, which is slightly bigger than the one of the dot diameter distribution. The main difference between the two distributions is the mean value, which is smaller for the wire diameter distribution (96 nm) than for the dot size distribution (101 nm).

Physically, the explanation of this difference relies on the values of surface tension which determine the characteristic shape of a nanowire. More in detail, the surface tension of the droplet

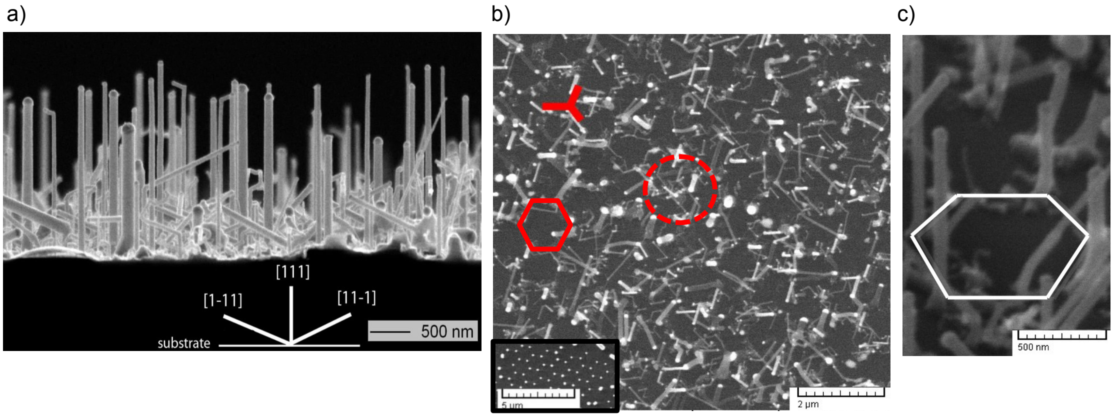


Figure 3.13: ***a)**: Cross sectional SEM micrograph. The $< 111 >$ directions, which correspond to the preferred growth directions, are shown in the inset near the scale. **b)**: Top-view SEM picture of the grown NWs of the same sample in a). The thick red lines show the preferred $< 111 >$ growth directions. The hexagon is a guide for the eye to recognize the hexagonal pattern considering that some of the nanowires grow in the $< 111 >$ directions not perpendicular to the sample surface, as is clear from picture a). The pattern is locally disturbed, see for instance the region in the dotted circle. This is caused by droplets which do not belong to the hexagonal pattern. They result from bigger droplets (see inset, its upper right corner) which were formed during the NSL process by undesired and uncontrollable inhomogeneities in the PS diameter. **c)**: High magnification 60°-tilted SEM picture where a single hexagon of the pattern is recognizable. The white line is a guide for the eye. The kinked NWs are due to defects occurring during the growth process. This sample was annealed at 1000°C for 1 h; therefore, some smaller satellite gold dots are present. No nanowires have grown from these smaller dots because of the chosen CVD process conditions. Reproduced with permission from [Ler10a].*

σ_l and the liquid-solid interface tension σ_{sl} on top of a nanowire are correlated by equation [Sch10]

$$\sigma_l \cos(\alpha + 90°) = -\sigma_{ls} \tag{3.2}$$

at the end of the growth process, where α indicates the angle between the gold droplet and the nanowire, as indicated in Fig. 3.16a. The value of α has been measured on high resolution SEM

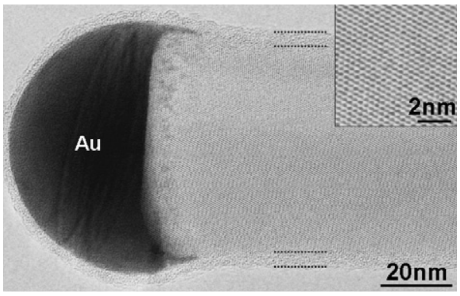


Figure 3.14: *TEM image of a single Si NW synthesized by the IPHT-Jena group with similar CVD parameters and the same process chamber as the ones used in this work. It looks absolutely similar to the wires shown in this chapter, so that it is believed that they have the same characteristics: low density of defects, monocrystallinity. Reproduced with permission from [Ste06].*

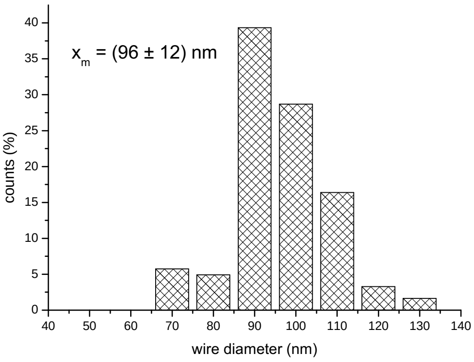


Figure 3.15: *Diameter distribution of the synthesized Si NWs catalyzed by the gold dot array. Reproduced with permission from [Ler10a].*

images of various wires grown with the described method. This leads to $\alpha \approx 20°$. Different values of α are found in literature, mainly depending on the process parameters. Nevertheless, α does not depend on the wire diameter, as shown in Fig. 3.16b. The value of α can be used

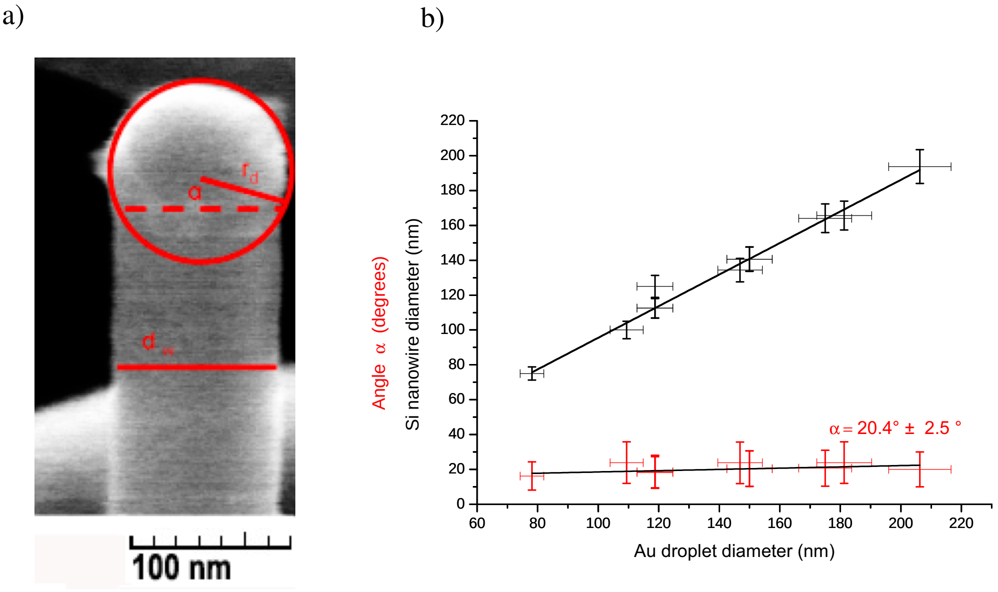


Figure 3.16: ***a)**: High-magnification SEM picture of a Si NW which is superimposed to the geometrical parameters considered in the text: the radius of the Au dot r_d, the diameter of the Si NW d_w and the angle α between them. **b)**: Plot of the wire diameter (black points) and angle size (red points) as a function of the Au dot diameter measured after the VLS growth. The uncertainty on the x-axis is given by 10% of the corresponding value, while the one on the y-axis has been calculated as the standard deviation of the measured values. The angle α between the wire and the droplet can be assumed to be independent of the wire size in the considered range of wire diameters (between 78 and 206 nm). The line connecting the points is a linear fit. In the case of α, the slope is zero (0.03 ± 0.08). For the fit of the wire diameter, the slope is 1 ± 0.06, which corresponds to cos(20) within error. Reproduced with permission from [Ler10a].*

for predicting the NW diameter based on the following consideration, which discusses the shape of the gold droplet in the whole process. After the annealing in Ar at 1000°C the droplet has an hemispherical shape and a radius r_d, as already shown in Fig. 3.4 and in Fig. 3.5. When the CVD process begins, the temperature raises and the droplet melts, forming the Au/Si alloy which catalyzes the wire. In this liquid phase, the droplet has lost its hemispherical shape and its angle with the substrate is quite small. During the NW synthesis, the droplet changes its form. When the process is ended, the droplet is again roughly hemispherical and forms the angle α with the wire. If the diffusion of gold into the wire during the growth is neglected, the droplet diameter can be considered approximately equal to r_d. With this assumption, the value of the angle α is useful for predicting the wire diameter by mean of geometrical considerations, if also the radius r_d of the gold dot is known:

$$r_w = r_d \cos\alpha \tag{3.3}$$

Using Eq. 3.3 with the value of the average dot diameter from Fig. 3.5b and $\alpha = 20°$, an average wire diameter of 95 nm is predicted, in excellent agreement with the average experimental diameter (96 nm, Fig. 3.15).

3.4.3 Silicon nanowires on glass

The results obtained using a glass substrate differ from the one on Si substrate by two characteristics: (i) the annealing step is performed at 600°C, so that the gold dot pattern presents few bigger droplets and many smaller ones, as shown in Fig. 3.3c (on wafer) and 3.17a (on glass); (ii) as the substrate is amorphous, the wire do not grow in a preferential direction, although they remain monocrystalline. The pattern is barely recognizable anymore.

While a preferential growth direction can not be achieved with this type of substrate, it has been investigated how to achieve a clean pattern of gold dots on glass even after an annealing step at lower temperature. First experiments have been performed changing the thickness of the sputtered gold layer, but the resulting pattern either did not show any significant change or could not form because too few gold had been deposited [Bec10]. Therefore, an additional sample

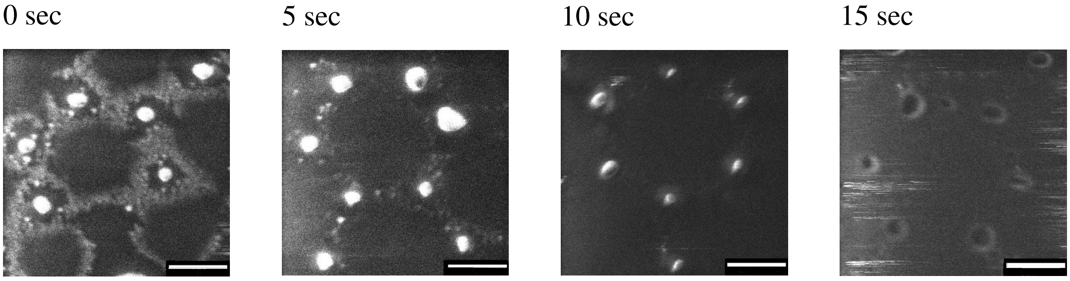


Figure 3.17: *SEM pictures of gold patterns on glass substrates etched in 1:10 water solution of KI/I_2 for different times: before etching (a), 5 sec (b), 10 sec (c), 15 sec (d). In d) the gold droplets have been completely removed and holes can be detected at their corresponding position prior to etching. The very bad quality of the SEM images is due to drift and charging issues caused by the non-conductive nature of glass. The scale bar indicates 500 nm in each image.*

processing step has been added, i.e. etching the sample in a 1:10 water solution of KI/I_2 for a few seconds. This etch removes the smaller gold droplets but does not shrink the bigger droplets on a measurable scale. Some examples of the obtained patterns are shown in Fig. 3.17. As the used solution removes gold at a very fast rate (around 7 nm/s), the etching time has to be checked very carefully. Alternatively, one can use a more diluted solution in water.

3.5 Conclusions

In this chapter a procedure for realizing regular patterns of dots and nanowires on different substrates has been presented. The method bases on a combination of nanosphere lithography and annealing in Ar at different temperatures, followed by Chemical Vapor Deposition for NW synthesis.

Regular hexagonal patterns of gold dots have been reproducibly obtained on large areas ($>$ 50 μm). The patterns change depending on the annealing temperature, as they are determined by different diffusion mechanisms: coalescence and Ostwald ripening dominate at lower temperatures, while gold evaporation and gold diffusion into the substrate become more influent at higher temperatures, leading to the disappearing of the gold pattern for temperatures higher than 1000°C. The obtained gold droplets could be used as catalysts for the epitaxial growth of Si NWs on a Si substrate after an adequate sample cleaning procedure, which removed the organic contaminants and the silicon oxide from the sample surface. Both the cleaning solution and the annealing temperature play a fundamental role in determining the oxide thickness and therefore the success of the cleaning procedure and of subsequent epitaxial NW growth. On a Si (111) substrate the careful choice of the CVD parameters determined the preferred growth in the [111] direction perpendicular to the sample surface. Monocrystaline Si NWs could be achieved also on a glass substrate.

The use of patterned catalysts allows to achieve not only NW arrays, but also to obtain nanowires with a sharp diameter distribution. It has also been shown that it is possible to accurately predict the NW diameter once that the catalyst droplet diameter and the dot/wire angle are known. Here, the diameter of the gold dot is known after the annealing process. The angle has been measured in SEM pictures and is diameter-independent.

In conclusion, these samples are characterized by a homogeneous density of nanowires, which are monocrystalline, have a sharp diameter distribution, and show a preferential growth direction, namely perpendicular to the substrate. They are therefore an ideal candidate for further processing towards a nanowire-based solar cell prototype, shown in this work in Chapter 6.

Chapter 4

Al-induced crystallization of Si combined with deposition techniques for the synthesis of Si nanostructures

In this and in the next chapter our goal is to characterize the Al-induced crystallization (AIC) of silicon in order to synthesize Si nanostructures and to achieve epitaxial *p*-doped Si shells around *n*-doped nanowires. The AIC process, sketched in Fig. 4.1, takes place when a layer of Al and a layer of amorphous Si deposited on a substrate are annealed at a temperature between 350°C and 550°C. The annealing time ranges from minutes to several hours. This process results in (i) the *p*-doping of Si by Al; (ii) the crystallization of Si; (iii) a layer exchange: the newly formed crystalline *p*-doped Si layer occupies the position which was of the Al layer. At the site of the amorphous Si layer there are now residuals of Si and Al, possibly oxidized. Although all three results characterize this process, it is usually called Al-induced crystallization (AIC) of silicon. As a terminology note, this process is also called Al-mediated solid phase epitaxy when performed on crystalline silicon (c-Si), since the resulting crystalline Si layer is epitaxial to the substrate.

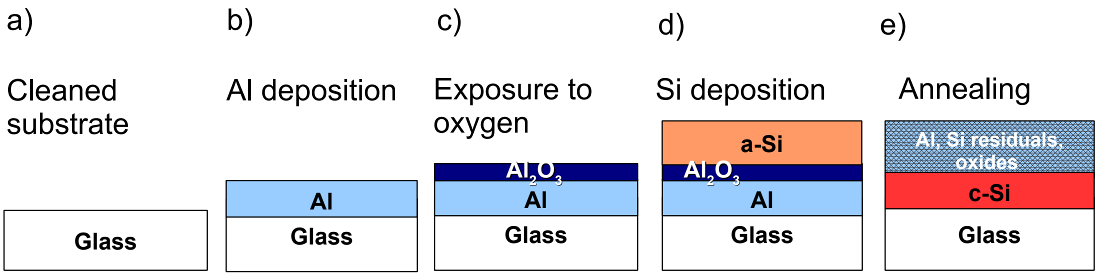


Figure 4.1: *Schematic representation of the AIC process on a glass substrate. More details will be given in this chapter and in the next one. On a clean glass substrate (a) an Al layer is deposited (b). The sample is exposed to air or to oxygen flow in order to achieve an Al oxide layer on the Al layer (c). After the deposition of the amorphous Si layer (d), the sample is annealed at maximum 550°C. The a-Si moves towards the substrate, crystallizes and becomes p-doped. After the AIC process, the upper layer is constituted by an Al matrix with Si residuals. The presence of oxides has been detected as well.*

Nevertheless, the driving forces are the same to the process performed on a glass substrate. In this work we use for both cases the term AIC process, as the only difference is the used substrate: glass or crystalline silicon.

The AIC of silicon has been known since 1972 [Her72], but only in the past decades some publications investigated it systematically [Nas00a, Nas00b, Nas00c, Nas01, Zha04, He05a, He05b, He06, Civ09], mainly driven by applications in the nanoelectronic and photovoltaic fields. The results published so far in literature agree with our findings, obtained reproducibly on various samples and shown in the next two sections, where the basic characteristics and parameters of the AIC mechanism on glass and on Si substrates are discussed. In the following part, the substrates are processed by AIC in combination with deposition techniques like Electron Beam Evaporation (EBE) or Chemical Vapor Deposition (CVD) for the synthesis of Si nanostructures. A summary of the experimental results closes the chapter. The thermodynamical description of the AIC process is presented in the next chapter.

4.1 Al-induced crystallization on glass substrates

In this section we study the case of AIC on a planar glass substrate with an oxide layer between the deposited Al and amorphous silicon (a-Si) layer. Only the obtained experimental results are reported; the theoretical calculations will be discussed in the next chapter, namely as case b) of Fig. 5.3 on page 68.

4.1.1 Experimental parameters

According to the work of Nast [Nas00b, Nas00c], many parameters influence the characteristic of the crystalline Si layer formed during the AIC process. For instance, the deposition rate of the Al layer is directly proportional to the final Si grain size, while a higher annealing temperature causes smaller Si grains. He also found out that for best results the Si layer must be equal or slightly thicker than the Al one. In addition to this, he showed that an oxide layer at the interface between the Si and Al layers is of crucial importance for obtaining a continuous layer of crystalline silicon (c-Si) after the annealing, although a thicker Al oxide layer can slow down the AIC process. The parameters chosen for the samples used in this work are based also on these results.

The default samples studied in this section are formed by: a Borofloat glass substrate, an Al layer, and an a-Si layer. The two layers have been deposited in the same Electron Beam Evaporation system with no substrate heating and have equal thickness (10 to 100 nm). The deposition rates are 7 Å/s (Al) and 1 Å/s (Si). In order to form an Al oxide layer at the interface between Al and Si, the chamber was purged with oxygen for 2 minutes between the depositions. For samples denoted as “oxide-free”, the depositions of Al and Si were performed without breaking the vacuum. These samples have been annealed in Ar atmosphere in a tube furnace at 550°C for 3 hours. The samples have been characterized by a Scanning Electron Microscope (SEM), by a Transmission Electron Microscope (TEM), and by Energy-dispersive X-Ray Spectroscopy (EDX).

In order to analyze the crystallinity of the Si layer after the annealing process the glass has been thinned in concentrated HF for about 3 or 4 hours. This etching step does not remove the glass completely, as the Borofloat glass contains some percentage of Na which reacts with the HF ($HF + NaOH \rightarrow NaF + H_2O$) forming sodium fluoride, that in HF undergoes a steady-state

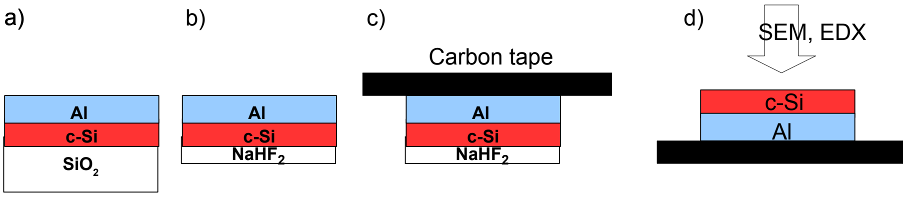


Figure 4.2: *Schematic representation of the sample preparation process for the analysis of the c-Si layer after the AIC process. The annealed sample (a) is etched in HF, which thins the glass substrate until* $NaHF_2$ *is formed (b). A carbon tape is glued on the Al layer surface (c) and the deposited layers are peeled off from the substrate (d), so that the Si layer can be analyzed.*

reaction: $HF + NaF \leftrightharpoons NaHF_2$. The HF is no more effective when a layer of $NaHF_2$ is formed and therefore only thins the glass. Nevertheless, this etch is necessary for decreasing the adhesion of the Si layer to the glass substrate.

After etching, a carbon tape has been glued to the Al layer, so that both layers could be peeled off from the remaining glass. This procedure is sketched in Fig. 4.2. In this way, the silicon surface which was facing the glass could be analyzed by Scanning Electron Microscope (SEM) and Electron Back-Scattered Diffraction (EBSD).

4.1.2 Results

After the annealing a complete layer exchange and a continuous layer of c-Si were obtained only on samples which (i) presented an Al oxide layer between the Si and Al layers and (ii) with Si and Al layers thicker than 10 nm. Samples without an Al oxide interface presented non continuous c-Si layer or no detectable difference with the non-annealed samples.

The c-Si layer has been characterized by EBSD and SEM. The SEM image in Fig. 4.3a shows that the Si grains have a size of approximately 10 μm^2. The EBSD analysis, displayed in Fig. 4.3b, could detect a preferential orientation around the [100] direction, indicated by the red color

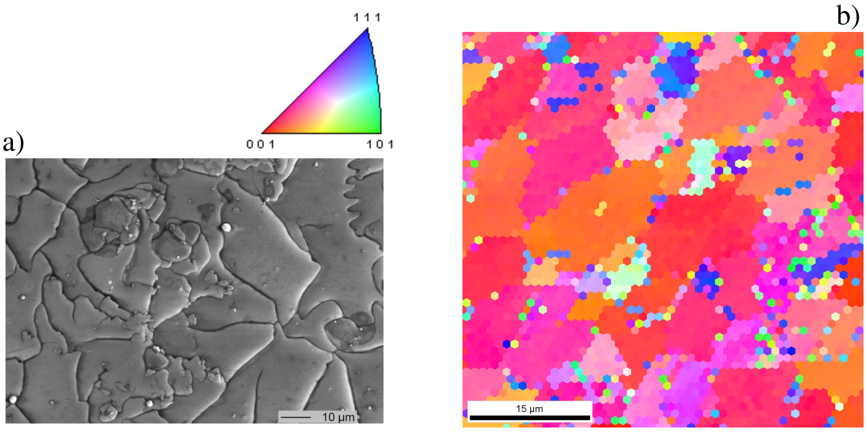


Figure 4.3: ***a)****: SEM picture of the resulting c-Si layer of an annealed sample. The glass has been thinned by HF etch to be able to detach the layers, glued to a carbon tape. EDX spectra (not shown) confirm that these are silicon grains.* ***b)****: EBSD pattern of c-Si obtained by AIC. A continuos c-Si layer is formed. The grains have preferential orientations around the (100) direction, as indicated by the color code on the left.*

(see the color code in Fig. 4.3).

The case of samples with very thin (10 nm) Al and Si layer has also been studied. Although the annealing parameters were the same as the other samples, no layer switch and Si crystallization could be observed, as clear from the cross-section TEM images and EDX maps shown in Fig. 4.4. The cause of the unsuccessful AIC process might be due to the oxidation of the Al layer. Al oxide could have formed either after the AIC process, during the preparation of the TEM lamella, or before the AIC process, as a result of the reactions $4Al + 3SiO_2 \rightarrow 2Al_2O_3 + 3Si$ or $2Al + B_2O_3 \rightarrow Al_2O_3 + 2B$, as boron is present in the glass substrate. In the glass also H_2O is present, which could form oxide in contact with Al as well. Nevertheless, the formation of the oxide layer should be limited to a few nanometers of Al, in contact with the substrate, and not affect the whole layer. If the Al layer thoroughly oxidized only after the AIC process, during TEM sample preparation, there has to be a reason why the AIC process did not take place. This reason might be related to the layer thickness and will be discussed in the next chapter (Sect. 5.5.4).

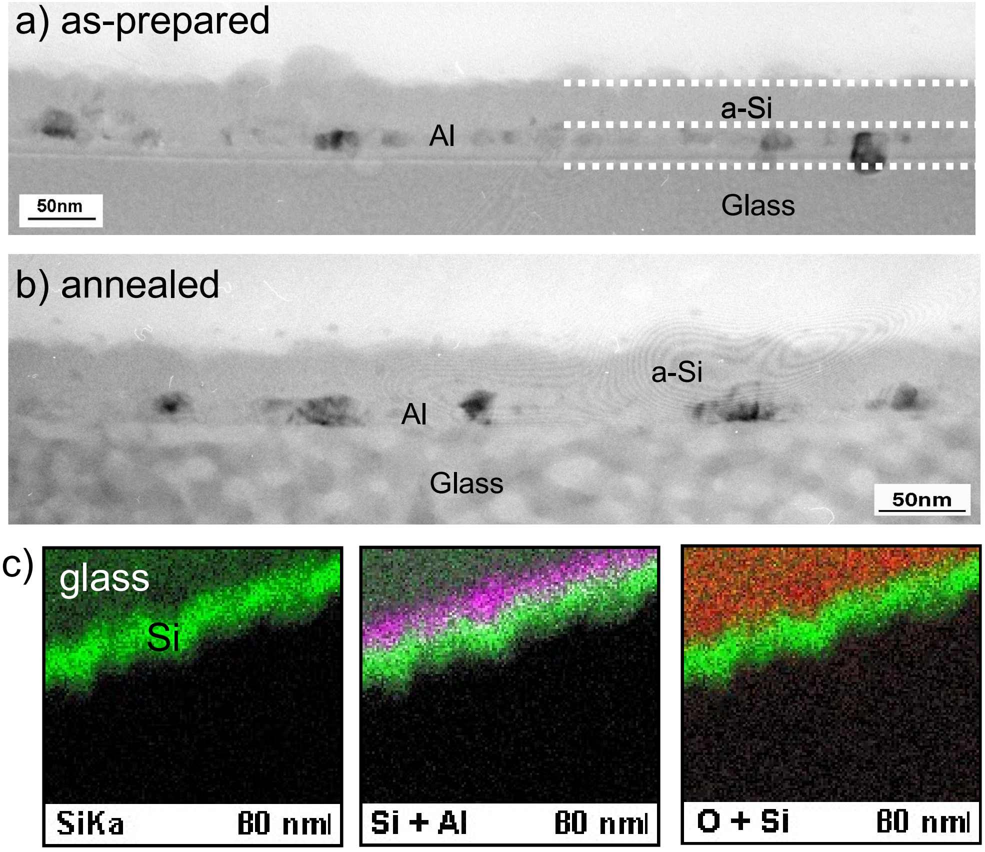


Figure 4.4: ***a)**: TEM cross-section image of an as-prepared sample on glass with nominal Si and Al layer thickness of 10 nm. **b)**: The same sample (different position) after annealing, which evidently did not lead to an AIC process. **c)**: EDX maps of the annealed sample. Note that in the EDX maps the Al appears to be completely oxidized. The oxidation could take place both during the process or between the transport of the TEM-lamella from the preparation to the analysis tool. The white dotted lines in a) are only a guide for the eye. In the images a) and b) the darker regions in the Al layers are Al grains with different orientations which have a dissimilar grey tone because of channeling contrast.*

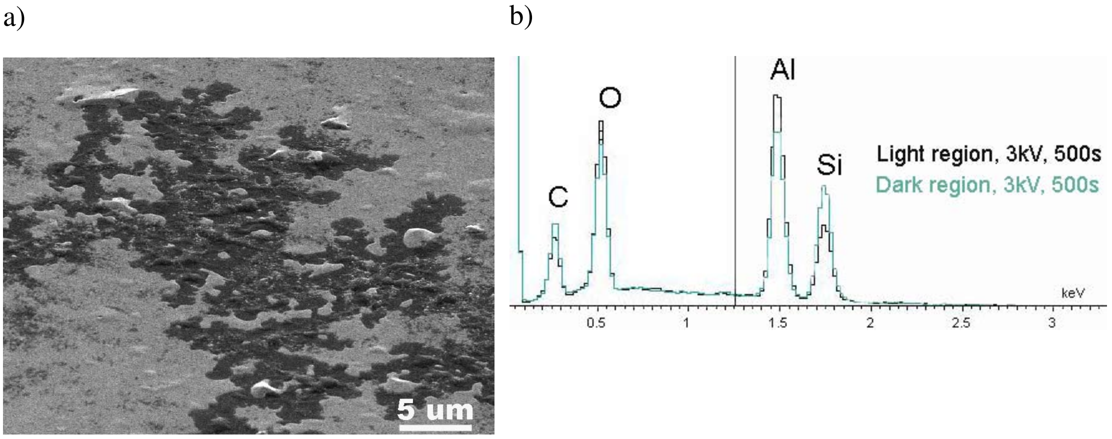


Figure 4.5: *60°-tilted SEM image (a) and corresponding EDX scans (b) of a glass substrate with an Al and Si layer after annealing. Both layers are 30 nm thick. In the EDX the spectra performed on both the dark and light grey regions of the SEM image are reported for comparison. The light region is prevalently constituted by Al, the dark one by Si. The signal coming from the underlaying substrate (mainly Si oxide) has also to be considered in the interpretation of the spectra.*

The surface of the sample after AIC process has been characterized as well. Even if the AIC process includes an exchange of the position of the Al and Si layers, the upper layer normally consists not only of Al but also of some Si islands, which were trapped by the surrounding Al and could not diffuse to the bottom for forming the crystalline Si layer [Nas00b, Nas00c]. As already shown by Nast, the surface of the annealed sample is characterized by Si dendrites in an Al matrix. Such features have been observed also in our samples and have been characterized by EDX, as shown in Fig. 4.5.

4.2 AIC on crystalline Si

Here, the results achieved by AIC on crystalline silicon are presented. Civale et al. [Civ09] investigated the AIC process on silicon wafer. We use as a substrate monocrystalline silicon nanowires, which we synthesized as described in Chap. 3.

The samples on crystalline silicon have been studied after the ones on glass as a further step towards the realization of a nanowire-based solar cell (see Chap. 6), where the AIC is performed for obtaining a crystalline p-layer on n-doped Si nanowires. Three main characteristics have to be considered: (i) the thickness of the deposited layers, so that the resulting c-Si would have a thickness comparable with the NW diameter; (ii) the presence of a native Si oxide on the substrate; (iii) the presence of the Al oxide layer between the deposited Al and Si layers. While the influence of the layer thickness on the AIC process is discussed in the next chapter (see Sect. 5.5.4), we show here the results achieved in the last two cases, schematically represented in Fig. 4.6.

The experimental procedure does not differ from the one described in Sect. 4.1.1 for planar glass substrates with regard to the deposition and the annealing parameters. One processing step is added prior layer deposition, namely the gold caps at the tip of the synthesized Si NWs are etched in aqua regia (HNO_3 : 3 HCl) for 2 minutes. Where mentioned, the silicon oxide layer has been removed prior to the deposition of the layers by an etch in 5% HF for 1 minute.

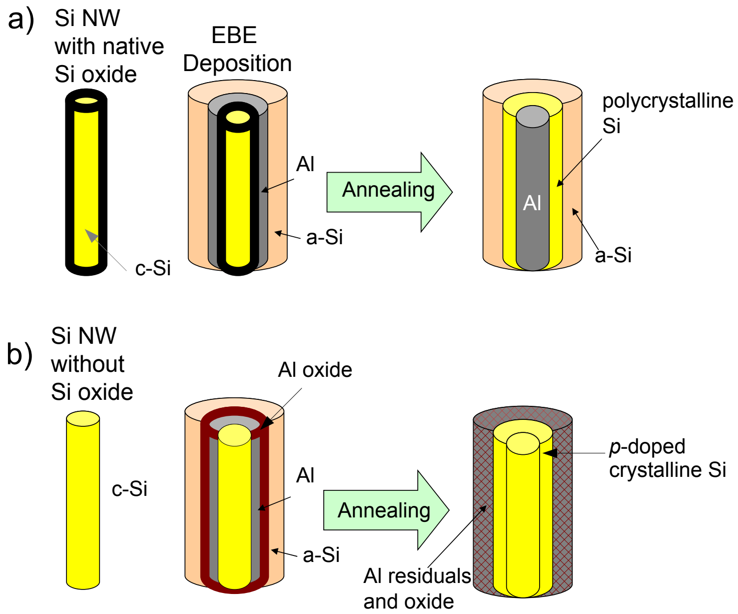


Figure 4.6: *Schematic representation of the AIC process on monocrystalline Si wires with (a) and without (b) a layer of native Si oxide before the EBE deposition of the Al and Si layers. The Si native oxide in b) has been removed by an HF etch. Note the absence of the Al oxide interface layer between Al and Si in a), while it is present in b).*

4.2.1 AIC on a Si nanowire with native Si oxide (Fig. 4.6a)

Consider a sample where a silicon nanowire is used as a substrate and it presents a native silicon oxide layer. This SiO_2 layer is approximately 5 nm thick (see Fig. 3.14 on page 38). On this substrate a layer of Al and one of a-Si are deposited. After annealing we observe a completely new result: the Al layer did not exchange its position with the deposited a-Si but with the crystalline core of the Si nanowire. The amorphous silicon layer did neither change its structure nor position. This is shown in the TEM pictures of Fig. 4.7. The thermodynamical calculations in Sect. 5.5.5 will show that this process is energetically more favorable than the expected AIC process.

4.2.2 AIC on a Si nanowire without native Si oxide but with an Al oxide interface layer (Fig. 4.6b)

In this case, the silicon substrate has been dipped in 5% HF for 1 minute, then etched with aqua regia and again left in 2% HF for 20 sec. Without any further delay it has been transferred to the process chamber for the deposition of Al and Si, with an Al oxide interface layer between them. After annealing, a c-Si layer epitaxially formed on the Si nanowire, covered by residuals of Al and Al oxide, as shown in the TEM and EDX results of Fig. 4.8. This is then the configuration which will be used for the realization of the solar cell in Chap. 6.

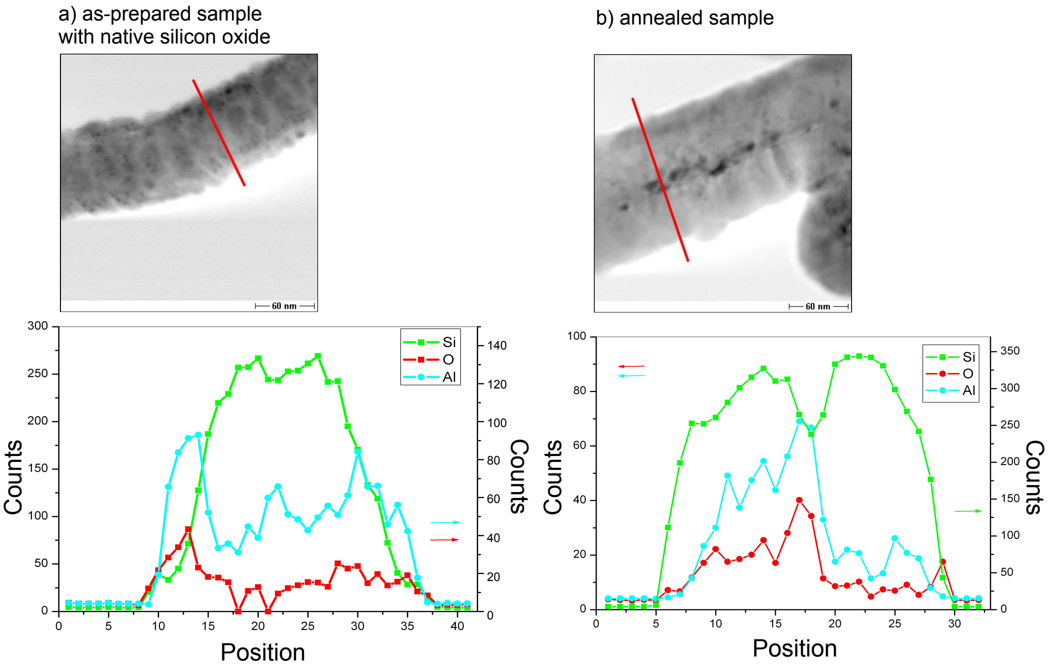


Figure 4.7: *TEM pictures (above) with the red line corresponding to the in situ EDX line scan (below) of a sample as in Fig. 4.6a before (a) and after (b) the AIC process. Note the different scale for silicon and the other two elements.* ***a)****: an Al and a Si layer have been deposited on a Si nanowire. The Al layer is sandwiched between the c-Si core of the nanowire and the a-Si layer.* ***b)****: after the annealing process, the Al exchanged its position with the Si core of the nanowire. As the oxygen measurement perfectly follows the Al one, it has been concluded (see next chapter) that the Al oxidized during the AIC process by an exchange reaction with the native Si oxide present on the nanowire.*

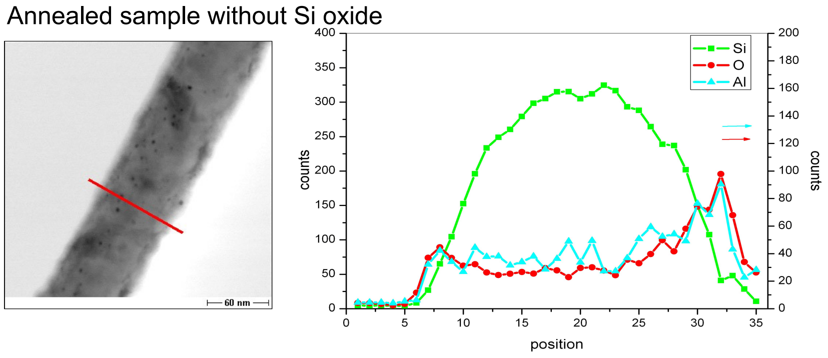


Figure 4.8: *TEM picture (left) and EDX analysis (right) of a sample of type as in Fig. 4.6b, i.e. the Al and Si layers present an Al oxide interface layer and have been deposited on an oxide-free Si nanowire. The red line in the TEM image indicates where the EDX line scan has been performed. Note that the Si scale in the EDX line scan is different than the one of oxygen and aluminium. The sample before the AIC process looks like in Fig. 4.7a. Here, after the AIC process, the Al is no more embedded in Si, as the green line of silicon does not increase on both sides of the Al peaks. To be noted that the Al looks completely oxidized, but the silicon is not.*

4.3 Synthesis of nanostructures

Until now we processed the samples in an oven filled with Ar for studying the Al/Si layer exchange and the crystallization of the Si layer. In this section, the annealing process is performed exclusively on glass substrates and in a chamber where Si can be deposited by either Electron Beam Evpoaration (EBE) or silane Chemical Vapor Deposition (CVD). The aim is to synthesize Si nanostructures, potentially using the Al which reaches the substrate surface during the AIC process as a catalyst. The Si is supplied by the gaseous phase in the deposition chamber and possibly per diffusion by the substrate. The annealing step has always been performed *in situ* in the process chamber just before the deposition process. The results consist of nanoballoons or nanowires, whose shapes mainly depend on their formation mechanism: diffusion-limited growth for the EBE-processed samples, reaction-limited growth for the structures synthesized by CVD. Additionally, they are influenced by process parameters like base pressure, deposition rate, deposition temperature, and processing time.

4.3.1 Nanostructures by Electron Beam Evaporation (EBE)

The samples studied in this section have been prepared by Electron Beam Evaporation (EBE) depositing a 60 nm thick Al layer with a rate of 7 Å/s on a quartz or borofloat glass substrate previously cleaned. The pressure during deposition was around 10^{-7} mbar. After exposure to air for a few hours, the samples have been transferred to a Si-only EBE system (Figure 4.9), where three different process steps take place. Firstly, a silicon layer with a thickness of 150 nm is deposited on the samples with no substrate heating. Secondly, the samples are annealed for 90

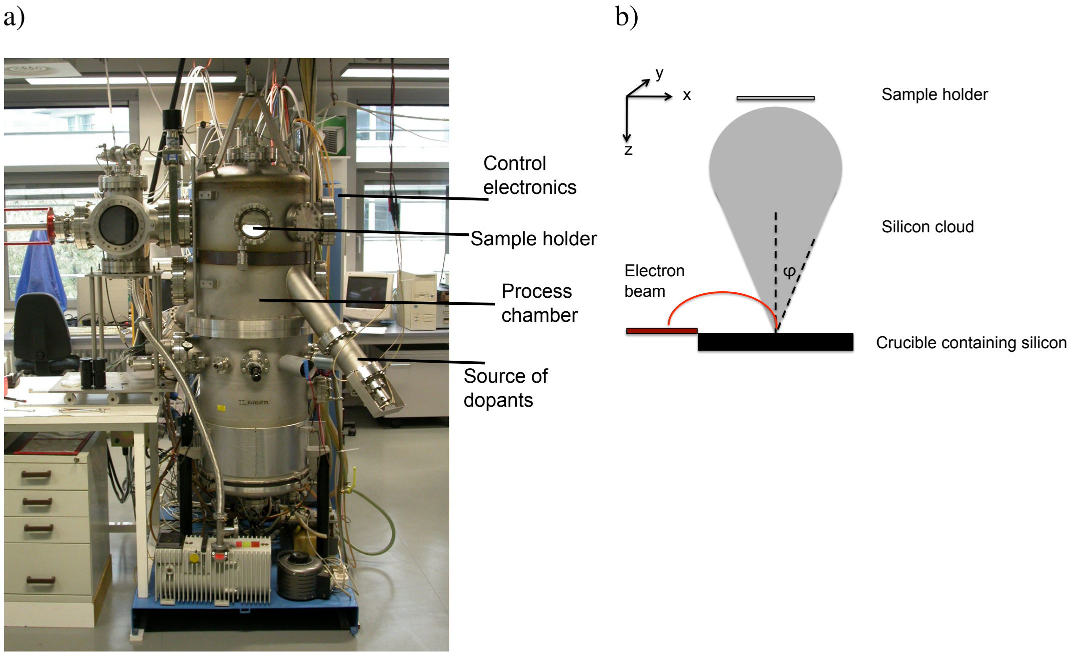


Figure 4.9: ***a)**: Electron Beam Evaporation system at the Institute for Photonic Technology in Jena, Germany. **b)**: Schematic representation of the geometry inside the EBE process chamber.*

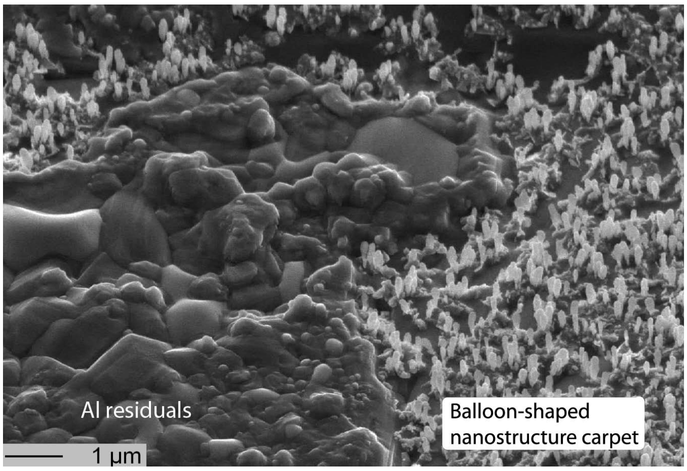


Figure 4.10: *SEM picture of the sample surface after the process in the EBE chamber. The two morphologies discussed in the text can be identified: a rough landscape of Al residuals (left) and a nanostructure carpet (right).*

minutes at 520°C. Finally, a second silicon deposition is performed for 40 minutes at 560°C at the slowest possible rate for this system, namely 15 nm/min. The base and process pressures in the Si-only EBE were 10^{-8} mbar and $5 \cdot 10^{-7}$ mbar, respectively. After the process, the sample surface presents two distinct morphologies (Fig. 4.10): (i) a rough landscape with unorganized grains of different size or (ii) a uniform distribution of balloon-shaped nanostructures. Such nanoballoons could only be achieved for a very narrow window of deposition parameters.

The rough landscape is constituted by Al residuals. The Al reaches the sample surface during the AIC process which takes place in the EBE chamber while annealing. During the layer exchange the Al might trap some Si in the upper layer [Nas00c]. Trapped Si islands can not participate in the formation of the lower crystalline Si layer on the glass substrate. These superficial Si islands become the substrate for the second morphology type, the nanoballoon carpet. In fact, TEM-analyses combined with EDX-scans show that the balloon-shaped nanostructures grow on regions in which both Al and Si are detected (Fig. 4.11). These results do not imply that an alloy

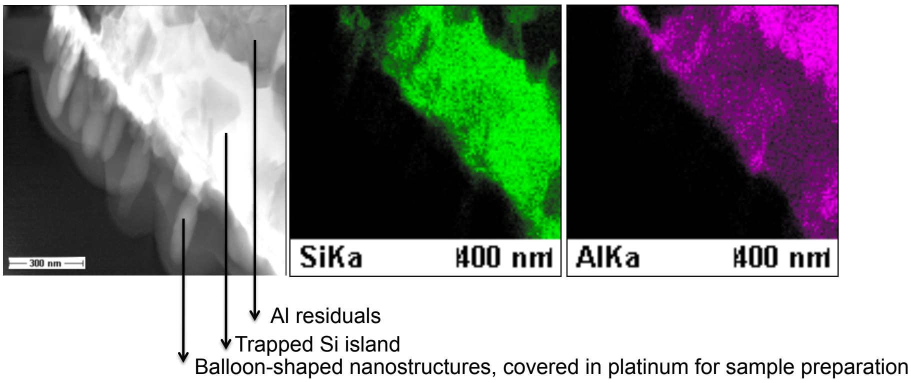


Figure 4.11: *EDX analysis performed on a cross section TEM-lamella prepared from a sample processed in the EBE. The substrate of the nanoballoons consists of both Al and Si.*

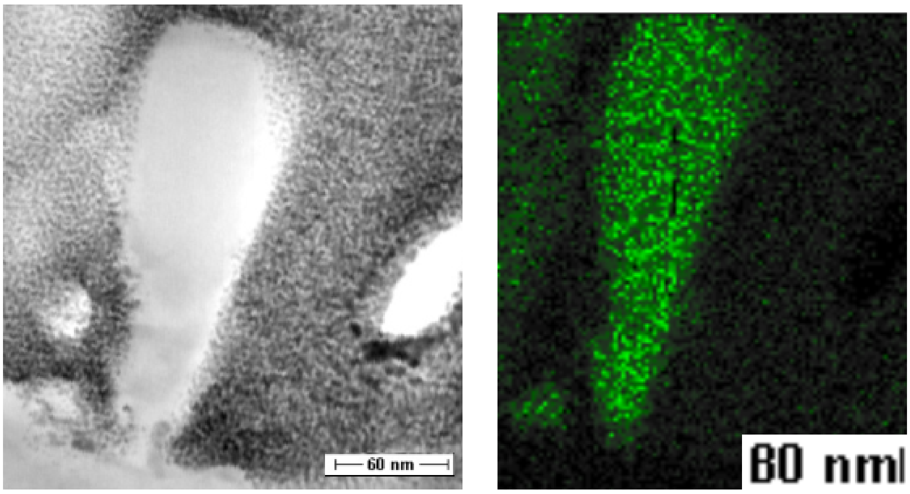


Figure 4.12: *TEM picture (left) and correspondent EDX analysis (right) of one silicon nanoballoon.*

is present, which is unlikely, as the process temperature is always carefully kept below the eutectic temperature of the Si/Al system. More probably, these elements are separately present, for instance as small Si islands embedded in Al matrix.

Further investigations show that the nanoballoons are of polycrystalline silicon (Fig. 4.12). We assume that they grow out from an aggregation point or seed, represented by a small Si cluster surrounded by Al residuals, as also suggested by the EDX results. Surface diffusion might contribute to the formation of the observed nanostructures but, considering that the nanostructures are formed by Si and that most of the surface around them consists of Al, it probably plays no crucial role. It will therefore be neglected in the following considerations, where the nanoballoon is considered as formed exclusively by particles evaporated from the crucible. Since the base pressure in the chamber is around 10^{-8} mbar, it is unlikely that the path of these particles is changed by impacts with molecules in the gas phase: their trajectory can be considered a straight line. In fact, the mean free path l of the Si particles is

$$l = \frac{kT}{\sqrt{2}\pi d^2 P} = 1.06 \cdot 10^3 \text{ m} \tag{4.1}$$

where k is the Boltzmann constant, d is the Si particle diameter (222 pm), and T and P the particle temperature and pressure, respectively. The process pressure (10^{-7} mbar) has been taken. The temperature of silicon in the crucible is not precisely known, but we can estimate it to be close to the silicon melting point. Therefore, the calculated value has to be considered as a lower limit, as the particle temperature might be higher. In conclusion, the flux of particles is unlikely to change direction because of impacts with other particles present in the process chamber. The particles reach the seed by ballistic transport.

Using the Maxwell–Boltzmann speed distribution one can also calculate their mean velocity v as

$$v = \sqrt{\frac{8 \cdot kT}{\pi \cdot m_{Si}}} \tag{4.2}$$

where T is the absolute temperature of the particle and m_{Si} the atomic mass of silicon. Again, we use the melting temperature of Si, which leads to $v = 1125$ m/s circa.

We define now a cartesian coordinate system where the x and y axes lay on the sample surface and z is perpendicular to it pointing to the crucible (Fig. 4.9b). It is assumed that all the particles with high v_x and v_y speed components do not reach the sample surface and therefore do not contribute to the crystal growth process. For the other particles, we assume v_x and v_y to be negligible. This assumption is realistic considering that the silicon cloud coming out from the crucible under action of the electron beam follows a $cos\phi$ distribution [Aub05], where ϕ is the angle between the z axis and the cloud at the crucible (Figure 4.9b). Known the distance between the crucible and the sample to be about 32 cm and the size of the sample comparably small (2.5 cm $\cdot$ 2.5 cm), the angle corresponding to the particles which can reach the sample is $\phi_o = 4°$. Therefore, we can approximate the particle flux to be unidirectional.

Nevertheless, the particles are not generated by a point source, but are extracted from the crucible at locations with different x and y coordinates. It is impossible to foresee the exact position in the crucible from which they are extracted or, more importantly, to predict the position in which the Si particles will land on the sample during the deposition process. Consequently, their landing point on the sample surface is random. In order to simulate the evaporation from the crucible as from an extended source, we adopt an unidirectional velocity perpendicular to the substrate combined with a random-walk model. We use the diffusion limited aggregation (DLA) theory as presented by Witten and Sander in 1983 [Wit81].

The DLA can be simulated as a process in which single particles successively coalescence with a seed particle. Particles which touch the boundaries of the simulated space are no further considered. The probability that coalescence takes place between a static and the walking particle is given by the sticking (or stickiness) coefficient S_c, which can assume values between 0 (no particle sticks) and 1 (all particles stick). The seed is reached by the other particles after a random walk, which describes a trajectory formed by a sequence of random steps. The main reason why this is definitely not the case for Si molecules in the EBE is that the transport of the evaporated particles is ballistic. Nevertheless, the particle arrival location is uncertain, due to random coordinates of the particle extraction point in the crucible. With all these comments and assumptions, we can apply the results of a DLA-based simulation to our experiment. In the next paragraphs, all aspects are explained in more detail.

The simulations have been performed using the online freely available program “dla-nd” by Mark Stock, in particular the three dimensional model of version 1.0. This model is based on the DLA theory already described before. Some parameters can be defined by the user as the sticking coefficient S_c, the particle number n, the particle velocity v, and a directional constraint. The parameters used in the simulation program are arbitrary but consistent. The dimensionless length is expressed in units of the particle radius.

S_c for silicon has been measured by various groups with different deposition processes and crystal orientations [And96]. We used $S_c = 1$ as in [And96] for silicon deposited by electron beam evaporation. The number of particles n can be roughly estimated from the volume of one of the balloon-shaped nanostructures from a SEM picture:

$$n = \frac{V}{V_{Si\ mol}} \cdot N_A \simeq 4 \cdot 10^7 \tag{4.3}$$

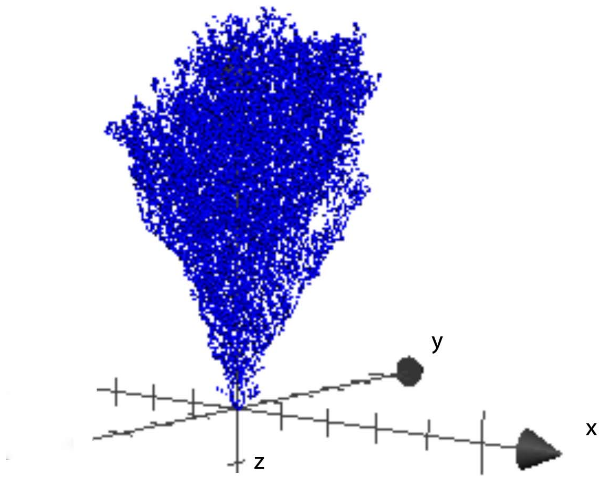


Figure 4.13: *Figure of the data obtained modeling a DLA-based formation process. It relies on a random-walk model which has to be interpreted as explained in the text. In particular, the random walk is used for representing the ballistic motion of particles evaporating from an extended source. As the motion is unidirectional, a directional constraint in the* z *direction is considered, which explains the growth direction of the structure. The data have been calculated with* $v = 10000$ *and* $n = 10000$.

where *V* is the estimated volume, $V_{Si\ mol}$ the Si molar volume and N_A the Avogadro number. This value is far too high for the computational power available, so that a lower value of 10^5 particles has been used for the simulations. Anyway, the number of particles seems only to influence the size of the final structures, but not its shape, wherefore this limitation is acceptable.

In order to motivate the value chosen in the simulation for the particle velocity, the structure of the used program needs to be mentioned again: it simulates a random walk where the trajectory is formed by subsequent steps, as usually defined, and not the random landing position of a particle in ballistic motion and extracted from an extended source. In the program, therefore, the particle velocity determines the angle that the sides of the obtained structure form with the substrate surface. Higher velocities correspond to steeper angles. In the extreme case that the previously calculated particle velocity would be used (Eq. 4.2), the particles would assemble in a straight line. This would not make any sense, as the role of the velocity in the two cases is different and the experimental particle velocity is not related to the speed value used in the model. For practical purposes, therefore, a value of v has been chosen which gives a nanostructure which has a similar angle to the substrate as the experimentally obtained ones.

Finally, the unidirectionality of the particle flux is represented by a directional constrain in the z direction [Kon86]. The presence of an unidirectional particle flux is crucial for the growth model, as it can explain why the crystals grow in the z direction and not otherwise.

The resulting data are plotted in Figure 4.13. The shape obtained is very similar to the one of the grown nanostructures.

4.3.2 Long straight nanowires by Chemical Vapor Deposition (CVD)

In this section, the AIC process is performed in a CVD chamber, prior to the SiH_4 flow. The samples are constituted of quartz or Borofloat glass substrates on which an Al and a Si layer

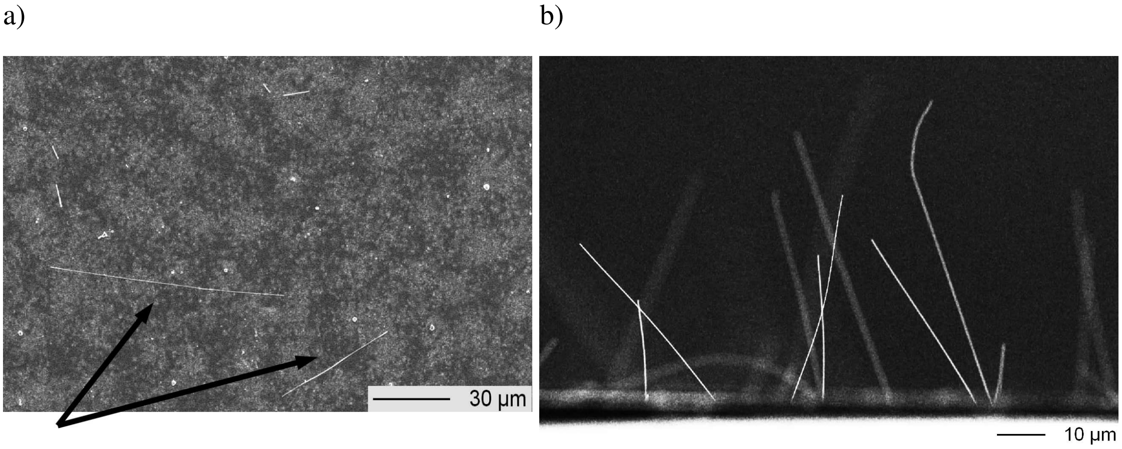


Figure 4.14: ***a)**: Top-view SEM picture of a sample after AIC and CVD process. Some nanowires are indicated by the arrows. The darker regions on the substrates are Si dendrites, the lighter ones consist of Al residuals, as in the EDX analyses shown in Fig. 4.5.* ***b)**: Cross section SEM picture, where the very long silicon nanowires can be seen. The contrast of both pictures has been adjusted for clarity.*

have been deposited by EBE. The layers are both 50 nm thick. The chamber pressure during the depositions is $5 \cdot 10^{-7}$ mbar. Between the depositions of the two layers the EBE chamber has been filled with oxygen for two minutes in order to form an Al oxide interface layer between the Al and Si layers. The samples have been loaded in the CVD chamber without any further preparation. They have been *in situ* annealed for 20 h in high vacuum (around $5 \cdot 10^{-7}$ mbar) at a nominal temperature of 530°C. Subsequently, they have been processed in 4 sccm SiH_4 and 5 sccm Ar at pressure of 0.5 mbar and at a nominal temperature of 658°C for 25 minutes.

The SEM pictures in Figure 4.14 show the features which characterize the sample after both the annealing and CVD processes. As already shown in Fig. 4.5, the dark areas on the sample surface represent silicon dendrites while the lighter regions are Al residuals. In addition to this, thick, long, straight wires are present. They grow preferentially at the boundary between a Si dendrite and the Al area (Fig. 4.15). Their average diameter is of about 150 nm and they can be longer than 30 μm. There is no visible macroscopic metal catalyst droplet at their tips, which are round-shaped (see Fig. 4.16). The wires are not visibly tapered. TEM analysis (Figure 4.17) show that the NWs have a complex crystalline structure which can be approximately described as consisting of a crystalline core and an oxide outer shell, the core presenting both elongated big grains and clusters. In addition to this, one can note that the nanowire surface is rough and therefore in contrast with the typical smooth surface of the nanowires synthesized by the Vapor-Liquid-Solid (VLS) mechanism. Moreover, the wires could not be formed in case either the annealing or the CVD step has been skipped, or if only an Al or a Si layer had been deposited. They do not grow also if a particularly good basis pressure (10^{-8} mbar) is achieved after a much longer pumping.

The appearance of the nanowires and the analyses performed do not give a clear hint about the possible growth mechanism. Among the various ones presented in literature [Sch07, Jia04, Wan98, Moh08, Zou06b, Zou06a, Sch10], the experimental results shown in this section can be explained by two main different growth process, schematically depicted in Fig. 4.18. Both present some questionable aspects and can explain only part of the wire characteristics. These possible

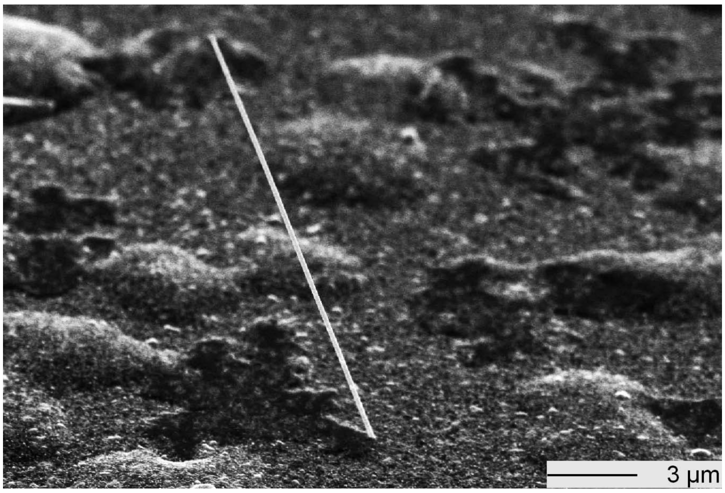


Figure 4.15: *60^o- tilted SEM picture of a single wire grown at the boundary between the Si dendrite (darker region) and the Al matrix (lighter region).*

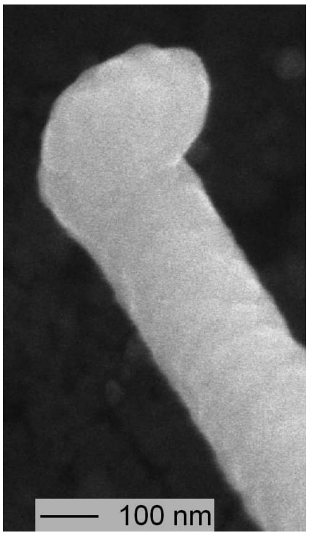


Figure 4.16: *High-magnification SEM picture of the top end of a Si NW. The round-shaped tip is characteristic of all the analyzed nanowires and suggests the presence of some particular phase or oxide distribution, possibly relevant for the growth process.*

mechanisms are: (i) the wires are catalyzed by an Al particle by VLS or VSS mechanism; (ii) the wires are catalyzed by a Si oxide particle or grow embedded in Si oxide via an Oxide-Assisted-Growth mechanism (OAG). These methods will now be described in more detail, with particular regard to their advantages and limitations.

The first case (Fig. 4.18a) considers the possibility that the nanowires are catalyzed by an Al particle, as this metal is present on the sample surface and it has already been reported as a catalyst material for both VLS and VSS mechanisms [Wan06, Sch10]. The Al particle might be isolated from all the Al residuals and incorporated in Si by the arms of a Si dendrite, which close around a tiny portion of Al while forming. This would explain why the nanowires mostly grow at the boundary between some ramification of the dendrite and the Al. Nevertheless, no catalyst

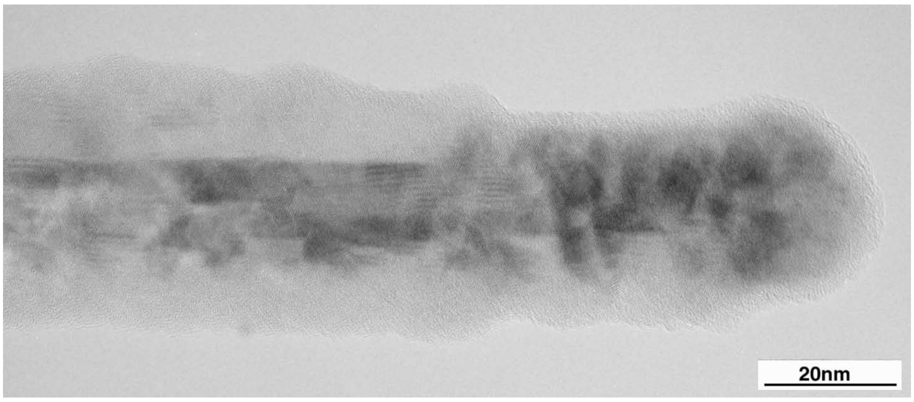


Figure 4.17: *TEM picture of a Si nanowire synthesized by CVD on a substrate processed by AIC. The long central grain is well visible. Some small crystalline clusters are also present.*

particle can be clearly seen at the top of the nanowires. The detection of Al in Si by SEM is difficult because of the poor contrast between these two materials. TEM and EDX analysis could not furnish clear evidence of a droplet particle. Despite of this, the idea of a catalyst droplet composed by a tiny particle embedded in another material has been reported [Moh08]. In our case, this would mean an Al particle embedded in a Si matrix. TEM can not resolve tiny particles embedded in another material, unless they are luckily positioned on the surface of the sample.

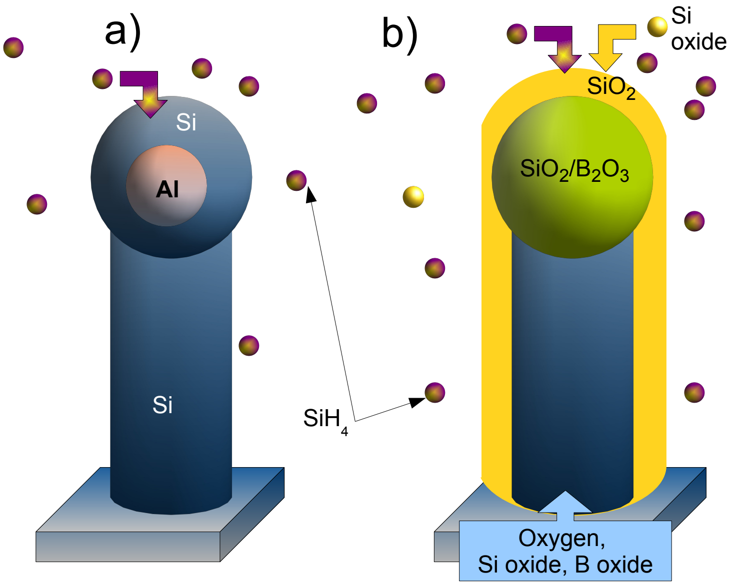


Figure 4.18: *Scheme of the two possible synthesis mechanisms which can partially explain the experimental results and are discussed in the text. The location of the wires at the boundary between a Si dendrite and the Al matrix is not sketched.* ***a)****: an Al particle is embedded in Si and might form a catalyst droplet which catalyzes the wire by VLS or VSS mechanism.* ***b)****: oxide-assisted-growth. Oxygen, silicon oxide, and, in the case of borofloat glass, also boron oxide, might be released from the glass substrate. These oxides can form a particle and catalyze the NW and also constitute the NW oxide shell during growth. The gas species present in the CVD chamber might form a cluster of Si and Si oxide and an oxide shell around the NW as well. The seed cluster is integrated in the NW when the process finishes.*

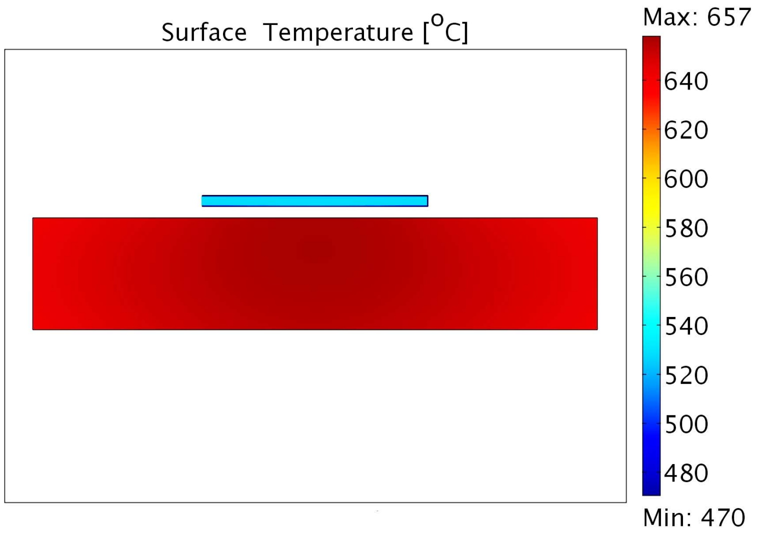


Figure 4.19: *Calculations of the temperature of the quartz surface heated by radiation in vacuum. The ambient and heater temperatures are set equal to the room and the nominal process temperature (658°C), respectively. The values of quartz emissivity have been taken from [Mik]. The calculated quartz surface temperature might be more than 30°C higher than the silicon surface temperature measured during the calibration (540 and 510°C, respectively). The calculations have been performed with the help of I. Sill.*

EDX on the contrary averages the results on the whole area hit by the beam, and tiny Al particles in a Si wire might just be below the noise level. It is not clear if the catalyst particle is in liquid or solid state. The process temperature (510°C) is thought to be well below the Al/Si eutectic temperature (577°C), which implies that the droplet is solid. Despite of this, an alloy might get formed for two concomitant reasons: (i) the particle could undergo melting point depression, if we assume it to be smaller than 10 nm. This assumption is realistic, as the wire diameter without oxide is approximately 15 nm (see Fig. 4.17). In this scenario, the eutectic temperature would be lower of about 35°C [Sch10] and therefore equal to 542°C. Furthermore, (ii) the use of a glass substrate might result in a higher effective temperature on the sample surface than expected. The calibration performed with a Si substrate affirms that at 0.5 mbar a nominal process temperature of 658°C corresponds to 510° on the sample surface. Nevertheless, the surface of a glass substrate is likely to be warmer, as clear from Fig. 4.19, calculated with the Heat Transfer Module package of the COMSOL Multiphysics modeling environment.

In addition to this, it can not be explained why the sides of the wire are rough and covered by oxide. Oxidized wires and their oxidation mechanism have been investigated [Siv09b], but using annealing parameters (temperature and time) which basically differ from the ones used in this work. Also the appearance of the wires is different: the oxide shell is here definitely rougher and the wires are not thoroughly oxidized. Alternatively, the oxide could have been formed after the unloading of the samples.

In conclusion, this growth model requires a quite exotic mechanism of formation of a catalyst droplet, which incorporates undetectable Al within Si, and does not explain the wire roughness. A further remark has to be mentioned: if silicon oxide is present, then also Al is likely to oxidize. If this occurs prior to the NW growth, the Al-oxide particles would not form an eutectic with silicon and, consequently, could not catalyze the nanowire. In addition to this, the wires are too long for having a VLS-comparable growth rate. Nevertheless, this model can explain the position of the wires on the sample surface.

The second possible mechanism (Fig. 4.18b) is represented by the oxide-assisted growth (OAG). In this case, the Si would be catalyzed by its own oxide. Such results have been obtained [Wan98, Lee99, Zha01, Zha03] by laser ablation with Si and SiO_2 powders and at a process temperature above 930°C, which is significantly higher than the one used in this work. Nevertheless, the wires present very similar characteristics: a thick SiO_2 shell which retard lateral growth, a round tip with a polycrystalline core, and stacking faults and twins in the Si NW which might result in a fast growth rate [Wan98]. The described mechanism consisted in four steps [Wan98, Lee99]: (i) Si nanoprecipitates are formed on the sample surface. Some of the atoms forming this particle have dangling bonds and can act as a nucleus, absorbing reactive silicon oxide present in the process chamber. Subsequently, (ii) the Si nanoparticles are embedded in a Si oxide matrix; (iii) the Si oxide layer on the Si nanocluster has a catalytic effect, enhancing atomic absorption, diffusion and deposition; (iv) Si continues to deposit in correspondence of the Si nanocluster, forming the nanowire.

While it is obvious that the oxide is supplied by the SiO_2 powder in the cited articles, the source of oxide is not clearly identified in our case, as the process takes place in silane and Ar with a base pressure of approximately 10^{-7} mbar. Oxygen or silicon oxide could be present in the process chamber, as discussed in the Appendix A, or might diffuse from the glass substrate to the sample surface. Still, the temperature would be too low for allowing the decomposition of oxide molecules into silicon nanoparticles: the reaction $2SiO \rightarrow Si + SiO_2$ takes place at high temperatures and the melting point of silica is well over 1000°C. But boron could diffuse from the borofloat glass substrate as well, for instance in form of boron oxide B_2O_3. Its melting point is around 500°C, allowing the formation of a liquid oxide droplet which could catalyze the Si NWs cracking silane. Concerning the oxide surrounding the nanowires, it could also be formed by oxygen present in the chamber or diffusing from the substrate. It is now important to define more precisely which reactants are in the process chamber and can interact with the droplet. In Appendix A it is shown that silane and silicon oxide are both present in the chamber although, for the used experimental parameters, in significant different amount. But they also have a highly dissimilar sticking coefficient to silicon. Combining these two factors, the two species can be considered having a similar probability of sticking to the droplet and form the nanowire. This means that the growth of the Si NW is simultaneous to the formation of the oxide shell around it, resulting in a straight nanowire with constant diameter for constant thermodynamic conditions [Moh08]. This agrees with the results obtained with both SEM and TEM investigation, as shown in Fig. 4.14b, 4.15, 4.17.

The amount of oxide present in the chamber might also determine the density of grown nanowires. It has been shown in the case of laser ablation [Lee99] that the yield of produced nanowires strongly depends on the percentage of oxide available in the target. This could be valid also in our case, where a low amount of oxygen is not enough for achieving a high NW density, as confirmed by the fact that processes started with basis pressure below 10^{-8} did not lead to the growth of nanowires.

When the SiH_4 flow is stopped, the reaction-limited growth terminates. The seed is integrated into the nanowire lattice and becomes non-detectable by TEM analysis, although the hemispherical form of the NW tip could represent an indirect evidence of its presence [Moh08].

To sum up, the OAG can explain the nanowire morphology in all its aspects with exception of the possible role of Al, for instance in determining the NW position or, more in general, the growth of the nanowires, which could not be observed on samples with no Al layer.

4.4 Conclusions

In the first part of this chapter the experimental results of the AIC process on a glass substrate and on Si NWs have been shown. The amorphous Si layer crystallizes, for the used annealing parameters, only if an oxide layer is present between the deposited Al and Si and if these deposited layers are thicker than 10 nm. In addition to this, the native Si oxide layer on the Si substrate has to be removed for allowing the layer exchange of the Al with the deposited amorphous silicon, and not with the crystalline nanowire core.

The AIC substrates on glass have been used for the growth of Si nanostructures by EBE and CVD. The deposition process has been performed *in situ* after the annealing step. In the case of deposition by EBE, the grown features resemble nanoballoons. They are formed by polycrystalline silicon and are located on silicon islands trapped on the sample surface during the AIC process, surrounded by Al residuals. Their formation mechanism can be explained using the diffusion-limited aggregation theory, although the random walk is redefined as an uncertainty of the landing location of the deposited Si particles due to an extended source (the Si crucible). In this scenario the DLA-based simulations can reproduce the achieved nanostructures.

Combining AIC with CVD we achieved long thick straight wires embedded in a Si oxide shell. As no catalyst droplet could be detected and the origin of the oxide is not clearly determined, two different growth mechanisms have been discussed, although none can fully describe the results. The questions regarding the origin of the Si oxide shell, not usual for VLS mechanism, was discussed considering the gas reactants present during the process in the CVD chamber or the diffusion of oxygen, Si oxide and B oxide from the substrate. The other main unclear point is the impossibility in detecting a catalyst particle. Therefore, the incorporation of the catalyst droplet into the NW or the presence of a tiny undetectable Al particle within a Si matrix have been suggested. In this latter possibility the AIC process is of fundamental importance, as it supplies the Al. In the other cases, it presumably creates some convenient seed nucleation sites at the boundary between the Al matrix and the superficial Si dendrites, still allowing NW growth, not achieved on glass substrates with only a Si or an Al layer.

Chapter 5

Thermodynamical description of the Al-induced crystallization process

In the previous chapter the AIC process has been introduced as the result from the interaction between three layers: a-Si, Al and Al oxide between them. Their characteristics, together with the AIC annealing parameters, determine the configuration of the layers after the annealing. Particularly important are the layer thickness, the presence of an Al oxide and, although not directly mentioned, the annealing temperature. The mechanisms which cause the AIC process, though, have not been discussed yet. Basically two slightly different approaches in literature have suggested explanations of the AIC process so far. The first one, summarized by Nast in his publications [Nas00a, Nas00b, Nas00c], considers a model based on the diffusion of Si, where the formation of crystalline silicon is due to the difference of chemical potential between amorphous and crystalline silicon (c-Si). In addition to this, such reports mention for the first time that the presence of an Al oxide layer is necessary for forming a continuous layer of c-Si by AIC. Counterintuitively, the oxide seems also to quicken the AIC process. This could be confirmed by the comparison of the annealing time at similar temperature needed by different authors for completing an AIC process (see Tab. 5.1): the samples which present an Al oxide layer present a continuous layer of crystalline Si or a complete layer exchange, although also temperature and layer thickness might play a role.

The other approach, by Zhao ([Zha04]; see also [He05a, He05b, He06]), calculates the Gibbs energy balance based on the macroscopic atom model (MAM), showing that the crystallization process takes place because it is energetically favorable. Part of these calculations additionally shows why also a layer exchange takes place. Still, the role of the oxide is not fully cleared. This is the main goal of this chapter.

After summarizing the experimental results achieved in the previous chapter, an overview of the established knowledge of the AIC process is offered, beginning with Nast's model. In the following section, the role of the Al oxide at the Al/Si interface is newly investigated. Successively, the MAM model is summarized, based on which the balances of Gibbs energy in the samples before and after AIC will be calculated in the subsequent section. The energy balances refer to samples with and without an Al oxide layer, on two different substrates, and are compared in order to establish which configuration is more favorable for the AIC process. Following the notation used in literature, the {} refers to the amorphous phase of the considered material, the <> to the

Al oxide	Annealing time	Continuous layer and complete exchange	Temperature [°C]	Layer thickness [Al/Si, nm]	Reference
yes	5 h	yes	425	270/500	[Pih07]
yes	10 min	yes	550	270/500	[Pih07]
yes	1 h	yes	475	500/500	[Nas01]
no	2 h	no	450	200/250	[Nas00a]
no	10 d	no	165	50/150	[He05a]
no	1 h	no	250	50/150	[He05b]

Table 5.1: *Table listing some AIC process data from authors who studied samples with or without an Al oxide layer between the deposited Al and Si layers. The references have been chosen among the fastest experiment for both cases to the best of the author's knowledge and for samples with comparable size of the crystallized region. Publications with evidence of a complete layer exchange and of the formation of a continuous c-Si layer have been preferred. The table might hint that, in general, an AIC process with Al oxide leads to a continuous c-Si layer, although also the layer thickness and the temperature have an influence. There are no standard process parameters yet.*

crystalline one. All the results are compared in the conclusions.

The understanding of the AIC process is fundamental for optimizing the process parameters, so that a complete layer exchange and a throughly crystallization of the Si layer can be achieved. Both are a fundamental prerequisite for realizing the *p*-doping of a nanowire-based solar cell, shown in the next chapter.

5.1 Experimental data and considered configurations

The results achieved by Nast [Nas00b, Nas00c] have already been mentioned in Sect. 4.1.1. Based on his conclusions, we realized the samples studied in this section with an Al layer (below) and a Si layer (above) of equal thickness (50 nm). An Al oxide layer at the interface between Si and Al has been achieved by purging the evaporation chamber with oxygen for 2 minutes between the depositions. So-called "oxide-free" samples have been obtained performing the Si and Al depositions without breaking the vacuum. Borofloat glass or own-synthesized Si nanowires, grown as described in Chapter 3, have been used as substrates. The samples have been annealed in Ar atmosphere in an tube furnace at 550°C for 3 hours. More experimental details are given in Sect. 4.1.1 and 4.2 of the previous chapter. Here we briefly summarize the achieved results, thermodynamically explained in this chapter. In particular, we will compare the Gibbs energy difference of layer configurations which are dissimilar only for the type of substrate (glass or Si) or for the presence or not of the oxide layer.

A complete layer exchange and a continuous layer of Si were reproducibly obtained on glass and on Si substrates exclusively on samples which presented an Al oxide layer. In addition to this, two particular cases have been investigated: (i) very thin layers (10 nm each) on a glass substrate with an Al oxide interface layer and (ii) samples without an Al oxide layer on Si nanowire covered by Si native oxide. In the first case the sample presented no significant difference after the annealing. The second type of sample showed a layer exchange between the crystalline core of the nanowire and the deposited Al layer, maintaining the a-Si layer untouched.

All cases are explained in more detail in the next sections. Before showing the related calculations, though, the corresponding model has to be presented and the role of the Al oxide interface layer has to be cleared. These are the subjects of the next three sections.

5.2 Nast's model

The model suggested by Nast [Nas00c, Nas00a] for analyzing the AIC process is based on the dissociation of the amorphous phase, so that Si atoms can diffuse within the Al and nucleate, incorporating other dissolved Si atoms. The question how the Si-Si bonds can be broken so that Si atoms are able to diffuse is answered by Hiraki's "screening model", where the mobile free electrons of the metal can screen the Coulomb interaction of the Si-Si bonds at the metal/Si interface. Because of this screening effect, few monolayers of Si at the interface present metal-like bondings, where the valence electrons are no more bounded to specific atoms and can therefore diffuse through the sample. When the diffusion takes place, a solid Al solution with Si solute develops. The atoms of the a-Si layer diffuse into the Al layer to increase the chemical potential of the Si solute [Nas00a], causing Al to reach supersaturation. The system then reduces its Gibbs energy, nucleating Si and forming a crystalline Si phase. The process continues as long as Si atoms diffuse into the Al layer, that is, until a layer exchange is completed.

Although this model is widely accepted, it does not clarify why the AIC process could not completely take place in absence of an oxide interface layer and, in particular, how atoms can pass through it when present. Nast studied the structures with a glass/Si/Al configuration, which presents a Si-oxide layer at the interface. He refers to the so-called "Al-spike"-formation problem: the Al film reduces the Si oxide diffusing through it and forming spikes [Bie98]. To us, it is not clear how Al spikes could form after that the Al reduced the SiO_2 and therefore oxidized. Furthermore, the AIC process takes place independently of the layer configuration. Therefore, Al spikes should form also in the case of an Al oxide interface layer. Nevertheless, the reduction of Al oxide is reported in literature as likely by Al only in combination with carbon at high temperatures [Hal07] or by electrolysis. In the next section we suggest other possibilities for the diffusion through the Al oxide.

5.3 The Al oxide layer

Two main surprises are caused by the presence of the Al oxide layer between the Si and the Al layers in the AIC process: (i) it allows diffusion, although it is known to be a good diffusion barrier and (ii) it allows the AIC process to take place, which means, it makes a difference in the balance of Gibbs free energy. The first point is discussed in this section, while the second one is developed in Sect. 5.5.2 in the calculation of the Gibbs energy difference.

Regarding the possibility for atoms to diffuse through Al oxide, scheduled values of diffusion coefficients of Si and Al in Al oxide ([Uso04, Gal94], respectively) are practically zero at the AIC process temperature. One can extrapolate the value for the diffusion coefficient of Al in Al oxide from [Gal94] at 773 K, obtaining values well below 10^{-25} cm^2/s. No diffusion of Si through Al oxide is observed in [Uso04], which we interpret as the diffusion coefficient being smaller than the measurement resolution. Comparing with the other results present in the cited article, we set such resolution limit around 10^{-16} cm^2/s. The minimum value D_{min} required to allow diffusion

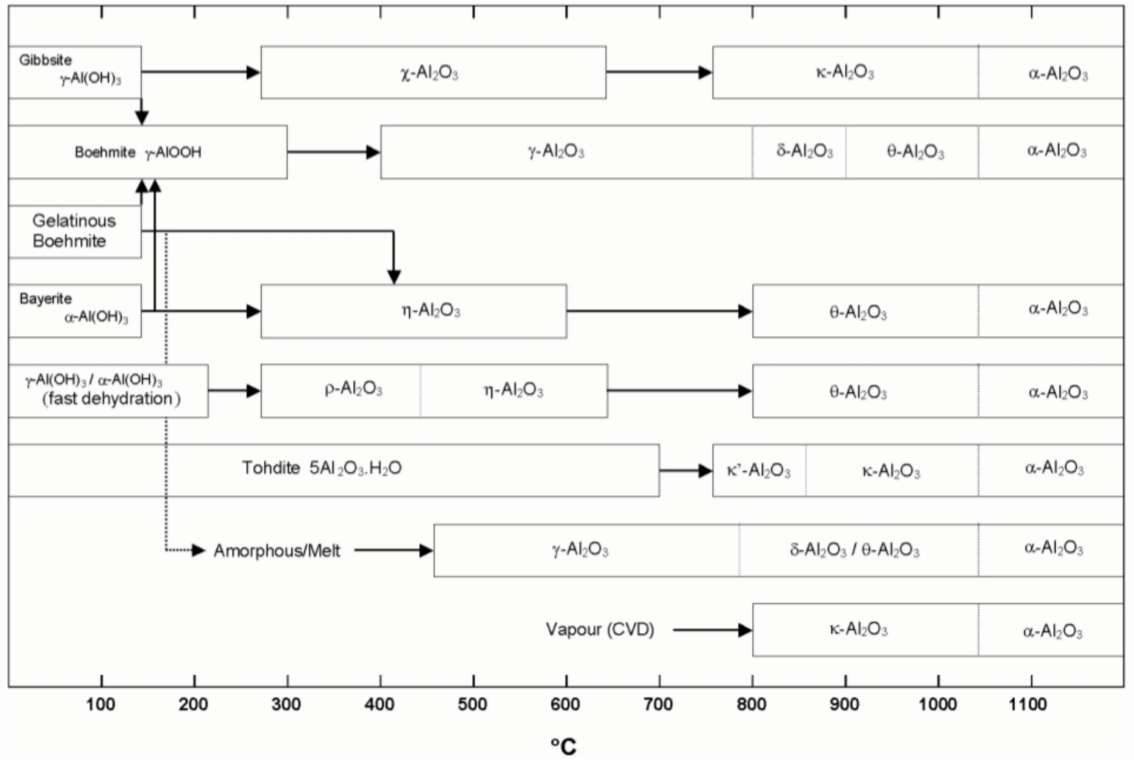


Figure 5.1: *Schematic representation of the transition sequences of the aluminas. From [Pag04].*

through a 5 nm thick Al oxide layer within 3 hours can be calculated as

$$D_{min} = \frac{L^2}{t} = \frac{(5 \cdot 10^{-7}\ \mathrm{cm})^2}{1.08 \cdot 10^4\ \mathrm{s}} = 2.31 \cdot 10^{-17}\ \mathrm{cm}^2/\mathrm{s} \tag{5.1}$$

Lacking experimental data, we can not conclude whether the diffusion of Si through a 5 nm thick Al oxide layer is possible with the considered annealing parameters. The diffusion of Al through such layer seems highly improbable.

The only other possibility of how the process can take place is that the Al oxide layer presents holes. The AIC process is not the first occasion in which an Al oxide layer is not considered to be continuous and homogeneous. Publications [Doy89, Pin97] about alumina scales on different substrates report voids in the film after high-temperature annealing and explain them either with the incorporation of void during the Al oxide deposition or by the change of the molar volume of the alumina itself when undergoing a phase transition. In particular, Al oxide can have an amorphous structure, $\{\mathrm{Al_2O_3}\}$ if stochiometric, or different crystalline forms: $<\alpha$-$\mathrm{Al_2O_3}>$, $<\gamma$-$\mathrm{Al_2O_3}>$, $<\delta$-$\mathrm{Al_2O_3}>$, $<\eta$-$\mathrm{Al_2O_3}>$, $<\kappa$-$\mathrm{Al_2O_3}>$, and $<\chi$-$\mathrm{Al_2O_3}>$ [Pag04]. The transitions between these phases, shown in Fig. 5.1, give an idea of how complex it could be to determine the structure of the Al oxide layer at circa $500°\mathrm{C}$ during the AIC process. Nevertheless, Jeurgens et al. [Jeu00] affirm that the thin Al oxide film forming on an Al substrate can be either amorphous or $<\gamma$-$\mathrm{Al_2O_3}>$. If this Al oxide film is thicker than the critical thickness $h^{crit}_{\{Al_2O_3\}}$ the Al oxide becomes $\gamma-$crystalline [Jeu00]; if it is thinner than $h^{crit}_{\{Al_2O_3\}}$, it is amorphous.

The critical thickness does not depend on pressure, but changes with the grain orientation of

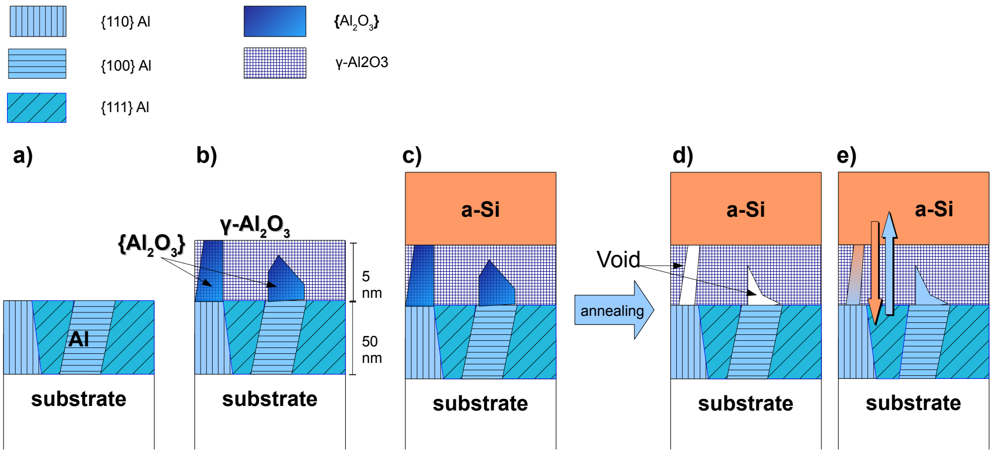


Figure 5.2: *Schematic representation of the role of the Al oxide interface layer during the AIC process.* ***a)****: aluminium is deposited on a general substrate. It results to be polycrystalline.* ***b)****: under exposure to oxygen, the Al surface oxidizes. The thickness of the Al oxide can be 3 to 5 nm (in the experiments it is assumed to be 3 nm), steered by the exposure time. Depending on the orientation of the Al grains, the Al oxide presents different phases: amorphous (on* $\{110\}$ *and* $\{100\}$ *Al) or* $<\gamma$*-*$Al_2O_3>$ *(on* $\{111\}$ *Al).* ***c)*** *a-Si is deposited on the Al oxide.* ***d)****: during the annealing, the amorphous Al oxide crystallizes, shrinking in volume, so that holes and channels can form.* ***e)****: the Si and the Al from the deposited layers fill the spaces left empty by the shrinking of the Al oxide. The so-formed channels might act as diffusion pipes for atoms, allowing diffusion.*

the Al substrate and, of course, temperature. At the default AIC process temperature in the present work, 773 K, $h^{crit}_{\{Al_2O_3\}}$ is approximately 6 nm for the $\{110\}$ grains, 3 nm for the $\{100\}$ grains and almost zero for the $\{111\}$ grains [Jeu00].

The Al deposited on a substrate is polycrystalline [Nas00b, Nas00c]. The Al oxide formed by exposure to oxygen is about 3 nm thick [Sai02]. Therefore, the Al oxide layer is presumably constituted by adjacent $\{\mathrm{Al_2O_3}\}$ and $<\gamma\text{-}\mathrm{Al_2O_3}>$ (Fig. 5.2b), as it will be thinner than the critical thickness on $\{100\}$ and $\{110\}$ grains, but thicker than $h^{crit}_{\{Al_2O_3\}}$ on $\{111\}$ grains. This has two consequences: (i) the boundaries between an amorphous and a crystalline region may allow diffusion of Al or Si atoms through the Al oxide layer; (ii), more important, the molar volumes V of the two phases are different: $V_{\{Al_2O_3\}} = 3.19 \cdot 10^{-5}$ m^3/mol while $V_{<\gamma-Al_2O_3>} = 2.81 \cdot 10^{-5}$ m^3/mol [Jeu00]. As a consequence, if some amount of Al oxide crystallizes, its volume would shrink, allowing the formation of holes or leaving space which can be filled by Si or Al atoms. This process is schematically represented in Fig. 5.2.

The phase change from amorphous Al oxide to $<\gamma\text{-}\mathrm{Al_2O_3}>$ is thermodynamically favorable at 773 K: the difference between energies due to the heat of formation of $<\gamma\text{-}\mathrm{Al_2O_3}>$ and of $\{\mathrm{Al_2O_3}\}$ can be calculated based on the macroscopic atom model explained in the next section. It results

$$\gamma^{form}_{<\gamma-Al_2O_3>} - \gamma^{form}_{\{Al_2O_3\}} = \frac{\Delta H^{form}_{<\gamma-Al_2O_3>}}{C_O V^{2/3}_{<\gamma-Al_2O_3>}} - \frac{\Delta H^{form}_{\{Al_2O_3\}}}{C_O V^{2/3}_{\{Al_2O_3\}}} = -0.48 \text{ J/m}^2 \qquad (5.2)$$

using the constant C_O = 4.5 $\cdot$ 10^8 and the values of $\Delta H^{form}_{<\gamma-Al_2O_3>} = -394$ kcal/mol and of $\Delta H^{form}_{\{Al_2O_3\}} = -377$ kcal/mol [Cha74] at the AIC process temperature.

Therefore, during the annealing, the amorphous Al oxide crystallizes reducing its volume in correspondence of the $\{110\}$ and $\{100\}$ orientation of the Al grains. This might form some empty space, from now on called holes. The holes can differ in shape. The longest ones, formed on $\{110\}$ Al grains, might become diffusion channels which connect the Al and the Si deposited layers. It is plausible that their elongated shape does not change with the annealing, as already observed for voids in Al layers, which remain straight also when shrinkage occurs [Vol67]. Consequently, the channels might act as diffusion pipes for atoms, allowing the exchange of Si and Al atoms to take place much faster. When the first Si and Al atoms enter the void channel from the two sides, they leave some space free in their origin layer. This space can be filled by similar atoms of the same layer, which will then also diffuse through the channel, or by the new atoms arriving from the channel, driven by a concentration gradient. Being the diffusivity of Al in Si much lower than the one of Si in Al ([Kra02, Fuj78], respectively), it is possible that aluminium will shift to the regions left free by Si.

Nast’s results [Nas00b] show that the oxide layer at the interface between Si and Al maintains its location in the sample for the whole AIC process. This remains valid also in our model. In fact, it is not implied that the Al oxide atoms change their position, once the channels are formed.

This model fixes a maximum oxide thickness for the Al oxide layer, namely circa 6 nm, above which the AIC process can not take place. If the oxide, in fact, is thicker than the higher value of the critical thickness (on $\{110\}$ Al grains, $h^{crit,110}_{\{Al_2O_3\}}$), the diffusion through the oxide layer is precluded, as presumably the whole Al oxide layer is crystalline, no phase change within it takes place and therefore no holes form. If, on the contrary, the oxide thickness does not reach the critical thickness, many channels can form and connect the Al and the Si layer. This also explains Nast’s observation about a slower AIC process for thicker Al oxide layer. If the oxide layer is thicker than $h^{crit,100}_{\{Al_2O_3\}}$ but thinner than $h^{crit,110}_{\{Al_2O_3\}}$, channels can form on the $\{110\}$ grains but not on the $\{100\}$ grains (Fig. 5.2e). Pipe diffusion still takes place, but the inferior number of available channels slows down the process compared to samples with thinner (<3nm) Al oxide layer.

5.4 The “macroscopic atom” model

The macroscopic atom model (MAM) has been formulated starting from the ’70s “for predicting the values of enthalpy of formation of binary alloys of arbitrary combinations with an accuracy comparable with that of the experimentally observed quantities” [dB88]. Highlighting the inadequacy of the traditional classification of solids and alloys for this purpose, the MAM introduces a new set of concepts and empirical quantities for structuring the experimental information. Two basic properties used in the model are the electron density at the boundary of the Wigner-Seitz atomic cell, n_{WS}, and the chemical potential for electronic charge, ϕ^*. They are both related to the corresponding molar volume *V* and, using tabulated values [dB88], allow to calculate the enthalpy of formation of solid and liquid alloys and hence the corresponding interface enthalpy ([dB88], page 26):

$$\Delta H^{interface}_{A\ in\ B} = \frac{V^{2/3}}{n^{-1/3}_{WS\ average}} \left[-P \cdot (\Delta\phi^*)^2 + Q \cdot (\Delta n^{1/3}_{WS})^2 \right] \tag{5.3}$$

where P and Q are constants, A and B the elements forming the considered binary alloy, $\Delta\phi^* = \phi^*_A - \phi^*_B$, $n^{-1/3}_{WS\ average}$ the average between $n^{-1/3}_{WS\ A}$ and $n^{-1/3}_{WS\ B}$, and $\Delta n_{WS} = n_{WSA} - n_{WSB}$. This formula bases on the concept of interfaces between neighboring atomic cells and on the fact that energy effects can be related to changes in the nearest-neighbor atomic surrounding. The energy calculations consider the interactions that take place at the interface between dissimilar atoms. Thinking of n_{WS} as the electron density average over the cell boundary, discontinuities in n_{WS} will form when dissimilar cells are brought into contact. Eliminating such discontinuities requires energy, so that a link to interfacial enthalpies can be formulated. $\Delta H^{interface}_{A\ in\ B}$ represents these chemical interactions between A and B, equal for liquid and solid state. Nevertheless, when dealing with chemical reactions, the change in Gibbs free energy ΔG is in general more meaningful than the change in enthalpy:

$$\Delta G = \Delta H - T\Delta S \tag{5.4}$$

where T is the temperature and S the entropy. The ΔH term in Eq. (5.4) includes not only $\Delta H^{interface}_{A\ in\ B}$ but also contributions arising from the mismatch of the lattice parameter or from the phase of the considered elements. Some of these values are tabulated, but others are not experimentally available. These extra contributes have been mostly calculated using the concept of surface energy γ. The surface energy is generally the sum of more terms which split the contributes due, for instance, to the structure or phase of the considered elements, the entropy related with the reaction or the formation of oxide. Its relations to either the interface enthalpy or the entropy term of equation 5.4 are, for instance,

$$\gamma^{entropy}_{<A>-\{B\}} = \frac{T\Delta S_{\{B\}} \cdot C_S}{V^{2/3}_{\{B\}}} \quad \text{and} \tag{5.5}$$

$$\gamma^{interface}_{<A>-<B>} = \frac{\Delta H^{o\ interface}_{A\ in\ B}}{C_0 V^{2/3}_A} \tag{5.6}$$

where $C_S = 5.2 \cdot 10^{-8}$ and $C_0 = 4.5 \cdot 10^8$ ([dB88], eq. 4.27) are constants. As all other constants appearing in the formulas used in this chapter, they are due to the use of the molar volume V_A to the 2/3 instead of the surface area O_A of a mole of atomic cells of the same metal A [dB88]; C_S has been estimated averaging over the ratio $V_A^{2/3}/O_A$ of different elements. The use of the molar volume is preferred, as it is easier to calculate or to find in literature for the materials of interest here. Eq. 5.5 is obtained comparing the ones in [Mie79, Jeu00]. Eq. 5.6 [dB88] is valid only if A and B have identical atomic cell volumes; if not, a mismatch term has to be added. Additional terms are normally obtained without using enthalpy but, as shown in the following calculations, from the surface energy at 0 K or by other considerations.

We used this model for evaluating all the contributes to the Gibbs energy which are present in a sample during the AIC process, considering them separately and again splitting these in different terms. The MAM, in fact, has the big advantage that the interfacial energy between two elements does not substantially differ from the enthalpy of formation of their alloys, allowing the use of scheduled values for pure metals. This has been widely used, for instance, in the calculations of the different surface energies of the Al oxide.

At the end, the values are summed; a negative balance implies that the process can take place spontaneously, while a positive total value would indicate that the process is not favored.

5.5 The Gibbs energy difference

In order to establish if the AIC process is more favorite when an Al oxide interface layer is present or not, or for a particular thickness of the deposited layers, or for a particular type of substrate, we calculate for each sample the Gibbs free energy difference between the layer configuration before and after the AIC process. The use of the MAM model allow us to separately consider the different contributions in each sample: crystallization energy of the Si layer (ΔG_1), energy related to the Al layer (ΔG_2), surface energy (ΔG_3), interface energy between the layers (ΔG_4), and interface energy with the substrate (ΔG_5). Such contributions are then summed up in the from now on so-called total energy difference ΔG. We use ΔG for comparing how favorite is the AIC process in the different layer configurations which characterize the studied samples. The samples for which ΔG has been calculated are shown in Fig. 5.3 and comprehend all the experimental data achieved so far in this work. In this scheme, the upper layer is simplified: it does not show the presence of Si residuals, as they are not determinant to the overall process. In addition to this, it has to be noted that the flat drawn c-Si substrate has been represented in the experiments by Si nanowires. Nevertheless, geometric constraints do not significantly play a role: the calculations, based on the MAM, consider the interactions between neighboring atoms and not the shape of the studied macroscopic object. Although nanowires are often considered to be small, they are still very big compared to the size of the single atoms and their neighbors, as in the MAM model. For this reason, the overall Gibbs energy of the system with a silicon substrate is not influenced by the type of substrate (wafer or Si wire).

This section dedicates a single subsection to every type of sample illustrated in Fig. 5.3. Firstly the results for the oxide-free system are presented (Fig. 5.3a), considering also the contributions due to the glass substrate, thermodynamically considered as amorphous SiO_2 without dopants for simplicity. Then the terms due to the Al oxide interface layer are added (Fig. 5.3b). Subsequently, the Gibbs energy differences of the oxide-free samples on crystalline silicon substrate with and without native silicon oxide are examined (Fig. 5.3c and e). The particular case of very thin layer is also investigated (Fig. 5.3d). At the end, the calculations for the samples with an Al oxide interface layers on SiO_2-free substrates are shown (Fig. 5.3f). The results are compared and summarized in the conclusions of the whole chapter.

In all calculations, again, the $\{\}$ brackets indicate the amorphous phase, the $<>$ the crystalline one. All constants and the values of entropy, of enthalpy and of molar volume used in this chapter for the following calculations are collected in Tab. 5.2.

Finally, it has to be mentioned that similar calculations have been performed by Zhao [Zha04] et al., who calculated the Gibbs energy difference for an oxide-free sample on a glass substrate before and after the AIC process. Zhao's results can not be taken directly, as the considered system

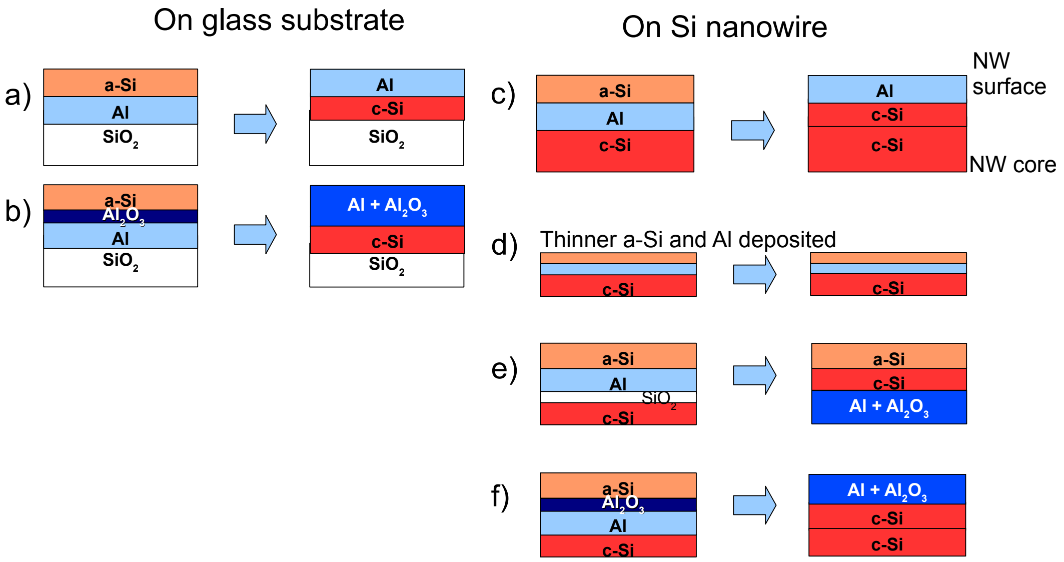


Figure 5.3: *Schematic representation of the cross-section of the different types of sample for which the Gibbs energy balances have been calculated. In each case, the arrow separates the scheme of the sample before (left) and after (right) the process. In the samples on Si, the upper layer forms the sample surface; the lower one corresponds to the NW core.* ***a)****: oxide-free sample on glass.* ***b)****: sample on a glass substrate with an Al oxide layer.* ***c)****: oxide-free system on a monocrystalline Si substrate.* ***d)****: same as c), but with thinner layers.* ***e)****: like c) but with a native silicon oxide layer between the substrate and the Al layer.* ***f)****: like c), but with an aluminium oxide layer between the Al and Si layers. The Al and Si layer thickness is 50 nm, with exception of case c) (see Sect. 5.5.4). The oxide layer thickness is considered to be 3 nm. The layers indicated as* Al_2O_3 *have to be interpreted as explained in section 5.3.*

V_{Si}	1.093	$\cdot 10^{-5}$		V_{Al}	1.101	$\cdot 10^{-5}$	
V_{SiO_2}	2.31	$\cdot 10^{-5}$		$V_{\{Al_2O_3\}}$	3.19	$\cdot 10^{-5}$	[Jeu00]
V_O	1.135	$\cdot 10^{-5}$		C_O	4.5	$\cdot 10^{8}$	[dB88]
C_f	2.5	$\cdot 10^{-9}$	[Mie79]	C_S	5.2	$\cdot 10^{-8}$	
$\Delta H^{int}_{O\ in\ Si}$	-455		[dB88]	$\Delta H^{int}_{O\ in\ Al}$	-558		[dB88]
ΔH^{fuse}_{Si}	50.21		[Sch73]	ΔH^{fuse}_{Al}	10.71		[Zha04]
$\Delta H^{int}_{Al\ in\ Si}$	-9		[dB88]	$\Delta H^{int}_{Si\ in\ Al}$	-9		[dB88]
ΔS_{SiO_2}	-6.46		[Nis]	$\Delta S_{Al_2O_3}$	-28.58		[Cha74, Nis]

Table 5.2: *Table of the values of the molar volumes (in* m^3*/mol), of the enthalpy differences (in kJ/mol), of the entropy differences [in J/(mol K)] and of the constants used for the calculations of this chapter. The constants* C_O*,* C_f *and* C_S *are pure numbers.*

has important differences with the one studied in this work. First of all, Zhao's sample does not present an oxide layer at the interface. Secondly, the process temperature is lower. Thirdly, both Si and Al layers are thicker. For these reasons, Zhao's results have been recalculated with a higher temperature and thinner layers for the oxide-free system (Fig. 5.3a). In addition to this, we also considered samples on a crystalline silicon substrate.

5.5.1 Oxide-free sample on glass (Fig. 5.3a)

This section studies the sample depicted in Fig. 5.3a: Al and a-Si are successively deposited on a glass substrate. No oxide layer is present. During annealing, a complete layer exchange and the Si crystallization take place. The total Gibbs energy difference between the system after and before the AIC process can be split into the following contributions:

$$\Delta G_1 = d_{Si}\, \Delta G_{<Si>-\{Si\}} \tag{5.7}$$

due to the crystallization of the a-Si

$$\Delta G_2 = d_{Al}\, \Delta G_{<Al\ as\ prepared>-<Al\ annealed>} = \Delta G_{2<Al>}^{GG} + \Delta G_{2<Al>}^{SS} \tag{5.8}$$

due to the changes in the Al layer during annealing, where

$\Delta G_2^{GG}$is due to the grain growth and

$\Delta G_2^{SS}$to the strain-stress

$$\Delta G_3 = \gamma_{<Al>} - \gamma_{\{Si\}} \tag{5.9}$$

for the change in surface energy

$$\Delta G_4 = \gamma_{<Al>-<Si>} - \gamma_{<Al>-\{Si\}} \tag{5.10}$$

for the interface energy between the two layers

$$\begin{aligned} \Delta G_5 &= \gamma_{<Si>-\{Glass\}} - \gamma_{<Al>-\{Glass\}} + \Delta G_{glass}^{diff} \approx \\ &\approx \gamma_{<Si>-\{SiO_2\}} - \gamma_{<Al>-\{SiO_2\}} + \Delta G_{glass}^{diff} \end{aligned} \tag{5.11}$$

from the interaction with the substrate, which is due by
the interface energy with the substrate (first two terms) and
the diffusion of oxygen from it (last term)

The first four values of the partial Gibbs energy differences are calculated in [Zha04] using a different temperature and layer thickness than the one in this work. The results, therefore, had to be recalculated for the own samples and are compared in Tab. 5.3. The step-by-step calculations for our samples are reported in Appendix B. The total Gibbs energy difference ΔG is sensitively less negative than the one obtained by Zhao [Zha04]. This is due to the higher process temperature and the thinner Si layer, which drastically influences ΔG_1, and it is not surprising: as explained later in Sect. 5.5.4, a critical layer thickness exists below which the AIC process does not take place. In their paper, Zhao et al. do not show the calculations for ΔG_5, which they affirm to be negligible. Nevertheless, it results that ΔG_5 is actually bigger than $\Delta G_2, \Delta G_3$ and ΔG_4 and it is therefore not negligible. Anyway, being a contribution present for any system with this type of substrate, it is not determinant for the overall process, but for the comparison of the total Gibbs energy difference of the AIC process on different substrates, which is treated in the next sections.

	Zhao* [Zha04]	own samples**
ΔG_1	-125.95	-47.14
ΔG_2	-0.53	-1.01
ΔG_3	0.22	0.13
ΔG_4	0.15	0.18
ΔG_5	n/a	-18.22
ΔG	-126.11	-65.98

* Zhao's samples: layer thickness is 150 nm (Si) and 50 nm (Al), annealing temperature is 523 K.

** Own samples: layer thickness is 50 nm (Si) and 50 nm (Al), annealing temperature is 773 K.

Table 5.3: *The columns collect the values for all contributions to the Gibbs energy difference in a sample during the AIC process. The middle column reports the values obtained by Zhao, the last one the calculated Gibbs energy differences for the own sample. The samples differ only for layer thickness and process temperature. The sample is schematically shown in Fig. 5.3a. All values are in J/m^2.*

The detailed calculations of ΔG_5 are reported in Appendix B, while here we explain the formula we used (Eq. 5.11). The term ΔG^{diff}_{glass} is due to the diffusion of oxygen from the glass substrate into the Al layer. It can be calculated from the reaction which takes place at the interface between Al and glass, which for simplicity is considered as SiO$_2$:

$$3\ \mathrm{SiO_2} + 4\ \mathrm{Al} \rightarrow 3\ \mathrm{Si} + 2\ \mathrm{Al_2O_3} + \ Q \tag{5.12}$$

where $Q = -208$ kJ/mol [Huo06]. Q can be used for calculating the Gibbs energy of formation of Al$_2$O$_3$:

$$\Delta G^{diff}_{glass} \quad = \quad \frac{Q}{V_{SiO_2}} \cdot d = -18.01\ \mathrm{J/m^2} \tag{5.13}$$

where $V_{SiO_2} = 2.31 \cdot 10^{-5}$ m^3/mol is the molar volume of silicon dioxide and d the thickness of the silicon oxide which actually participates to the reaction. Considering that the native Al oxide formed by exposure to oxygen is circa 3 nm, it has been supposed that d is about 2 nm imposing a rough stoichiometric parallelism. Adding the other terms (see App. B), one obtains ΔG_5 = -18.22 J/m^2.

5.5.2 Sample with an Al oxide interface layer on glass (Fig. 5.3b)

The sample considered in this section differs from the previous one for the presence of an Al oxide layer at the interface between the deposited Si and Al layers, as depicted in Fig. 5.3b. After the process, the sample is constituted by a continuous c-Si crystalline layer covered by Si, Al and Al oxide residuals. Compared to the previous case, the contributions ΔG_1, due to the crystallization of Si, and ΔG_5, due to the substrate, do not vary. But the other ones have to be written as:

$$\Delta G_2 = \Delta {G_2}^{SS}_{<Al>} + \Delta {G_2}^{SS}_{<\gamma-Al_2O_3>} + \Delta {G_2}^{form}_{\{Al_2O_3\}} \tag{5.14}$$

as Al oxidizes, its grains do not grow, so that $\Delta G_2^{GG} = 0$ and only its stress-strain term is considered; the terms of the formation and of the stress-strain of the Al oxide are added

$$\Delta G_3 = \gamma_{\{Al_2O_3\}} - \gamma_{\{Si\}} \tag{5.15}$$

$$\Delta G_4 = \gamma_{\{Al_2O_3\}-<Si>} - \gamma_{\{Al_2O_3\}-\{Si\}} - \gamma_{\{Al_2O_3\}-<Al>} \tag{5.16}$$

The calculation of ΔG_2 is now addressed in more detail. The new term $\Delta G_2{}^{SS}_{<\gamma-Al_2O_3>}$ concerning the stress-strain of the Al oxide has been calculated as explained in [Jeu00] and used in Eq. B.7, substituting σ_l with the mismatch factor f:

$$f = \frac{2a_{<Al>}}{a_{<\gamma-Al_2O_3>}} - 1 = 0.03 \tag{5.17}$$

using the constants given in [Jeu00] for calculating $a_{<Al>}$ = 4.11 $\cdot$ 10^{-10} m and $a_{<\gamma-Al_2O_3>}$ = 7.95 $\cdot$ 10^{-10} m, which represent the unstrained lattice spacing of the Al and of the γ-Al_2O_3 unit cells at the process temperature (773 K), respectively. It results $\Delta G_2{}^{SS}_{<\gamma-Al_2O_3>} = 1.06$ J/m^2.

For the contribution due to the oxide formation, it has been assumed that the Al oxide forming during the AIC process and substituting the Al is amorphous, as the new oxide which first forms on the Al substrate is thinner than the critical thickness (see section 5.3). One obtains

$$\Delta G_2{}^{form}_{\{Al_2O_3\}} = \frac{\Delta H^{form}_{Al_2O_3}}{V^{2/3}_{\{Al_2O_3\}}} \cdot d_{\{Al_2O_3\}} = \frac{-335 \text{ kJ/mol} \cdot 3 \cdot 10^{-9} \text{ m}}{4.5 \cdot 10^{-8} \cdot 3.19 \cdot 10^{-5} \text{ m}^3\text{/mol}} = -31.50 \text{ J/m}^2 \tag{5.18}$$

The value of the enthalpy of formation is from [dB88]. The thickness of the native Al oxide formed by oxygen exposure is around 3 nm [Sai02].

The final result for ΔG_2 for a sample with an oxide interface layer on glas substrate is therefore

$$\begin{aligned}\Delta G_2 &= \Delta G_2{}^{SS}_{<Al>} + \Delta G_2{}^{SS}_{<\gamma-Al_2O_3>} + \Delta G_2{}^{form}_{\{Al_2O_3\}} = \\ &= -0.76 \text{ J/m}^2 + 1.06 \text{ J/m}^2 - 31.50 \text{ J/m}^2 = -31.20 \text{ J/m}^2\end{aligned} \tag{5.19}$$

For the value of ΔG_3, the surface energy of the Al oxide has been linearly extrapolated using $\gamma_{\{Al_2O_3\},300\ K} = 0.88$ J/m^2 and $d\gamma/dT = -0.187 \cdot 10^{-3}$ in [Jeu00], obtaining $\gamma_{\{Al_2O_3\},773\ K} = 0.79$ J/m^2. Using the value of $\gamma_{\{Si\}}$ known from Appendix B, one obtains

$$\Delta G_3 = \gamma_{\{Al_2O_3\}} - \gamma_{\{Si\}} = 0.79 \text{ J/m}^2 - 0.89 \text{ J/m}^2 = -0.10 \text{ J/m}^2 \tag{5.20}$$

The calculation of ΔG_4 for the AIC process on glass substrate with an Al oxide interface layer between Al and Si is more challenging. Based on the MAM, the first term of Eq. 5.16 ($\gamma_{\{Al_2O_3\}-<Si>}$) can be calculated as the sum of three different contributions: (i) the one due to the interaction between the different atomic cells, $\gamma^{interface}_{\{Al_2O_3\}-<Si>}$; (ii) the one representing the entropy contribution, $\gamma^{entropy}_{\{Al_2O_3\}-<Si>}$; and (iii) the one which takes in account that at an interface between an amorphous and a crystalline material the atoms of the crystalline phase have a higher enthalpy than the corresponding atoms in the bulk, as the interface itself is no more considered crystalline-crystalline but rather liquid-crystalline [dB88, Jeu00]. This contribution is given by $\gamma^{enthalpy}_{\{Al_2O_3\}-<Si>}$. As suggested in [Jeu00], the interface energy between the metal substrate and the oxide film can be split in two further terms, namely

$$\gamma^{interface}_{\{Al_2O_3\}-<Si>} = \gamma^{interface}_{O-<Si>} + \gamma^{interface}_{<Al>-<Si>} \tag{5.21}$$

This is true also if the oxide is not the own oxide of the substrate. One could object that this formula is not valid for silicon, as it is classically classified as a semiconductor and not as a metal. The MAM, though, considers Si a metallic crystal, pointing out that "the distinction between metallic and covalent binding is sometimes rather artificial" ([dB88], page 15). In this view, the formula (5.21) can be used also for silicon.

All these terms can be calculated using tabulated values of enthalpy and entropy values and the formulas of the MAM (Eq. 5.5 and Eq. 5.6, and also [dB88]). One can write

$$\begin{aligned}\gamma_{\{Al_2O_3\}-<Si>} &= \gamma^{interface}_{O-<Si>} + \gamma^{interface}_{<Al>-<Si>} + \gamma^{entropy}_{\{Al_2O_3\}-<Si>} + \gamma^{enthalpy}_{\{Al_2O_3\}-<Si>} = \\ &= \frac{\Delta H^{o\ interface}_{O\ in\ Si}}{C_0 V_O^{2/3}} + \frac{\Delta H^{o\ interface}_{Al\ in\ Si}}{C_0 V_{Al}^{2/3}} - \frac{C_S \cdot T \Delta S_{\{Al_2O_3\}}}{V_O^{2/3}} + \frac{C_f \cdot \Delta H^{o\ fuse}_{<Si>}}{V_{Si}^{2/3}}\end{aligned}$$

The entropy difference is defined here as $\Delta S_{\{Al_2O_3\}} = S_{<\gamma-Al_2O_3>} - S_{\{Al_2O_3\}} =$ 38.66 J/K mol^{-1} - 67.2 J/K mol^{-1} = -28.58 J/K mol^{-1}. The two values are taken from [Cha74] and [Nis], respectively, while the constant $C_f = 2.5 \cdot 10^{-9}$ is from [Mie79]. It results

$$\begin{aligned}\gamma_{\{Al_2O_3\}-<Si>} &= \frac{1}{4.5 \cdot 10^8}\left(\frac{-455 \text{ kJ/mol}}{(1.135 \cdot 10^{-5} \text{ m}^3\text{/mol})^{2/3}} + \frac{-9 \text{ kJ/mol}}{(1.101 \cdot 10^{-5} \text{ m}^3\text{/mol})^{2/3}}\right) - \\ &\quad - \frac{773\ K \cdot (-28.58 \text{ J/(K mol)}) \cdot 5.2 \cdot 10^{-8}}{(1.135 \cdot 10^{-5} \text{ m}^3\text{/mol})^{2/3}} + \frac{2.5 \cdot 10^{-9} \cdot 50.21 \text{ kJ/mol}}{(1.093 \cdot 10^{-5} \text{ m}^3\text{/mol})^{2/3}} = \\ &= 0.49 \text{ J/m}^2 \end{aligned} \tag{5.22}$$

Similarly it is possible to calculate the last term of Eq. 5.16:

$$\gamma_{\{Al_2O_3\}-<Al>} = \gamma^{interface}_{O-<Al>} + \gamma^{interface}_{<Al>-<Al>} + \gamma^{entropy}_{\{Al_2O_3\}-<Al>} + \gamma^{enthalpy}_{\{Al_2O_3\}-<Al>} \tag{5.23}$$

where the $\gamma^{interface}_{<Al>-<Al>} = 0$, since the enthalpy of 1-mol M atoms in an infinite reservoir of $< M >$ atoms is zero. The result is $\gamma_{\{Al_2O_3\}-<Al>} = 0.13$ J/m^2.

The interface energy between $\{$Al$_2$O$_3\}$ and a-Si, e.g. the second term in Eq. 5.16, is estimated from [Nik94], where the values of the interface energy between $\{$Al$_2$O$_3\}$ and various materials, but not Si, are reported. As such values scatter within 10%, $\gamma_{\{Al_2O_3\}-\{Si\}}$ has been obtained as their arithmetic media at our process temperature. It results $\gamma_{\{Al_2O_3\}-\{Si\}} = 3.43$ J/m^2. Summing the other contributions, $\Delta G_4 = 3.79$ J/m^2.

The total Gibbs energy difference is then -92.87 J/m^2. This result is compared with the ones for the other layer configurations in Tab. 5.4 on page 79.

5.5.3 Oxide-free sample on crystalline silicon (Fig. 5.3c)

The samples on crystalline silicon have been studied after the ones on glass as a further step towards the realization of a nanowire-based solar cell, where the AIC is performed for obtaining a crystalline *p*-layer on *n*-doped Si nanowires. We first consider the samples which do not present any Al oxide interface layer between the Al and the Si layers. The substrate is represented by a monocrystalline Si nanowire grown as described in Chapter 3: by Chemical Vapor Deposition using a gold droplet as a catalyst. The gold has been removed prior to the Al and Si deposition by aqua regia (2 minutes in 1 HNO_3 : 3 HCl).

The only contribution which has to be changed with respect to the oxide-free sample on glass (see section 5.5.1) is the substrate contribution ΔG_5. This can be split in further contributions given by $\gamma^{interface}$, already discussed, and by the terms due to the mismatch between two crystalline phases, $\gamma^{mismatch}$, calculated in Appendix B (Eqs. B.13 and B.15). It results:

$$\begin{aligned} \Delta G_5 &= \gamma_{<Si>-<Si\ wire>} - \gamma_{<Al>-<Si\ wire>} = \\ &= \gamma^{interface}_{<Si>-<Si>} + \gamma^{mismatch}_{<Si>-<Si>} - \gamma^{interface}_{<Si>-<Al>} - \gamma^{mismatch}_{<Si>-<Al>} = \\ &= 0 + 0 - \frac{\Delta H^{interface}_{Al\ in\ Si}}{C_O V_{Al}^{2/3}} - \frac{1}{6}(\gamma_{<Al>} + \gamma_{<Si>}) = \\ &= -0.28 \text{ J/m}^2 \end{aligned} \tag{5.24}$$

The term $\gamma_{<Si>-<Si\ wire>} = 0$ because (i) the enthalpy of 1-mol M atoms in an infinite reservoir of $< M >$ atoms is zero and (ii) there is no mismatch between the Si of the substrate and the newly crystallized Si (epitaxy).

The total Gibbs energy difference for this sample is then -48.04 J/m^2.

Starting from this result, we now consider three main characteristics: (i) the thickness of the deposited layers (see next section); (ii) the presence of a native Si oxide on the substrate (see Sect. 5.5.5); (iii) the presence of the Al oxide layer between the deposited layers (see Sect. 5.5.6). The experimental analysis after the annealing, in fact, showed that the AIC process took place in sample c only if the layers were not too thin, while the presence of a native Si oxide on the Si substrate let Al switch its position with the crystalline NW core and not with the a-Si layer. The following calculations explain both cases: the total Gibbs energy difference approaches or even pass zero when the deposited layers are too thin, while it has a significantly more negative value when native silicon oxide is present.

5.5.4 Thinner oxide-free sample on crystalline silicon (Fig. 5.3d)

It is noteworthy that the sum of all the contributions to the total Gibbs energy in the oxide-free Si/Al system on Si substrate depends on the thickness of the deposited layers and on the temperature T. These are therefore the factors which determine whether the AIC process can take place. In particular, it exists a critical thickness h_{crit} of the Si layer. He et al. [He05a] distinguish between two ways of considering the critical thickness. The first one, h^{cr}_{crit}, represents the thickness of an amorphous Si layer below which it will not crystallize:

$$h^{cr}_{crit} = \frac{2(\gamma_{<Al>-<Si>} - \gamma_{<Al>-\{Si\}})}{-\Delta G_{<Si>-\{Si\}}} \tag{5.25}$$

The second one, h^{int}_{crit}, is the critical thickness which corresponds to the range of Hiraki's screening effect:

$$h^{int}_{crit} = \frac{\gamma_{<Al>-<Si>} + \gamma_{<Si>-\{Si\}} - \gamma_{<Al>-\{Si\}}}{-\Delta G_{<Si>-\{Si\}}} \tag{5.26}$$

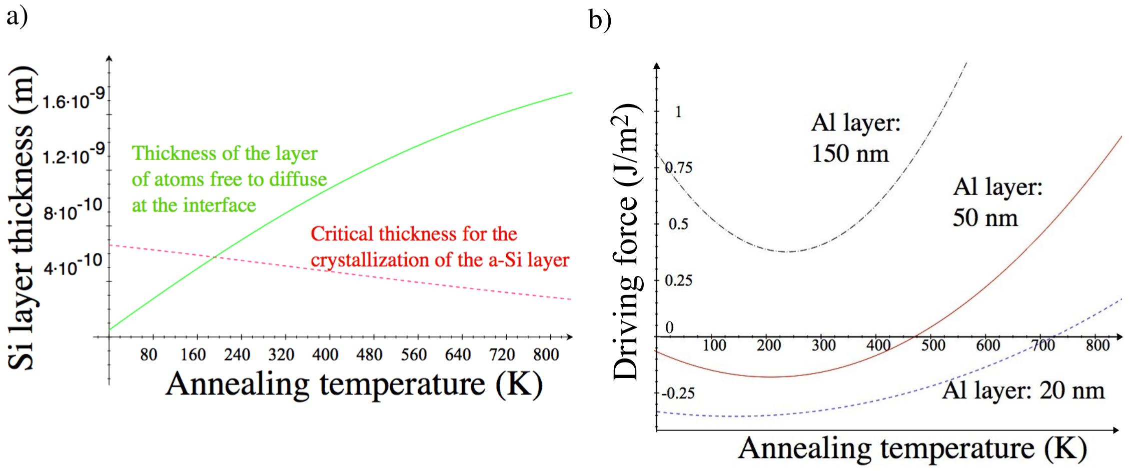


Figure 5.4: ***a)**: Plot of the critical thickness for the crystallization of the a-Si layer (red) and the one at the Al/Si interface (red) as defined in [He05a] as functions of the process temperature. **b)**: Plot of the driving force defined in [He05a] as a function of the temperature for different thickness of the Al layer. The label of the x axis has been shifted to the bottom of the graph for clarity.*

At this interface the screening effect described by Hiraki's model takes place, so that the Si atoms are "free" to diffuse towards and in the Al layer. The screening force should leave this interface amorphous, so that the atoms can diffuse more easily. To sum up, the Si layer must be thicker than both these values.

We show that both ways of calculating the critical thickness depend on the AIC process temperature. As plotted in Fig. 5.4a, h^{cr}_{crit} decreases with increasing temperature, as the crystallization is favored by higher temperature. On the contrary, h^{int}_{crit} increases for higher temperatures, which corresponds to a higher number of free atoms which can diffuse from the amorphous layer at the interface. The range of values for both h^{cr}_{crit} and h^{int}_{crit} which can be read in the plot (Fig. 5.4a) agree with the ones published by [He05a, He06] for some precise temperature and are of the order of magnitude of few monolayers of silicon. A monolayer of (100) Si is circa 1.36 Å [Oh07].

Another important parameter defined by He [He05a] is the so-called driving force, used for quantifying whether the layer exchange process will take place. As the crystallization of silicon (ΔG_1) and the substrate interface energy (ΔG_5) are believed not to contribute to the layer exchange, the driving force is calculated as -($\Delta G_2 + \Delta G_3 + \Delta G_4$). With this definition, which is not dependent on the thickness of the Si layer, a positive driving force allows the layer exchange, a negative one prevents it [He06]. We plotted the resulting dependence on the AIC process temperature in Fig. 5.4b. The values for $d_{Al} = 50$ nm agree with the ones published in [He05a] for 438 K and 523 K, i.e. -0.17 and 0.10 J/m^2, respectively; tiny discrepancies are due to the use of different constants. The graph shows that there is a minimum annealing temperature for the layer exchange to take place only if the Al layer is not very thick (lines for d_{Al} =50 and 20 nm). There exist values for the Al layer thickness for which the driving force is positive for every temperature: this would mean that the layer exchange would always take place, independently of the Si layer thickness (line for d_{Al} =150 nm). This is experimentally not true.

Here, anyway, we are interested in finding the critical thickness for which both the silicon crystallization and the layer exchange process take place. In fact, in this work the expression "AIC process" includes both concomitant mechanisms. Therefore, we define the critical Si layer thickness d_{crit}^{AIC} behind which the AIC process can not take place, which means, either is the layer exchange not complete or some amorphous silicon is still present. For the application which will be shown in the next chapter, in fact, it is crucial that all silicon crystalizes and completely exchanges its position with the Al layer. The AIC critical thickness is then defined as the thickness of the Si layer for which the total Gibbs energy difference is equal to zero:

$$\Delta G(d_{crit,Si}^{AIC}, d_{Al}, T) \quad \overset{!}{=} 0 \qquad \Rightarrow \qquad d_{crit}^{AIC}(T, d_{Al}) \tag{5.27}$$

d_{crit}^{AIC} depends linearly and logarithmically on the temperature and linearly on the thickness of the Al layer. The dependence on the annealing temperature is shown in Fig. 5.5a, where curves for different values of the Al layer thickness are plotted. As expected, the values for d_{crit}^{AIC} are comparable with or higher than the ones for h_{crit}^{int} and h_{crit}^{cr}. The two points of intersection of the three plotted curves are due to the common factor of the crystallization energy and the molar volume of silicon. The other contributions to the total Gibbs energy difference influence the concavity of the curve. In particular, the more influent term is the stress-strain energy in the Al layer, $\Delta G_2{}_{<Al>}^{SS}$, which increases for thicker layers (Eq. B.7). The negative values at higher temperatures are probably due to some inconsistence caused by the fact that no diffusion process is quantified in the formula: with a thick Al layer and a very thin Si layer (few angstroms) it should be considered the diffusion of the Si atoms inside the Al layer and the consequent dissolving of the Si layer, in particular for higher temperature. The dependence at temperatures near 0 K has to be considered with care, as no low-temperature effect of any kind is considered in the calculation. The plots stop at 800 K, just before of the Al/Si eutectic temperature, as a melted or partially-melted system would follow other laws than the AIC process. It is worth mentioning that the thinner plotted layer is very similar to the h_{crit}^{cr} shown in Fig. 5.4a. This is simply related to the fact that for a thin Al layer ΔG_2 decreases and the other terms become more influent, so that the formula resembles the one for h_{crit}^{cr}.

Although it is difficult to experimentally prove the existence of a critical thickness because the deposition and even more the analysis would be particularly challenging, no AIC process was observed for samples annealed with default parameters but presenting thinner layers (10 nm, see figure on page 45). Even if the experimental sample is 10 times thicker than d_{crit}^{AIC}, it can be argued that the process is slowed down and need either longer annealing time or higher process temperature than the default ones. In fact, the total Gibbs energy difference depends on the layer thickness. The value of ΔG can be calculated using Eqs. 5.7 to 5.10 in Sect. 5.5.1 and 5.24 in the previous section for a layer thickness of 10 nm each. As a consequence, the total Gibbs energy difference shifts from the values of -48.04 (layer thickness of 50 nm) to -9.72 J/m^2 (layer thickness of 10 nm; see also Tab. 5.4 on page 79).

More in general, a representation for the dependence of the total Gibbs energy upon the Si layer thickness is given in Fig. 5.5b for a temperature of 773 K. A thinner Si layer results in a smaller absolute value of the Gibbs energy difference, and consequently the AIC process is less favored. The Al thickness has no significant influence in the considered range of values.

We also calculated the dependence of the total Gibbs energy upon temperature. The Gibbs energy does not depend anymore on the process temperature if very thin layers are considered.

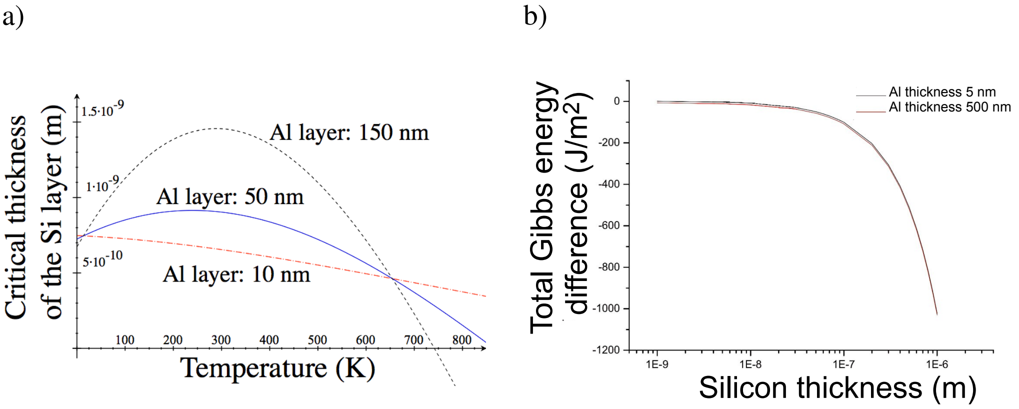


Figure 5.5: ***a)**: Plot of the critical thickness of the Si layer as a function of the AIC process temperature for different values of thickness of the Al layer. It has been calculated considering all contribution to the total Gibbs energy difference. **b)**: Plot of the total Gibbs energy difference for different thickness of the Al layer as a function of the Si layer thickness, calculated for a process temperature of 773 K. The value of the Al layer thickness is not significant in the considered range of values.*

5.5.5 Oxide-free sample on crystalline silicon with native Si oxide (Fig. 5.3e)

Consider now the case depicted in Fig. 5.3e: a layer of Al and a layer of Si with default thickness (50 nm) on a c-Si substrate which presents a thin native oxide layer (5 nm). The experimental results are shown in the TEM and EDX analysis in Fig. 4.7 on page 48: the Al switches its position with the Si nanowire, while the a-Si does neither crystallize nor move. This differs from the expected result, where the c-Si substrate and the Si oxide layer would have not participated to the AIC process, which would have involved only the a-Si and Al layers. The expected result (c-Si substrate / Si oxide / c-Si / Al) would have a total Gibbs energy difference of -65.98 J/m^2, similarly to the case of Fig. 5.3a.

The following calculations show that the contributions due to the thin silicon oxide layer on Si significantly lower the negative value of the total Gibbs energy difference of the system, because of the reduction of Si oxide by Al at the interface. The contributions due to the Si oxide layer are such that overcompensate the contribution related to the Si crystallization, now missing. Therefore, it is energetically more favorable to switch the position between the Al layer and the c-Si substrate instead of crystallizing the a-Si layer by mean of a standard AIC process: as it will be calculated now, ΔG for the observed result is -81.50 J/m^2.

The Gibbs energy difference for the sample represented in Fig. 5.3e is the sum of:

$\Delta G_1 = 0$ as the a-Si does not crystallize

$$\Delta G_2 = \Delta G_{2<Al>}^{SS} + \Delta G_{2\{Al_2O_3\}}^{form} + \Delta G_{2\{SiO_2\}}^{exc} \tag{5.28}$$

where $\Delta G_{2\{SiO_2\}}^{exc} = \dfrac{Q}{C_O V_{SiO_2}} \cdot d$ is the term due to the exchange reaction between SiO$_2$ and Al$_2$O$_3$ already used in Eq. 5.13, now with a different value for the Si oxide thickness

$\Delta G_3 = 0$ as there is no change in surface energy

$$\Delta G_4 = \gamma_{\{Al_2O_3\}-<Si>} - \gamma_{<Al>-\{SiO_2\}} - \gamma_{<Si>-\{SiO_2\}} + \gamma_{\{Si\}-<Si>} - \gamma_{<Al>-\{Si\}} \tag{5.29}$$

where the first three terms represent the interface energy difference at the Si oxide layer and the last two terms the interface energy difference at the a-Si layer

$$\Delta G_5 = \gamma_{<Si>-<Al_2O_3>} - \gamma_{<Al>-<SiO_2>} \tag{5.30}$$

because of the layer exchange with the substrate and not with the deposited a-Si layer

For calculating ΔG_2 we use a thickness d equal to 5 nm, as this is the thickness of the native Si oxide layer. No Si oxide has been detected by EDX in TEM after the process. It results ΔG_2 = -77.51 J/m^2.

Considering ΔG_4, the first term of Eq. 5.29 has already been calculated in Eq. 5.22. For the following terms, with $\Delta S_{\{SiO_2\}}$ = 41.46 J/(mol K) - 47.92 J/(molK) = -6.46 J/(mol K) [Nis], it is valid

$$\begin{aligned}
&\gamma_{<Al>-\{SiO_2\}} + \gamma_{<Si>-\{SiO_2\}} = \\
&= \gamma^{interaction}_{<Al>-\{SiO_2\}} + \gamma^{entropy}_{<Al>-\{SiO_2\}} + \gamma^{enthalpy}_{<Al>-\{SiO_2\}} + \gamma^{interaction}_{<Si>-\{SiO_2\}} + \gamma^{entropy}_{<Si>-\{SiO_2\}} + \\
&+ \gamma^{enthalpy}_{<Si>-\{SiO_2\}} \\
&= \frac{\Delta H^{interface}_{O\ in\ Al}}{C_O V_O^{2/3}} + \frac{\Delta H^{interface}_{Si\ in\ Al}}{C_O V_O^{2/3}} - \frac{T\Delta S_{SiO_2}}{V_O^{2/3}} \cdot C_S + \frac{H^{fuse}_{Al} \cdot C_f}{V_{Al}^{2/3}} + \frac{\Delta H^{interface}_{O\ in\ Si}}{C_O V_O^{2/3}} - \\
&- \frac{T\Delta S_{SiO_2}}{V_O^{2/3}} \cdot C_S + \frac{H^{fuse}_{Si} \cdot C_f}{V_{Si}^{2/3}} = \\
&= -4.1 \text{ J/m}^2
\end{aligned}$$

and

$$\begin{aligned}
&\gamma_{<Si>-\{Si\}} - \gamma_{<Al>-\{Si\}} = \\
&= \gamma^{interaction}_{<Si>-\{Si\}} + \gamma^{entropy}_{<Si>-\{Si\}} + \gamma^{enthalpy}_{<Si>-\{Si\}} + \gamma^{interaction}_{<Al>-\{Si\}} + \gamma^{entropy}_{<Al>-\{Si\}} + \gamma^{enthalpy}_{<Al>-\{Si\}} = \\
&= \frac{\Delta H^{interface}_{Si\ in\ Al}}{C_O V_{Si}^{2/3}} + \frac{H^{fuse}_{Al} \cdot C_f}{V_{Al}^{2/3}} - \frac{H^{fuse}_{Si} \cdot C_f}{V_{Si}^{2/3}} = \\
&= -0.24 \text{ J/m}^2
\end{aligned} \tag{5.31}$$

The total sum for ΔG_4 is then

$$\Delta G_4 = 0.49 \text{ J/m}^2 + 4.1 \text{ J/m}^2 - 0.24\text{J/m}^2 = 4.35 \text{ J/m}^2 \tag{5.32}$$

The contribution of the substrate is given by:

$$\Delta G_5 = \gamma^{interaction}_{<Si>-<\gamma-Al_2O_3>} + \gamma^{mismatch}_{<Si>-<\gamma-Al_2O_3>} - \gamma^{interaction}_{<Si>-\{SiO_2\}} - \gamma^{entropy}_{<Si>-\{SiO_2\}} - \gamma^{enthalpy}_{<Si>-\{SiO_2\}} \tag{5.33}$$

All terms have already been calculated in the previous equations with exception of the second one. The mismatch term between crystalline silicon and $<\gamma - Al_2O_3>$ is calculated using [Zha04]

$$\gamma^{mismatch}_{<Si>-<\gamma-Al_2O_3>} = \frac{1}{6}(\gamma_{<Si>} + \gamma_{<\gamma-Al_2O_3>}) \tag{5.34}$$

but, as no value could be found for $\gamma_{<\gamma-Al_2O_3>}$, we used $\gamma_{<\alpha-Al_2O_3>} \approx 1700$ mJ/m^2 at 773 K [Wei99]. Using the result in B.14, $\gamma^{mismatch}_{<Si>-<\gamma-Al_2O_3>} \approx 0.47$ J/m^2 is obtained.

Summing all terms, the value for ΔG_5 as in Eq. 5.33 is -0.14 J/m^2. The total Gibbs energy difference is then $\Delta G =$ -81.50 J/m^2. Again, for the comparison with the other cases, we refer to Tab. 5.4 on page 79.

5.5.6 With an Al oxide interface layer on oxide-free Si substrate (Fig. 5.3f)

Last but not least, we consider the case of a sample with an Al oxide interface layer between the deposited Al and Si layer. The layers have been deposited on an oxide-free Si nanowire, as depicted in Fig. 5.3f. The result consists in a c-Si layer epitaxially formed on the Si nanowire and covered by residuals of Al and Al oxide, as shown in the TEM and EDX results of Fig. 4.8 on page 48 in the previous chapter. This is the configuration we wanted to obtain and which will be used for the realization of the solar cell in the next chapter.

The equations for the Gibbs energy balance are in this case quite similar to the ones reported for sample b) on page 70, but this time on a silicon substrate:

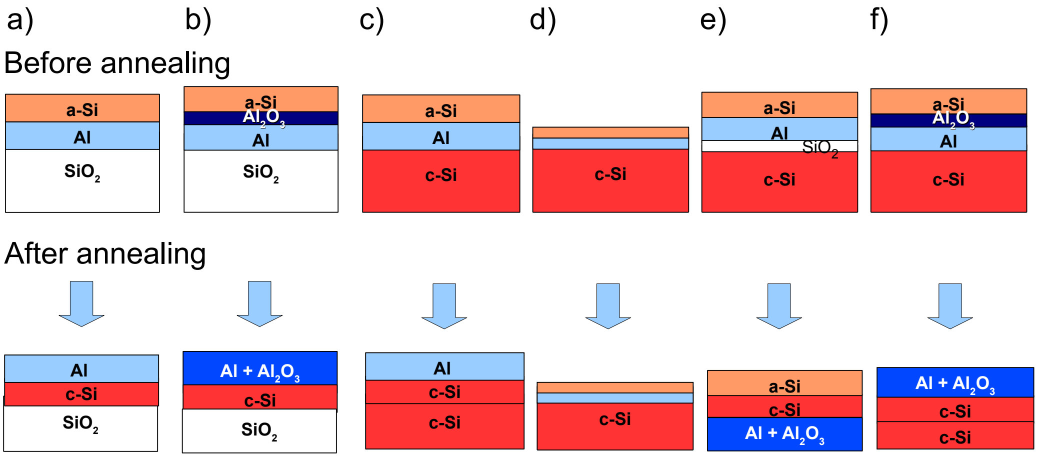
$$\begin{aligned}
\Delta G_1 &= d_{Si}\, \Delta G_{<Si>-\{Si\}} && (5.35)\\
\Delta G_2 &= \Delta G_2^{SS}{}_{Al} + \Delta G2^{SS}_{Al_2O_3} + \Delta G2^{form}_{Al_2O_3} && (5.36)\\
\Delta G_3 &= \gamma_{\{Al_2O_3\}} - \gamma_{\{Si\}} && (5.37)\\
\Delta G_4 &= \gamma_{\{Al_2O_3\}-<Si>} - \gamma_{\{Al_2O_3\}-\{Si\}} - \gamma_{\{Al_2O_3\}-<Al>} && (5.38)\\
\Delta G_5 &= \gamma_{<Si>-<Si\ wire>} - \gamma_{<Al>-<Si\ wire>} && (5.39)
\end{aligned}$$

The total Gibbs energy is ΔG = -74.93 J/m^2.

5.6 Conclusions

In the first part of this chapter a new explanation of the diffusion of Al and Si atoms through the Al oxide interface layer during the AIC process has been suggested: channels can form during the annealing as a result of a phase change of the alumina. In addition to this, the diffusion along these channels could be considered like pipe diffusion and therefore at least two order of magnitude faster than normal diffusion. This would explain why the Al oxide interface layer enhances the diffusion process.

Subsequently, the basics of the macroscopic atom model have been summarized. This model has been used for establishing whether the AIC process is more favorite in presence of the Al oxide interface layer, or it is limited by the layer thickness of the deposited layers, or it depends on the used substrate. We calculated by MAM the difference in the Gibbs energy before and after the AIC process of samples annealed in equal conditions but with dissimilar layer configurations. The results are compared in Tab. 5.4. For the convenience of the reader the schematic representation of all considered layer configurations of Fig. 5.3 is reported again. The system with bigger absolute value of Gibbs energy difference is, for each type of substrate, the one where an Al oxide layer is present (b, f). This is due to the Al oxidation process, whose reaction energy is sensitively more negative than the other contributions. As a consequence, the AIC process is more favorable and it



		on glass		on Si substrate			
		a)	b)	c)	d)	e)	f)
ΔG_1	Si crystallization	-47.14	-47.14	-47.14	-9.43	0	-47.14
ΔG_2	Al characteristics and oxidation	-1.01	-31.20	-1.01	-0.4	-77.51	-31.20
ΔG_3	surface energy	0.13	-0.10	0.13	0.13	0	-0.10
ΔG_4	interface energy	0.26	3.79	0.26	0.26	4.35	3.79
ΔG_5	substrate contribution	-18.22	-18.22	-0.28	-0.28	-0.14	-0.28
ΔG	sum	-65.98	-92.87	-48.04	-9.72	-81.50	-74.93

Table 5.4: *This table collects the values of the total Gibbs energy difference before and after the AIC process for the different types of sample shown above it and calculated in this chapter. All values are in J/m*^{2}.

needs less time for being completed, if the other parameters are kept constant. The oxygen driving this process might be supplied by the substrate or by a leak in the oven; it is noteworthy that even a tiny amount of oxygen cause the oxidation to take place. The substrate can supply oxygen by diffusion (on a glass substrate) and by exchange reaction (with native Si oxide on c-Si substrate). Except for this reason, the substrate has a relatively small influence on the value of ΔG. The case of a thin SiO_2 layer on a c-Si substrate (e) is interesting, as the oxide favors the exchange process of Al with the c-Si core instead than as expected with the a-Si. The thickness of the deposited layers is crucial when it is in the range of few angstroms. The absolute value of ΔG becomes smaller for thinner layers (case d and Fig. 5.5b), while losing its dependence on temperature. This agrees with the experimental data: no AIC process could be observed for deposited layers as thin as 10 nm (Fig. 4.4). For thicker layers, the total Gibbs energy difference strongly depends on the Si layer thickness, while the Al layer thickness is not significant in the studied range.

It has been demonstrated that the AIC process is predictable by mean of thermodynamical calculations. The understanding of the influent process parameters on the final layer configuration has been used for achieving a *p*-doped crystalline Si layer on Si nanowires used as a substrate if the layers are not too thin, if the Si nanowire does not present any native oxide, and if an Al oxide interface is present between the deposited layers. This procedure will be used in the next chapter for the realization of a nanowire-based solar cell.

Chapter 6

A nanowire-based solar cell *p*-doped by Al-induced crystallization

This chapter describes the realization of a nanowire-based solar cell prototype where the Al-induced crystallization (AIC) process plays a crucial role. The advantages deriving from the use of the AIC process for the realization of the *p*-doped region are shown in comparison with the state of the art of similar devices and summarized in the next section. After introducing the basic theory and the main parameters of a solar cell, the particular case of a nanowire-based solar cell is considered. In the subsequent section, the experimental realization of our prototype is described. Successively, the results are presented and discussed. Finally, some suggestions and insight in possible future work are offered.

6.1 State of the art in solar cell technology

The solar cell is a device which converts radiation to electrical power. As shown in Fig. 6.1, the interest towards solar cell technology by important companies and research institutes started in the '70s after some first trials back in the previous century and the first high-efficiency solar cell by Chapin, Fuller, and Pearson in 1954 [Cha54]. Research was predominantly driven by either increasing the solar cell efficiency or by reducing production costs, for instance by using cheaper materials. These two often times competing goals divided solar cells in two categories.

High-efficiency solar cells are generally characterized by the use of particular geometries and material combinations (e.g. InGaAs, InP). Their most common representation includes two or more subcells connected in series by tunnel junctions, so that ideally the whole sunlight spectrum can be captured efficiently. Nevertheless, the use of some expensive materials and the multistep procedure for the realization of the devices make high-efficiency solar cells not affordable on the large scale. To date, the primary application for high-efficiency solar cell is on space satellites.

There are different possibilities for decreasing the production costs. The use of cheaper materials, for instance polycrystalline Si instead of single crystalline wafers, is often combined with the use of inexpensive substrates [Ber99]. In this way, the amount of active material used for the realization of the device can be reduced without severely affecting the efficiency of the solar cell; the classical example is the thin-film technology, where layers of a-Si are deposited on glass or foil [Cho04]. Attention has been paid also to the costs related to the production of the device,

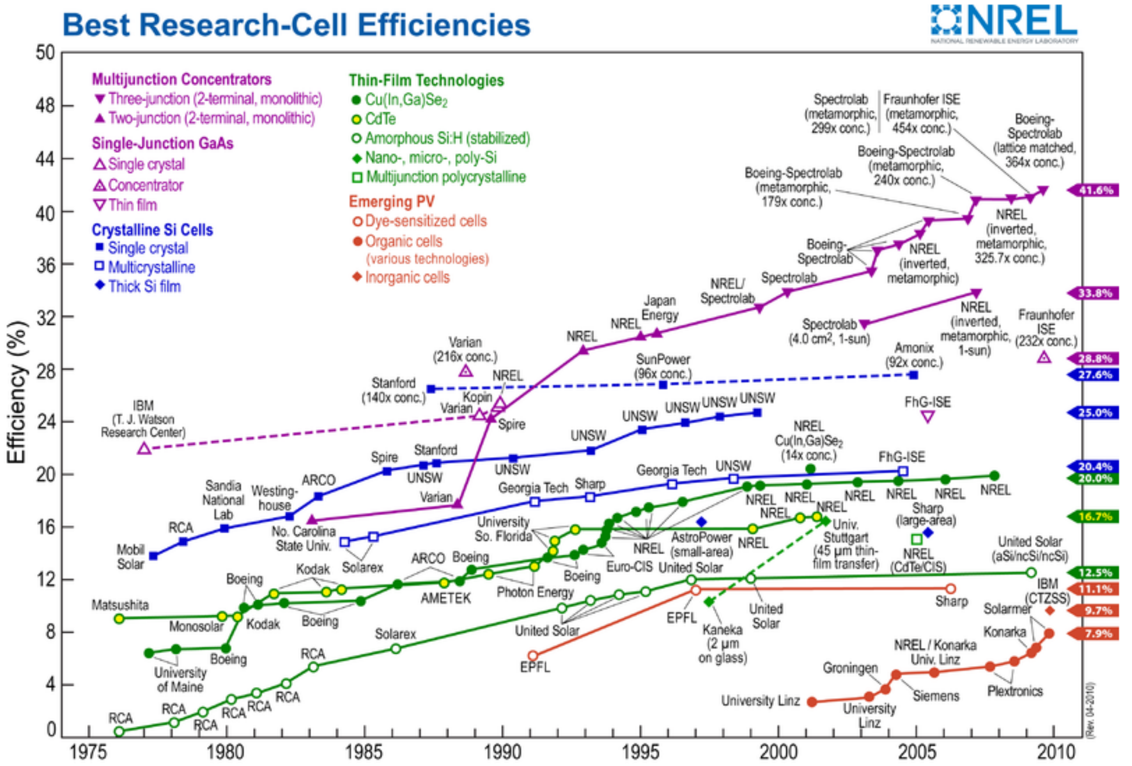


Figure 6.1: *Improvement of the solar cell efficiency in time. Note the spread of cell efficiencies, depending on the material and configuration used. Reproduced with permission (PD-USGov-DOE) from www.nrel.gov; by L. Kazmerski.*

where some attempts are in progress to substitute expensive high temperature processes or high-vacuum technologies. In this context also the low-temperature crystallization of silicon induced by aluminium is an option.

Recently, new geometries for solar cells have been proposed which include the use of nanostructures: for instance, mesoporous films for photoelectrochemical cells [Grä01], nanoparticles for exciton [Gre03] and organic solar cells [Jør08], up to the nanowire-quantum-dot solar cell [Les09] based on ZnO nanowire arrays. In addition to these possibilities, silicon nanostructures have been investigated as well, advantaged by a solid technological background developed for classical solar cells around this Earth-abundant material. In particular, Si nanowires (Si NWs) are a promising candidate for applications in the photovoltaics. Calculations show that they can reach efficiencies of 13% [Kay05]. The high aspect-ratio which characterizes nanowires is thought to improve the cell performances (see Sect. 6.2.3) [Kay05, Tha08]. In addition to this, single nanowires can be integrated in nanoelectronics as photovoltaic power elements [Tia07], or used as a single-nanowire solar cell [Kel08], while large scale applications can profit of Si NW arrays grown on different substrates like e.g. metal foil [Tsa07], ITO-covered glass [Yu10], glass [Siv09a], or crystallized silicon [Ste08]. Also the use of nanoparticles along the nanowires has been reported to increase the photovoltaic efficiency [Pen09].

Although many nanowire-based solar cells have been proposed, some problems affecting the solar cell performances have not been entirely solved yet. A first problem can arise when the

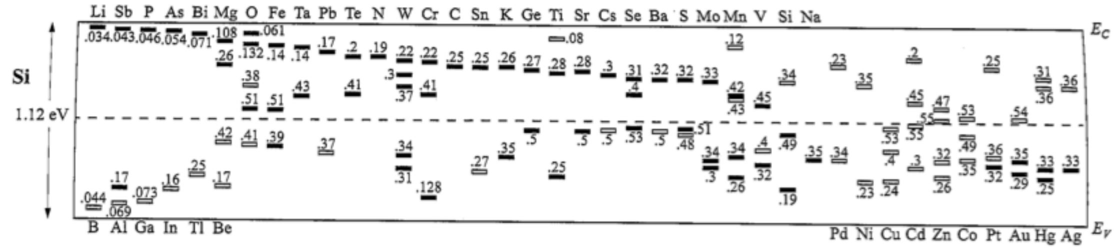


Figure 6.2: *Measured ionization energies for different impurities in silicon. Level below the gap center are measured from the valence band E_v, level above the gap center from the conduction band E_c. Solid and hollow bars represent donor and acceptor levels, respectively. Reproduced with permission from [Sze06]*

nanowires have been synthesized by VLS mechanism using a catalyst which diffuses into the silicon during growth. Therein, it forms trap states for charge carriers. This problem is well known for gold. Searching for the best catalyst in view of solar cell applications, one criterion is the location of the ionization energies for the catalyst material in silicon. If these energy levels are near to the center of the silicon energy gap, it is more probable that the material will act as a recombination center for the charge carriers (see Fig. 6.2). Additionally, other factors influence how deteriorative the impurities of a particular material are for the final performance of the solar cell. The model suggested by Hopkins and Rohatgi [Hop86] relates the final efficiency of the solar cell to the impurity content. Fitting the experimental data, one can obtain a “degradation threshold” parameter [Hop86] which characterizes how severely a material might affect the Si solar cell performance. The values are shown in Fig. 6.3. Based on this, gold should be substituted

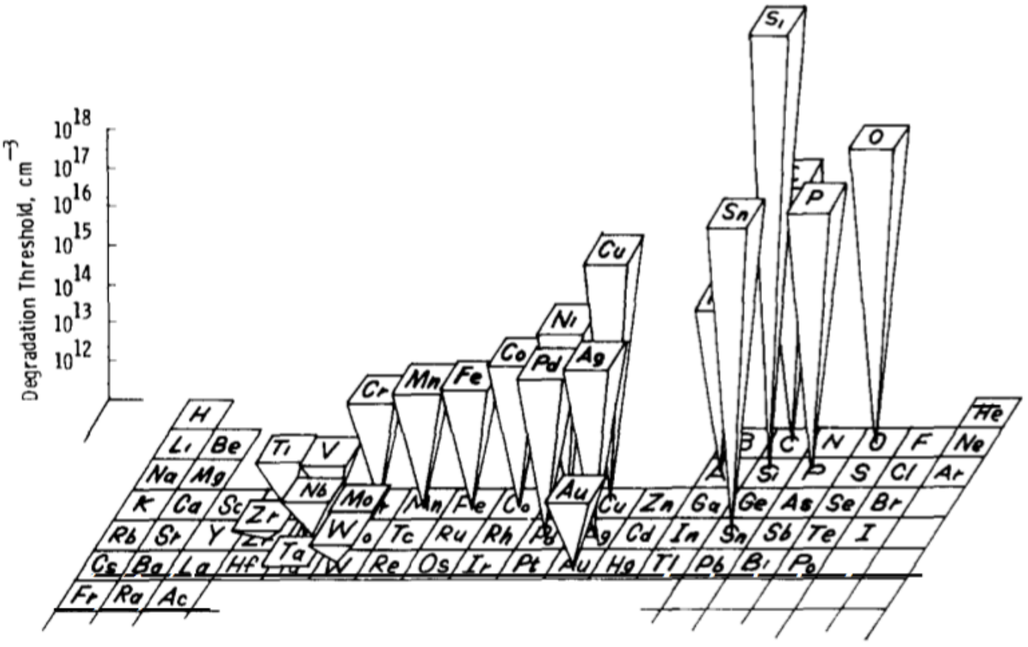


Figure 6.3: *The parameter quantifying the degradation threshold of different materials as an impurity in silicon for photovoltaics applications. Above the threshold density, the solar cell is significantly affected by the impurities in its performances. From [Hop86]*

by, e.g., Al or, better, Cu or Sn. The growth of Al-catalyzed Si NWs has already been reported [Wan06], but to date it has not been implemented towards photovoltaic applications. Nevertheless, the use of Ni [Kel08], In [Kay06], Sn [Jeo09] and Cu [Kay07] explicitly for solar cell applications has been published. Obviously, using nanowires produced by methods not requiring a catalyst material is an alternative. In particular, the use of etched silicon nanowires [Siv09a] has been tested, although in the first experiments severe shunting and high series resistance were observed which affected the solar cell performances.

A further problem for NW-based solar cells might be caused by the mechanism for doping the nanowires. A dopant is a material which acts as a donor or acceptor of charge carriers when inserted in another material, e.g. silicon. The common solar cell works based on both types of doping, *p*-type (with acceptors) and *n*-type (with donors). The doping must be well-defined and achieved with high spatial resolution without affecting the crystalline quality of the material. In addition to this, for large-scale production the doping density must be reproducible. These requirements are problematic at the nanoscale from both a physical and technological point of view. Physically, the electrical properties of nanowires are not solely determined by the concentration of the dopant material, but also by the nanowire diameter, possible surface effects and the mobility of the carriers, which can differ from the one of the bulk material (see page 96) [Sch10]. Technologically, it is not trivial to achieve a well-defined doping of such nanostructures. Some of the procedures reported in literature for the doping of silicon nanowires are listed in the next paragraphs, pointing out their advantages and drawbacks.

Some techniques are based on melting a dopant metal in contact with the Si nanowire [Kel08]. Despite the advantage of realizing at the same time a low ohmic contact, the drawback is that no control of the doping density of the silicon can be achieved. Though, the ohmic contact is a great advantage for the solar cell realization, as it will not add a significant parasitic impedance to the structure on which it is used and will not sufficiently change the equilibrium carrier densities within the semiconductor, by this affecting the device characteristics [Sze69a].

Another doping procedure for VLS-grown wires relies on adding a dopant precursors during the growth process. In some cases [Tia07, Zhe04] one dopant precursor is supplied during the NW growth; the other doped region is achieved by depositing a layer on the grown nanowire. The problems of this procedure can arise from the interface between the *n* and *p* doped regions, as well as from the crystalline quality of the deposited layer. Alternatively [Ste08], two different precursors in two different steps may be used in order to achieve a *p*-*n* junction. By this method one can achieve different doping densities dependent on the amount of dopant precursor introduced into the chamber. The main problem in this case is that the obtained junction is probably not sharp, both because of diffusion of the dopant through the growing nanowires and because of possible residuals of the first dopant gas in the chamber when the second is introduced. Some reports also showed that the dopant gas precursors might negatively influence the growth of the nanowires, sometimes adding crystalline defects and kinks [Pan05, Sch08]. A tedious aspect of this procedure is the calibration, as the values can strongly differ (e.g. for diborane [Sch10]) subject to process conditions.

As a final mentioned example, nanowires obtained by chemical etching of Si could be doped when differently doped layers of multicrystalline silicon are used as a starting material. The layers have the desired doping and an axial *p*-*n* junction can be obtained [Siv09a]. In this case, the problems might be related to the quality of the interface between the deposited layers, which

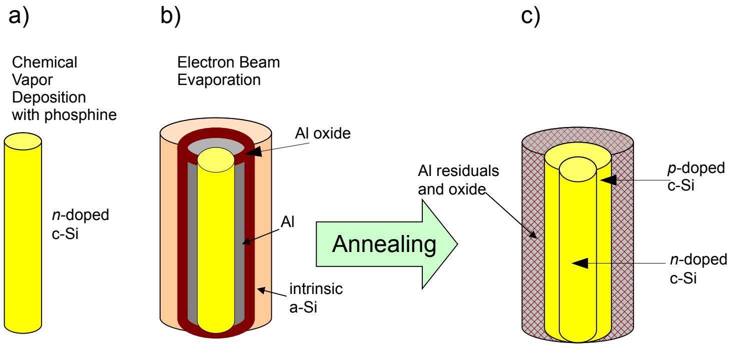


Figure 6.4: *Schematic representation of the realization of the radial p-n junction in each nanowire forming the studied NW-based solar cell.* ***a)****: growth by CVD with phosphine of a monocrystalline n-Si nanowire.* ***b)****: Electron Beam Evaporation on the wire of a layer of Al and one of intrinsic a-Si.* ***c)****: during AIC process, the a-Si layer crystallizes and becomes p-doped. The n-Si wire is surrounded by an epitaxial crystalline p-doped layer. See also the TEM image on page 48.*

then also decreases the crystalline quality of the etched nanowires and therefore the solar cell performances. Moreover, an axial *p-n* junction gives a lower solar cell efficiency than a radial one, as its absorbing region is smaller.

We have realized the solar cells studied in this chapter by doping the *p* and *n* regions in two steps and by different procedures. The *n*-doping has been achieved using a gas precursor (phosphine) during the growth process, leading to *n*-doped monocrystalline Si NWs (Fig. 6.4a). Subsequently, a layer of Al and one of Si have been deposited on the wires (Fig. 6.4b). The samples have been annealed so that the Al-induced crystallization of Si could take place. In particular, while the Si layer switches its position and crystallizes, it grows epitaxially on the substrate, i.e. the monocrystalline wire, and becomes *p*-doped, because of the diffusion of Al during the exchange process (Fig. 6.4c). After the etching of the external layer containing Al and Si residuals, a radial *p-n* junction is obtained for each wire, formed by a monocrystalline as-grown *n*-doped Si core surrounded by a *p*-doped epitaxial Si layer. Differently from other doping methods, the epitaxy has the advantage of not adding defects at the interface between the *n* and *p* region.

The results and the peculiarities of the solar cell formed by arrays of nanowires with radial and epitaxial *p-n* junction are described in the next sections after an introduction about the principle of the planar solar cell and the nanowire-based solar cell.

6.2 A solar cell: theoretical description

As already mentioned, the solar cell converts radiation to electrical power. The active part is the so-called *p-n* junction, where a semiconductor with excess of free positive charge carriers (“holes”, *p*-type semiconductor) is in contact with one characterized by an excess of free negative charge carriers (“electrons”, *n*-type semiconductor). Before summarizing the main characteristics of a solar cell, the *p-n* junction shall be briefly explained.

6.2.1 The *p-n* junction

At thermal equilibrium (Fig. 6.5) the juxtaposition of the p-doped region and the n-doped region changes the potential at the interface: charge carriers diffuse from one side to the other, leaving behind fixed ions. In this way, a space charge region or depletion region is formed, characterized by a local net charge due to the ionized dopants. Simultaneously to the formation of the space charge region a potential V_{bi}, the so-called built-in potential, builds up across the depletion region. The value of V_{bi} depends on the p and n doping levels and mainly determines the open circuit voltage of a solar cell, V_{oc} [Cap10].

Applying a voltage V across the p-n junction in reverse bias (that is, applying on the n region a positive voltage with respect to the p region), the total potential variation across the junction becomes $(V_{bi} + V)$ [Sze69b]. One can calculate the current-voltage characteristics of an ideal p-n junction by assuming valid (i) the abrupt depletion-layer approximation (the depletion region around the junction and the transition between the depleted and the adjacent quasi-neutral region have well-defined edges); (ii) the Boltzmann approximation (the Fermi level is several kT below the energy of the conduction band in nondegenerate semiconductors); and (iii) the low-injection assumption (the minority carrier density is small compared to the majority carrier density). In addition, (iv) the electron and hole currents are assumed constant through the depletion layer. After some calculations [Sze69b], one obtains the Shockley equation, the current voltage characteristic of an ideal diode:

$$\begin{aligned} J &= J_s(e^{qV/kT} - 1) \qquad \text{where} && (6.1) \\ J_s &\equiv \frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{po}}{L_n} && (6.2) \end{aligned}$$

and q is the electron or hole elementary charge, V the applied voltage, k the Boltzmann constant, T the measurement temperature, D_n and D_p the corresponding minority carrier diffusion constants, p_{no} the majority carrier density at thermal equilibrium, n_{po} the minority carrier density at thermal

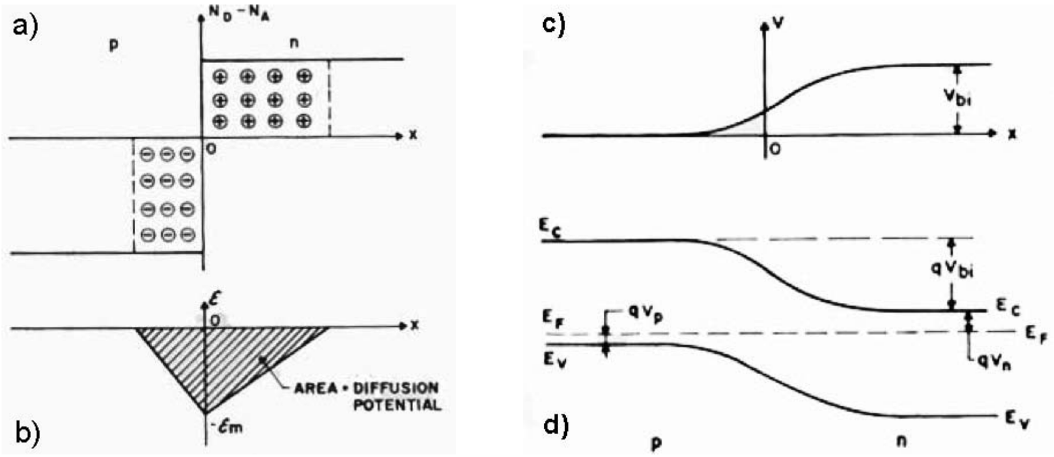


Figure 6.5: *Schematic representation of the dopant density (a), the electric field (b), the voltage (c) and the band structure (d) at the interface between a p- and an n-doped regions at thermal equilibrium. Reproduced with permission from [Sze69b].*

equilibrium, and L_n and L_p the diffusion length of the corresponding minority charge carrier.

The Shockley equation can only give a qualitative indication of the current-voltage characteristics of a silicon *p-n* junction, as it does not take in account surface effects, generation and recombination of carriers in the depletion layer, and series resistance effects [Sze69b], which might significantly affect the experimental IV-curves. If these effects are not negligible, the I-V curves can not be adequately predicted by this equation and the two-diode model might be used.

6.2.2 A solar cell

Basically, a solar cell is represented by a *p-n* junction with a large surface area and low ohmic contacts on the *p*- and on the *n*-type region. The simplest equivalent circuit of the solar cell might be represented by an ideal diode with a constant-current source in parallel with the junction. The current-voltage characteristics are similar to the Shockley equation:

$$J = J_s(e^{qV/nkT} - 1) - J_L \qquad \text{where} \tag{6.3}$$

$$J_s = qn_i^2\left[\frac{1}{N_A}\left(\frac{D_n}{\tau_n}\right)^{1/2} + \frac{1}{N_D}\left(\frac{D_p}{\tau_p}\right)^{1/2}\right] \tag{6.4}$$

with n_i indicating the Si intrinsic density, N_A (N_D) the acceptor (donor) impurity density, and τ the corresponding carrier lifetime. The new term J_L represents the strength of the constant current source due to the incident light. The I-V characteristics for $I_L = 0$, i.e. the dark I-V curves, are the characteristics of a diode, already discussed for the basic *p-n* junction. J_s is the so-called saturation current. The ideality factor *n* is equal to 1 in the ideal case of Shockley's theory. For real solar cells, *n* normally assumes values between 1 and 2 depending on the amount of defects and impurities. It approaches two for high doping levels [Jai05].

Eq. 6.3, plotted in Fig. 6.6a, also introduces other important parameters of a solar cell: the short-circuit current I_{sc} and the open-circuit voltage V_{oc}. One can also define the current and the voltage for the maximum power output, I_{mp} and V_{mp}, respectively, given by the maximum rectangle fitting within the axes and the current-voltage characteristic of the forth quadrant (negative current, positive voltage), as represented in Fig. 6.6a. The solar cell efficiency η is then given by

$$\eta = \frac{P_{max}}{P_{in}} = \frac{I_{mp} \cdot V_{mp}}{E \cdot A} \tag{6.5}$$

where P_{max} is the maximum power output and P_{in} is the solar power input, taken equal to the product of the solar power irradiance $E = 0.1$ W/cm^2 with the solar cell surface A.

Various phenomena can influence the shape of the I-V curves, as already mentioned for the characteristics of a *p-n* junction in the previous section, for instance if charges recombine in the depletion region, causing a decrease of the device efficiency. The main problem associated with the recombination rate and the presence of defects or trap states is the shortening of the diffusion length of the charge carriers. In particular, the majority carriers can recombine with the minority carriers without contributing to the outcoming current, or can be trapped by the defects. A possible solution to this issue can be represented by the use of high quality material, but this implies much higher costs. Alternatively, new solar cell geometries can be tested (see next section).

These problems can significantly affect the IV-curves, although until now only the ideal case

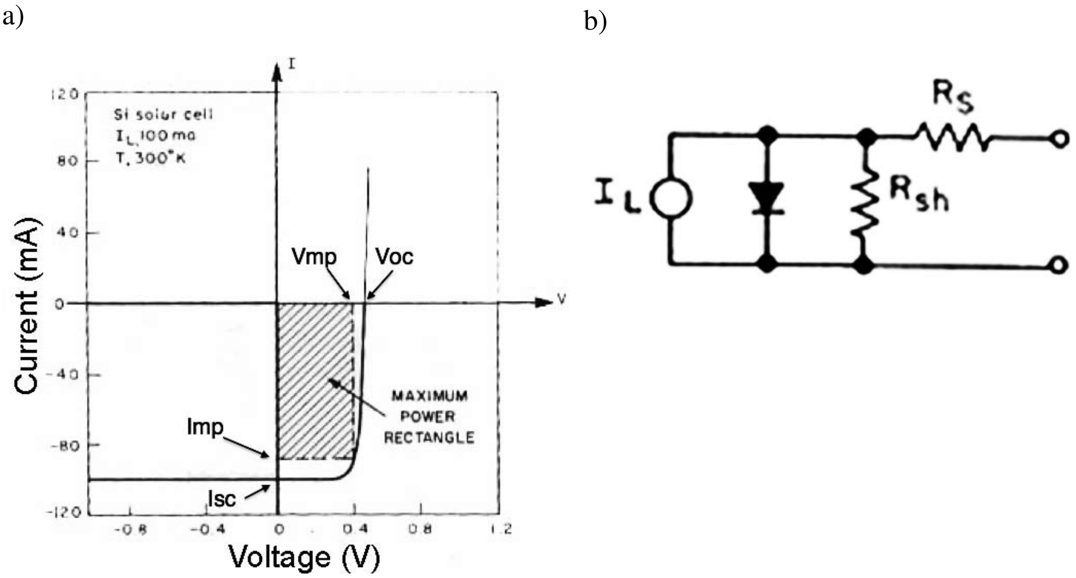


Figure 6.6: ***a)**: Plot of Eq. 6.3, representing the IV-characteristic of an ideal solar cell. The typical solar cell parameters I_{sc}, I_{mp}, V_{oc}, and V_{mp} are indicated. **b)**: Equivalent circuit of a non-ideal solar cell. Both images reproduced with permission from [Sze69c].*

is considered. In real solar cells additional factors can worsen the photovoltaic performances. Let us now consider the non-ideal case. The equivalent circuit of a real solar cell is composed by the diode and the current source plus a series resistance R_s and a shunt resistance R_{sh}, as shown in Fig. 6.6b [Sze69c]. The resistances change the I-V equation, which is now given by

$$\ln\left(\frac{I+I_L}{I_s} - \frac{V-IR_s}{I_sR_{sh}} + 1\right) = \frac{q}{kT}(V - IR_s) \tag{6.6}$$

where I_L is the photogenerated current or, in the equivalent circuit, the strength of the constant current source due to the incident light. The ideal case is obtained for an infinite R_{sh} (so that the current can not flow through an alternative path) and $R_s = 0\ \Omega$, so that no further drop in the voltage is due to the presence of the load. In practice, the series resistance is crucial for the value of the extractable power and the efficiency of the solar cell (Fig. 6.7a): already for $R_s = 5\ \Omega$ the available power is reduced to less than 30% of the corresponding power with $R_s = 0\ \Omega$. On the contrary, the influence of the shunt resistance is less dramatic and no significant changes can be noted in the I-V curves, unless R_{sh} assumes values lower than approximately 100 Ω (Fig. 6.7b). In fact, for very low values of R_{sh} the characteristics of the solar cell approaches a linear behavior. The fill factor and consequently the efficiency are affected in both cases.

6.2.3 A nanowire-based solar cell

The nanowire-based solar cell is characterized by a new geometry compared to the classical planar solar cell: the *p-n* junction, normally situated within a layer of active material, is now inside or along nanowire structures, repeated in an array. The *p-n* junction can extend either radially or axially within the nanowire. Here, the radial *p-n* junction is considered.

This new geometry aims to offer a solution to the problem of the low diffusion length of

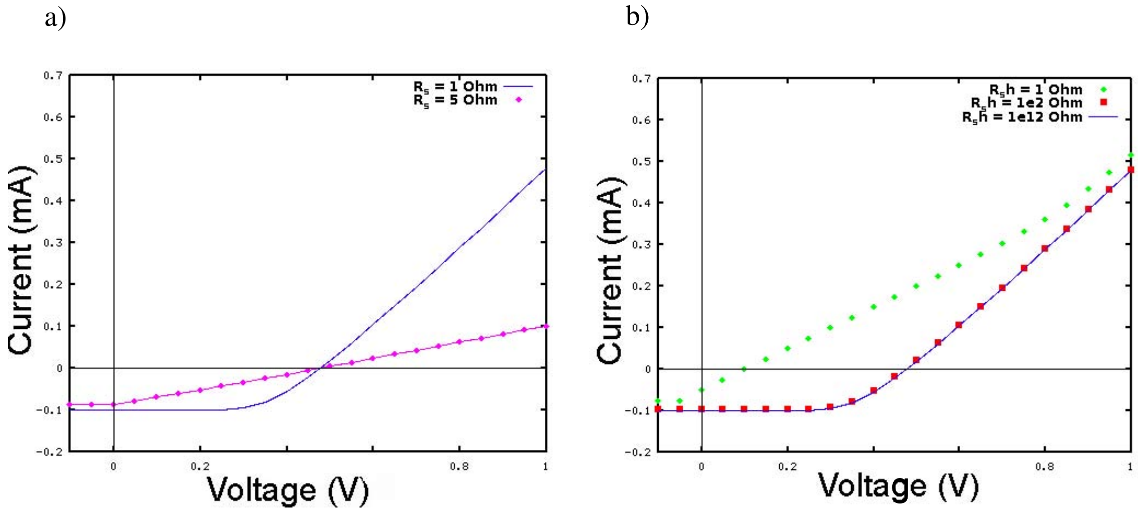


Figure 6.7: *Plot of Eq. 6.6 for different values of the series (a) and shunt resistance (b), indicated in the graphs. The black plain curve is the same in both graphs with $R_s = 1\ \Omega$ and $R_{sh} = 10^{12}\ \Omega$. The other values are $I_L = 0.1$ A and $I_s = 10^{-9}$ A, taken from [Sze69c]. The calculations have been performed by an Octave program written by the author and her colleague G. Brönstrup.*

majority charge carriers, “decoupling the requirements for light absorption and carrier extraction into orthogonal spatial directions” [Kay05]. In fact, on one hand, light absorption is optimized, with the *p-n* junction along the direction of the incident light. On the other hand, the nanowires are thin enough for allowing effective carrier collection even for short diffusion length.

Kayes et al. showed [Kay05] that the nanowire-based solar cell can have a high efficiency despite a significant trap density outside the depletion region, provided that in the depletion region the trap density is relatively low. This is new compared to the planar geometry, where the traps outside the depletion region cause a low I_{sc}. They also showed that an optimal radius and length for the nanowires exist for which the best solar cell performance can be obtained, as the nanowire radius has to be comparable to the minority carrier diffusion length. In addition to this, longer nanowires favor I_{sc} but decrease V_{oc}, so that the optimal nanowire length has to be calculated for the specific case. Regarding the doping, higher doping levels give a higher efficiency, as they increase the built-in voltage. But higher doping levels might also mean lower charge carrier mobility and a thinner depletion region. This possible drawback can be solved, again, by a low trap density in the space charge region.

Another important advantage of the nanowire-based solar cell is given by its spectral response. The spectral response of a solar cell is defined as the plot of the short-circuit current as a function of the wavelength of the incident light [Sze69c]. There are numerous recent publications which compare the absorption, transmission, or spectral response of silicon nanowires with the ones of plain silicon [Zhu09, Gar10, Zhu10]. Additionally to the higher spectral absorption of the Si NWs, the absorption of various types of nanowires has been reported [Str08, Yu10, Kel10], as well as the comparison with different nanostructures (nanoporous Si, [Xio10]; Si nanocones, [Zhu09].

As already mentioned, different procedures for obtaining radial *p-n* junctions in nanowires have been published. Nevertheless, to the best of the author’s knowledge, no reports are available regarding the use of the Al-induced crystallization of silicon on nanowires for obtaining the *p*-

doped region. This procedure has been investigated with regard to a planar geometry [Nas01], though without realizing a prototype, and never for a nanowire-based solar cell. In addition to this, it is worth to mention that Huang et al. patented this procedure on ITO-covered glass substrate [Hua10]. This means that, although further studies and device optimization are needed, the AIC process is generally believed to play an important role in the future solar cell technology.

6.3 Description of the studied nanowire-based solar cell

The nanowire-based solar cell presented in this work is particular because the AIC process is used for growing an epitaxial *p*-doped layer on the *n*-doped substrate, i.e. the nanowires.

The samples considered here are based on an *n*-doped Si nanowire carpet, which we grow as explained in Chapter 3 on *n*-doped Si wafer. The nanowires, which are monocrystalline, are used as a substrate for the AIC process, similarly to the case f) shown in the calculations of Chapter 5. The optimized AIC process allows to obtain an epitaxial *p*-doped Si layer all around each nanowire. The *p*-*n* junction key-element of the solar cell is therefore given by the *n*-doped monocrystalline core (the grown nanowires) and the *p*-doped Si layer obtained by AIC process. The so-grown *p*-Si and the back of the wafer are then contacted for the measurement of the I-V curves. The whole process is described in detail in the next section.

One of the challenges regarding this geometry is to obtain low ohmic contacts to the *p*-doped nanowire shells. The ideal solution would be the use of a *p*-doped transparent conductive oxide (TCO) with high adhesion to silicon. So far three TCOs have been tested [Bey07]: indium-tin oxide (ITO), tin oxide (SnO_2), and zinc oxide (ZnO). ITO is very expensive because of the continuously increasing price of indium, so that research is recently focusing more on alternatives. High *n*-type conductivities can be achieved by doping of both ZnO and SnO_2 films [Bey07]. *n*-doping of ZnO films can be achieved using aluminium [Min84, Min85], which acts as a donors in ZnO. It has also been tentatively studied how to achieve *p*-doped ZnO using doping materials like P, As, Sb, Li, Na, Cu and others or by hydrogenation [Mon09]. The hydrogenation is a reducing chemical process where hydrogen atoms join a molecule of another material. In the case of ZnO, a hydrogenation step might crucially change its properties: hydrogen normally acts as shallow donor in ZnO either in the form of an isolated proton or of an O-H group [Mon09]. But in *p*-type ZnO hydrogen tends to electrically passivate defects or acceptors having dangling bonds rather than compensating them forming a hydrogen donor. Nevertheless, hydrogenated aluminium-doped ZnO (AZO) has been used for contacting *p*-doped silicon in solar cells: Tark et al. [Tar09] contacted the *p*-doped side of microcrystalline Si solar cells with hydrogenated AZO obtaining an efficiency of over 7%.

In our case, the IV-curves of the solar cell studied in this chapter contacted on the *p*-Si with AZO showed a non-interpretable behavior. Therefore the use of AZO as a contacting material was discarded. Lacking feasible alternatives, we used as a contact for the *p* side a drop of InGa paste. This is definitely not an ideal solution, although reported in literature [Kay08]. A part from the issues of control, reproducibility and large-scale implementation of this procedure, the main drawback is that InGa is not transparent. This implies that the region covered by it does not receive light and does not contribute to the measured photovoltaic effect. Assuming that the *p* layer does not present discontinuities, one can calculate the distance L from the contact within which the charge carriers are still collected. In particular,

$$L = \frac{\rho}{R_s \cdot d_{p\ Si} \cdot d_{InGa}} = 7\mu m \tag{6.7}$$

assuming a specific resistance ρ of 10^{-2} Ω (corresponding to a doping level of 10^{18} cm^{-3}), a series resistance R_s= 1.7 Ω (see page 94), a p-Si layer thickness $d_{p\ Si} = 100$ nm and a length of the InGa contact d_{InGa}= 4 mm. This value of L is very limiting, as it implies that the solar cell area contributing to the photovoltaic effect is tiny.

Other challenges due to the use of the AIC process for the realization of a solar cell are the degree of crystallinity of the obtained p-Si layer and the doping density. The grain size of the crystallized layer can be controlled over one or two orders of magnitude by the Al deposition conditions [Nas00b] and the annealing parameters (temperature and time) [Nas00c]. The doping of the p-Si layer obtained by AIC can not be easily controlled. Although this might seem a problem, the acceptor density of the achieved layer is at the upper limit of what is typically used for the realization of solar cells (approximately 10^{18} cm^{-3}). In addition to this, the dopant ionization in nanostructures might be lower compared to bulk [Sch10], leading to a charge carrier density in the standard range. This will be discussed in Sect. 6.4.

The proposed nanowire-based solar cell can also be synthesized using a TCO-covered glass substrate instead of an n-doped wafer. In Chapter 3 we reported that it is possible to synthesize arrays of gold-catalyzed Si nanowires on glass substrate by combining nanosphere lithography, sputtering, annealing, and CVD.

6.4 Experimental parameters

An n-doped (111) RCA-cleaned Si wafer (0.1-0.6 Ωcm) has been used as a substrate. The wafer is patterned by nanosphere lithography as described in Chapter 3 and annealed at 1000°C. The samples are loaded in the CVD chamber and processed in 10 sccm Ar, 5 sccm SiH_4, and 0.1 sccm PH_3, the latter injected into the chamber already diluted to 2% Ar. The process duration is typically 15 minutes; the phosphine is added 5 minutes after process begin for not risking to compromise the starting step of the nanowire growth [Sch08]. Process temperature is approximately 525°C, while the base pressure and the process pressure are in the range of 10^{-7} mbar and 2 mbar, respectively. After the process, the samples are cooled down to room temperature and unloaded. They are etched 1 minute in 5% HF and then in aqua regia (1 HNO_3 : 3 HCl) for 2 minutes for removing the native silicon oxide and the gold catalyst particles, respectively. Just before loading the samples into the electron beam evaporation (EBE) system, they are etched again in 2% HF for 20 seconds. The EBE is used to deposit both an Al and a Si layer of typically 100 nm each. Between the two depositions, the vacuum is broken by an oxygen flow for two minutes, in order to create an Al oxide layer covering the deposited Al layer. As discussed in Chapter 5, the presence of this Al oxide layer is crucial for the layer exchange and the crystallization of silicon during the AIC process. Both depositions are performed onto a rotating sample, tilted by 60° in order to guarantee a homogeneous deposition all around the nanowire. The samples are then transferred to the oven, where they are annealed at 550°C for 4 or 5 hours under Ar flow (2 liters per minute). During

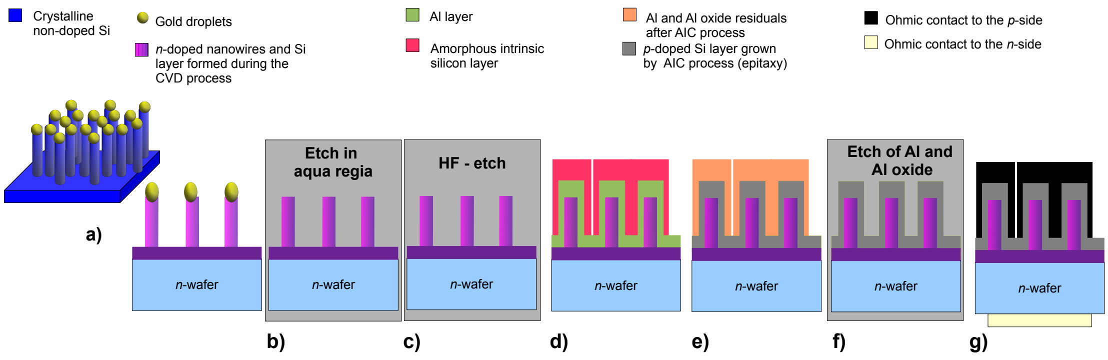


Figure 6.8: *Schematic representation of the overall process for the realization of a nanowire-based solar cell. The pictures represent the solar cell cross section for clarity.* ***a)*** *The wires are synthesized as described in chapter 3 (Fig. 3.1 on page 26) with the only difference that phosphine is also used during the CVD process, in addition to argon and silane. In this way, n-doped Si nanowires are synthesized.* ***b)*** *The gold caps at the top of the nanowires are chemically removed.* ***c)*** *The oxide layer around the nanowires is removed by HF just prior to loading the sample into the EBE chamber for the deposition of Al and intrinsic a-Si, shown in* ***d)****.* ***e)*** *The annealing step allows the AIC process to take place: the deposited layers exchange their position, while the Si layer crystallizes and becomes p-doped.* ***f)*** *The Al and Al oxide residuals on the NW surface are chemically removed.* ***g)*** *Ohmic contacts are achieved on both the n and p regions of the sample. The p contact might cover all the nanowires, as shown here, or consists of a single spot on the sample surface.*

this annealing step the Al and Si layer switch their position leading to a *p*-doped polycrystalline Si layer covering the *n*-type nanowires (see Fig. 6.4 again). After the annealing the outermost layer around each nanowire, constituted by Al and Si residuals possibly oxidized, is removed wet chemically. After an etch in HF (2%, 30 seconds), the samples are loaded again in the EBE for depositing 5 nm Ti and 200 nm Ag on the back side of the *n*-wafer, in order to achieve a low ohmic contact to the *n*-region. During the deposition the sides of the sample are covered by a mask for avoiding future shortcuts. The *p*-region is contacted using InGa, as already discussed in the previous section.

The overall process for the realization of the solar cell is schematized in Fig. 6.8.

The I-V curves were measured using a sun simulator (AM1.5, 1000 W m^{-2}, SS-80 PET) with two adjustable gold tips.

6.5 Results

Prior to discussing the NW-based solar cell, a preliminary test solar cell is shown. We tested the overall process on a plain substrate, e.g. an *n*-Si wafer processed by AIC with the same experimental conditions, but without NWs. The measured IV curve is shown in Fig. 6.9. We estimate the solar cell area contributing to the photovoltaic effect equal to maximally 0.01 cm^2 (see Eq. 6.7). The open circuit voltage and the short circuit current density are 91.20 mV and 43.40 mA/cm^2. The solar cell efficiency is 0.99%. Considered the bad quality of the *p* contact and the absence of any optimization step, this result can represent a good starting point.

We realized then a nanowire-based solar cell with the same experimental parameters, as de-

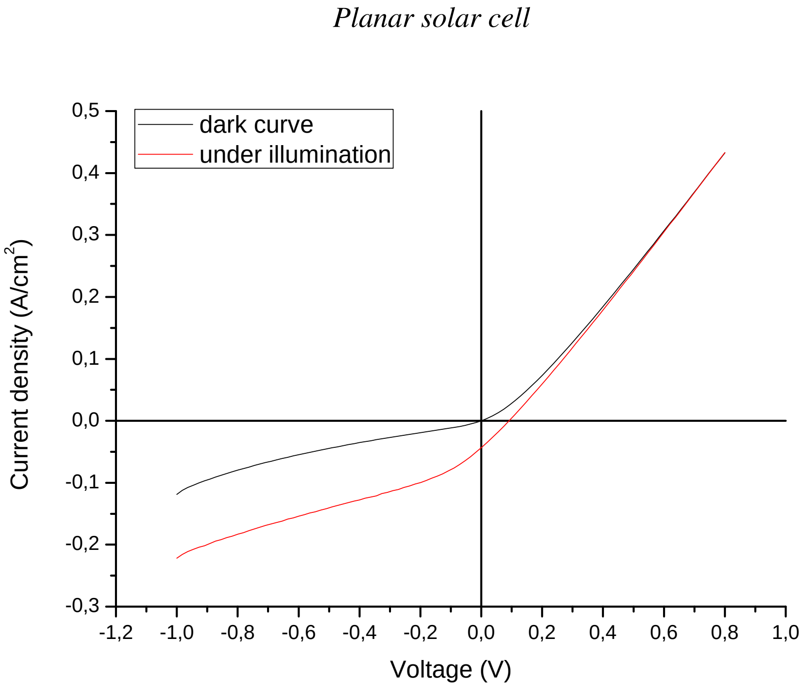


Figure 6.9: *IV-characteristics of a planar solar cell constituted by an n-doped Si wafer substrate and a polycrystalline p region, achieved by AIC process.* V_{oc} *= 91.20 mV,* I_{sc} *= 43.40 mA/cm*^{2}*, and* η *= 0.99%. The x=0 and y=0 lines are only a guide for the eye.*

scribed in Sect. 6.4. Preliminary indications of the existence of a radial p-n junction within each wire have been obtained by AFM Kelvin Probe measurements. Other methods are under investigation. Due to the small feature sizes, the mapping is difficult and therefore not reported here.

The best nanowire solar cell IV-characteristic obtained so far is shown in Figure 6.10. For the analysis of V_{oc} and I_{sc} the curves normalized by the solar cell area are used. Again the solar cell area contributing to the photovoltaic effect is estimated to be maximum 1 mm^2. It results $V_{oc} \approx$ 37 mV and $I_{sc} \approx$ 3.02 mA/cm^2, with an efficiency of 0.03%. The interpretation of these values is not unique; they are significantly lower than the best values published in literature for a silicon nanowire-based solar cell (190 mV and 5.0 mA/cm^2 [Kel08] and 505 mV, 19.7 mA/cm^2 [Kay08] for VLS synthesized wires; 402 to 453 mV and up to 40 mA/cm^2 for etched nanowires [Siv09a]), although very similar to the ones measured for the first prototypes of solar cells constituted by nanowire arrays [Tsa07, Ste08]. Therefore, they might be given either by the back contact on the Si wafer or by a non-optimized prototype solar cell. Such low performance values could be justified by the non-optimization, which includes poor-quality contacts and non-effective parameters for the crystalline quality of the p-Si layer around the n-wires: the AIC process temperature and the annealing duration determine the size of the p-Si grains, which influences the solar cell performance. In addition to this, the surface itself of the nanowire has not been processed for limiting surface roughness or the presence of surface states. Last but not least, the n-doping of the wire achieved during the nanowire growth can be varied.

It is now of crucial importance to understand what are the parameters affecting the solar cell and how to control them. Most information can be obtained from the IV-curves themselves. In

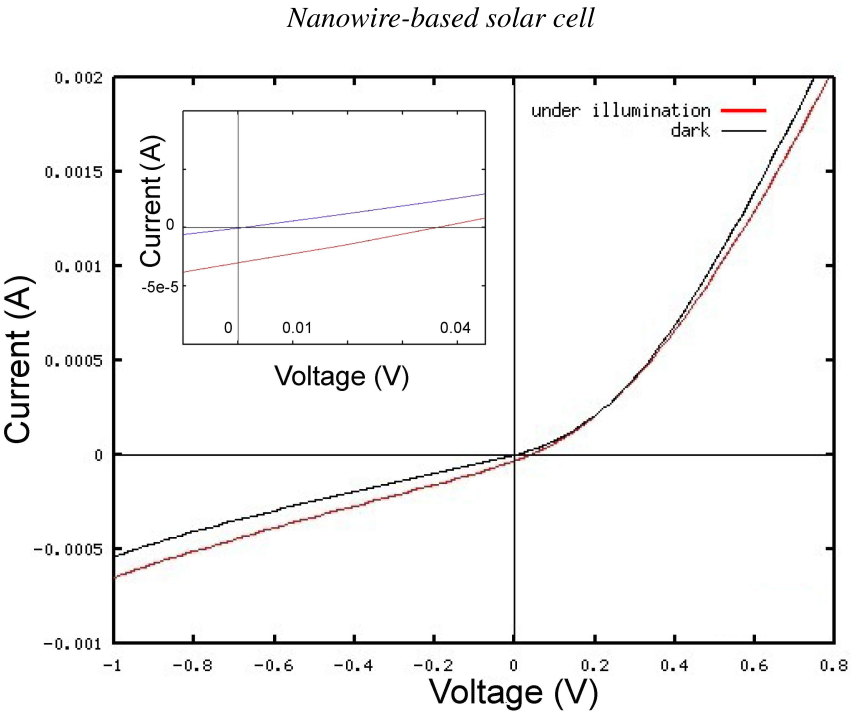


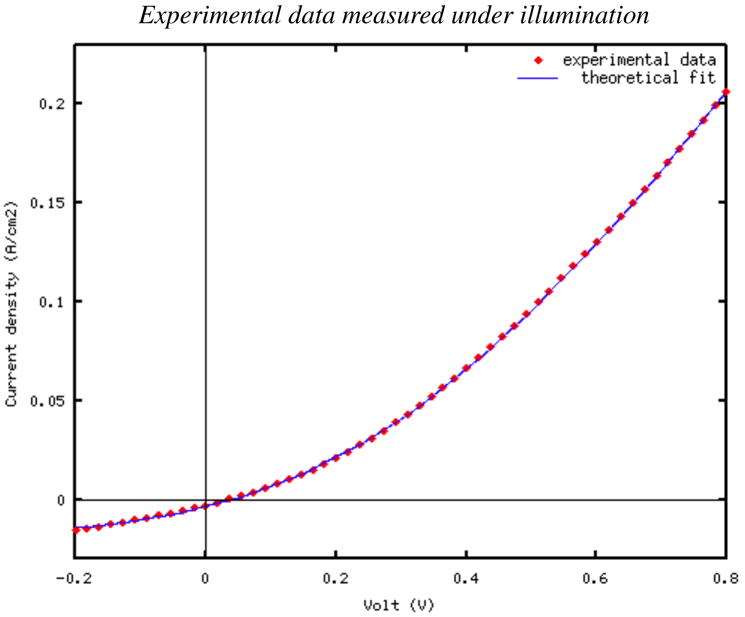
Figure 6.10: *Measured IV curves under illumination (red) and in the dark (black) of the NW-based solar cell studied in this chapter. These curves are not normalized to the solar cell area. The x=0 and y=0 lines are only a guide for the eye. The inset zooms on the region where the curve measured under illumination crosses the axes.*

particular, it is possible to estimate an upper limit for the values of the shunt and series resistances calculating the inverse of the slope of the IV curves. Alternatively, one can fit the data obtaining the values of R_s, R_{sh}, I_s, I_L and n from the best fitting parameters. In the next two paragraphs, the values of the resistances are calculated. Successively, the IV-curve is fitted and the values for all parameters are discussed. In both cases, the current density values are used; strictly speaking, the current in Eq. 6.6 is replaced by the current density and, consequently, J_L and J_s are used.

The value of the shunt resistance is given by the inverse of the slope of the dark IV line passing in the III quadrant (lower left). In the measured IV curve the value of R_{sh} changes significantly upon the region where the slope is measured. Near to the intersection with the y-axis $R_{sh} \approx 1.9\,\mathrm{k\Omega}$ has been found. This value is high enough for not affecting the solar cell performances, that is, the current can not significantly pass through this resistance, as seen in Fig. 6.7.

The upper limit for the value of the series resistance can be estimated from the inverse of the slope of the IV-curves at V_{oc} under illumination. For the considered solar cell a value of circa 10 Ω has been obtained.

For comparison and completeness, the IV curve has been fitted to Eq. 6.6 using the freely available Levenberg-Marquadt algorithm by www.gnu.org/software/gsl/ implemented in C by G. Brönstrup and then transferred into an Octave program. The best fit is shown in Figure 6.11, which includes a table of the obtained fitting values. Such values of the resistances are lower than the estimated maximum values calculated in the previous paragraphs. These new values show that (i) there is no significant current passing by the solar cell, as R_{sh} is bigger than 100 Ω, and (ii)



	Fit values	Search range	Units	Error
R_s	1.7	1 - 10	Ω	±1.1
R_{sh}	0.175	0.01 - 1.00	kΩ	±0.001
J_s	13.7	0.5 - 30.0	mA/cm^2	±1.5
J_L	4.1	0.1 - 5.0	mA/cm^2	±0.4
nT	1855	300 - 3000	K	±4
n = $(nT)_{dark}$/325 K = 5.6 ± 0.1				

Figure 6.11: *The graph plots the IV curve of the studied nanowire-based solar cell measured under illumination and its fit. These curves are normalized to the solar cell area. The x=0 and y=0 lines are only a guide for the eye. The fit has been performed by G. Brönstrup optimizing the values of* R_s, R_{sh}, J_s, J_L *and the product (nT). The resulting values and the parameter search range are reported in the table. The ideality factor n can be calculated from Eq. 6.6 dividing by the temperature at which the measurements have been performed (325 K) the product (nT)*$_{dark}$ *obtained as the best fit for the IV curves in the dark. The errors are given by the square roots of the diagonal elements of the covariance matrix used by the fitting program for establishing the best fit.*

the contacts are quite low ohmic, as R_s is acceptably small. The other two important parameters given by the fitting data are the ideality factor *n* and the saturation current density. Both of them are strongly correlated to the doping levels and the minority charge carrier diffusion length within the solar cell. The ideality factor is obtained dividing the product $(nT)_{dark}$, given by the values fitting the IV curve in the dark, by the measurement temperature (325 K). It could also be calculated by other methods [Jai05], although some of them need experimental data which could not be obtained (e.g. the dependence of the power output on the illumination [Wol63]), or are not valid for the parameters of this solar cell. For instance, the “method for the direct measurement of the solar cell junction ideality factor” proposed by Quanxi et al. [Qua87] is not valid for $R_s > 1\ \Omega$, as the obtained value of *n* becomes unrealistic. The ideality factor has been introduced in literature for indicating the discrepancy between the behavior of the studied solar cell and the ideal case, represented by *n* = 1. It normally ranges up to 2, although values bigger than two and lower than one have been published [Zhu05]. In particular in the case of nanowire-based solar cells, a high ideality factor seems common even in single-nanowire solar cells (*n* = 4.52 [Tia07]; *n* = 3.6, 2.4 [Kel08]). If these values are achieved for localized single-wire IV-characteristic, it can be expected that for IV curves regarding a NW carpet with tausends of nanowires the ideality factor increases even further. In the studied solar cell, the ideality factor confirms this idea, as *n* = 5.6. On the other hand, this might be a hint for the absence of measurable photovoltaic activity in the nanowires.

The saturation current density indicates the current which is generated by the ionized dopants within the device and which does not contribute to the photovoltaic effect. Therefore, it has to be minimized for achieving high efficiencies. It is generally defined by Eq. 6.4, but only if the assumptions listed in Sect. 6.2.1 are fulfilled. That is not the case in the studied solar cell, as at least the assumption of low-injection is not valid: as it will be discussed later, the doping levels of both regions are presumably greater than 10^{-18} cm^{-3}. Therefore, the solar cell could be more precisely modeled by a two-diode model, where the current source is connected in parallel with two diodes, one representing the recombination in the depletion region, the other representing the recombination in the neutral regions [Tar03]. In this case, the J/V characteristics of the two-diode model are given by

$$J = J_{01}(e^{\frac{V}{n_1 V_t}} - 1) + J_{02}(e^{\frac{V}{n_2 V_t}} - 1) - J_{sc} \tag{6.8}$$

where the saturation current density J_{01} considers the neutral region and J_{02} takes in account the recombinations formed in the space-charge region. This distinction is crucial because, as explained in [Kay05] and summarized in Sect. 6.2.3, the recombinations in the space-charge region are responsible for the quality of the device. The high values of the saturation current obtained by fitting the IV curves with a one-diode model are therefore a hint for the need of the two-diode model and for the poor quality of the photovoltaic performances of this prototype.

In this model the effective diffusion length of the minority carriers can be defined as [Zhu05]:

$$\begin{aligned} L_{eff} &= \frac{z + \sqrt{z^2 + 2\pi V_t J_{sc} \sqrt{\frac{2D_n \epsilon_s z}{V_{bi}}}}}{2J_{sc}} && (6.9) \\ z &= q n_i D_n \exp\left(\frac{V_{oc}}{V_t} - \ln\frac{N_A}{n_i}\right) && (6.10) \end{aligned}$$

where the built-in potential is

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{6.11}$$

and the thermal voltage V_t = 25.82 mV, the absolute dielectric constant of silicon $\epsilon_s = 1.0 \cdot 10^{-12}$ F/cm, and the intrinsic carrier concentration $n_i = 1 \cdot 10^{10}$ cm^{-3}. D_n is the diffusion coefficient of the minority carriers. These parameters are important because the width of the depletion region must be smaller than the effective length. As explained in section 6.2.1, in fact, the depletion region forms when the charge carriers diffuse to the region of the semiconductor with different doping, leaving behind ionized atoms. In the space charge region (SCR) light creates carriers which are collected outside it. In order to leave the SCR, the carrier diffusion length must be

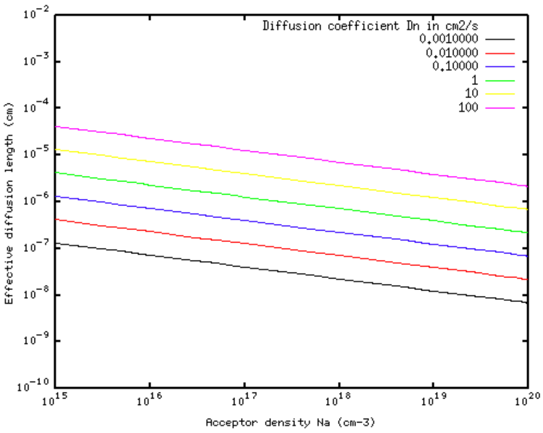


Figure 6.12: *Plot of the effective diffusion length L_{eff} as a function of the acceptor density N_A, obtained from Eq. 6.9 for different diffusion coefficients. N_D= 10^{19} cm^{-3}. V_{bi} is calculated for every line depending on N_A.*

greater than the width of the depletion region.

The value of L$_n$ is calculated from Eq. 6.9 for a diffusion coefficient of circa 1.6 cm^2/s, as measured by Nast [Nas01]. It results L_n= 5 nm. This is a very low value which can be explained by the presence of the tiny grains of the polycrystalline *p*-layer, which is also highly doped. As shown in Fig. 6.12, the effective length increases for decreasing doping, as expected.

The width of the depletion region can be calculated by

$$W = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{N_A + N_D}{N_A \cdot N_D}\right)V_{bi}} \tag{6.12}$$

under the full depletion approximation and having an abrupt junction, e.g. when the impurity concentration in the semiconductor changes abruptly from acceptor impurities to donor impurities [Sze69b]. To date, to the best of the author's knowledge, there are no reports about the abruptness of a *p*-*n* junction at the nanoscale, as also pointed out in other publications [Sch08]. It is questionable whether the *p*-*n* junction under study fulfills the requirements: for instance, it is likely that during the deposition of the Al layer on the *n*-Si NW prior to the AIC process the Al diffuses into the *n*-Si, causing a broadening of the junction. In addition to this, phosphor donors could diffuse from the *n*-wire to the *p*-Si as in a continuous crystal lattice formed by solid phase epitaxy.

Apart from the prerequisites, the application of this formula requires some further checking concerning the doping levels. The dopant concentration of the *p* region realized by AIC has been estimated by Nast [Nas00c] to be around $2 \cdot 10^{18}$ cm^{-3}, while the acceptor density in silicon nanowires obtained adding phosphine to the precursor gases during the growth process has been studied in [Sch08]. Using such data, the doping density should be around N$_A$ $\approx 10^{20}$ cm^{-3} under our process conditions. Nevertheless, the dopant level can differ from the nominal one because of the influence of surface states. When speaking of surface states, one normally refers to charges that may occur in or at the interface between Si and another material, as a consequence of the interruption of the silicon crystal periodicity [Sze69d]. Generally, the surface states present at the interface between Si and its oxide are investigated, as they have important implication in electronics, but they can influence also the contact between a semiconductor and a metal, changing the barrier height of the Schottky contact [Arc63, Rho70]. In addition, it can not be excluded that some silicon oxide or aluminium oxide is still present on the nanowire surface also after the etching steps, for instance if the deposition of the contact has not been performed fast enough. Considering therefore the case of a nanowire interface where surface states are present, the so-called interface trap states can exchange charges with Si, releasing or trapping electrons depending on the position of the Fermi level [Sch10]. Consequently, these states can act both as donors (if below the middle of the band gap) or acceptors (if above). Such states can be charged or neutral depending on the position of the Fermi level at the Si surface and they can significantly change the bending of the band structure [Sch10]. Because of the band bending, the nanowire is depleted from its surface radius r_{nw} to a certain so-called depletion radius r_d, while it is non-depleted between r_d and its center [Sch10]. It can happen that the nanowire is fully depleted in the case $r_d = 0$. The full depletion occurs for nanowires whose radius is smaller than the critical radius r_{crit}. From the calculations in [Sch10], it results that for a donor concentration above 10^{18} cm^{-3} and an average nanowire diameter of 96 nm (see Chap. 3, page 39), as in our case, the nanowire is not fully depleted. Still, the interface trap level density D_{it} influences the electron concentration in the NW, so that such concentration might be different from the one for similarly doped bulk silicon. This could influence our estimation of the p-doping of the nanowires, as the value taken from Nast's results had been obtained for planar geometries [Nas00c, Nas00a]. Considered that the nanowires have not been passivated during the solar cell processing, the worst reported value for the trap level density of non-passivated Si NWs has been used, namely $D_{it} = 1 \cdot 10^{12}$ eV^{-1} cm^{-2}. With this parameter, the doping of a NW with diameter of 96 nm does not change dramatically, but it still results one order of magnitude less than expected: N$_D$ $= 10^{19}$ cm^{-3}. On the contrary, the wire is thick enough for not presenting sensible changes in the efficiency of the donor ionization [Sch10]. It is realistic to imagine the same shift in the doping level in all the nanowires, as they are characterized by a sharp diameter distribution (see again Chap. 3, page 39).

Additionally, it has to be considered that the ionized impurity density is normally assumed to be equal to the doping concentration, but this is not true here: with regard to the p-doped region obtained by AIC, Nast ([Nas00c] and [Nas00a], page 76) calculated that only 28% of the Al atoms on substitutional sites are ionized and therefore contribute to the free carrier concentration of the p-Si at room temperature. If N$_A$ $= 2 \cdot 10^{18}$ cm^{-3}, it follows that $N_{I,p} \approx 7 \cdot 10^{17}$ cm^{-3} if no other effects are assumed, like for instance the incorporation of oxygen. Concerning the n-doped nanowire, it has been suggested [Sch08] that all the phosphorus donors incorporated during *in situ* growth are electrically active. Therefore, we assume $N_{I,n} = N_D = 10^{19}$ cm^{-3}.

Now we can calculate the built-in voltage (Eq. 6.11), obtaining V_{bi} = 0.96 V, and the width of the depletion region W. We use Eq. 6.12, although this might be questionable, as already mentioned. It results W = 50 nm. This value is probable the highest acceptable one, considering that more than half of the depletion region lies inside the n-doped nanowire, which has a radius of less than 50 nm. In addition to this, it results to be not acceptable if compared with the estimated value of the effective diffusion length (5 nm). For improving the solar cell performance it is necessary to increase the effective diffusion length. A way could be represented by optimizing the AIC process for achieving a very low amount of defects in the p-layer, which would increase the effective diffusion length. Moreover, the doping levels could be optimized, influencing both the width of the depletion region and the effective diffusion length. In particular, one could determine the best amount of phosphine to be used during the CVD process.

6.6 Conclusions

A new type of nanowire-based solar cell has been presented and contextualized in the most recent state of the art. The advantages of a nanowire-based solar cell include a broad spectral density and the decoupling of light absorption and carrier extraction requirements. The publications on the subjects report promising photovoltaic performances, but also evidence various challenges. Some of these problems can find a solution when the nanowire-based solar cell is realized combining the CVD growth mechanism with the AIC process. The first one is used for achieving wires with adjustable n-doping level maintaining high crystalline quality and a sharp diameter distribution thanks to the prepatterning of the substrate. The second one allows to obtain an epitaxial p-doped crystalline layer around the wires.

The measured solar cell characteristics of this very first non-optimized prototype have not a unique interpretation. The V_{oc} and I_{sc} values are so low that the back contact could have been causing the measured shift in the IV curves under illumination. But the very first electrical characterization of a NW-based solar cell doped by AIC can also hint to the following interpretation: a prototype which needs to improve the minority carrier diffusion length, which would allow to achieve better performances. The diffusion length is now presumably limited by the polycrystallinity of the p-Si layer, whose characteristics can still be steered by a careful choice of the AIC process parameters. In addition to this, a better procedure for achieving low ohmic contacts to the p-doped region has to be investigated. A transparent p-doped contact material is needed for increasing the area of the solar cell exposed to light. Alternatively, the wires can be grown on a glass substrate and be contacted with the already available n-doped TCO. Nevertheless, an adequate deposition technique for guaranteeing optimal adhesion of the nanowires to the other elements would need to be included in this future work.

In addition, the influence of the nanowire diameter on the doping levels has been considered. The tested high doping levels resulted in a wide depletion region compared to the diffusion length. Therefore, also the doping levels might need to be optimized. With this goal, the nanowire diameter can be changed, meaning with this only the n-doped wire diameter, or the deposited p-Si layer thickness, or both. In this context, also possible steps for the nanowire surface passivation can be explored.

Chapter 7

Conclusions: achieved results and future work

This thesis investigates two fields: (i) the growth of silicon nanowires by VLS mechanism via CVD either singularly in-place or on large areas and (ii) the Al-induced crystallization of silicon (AIC). Parts of these findings are then combined for realizing a nanowire-based solar cell prototype, where the wires are doped by AIC and patterned by nanosphere lithography, as in the title of this thesis.

We first studied a procedure for the selective in-place growth of NWs (Chap. 2). The catalyst has been patterned by Focused Electron Beam Induced Deposition, achieving high growth selectivity by mean of a sacrificial layer and combining FIB, FEBID and CVD in an industrially scalable procedure. In-place grown monocrystalline Si NWs have been obtained on both Si wafer and AFM tips with high control of their position and diameter. This is a significant improvement which fulfills the requirements of some applications, for instance tip-enhanced Raman spectroscopy. Nevertheless, applications in other fields, as for example microelectronics, also need the control on the nanowire growth direction. Although it has been observed to be limited within 50° from the surface normal, it is not predictable, as the wires are generally not epitaxial. The epitaxy is probably prevented by the Ga-implanted amorphous layer on the substrate surface formed by the FIB. A selective chemical etch might be investigated for its removal. Alternatively, the FIB milling step can be substituted by gas-assisted FEB etching, which does not cause amorphization nor implantation. This will be the subject of future work.

Large substrate areas covered by Si nanowire arrays have been achieved by CVD after patterning via nanosphere lithography (Chap. 3). An annealing prior to CVD processing is crucial for determining the catalyst droplet size and therefore predicting the diameter of the synthesized nanowires, which are characterized by a narrow diameter distribution. Of the same importance is the cleaning step prior to NW synthesis for allowing monocrystallinity and epitaxy. These two characteristics, constant diameter and epitaxy, are fundamental for the studied application, that is, a nanowire-based solar cell. The NW diameter, in fact, influences the doping level achieved in the nanowires themselves, which ideally should be the same throughout the device. Monocrystallinity and epitaxy assure good electronic transport and a mechanically and electrically stable connection to the substrate material. In addition to this, it allows to predict the direction of the wires, possibly facilitating the device integration.

The *p*-doped region of the realized solar cell has been achieved by Al-induced crystallization of silicon. The AIC process has been introduced in Chap. 4, showing its basics characteristics from an experimental point of view. Additionally, planar substrates processed by AIC combined with deposition techniques have been used for achieving Si nanostructures like nanoballoons and nanowires. The nanoballoons obtained by EBE grow following a diffusion-limited aggregation theory. No unique growth mechanism is suggested for the formation of the nanowires by CVD, as no evidence of catalyst particles could be detected, possibly constituted of Al or some oxide and incorporated in the NW at the end of the process. The formation mechanism of the NW oxide shell is discussed as well. Such crystalline nanostructures could be used as starting points for further investigations. For instance, a cleaner sample preparation or other process parameters could lead to the growth of Al-catalyzed nanowires in non ultra-high-vacuum conditions and on cheap substrates.

The thermodynamical description of the AIC process is presented in Chap. 5. The overview of the published results and explanatory models points out that the role of the oxide layer between Si and Al had never been clearly described. We offer an explanation based on considerations about the different phases of Al oxide. In addition to this, using the macroscopic atom model, the Gibbs energy difference of the Al/Si layer system before and after annealing have been calculated for five layer configurations, with and without oxide, on glass and on a Si substrate. The results explain the experimental findings: the layer configuration observed after the AIC process is the one characterized by a more negative value of total Gibbs energy difference. This allows to control the AIC process predicting the final layer configuration depending on the initial one, if the process parameters are kept constant. In addition to this, the presence of a critical thickness and the dependence of the total Gibbs energy difference on the layer thickness have been discussed.

The case of AIC on a Si substrate has been applied on Si nanowires which had been patterned by NSL and grown *n*-doped introducing phosphine in the CVD chamber. As a result of the AIC process an epitaxial *p*-doped Si shell could be achieved around the nanowires. The resulting *p*-*n* junction represents the basic element for the realized prototype of a nanowire-based solar cell, described in Chap. 6. Its characterization does not offer a unique interpretation. The measured open-circuit voltage, short-circuit current and efficiency do not equal the performances of other published nanowire-based solar cells. The studied solar cell definitely needs to be optimized, with particular regard to the *p*-side contacts and the grain size of the *p*-Si, which is steered by the AIC process parameters. The Si crystallinity, in fact, influences the diffusion length and the width of the depletion region, which depend on the crystalline quality and the doping levels. A problem in the choice of the *p* contact has been pointed out as well. Nevertheless, the use of AIC for *p*-doping a solar cell could be doubtless demonstrated for a planar geometry, which although non-optimized is characterized by an efficiency of circa 1%. Despite the need of optimization, the solar cell based on NSL-patterned Si NWs *p*-doped by AIC has various advantages: the control on wire diameter and therefore on the effective doping level, an epitaxial interface between *p*- and *n*-doped regions, a low-temperature inexpensive scalable processing, no use of expensive ultra-high-vacuum equipment, controllable doping techniques within some extent. Although it has been realized on a Si wafer, nothing theoretically prevents its realization on other substrates.

It still has to be mentioned that all VLS-synthesized nanowires have been catalyzed by gold. Although the limitation of gold are known, represented for instance by its high costs and by its deep trap levels in Si, this material has been used for realizing proof-of-concept samples. Many publications report the synthesis of high-quality Si NWs using other catalysts. It is therefore realistic to think that soon also the VLS-processing with other materials, more suitable for most applications, will be part of standard procedures. Combining all results, the nanowire-based technology will then be the key element of devices in the most different fields.

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Appendix A

Reactants in the CVD process chamber

Here we want to investigate the types of reactants present in the CVD process chamber at a base pressure of 10^{-7} mbar. The residual impurities are mostly hydrocarbons and oxygen-bearing compounds, such as water [Jac00]. The formation of Si-O or Si-C bonds is preferred to the Si-Si bondings, being the bond strengths 191.1, 107.9 and 78.1 kcal/mol, respectively. The amount of H_2O in the process chamber must be very small to avoid the formation of silicon oxide by the reaction

$$\mathrm{Si} + 2\mathrm{H_2O} \Leftrightarrow \mathrm{SiO_2} + 2\mathrm{H_2} \tag{A.1}$$

This reaction is characterized by the equilibrium coefficient

$$K_{SiO_2} = \left(\frac{P_{H_2}}{P_{H_2O}}\right)^2 = e^{\left[\frac{-\Delta G}{RT}\right]} \tag{A.2}$$

where P_{H_2} and P_{H_2O} are the partial pressure of hydrogen and water, respectively, and ΔG is the free energy of the reaction. The plot of the H_2O/H_2 ratio as a function of the process temperature is shown in Figure A.1. Ratio values above the line can lead to the formation of oxide. In the case of silicon, a water concentration of less than 1 parts per trillion is required. Therefore, the presence of silicon oxide in the process chamber can not be excluded.

$(SiO)_x$ decomposes at 600°C within several hours leading SiO_2 and Si [Wib01]. Silicon monoxide, if present, plays a negligible role in the overall mechanism, as it is volatile only for

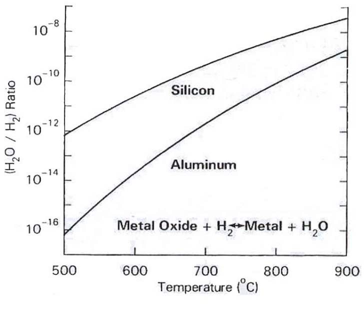

Figure A.1: *Plot of the H_2O/H_2 ratio as a function of the process temperature. Reproduced with permission from [Jac00]. Copyright Wiley-VCH Verlag GmbH & Co. KGaA.*

temperatures higher than 1000°C and tiny amounts in the substrates would be irrelevant. SiO_2 and Si can react with the oxygen residuals present in the chamber as follows:

$$\begin{aligned} SiO_2 \Rightarrow &\quad SiO + \tfrac{1}{2}O_2 \\ Si + 2H_2O \Rightarrow &\quad SiO_2 + 2H_2 \\ Si + O_2 \Rightarrow &\quad SiO_2 \end{aligned}$$

When the process starts, SiH_4 flows in the chamber and further reactions can take place, considered:

$$SiH_4 \rightarrow Si + 2H_2 \tag{A.3}$$

Silane can also decompose in the gas phase leading to the formation of Si_2, SiH_2 and Si_2H_4 [Bus88], but these reactions are slower than the ones with the substrate under these process conditions and will not be further considered. Nevertheless, the silicon formed by silane can react with the oxygen, water or oxides present in the chamber. As a consequence, it is possible that silicon or silicon oxide particles are present in the chamber and are not yet bound to the substrate. To sum up, the reactant species able to initiate a reaction with the seed are the residual impurities (of interest here: oxygen, hydrogen, water), silane molecules, silicon, silicon dioxide. Considering the main interactions among them and for simplicity, in the next paragraph only the reactions concerning silicon dioxide and silicon molecules will be discussed. We are interested in knowing what is the probability that an oxide particle reaches the seed and stick on it compared to a silicon particle. If the oxide particles stick on the seed, nanowires with cluster-like inner structure grow. Alternatively, the oxide particles shift on the sides of the seed, leading to defect-free nanowires embedded by an oxide shell [Moh08].

The wetting properties of silicon oxide on a silicon surface is discussed by [Tan08], where Si oxide islands are observed on a bare substrate or on a thin layer of Si oxide (so-called partial wetting behavior). From this consideration, we estimate the sticking coefficient of silica to be $S_{SiO_2} \approx 0.5$. Values for the sticking coefficient of Si from silane on silicon substrate are present in literature. S_{SiH_4} has been measured with different systems and it ranges from approximately 10^{-5} [Gat89, Bus88], to $2 \cdot 10^{-3}$ [Sue96]. This low value of S_{SiH_4} indicates that the probability that a silicon molecule sticks on the seed is remote. Nevertheless, the number of silicon molecules in the chamber are orders of magnitude more than the silicon oxide reactants because of the way itself that the process is performed, that is, freeing the chamber from the impurities reaching a high-vacuum basis pressure and only then suppling silane obtaining, together with the Ar, a pressure of 0.5 mbar. We assume only for now that all impurity residuals determining the basis pressure consist of silicon dioxide and no Ar is present in the chamber during process. Introducing the partial sticking probability $Sp = S \cdot P$, where P is the pressure, and using the values discussed earlier (with $S_{SiH_4} \approx 10^{-5}$), one obtains

$$Sp_{SiH_4} = S_{SiH_4} \cdot P_{SiH_4} \approx 10^{-5} \cdot 0.5 = 5 \cdot 10^{-6} \tag{A.4}$$

$$Sp_{SiO_2} = S_{SiO_2} \cdot P_{SiO_2} \approx 0.5 \cdot 10^{-7} = 5 \cdot 10^{-7} \tag{A.5}$$

Therefore, the two species can be considered as having a similar probability of sticking to the droplet if both the sticking coefficient and the number of molecules in the chamber are considered.

Appendix B

Contributions to the Gibbs energy difference (oxide-free sample on glass)

We show here the calculations for the single contributions to the total Gibbs energy difference for the case of Fig. 5.3a, that is, on a glass substrate without any oxide layer. The equations, with exception of the one for ΔG_5, are taken from [Zha04] and have been recalculated for our layer thickness and AIC process temperature. All the data needed for the following calculations, where not expressively otherwise indicated, are taken from [Zha04]. The used values of molar volume, of enthalpy, of entropy, and the related constants are collected in Tab. 5.2 at page 68.

Calculation of ΔG_1

ΔG_1 can be calculated directly using Eq. 5.4 for the change of phase [Zha04]:

$$\Delta G_1 = d_{Si} \Delta G_{<Si>-\{Si\}}(T) = d_{Si} \cdot (\Delta H_{<Si>-\{Si\}}(T) - T\Delta S_{<Si>-\{Si\}}(T)) \tag{B.1}$$

where d_{Si} is the Si layer thickness. Considering the crystallization temperature T_c, the specific heat difference at constant pressure between c-Si and a-Si $c_{p<Si>-\{Si\}} = 0.224 - (4.8\, T\, /\, 1685)$ [Zha04], the process temperature T, and the gas constant R, one can calculate [Zha04]:

$$\begin{aligned} \Delta H_{<Si>-\{Si\}}(T) &= \Delta H_{<Si>-\{Si\}}(T_c) + \int_{T_c}^{T} \Delta c_{p<Si>-\{Si\}}\, dT' = \\ &= -11.9 \text{ kJ/mol} + \int_{960\ K}^{773\ K} \left(0.224 - \frac{4.8\, T'}{1685}\right) \text{J/mol}\, dT' = \\ &= -11484.303 \text{ J/mol} \end{aligned} \tag{B.2}$$

and

$$\begin{aligned} T\Delta S_{<Si>-\{Si\}}(T) &= T\left(S_{o<Si>-\{Si\}} + \int_0^T \left(\frac{\Delta c_{p<Si>-\{Si\}}}{T'}\right) dT'\right) = \\ &= 773 \text{ K} \cdot \left(0.2\, R + 0 + \int_{78}^{773} \left(\frac{0.224}{T'} - \frac{4.8}{1685}\right) \text{J/mol}\, dT'\right) = \\ &= 151.508 \text{ J/mol} \end{aligned} \tag{B.3}$$

Transforming the J/mol in J/m^2 using the Si molar volume, one obtains

$$\Delta G_1 = d_{Si}[\text{nm}] \cdot \Delta G_{<Si>-\{Si\}}(T) \text{ [J/mol]} \approx -47.14 \text{ J/m}^2 \tag{B.4}$$

where d_{Si}= 50 nm is the default Si layer thickness.

Calculation of ΔG_2

The Gibbs energy change in the Al layer is due to both the Al-grain growth, ΔG_2^{GG}, and the relaxation of stress and strain, ΔG_2^{SS} [Zha04]. One can calculate ΔG_2^{GG} as

$$\begin{aligned} \Delta G_2^{GG} &= \Delta S^{GG} \gamma^{GB}_{<Al>} = \qquad\qquad (\text{B.5}) \\ &= 2 d_{Al} \left(\frac{1}{d_{<grain\ annealed>}} - \frac{1}{d_{<grain\ as\ prepared>}} \right) \cdot \left(\gamma^{GB,0}_{<Al>} - T \frac{d\gamma^{GB}_{<Al>}}{dT} \right) = \\ &= 2 \cdot 50 \text{ nm} \cdot \left(\frac{1}{70 \text{ nm}} - \frac{1}{45 \text{ nm}} \right) \cdot \left(0.378 \text{ J/m}^2 - 773 \text{ K} \cdot 0.12 \text{ mJ/(m}^2\text{K)} \right) = \\ &\approx -0.226 \text{ J/m}^2 \end{aligned}$$

where d_{Al} = 50 nm is the default Al layer thickness, $d_{<grain\ as\ prepared>}$ and $d_{<grain\ annealed>}$ the Al grain size before and after the AIC process, respectively, and $\gamma^{GB,0}_{<Al>}$ the Al grain boundary energy at 0 K.

The calculation of ΔG_2^{SS} is

$$\Delta G_2^{SS} = A_a + G_{rel} \tag{B.6}$$

where $G_{rel} = 0.025$ J/m^2 [Zha04] is the energy due to the microstrain relaxation of the layer and

$$A_a = d_{Al} \cdot \frac{1-\nu}{E} \cdot \sigma_l^2 \tag{B.7}$$

the strain energy per unit area parallel to the surface, with E being the Young's modulus of Al (70.6 GPa) and ν the Poisson's ratio of Al (0.345). The compressive stress parallel to the surface σ_l is defined as [Zha04]

$$\sigma_l = \frac{E}{1-\nu}(\alpha_{Si} - \alpha_{Al})(T - T_{room}) - \sigma_{l\ AP} \tag{B.8}$$

Substituting the values of the linear coefficients of thermal expansion $\alpha_{Si} = 3 \cdot 10^{-6}$ K^{-1} and $\alpha_{Al} = 25 \cdot 10^{-6}$ K^{-1}, the room temperature $T_{room} = 293$ K, and the compressive stress parallel to the surface of the as prepared sample $\sigma_{l\ AP} = 139$ MPa, one finally obtains $\Delta G_2^{SS} = (0.76 + 0.025)$ J/m$^2 \approx 0.79$ J/m^2.

The total value is then

$$\begin{aligned} \Delta G_2 &= d_{Al} \Delta G_{<Al\ as\ prepared>-<Al\ annealed>} = \qquad (\text{B.9}) \\ &= \Delta G_2^{GG} + \Delta G_2^{SS} = -1.01 \text{ J/m}^2 \qquad (\text{B.10}) \end{aligned}$$

Calculation of ΔG_3

For calculating ΔG_3 the surface energy of the pure element is needed. It can be extrapolated by the corresponding surface energy at 0 K, γ^0_{Al}, so that for aluminium [Zha04]

$$\begin{aligned} \gamma_{<Al>} &= \gamma^0_{Al} + \frac{d\gamma}{dT} T = \\ &= 1.160\ \mathrm{J/m^2} - 0.18\ \mathrm{mJ/m^2} \cdot 773\ \mathrm{K} = \\ &\approx 1.02\ \mathrm{J/m^2} \end{aligned} \tag{B.11}$$

This relationship is valid also for c-Si and will be used in the calculation of ΔG_4, but not for amorphous silicon. One can calculate the surface energy of a-Si as [Zha04]

$$\begin{aligned} \gamma_{\{Si\}} &= \frac{(\gamma V^{2/3})_0 + bT}{V^{2/3}_{773\ K}} = \\ &= \frac{0.480\ \mathrm{mJ/mol} - 0.50 \cdot 10^{-7}\ \mathrm{J/(K\ mol)} \cdot 773\ \mathrm{K}}{\left(11.01 \cdot 10^{-6}\ \mathrm{m^3/mol}\right)^{2/3}} \\ &\approx 0.89\ \mathrm{J/m^2} \end{aligned} \tag{B.12}$$

In total,

$$\Delta G_3 = \gamma_{<Al>} - \gamma_{Si} = +0.13\ \mathrm{J/m^2}$$

Calculation of ΔG_4

The interfacial energy difference between a-Si/c-Al and c-Si/c-Al can be split into different contributes. In the case both materials at the interface are crystalline, the interfacial energy is the sum of the term due to the atomic cell interface, $\gamma^{interface}$, and the one representing the mismatch between two crystalline phases, $\gamma^{mismatch}$. If one phase is amorphous and one is crystalline, like for $\gamma_{<Al>-\{Si\}}$, the interfacial energy is given by the sum of three terms: (i) as before, the term taking in account the interactions at the interface, $\gamma^{interface}$; (ii) a term due to the entropy contribution, $\gamma^{entropy}$; and (iii) the term due to the higher enthalpy value that the atoms at the interface have with respect to the corresponding atoms in the bulk [dB88, Jeu00], $\gamma^{entalpy}$. Therefore, one can write ΔG_4 as:

$$\begin{aligned} \Delta G_4 &= \gamma_{<Al>-<Si>} - \gamma_{<Al>-\{Si\}} = \\ &= \gamma^{interface}_{<Al>-<Si>} + \gamma^{mismatch}_{<Al>-<Si>} - \gamma^{enthalpy}_{<Al>-\{Si\}} - \gamma^{entropy}_{<Al>-\{Si\}} - \gamma^{interface}_{<Al>-\{Si\}} = \\ &= \frac{\Delta H^{interface}_{Al\ in\ Si}}{C_0 V^{2/3}_{Al}} + \frac{1}{6}(\gamma_{<Al>} + \gamma_{<Si>}) - \\ &\qquad -2.5 \cdot 10^{-9} \frac{\Delta H^{fuse}_{<Al>}}{V^{2/3}_{Al}} - 0.52 \cdot 10^{-7} \frac{T}{V^{2/3}_{\{Si\}}} - \frac{\Delta H^{interface}_{Al\ in\ Si}}{C_0 V^{2/3}_{Al}} \end{aligned} \tag{B.13}$$

The surface energy of crystalline silicon can be calculated as the Al one (Eq. B.11), that is

[Zha04]:

$$\begin{aligned}\gamma_{<Si>} &= \gamma^0_{Si} + \frac{d\gamma}{dT}T = \\ &= 1.25\ \text{J/m}^2 - 0.15\ \text{mJ/m}^2 \cdot 773\ \text{K} = \\ &= 1.13\ \text{J/m}^2\end{aligned} \tag{B.14}$$

Using the results in Eqs. B.11 and B.14 and eliminating the interaction terms (which are equal but have different sign), the equation for ΔG_4 becomes

$$\begin{aligned}\Delta G_4 &= \frac{1}{6}(1.02\ \text{J/m}^2 + 1.13\ \text{J/m}^2) - 2.5 \cdot 10^{-9} \frac{10.79\ \text{kJ/mol}}{(10.5 \cdot 10^{-6})^{2/3}\ \text{m}^3\text{/mol}} - \\ &\qquad -0.52 \cdot 10^{-7} \frac{773\ \text{K}}{11.01 \cdot (10^{-6}\ \text{m}^3\text{/mol})^{2/3}} = \\ &= +0.26\ \text{J/m}^2\end{aligned} \tag{B.15}$$

Calculation of ΔG_5

The contribution of the substrate to the total Gibbs energy difference is not reported in [Zha04]. The following formula is explained in Sect. 5.5.1 of this thesis. Here we show the detailed calculations:

$$\begin{aligned}\Delta G_5 &= \gamma_{<Si>-\{SiO_2\}} - \gamma_{<Al>-\{SiO_2\}} + \Delta G^{diff}_{glass} = \\ &= \gamma^{interface}_{<Si>-\{SiO_2\}} + \gamma^{entropy}_{<Si>-\{SiO_2\}} + \gamma^{enthalpy}_{<Si>-\{SiO_2\}} - \gamma^{interface}_{<Al>-\{SiO_2\}} - \gamma^{entropy}_{<Al>-\{SiO_2\}} - \\ &\quad - \gamma^{enthalpy}_{<Al>-\{SiO_2\}} + \frac{Q}{V_{SiO_2}} \cdot d = \\ &= \frac{\Delta H^0_{O\ in\ Si}}{C_0 V_O^{2/3}} - \frac{C_s \cdot T\Delta S^{def}_{\{SiO_2\}}}{V_O^{2/3}} + \frac{C_f H^{fuse}_{<Si>}}{V_{Si}^{2/3}} - \frac{\Delta H^0_{O\ in\ Al}}{C_0 V_{Al}^{2/3}} - \frac{H^0_{Si\ in\ Al}}{C_0 V_{Si}^{2/3}} + \\ &\quad + \frac{C_0 \cdot T\Delta S^{def}_{\{SiO_2\}}}{V_O^{2/3}} - \frac{C_f H^{fuse}_{<Al>}}{V_{Al}^{2/3}} + \frac{Q}{V_{SiO_2}} \cdot d = \\ &= \frac{\Delta H^0_{O\ in\ Si} - \Delta H^0_{O\ in\ Al}}{C_0 V_O^{2/3}} - \frac{H^0_{Si\ in\ Al}}{C_0 V_{Si}^{2/3}} + C_f \cdot \left(\frac{H^{fuse}_{<Si>}}{V_{Si}^{2/3}} - \frac{H^{fuse}_{<Al>}}{V_{Al}^{2/3}}\right) + \frac{Q}{V_{SiO_2}} \cdot d = \\ &= \frac{1}{4.5 \cdot 10^8}\left(\frac{(-558 + 455)\ \text{kJ/mol}}{(1.135 \cdot 10^{-5}\ \text{m}^3\text{/mol})^{2/3}} + \frac{9\ \text{kJ/mol}}{(1.093 \cdot 10^{-5}\ \text{m}^3\text{/mol})^{2/3}}\right) + \\ &\quad + \frac{208\ \text{kJ/mol} \cdot 2 \cdot 10^{-9}\ \text{m}}{2.31 \cdot 10^{-5}\ \text{m}^3\text{/mol}} + \\ &\quad + 2.5 \cdot 10^{-9} \cdot \left(\frac{50.21\ \text{kJ/mol}}{(1.093 \cdot 10^{-5}\ \text{m}^3\text{/mol})^{2/3}} - \frac{10.71\ \text{kJ/mol}}{(1 \cdot 10^{-5}\ \text{m}^3\text{/mol})^{2/3}}\right) - 18.01\ \text{J/m}^2 = \\ &\approx \frac{10^4}{4.5 \cdot 10^8}(-20.39 + 1.83)\ \text{kJ/m}^2 + 2.5 \cdot 10^{-5}(10.20 - 2.31)\ \text{kJ/m}^2 - 18.01\ \text{J/m}^2 = \\ &\approx -0.41\ \text{J/m}^2 + 0.20\ \text{J/m}^2 - 18.01\ \text{J/m}^2 = \\ &= -18.22\ \text{J/m}^2\end{aligned} \tag{B.16}$$

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- M. Becker, Th. Stelzner, A. Steinbrück, A. Berger, J. Liu, D. Lerose, U. Gösele, S. Christiansen, “Selectively deposited silver coatings on gold-capped silicon nanowires for surface-enhanced raman spectroscopy”, Chem. Phys. Chem., 2009, 10 (8), pp 1219-1224

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Lebenslauf

Name, Vorname:	Lerose, Damiana
Geburtsdatum:	23. März 1983
Geburtsort:	Verona, Italien
Nationalität:	Italienisch
Geschlecht:	weiblich
Akademischer Grad:	Diplom-Physikerin Univ.
Familienstand:	ledig

Werdegang

Sep 97 - Jun 02	Besuch des Gymnasiums “G. Fracastoro” in Verona	
Jul 02	**Abitur** am Gymnasium “G. Fracastoro”	
Sep 02 - Apr 04	Physik Studium an der Universität Trient, Italien	
Apr 04 - Jul 07	Physik Studium an der Universität Tübingen, Deutschland	
Sep 04	**Physik Vordiplom** an der Universität Trient	
	Thema:	“Design, processing and testing of impregnated porous silicon multilayer samples”
	Betreuer:	Prof. Dr. L. Pavesi, Dr. M. Ghulinyan
Aug 06 - Feb 07	Diplomarbeit in der “Microphotonic and Photonic Crystal Group” von Prof. Th. Krauss an der Universität von St. Andrews, Schottland	
Jul 07	**Physik Diplom** an der Universität Tübingen und an der Universität Trient	
	Thema:	“Optical characterization of photonic crystal waveguides in silicon on insulator”
	Betreuer:	Prof. Dr. L. Pavesi, Prof. Dr. D. Wharam, Prof. Dr. Th. Krauss
seit Okt 07	Doktorarbeit am Max-Planck-Institut für Mikrostrukturphysik, Halle, Deutschland	
	Thema:	“Patterned Silicon Nanowires *p*-doped by Al-induced Crystallization for Photovoltaic Applications”
	Betreuer:	Prof. Dr. U. Gösele (†8.11.2009), Prof. Dr. Wehrspohn, Dr. S. Christiansen, Dr. V. Schmidt
Nov 08	Aufenthalt als Gastwissenschaftlerin in der Gruppe von Dr. Michler am EMPA, Thun, Switzerland	
Apr 09 - Jun 09	Aufenthalt als bezahlte Praktikantin bei der Solarzelle-Firma Solexant Corp. in San Jose, Kalifornien (als erster Preis von NEnA II)	