Epitaxial Semiconductor Nanostructure Growth with Templates

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Preface

Today, the prefix “nano” is not merely a unit of measure, but used widely in physics, chemistry, biology, and material science. Since the last two decades, nanoscience & nanotechnology have experienced a quick development. Named as nanotechnology, it mainly deals with science and technology on the nanoscale, utilization of nanomaterials for newer systems and devices. It is a field of applied science and technology whose primary theme is how to deal with the matter in the scale of nanometers, i.e. an extension of existing science & technology into the nanoscale, normally 1 to 100 nanometers. Generally, a nanomaterial is classified, according to its dimensionality, as zero-dimensional (nanoparticle), one-dimensional (nanowire & nanotube), or two-dimensional (thin film). Especially the zero- and one-dimensional nanomaterials possess low-dimensional structures which behave quite differently from their bulk counterpart. Scientists try to understand the fundamentals governing the nanomaterials, and develop theories related to the novel phenomena arising in these small structures. Design, fabrication, and integration of the systems and devices related to nanotechnology are transfered into industry.

In this thesis, several aspects regarding the controlled growth of semiconductor nanostructures with the assistance of several templates are illuminated. Chapter 1 gives a general introduction into the synthesis of one dimensional (1-D) semiconductor nanostructures. After a detailed description of the experimental setup, synthesis of Anodized Aluminium Oxide (AAO) which is one of the most important templates with controllable porous structure is the emphasis of Chapter 2. Given the requirement of Si integration and structural control, the methods presented here are devoted to the integration of AAO membranes with Si substrates. Several issues, such as the bottom anodization, barrier layer removal, and bonding, are crucial and determine the epitaxial growth starting from the interfaces. As an exception from the approach of growing nanowires, in the subchapter 2.5, the metal-assisted chemical etching of Si utilizing AAO templates is presented. In this case the nanowires are produced starting from a Si single crystal and remain after selective etching. Solving the problem of dependence of the etching direction on several parameters, the interconnected metal film synthesized utilizing AAO has the capability of realizing ordered Si nanowire arrays vertically aligned on all kinds of Si substrates. Afterwards, the AAO membranes, either free-standing or integrated with Si substrate, are used as growth template for Si and Ge/Si nanowires in Chapter 3. Several aspects of the standard vapor-liquid-solid (VLS) epitaxial growth mechanism are reconsidered, based on the analysis of Au-catalyzed Si isotope nanowire growth. An interpretation for the sharp Ge/Si heteroepitaxial nanowire interface is given in terms of a vapor-solid-solid (VSS) growth model for the Ge epitaxy inside AAO template. Chapter 4 is focused on a new technique which combines AAO both as imprint mask and growth template for the semiconductor nanowire epitaxy. Through the imprint process, a metal film could be repositioned at each pore bottom working as catalytic nanoparticle. Different catalytic metals as well as growth materials were investigated using this method.

Other templates assisting nanowire growth will be subjects of the last two chapters, with emphasis to further diameter shrinkage and diverse epitaxial structures. In the beginning of

Chapter 5, bio-templated Au nanoparticles will be demonstrated as a substitute catalyst for positioning of sub-10 nm diameter Si nanowires. Subsequently, Si substrates with surface decoration are presented to control the epitaxial growth of sub-10 nm Si nanowire arrays. Based on high resolution TEM images of the growth interfaces, a model for the dependence of epitaxial growth direction of Si nanowires on the orientation of Si substrates is derived. The size-dependence of the sub-10 nm Si nanowire growth rate is related to different nucleation behaviours. Chapter 6 deals with size-control in the sub-10 nm regime with III-V materials, still using the surface-templated conception. Diverse heteroepitaxial nanowire structures together with sub-10 nm diameter control and the new catalyst Ag are presented. The feasibility of Si-integrated photoelectric device application is demonstrated by an optical characterization of both the photoluminescence and the emission life-time with these nanostructure arrays.

Contents

Chapter 1

General Introduction

During the last half century, low-dimensional structures dominated the modern semiconductor technology. The rapid developments of their products drive the dramatic downscaling of electronics, a miniaturization that the industry expects to continue for at least another two decades. Since the 1970s, the field-effect transistor (FET) became the fundamental logic element in semiconductor chips [Isa00]. Moore's Law states that the number of transistors on a given chip area doubles roughly every 18 months. Most of the functional semiconductor nanostructures are based on the Si platform at the present. Highly-controllable epitaxial growth methods such as molecular-beam epitaxy (MBE) and chemical-beam epitaxy (CBE) enable the precise control of composition and doping in the nanoscale. Although Ⅲ-Ⅴ compound semiconductors have been considered as building blocks for high speed and high frequency electronic devices [Kuz03, Gio07], recently, Si/Ge and Si/SiGe heteroepitaxial nanostructures have attracted much attention [Moo00, Dam04]. Low-dimensional nanostructures are promising for new, emerging semiconductor devices. Development of new methods for the down-scaling of homoepitaxial and heteroepitaxial semiconductor nanowires is indispensable for future nanoelectronics. Compositionally sharp hetero-interfaces in grown nanowires would allow to use quantum effects for devices. The key factor for the production of compositionally sharp Si-Ge hetero-interface is a low solubility of the elements Si and Ge in the catalyst. In contrast to the widely used vapor-liquid-solid (VLS) growth mechanism with a high solubility of Si and Ge in the liquid Si-Ge-Au catalyst, the vapor-solid-solid (VSS) growth mechanism offers a low solubility of Si and Ge in the solid Au-based catalyst. Generally, nanowire structures offer more prospects for defect free heteroepitaxial growth, with diameter control down to 10 nm (the requirement of post-CMOS), especially in material systems with big lattice mismatch [K ä04].

1.1 Semiconductor Nanowire Growth

A semiconductor nanowire is generally a solid rod with a diameter less than 100 nm, which is composed of one or several semiconductor materials. A lower limit of a few nm in diameter was defined from a technological point of view [Xia03]. Experimentally, many techniques for the control of composition, doping, and the interface definition along the one-dimensional nanostructure have been developed, such as MBE, CBE, chemical-vapor epitaxy (CVD), and vapor-phase epitaxy (VPE) [Bar01]. The "growth" here means that the semiconductor nanowires are nucleated from precursors, no matter if in vapor or in liquid phase. Particularly, the growth is catalyzed by a metal particle, which strongly accelerates the growth rate and determines the diameter. Wagner and Ellis presented a model on the growth of silicon whiskers, which is generally described as the vapor-liquid-solid (VLS) growth mechanism [Wag65]. With several

metal catalysts, most of the semiconductor nanowires (Si, Ge, III-V compounds) have been synthesized via VLS growth [Giv87]. The target semiconductor materials should exhibit a binary-phase eutectic alloy with the catalyst at the growth temperature. The related crystal growth rate, in one dimension confined by the catalytic particle, is greatly enhanced resulting in the 1-D structure. The catalyst particle can also be a solid at growth temperature, the mechanism is then called VSS (vapor-solid-solid) [Sch09]. In general, there are two kinds of solid catalysts, compounds or metals. For Si this can be a silicide [Kam00] or a metal with high eutectic temperature [Wit10]. Otherwise, semiconductor nanowires can be grown catalyst-free, i.e. without any metallic catalyst involved, such as the Si and Ge nanowire growth with the decomposition of the corresponding oxide [Kim09], or the selective III-V nanowire growth by masking a substrate [Nob05].

It is forecasted that, by the end of the next decade, it will be necessary to augment the capabilities of the complementary metal-oxide semiconductor (CMOS) process by introducing multiple new devices. Such an attempt will hopefully realize some properties beyond the ones of CMOS devices. However, it is believed that, most likely, these new devices will not have all the properties of CMOS devices. Therefore, although silicon based technology will remain the mainstream semiconductor technology, it is anticipated that heterogeneous integration, either at the chip level or at the package level, will integrate these new capabilities around a CMOS core [Ard02]. 1-D nanostructures, such as semiconductor nanowires and carbon nanotubes, are explicitly mentioned as realistic additions. Among the potential feasibilities, researchers have focused a lot of efforts on studies of nanowire-based vertical surround-gate field-effect transistors (VS-FET) [Ng04]. The generic process for fabrication of a wrap-gated VS-FET could also be based on epitaxially grown Si nanowires [Sch06] and InAs nanowires [Bry06]. The advancement of doping techniques and high-quality heterostructures together with the simulation works of bandgap engineering to tuning the properties of FETs are quite promising [App08, Ver08]. Si nanowire-based solutions have been proposed in literature for optoelectronic devices [Tia07], biosensors [Cui01], and energy sources [Cha08], not mentioning other functional semiconductor materials.

The roadmap for downscaling and introducing new technologies in the semiconductor industry from the International Technology Roadmap for Semiconductors (ITRS) 2008-update has summarized, that all of these improvement trends, sometimes called “scaling” trends are well laid out for the next ten years [Htt08]. As shown in Figure 1.1, although compared with ITRS 2007, the predicted trend has been amended to be less aggressive. The delay of gate-length shrinkage of logic CMOS is 3 years in near future, even 5 years in the middle term [Iwa09]. At the time of writing, devices based on semiconductor nanowires are, however, still in an embryonic stage from an industrial point of view. Their introduction as new technologies would require a long-term research and development (R&D) process in the electronics industry. Whether they will really have an impact on future post-CMOS technology which requires nanostructures smaller than 10 nm, depends on other factors like the intensive exploration of alternative materials, such as GaAs or InAs instead of Si. Controllable size and crystallographic orientation of semiconductor nanowires with high reproducibility is, therefore, one of the key issues on potential applications. In this thesis, the template-assisted growth of semiconductor nanowires will be demonstrated as

one promising solution, which could provide size controlled nanostructures while also enabling selective crystallization within the limited space.

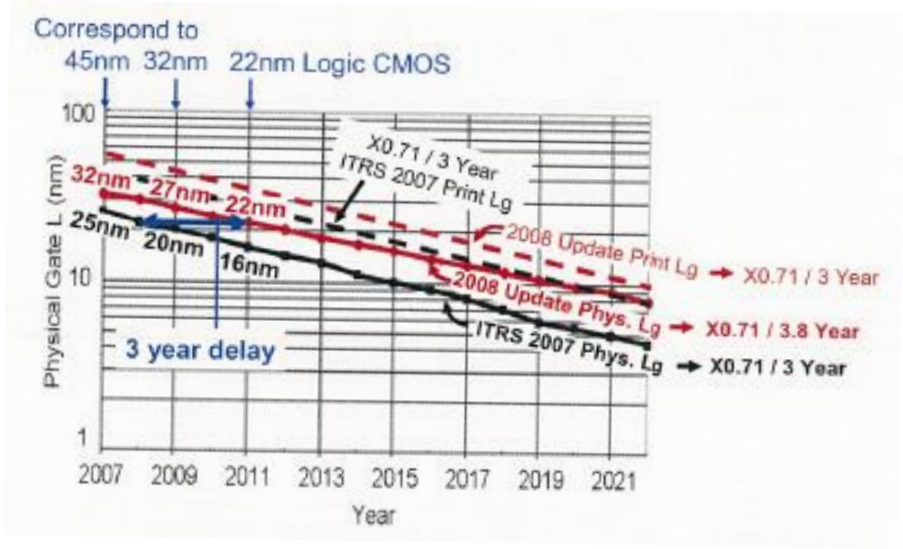

Figure 1.1 Comparison of International Technology Roadmap for Semiconductors (ITRS) Overall Roadmap Technology Characteristics (ORTC) trends of printed (resist) and physical gate length to illustrate the "scaling" trends in near future [Iwa09].

In order to control the parameters such as nanowire positioning, growth direction, diameter, and catalytic material, an innovative bottom-up approach for fabrication and integration of semiconductor nanowires compatible with conventional Si technology will be the subject of Chapter 4. The specific target was to realize vertically aligned epitaxial Si<100> nanowires on Si (100) substrate with diameter less than 22 nm, together with ordered spacing. Moreover, the diameter size distribution has to be as small as possible. Before introducing this topic, an understanding of the fundamental issues related to material growth inside porous templates is of great importance. In particular, the metal catalysts commonly used for VLS growth, such as Au, must be integrated within the template properly. Chapter 2 will discuss the growth inside AAO (anodic aluminum oxide) templates, the conditions under which one-dimensional nanostructure preferentially form, and how the various structures can be used for integration with Si. The thermodynamic model for the size limitation of Au-catalyzed Si nanowire epitaxial growth pointed out by Tan *et al.* [Tan04], will be compared to experiment in Chapter 5. An extension of a bio-nanoprocess in order to break through the size barrier of post-CMOS devices is presented, through the use of bio-template with effective Au encapsulation with diameter below 5 nm. Complementary to the bottom-up growth, an improved method based on metal-assisted etching of Si, demonstrated the potential for the fabrication of vertically aligned sub-10 nm Si nanowires [Hua08].

The semiconductor nanowires discussed in this dissertation were grown by the use of vapor deposition synthesis techniques, i.e. ultra-high vacuum- (UHV-) CVD for Si, Ge, and III-V compounds growth. Semiconductor nanowire heterostructures can be realized through the growth on a desired hetero-substrate, or by adjusting the composition of gaseous precursors during growth. Compared with the two bulk materials, stress caused by a lattice mismatch could be relaxed

through the elastic deformation near the nanowire interface [Bak08], without introducing dislocations that detrimentally influence its physical properties. Axial heterostructures, along the nanowire growth direction, can be achieved using normal semiconductor nanowire growth techniques, i.e. the metal particle-catalyzed growth mechanism [Bjö02]. From an application point of view involving semiconductor nanowires for FET devices, the band gap can be tuned locally along the length of a Si nanowire, by introducing a segment of germanium with a sharp Ge/Si interface [Ver08]. Such techniques give access to completely new alternatives for device optimization, by the formation of tunnel barriers and quantum confined structures. The growth of a Ge/Si axial heterostructure will be the topic of Chapter 3. Ge nanowires also have promising electrical characteristics due to the high hole mobility of Ge compared to Si [Rod72]. In addition, a Ge/Si buffer structure on a Si substrate would be interesting for the integration of III-V semiconductor nanowire lasers with Si-based logic circuits. Due to the special one-dimensional character of nanowires, a Ge/Si buffer structure could work as a relaxed buffer layer for the growth of InGaAs/GaAs on Si substrate, without introducing dislocations, if the nanowire diameter is below the critical radius [Käs04].

1.2 Controlled Epitaxial Nanostructures

Epitaxial growth refers to a method of crystal formation on an underlying crystalline substrate. Semiconductor epitaxy can be realized from gaseous or liquid precursors. With the substrate surface intrinsically serving as a seed crystal, or by a surface modification, the deposited material crystallizes in a lattice structure and orientation identical to those of the substrate. Ideally, a 2-D film epitaxial structure is formed after several atomic layer depositions onto a substrate. If the material is deposited on a substrate of the same composition, the process is called homoepitaxy. Otherwise, it is called heteroepitaxy.

Without introducing additional forces, the morphology at the initial stage of homoepitaxial growth is, based on the thermodynamic "wetting" model, determined by the minimum of interfacial free energies [Sch00]. Briefly, the smaller one of the total free energy of epilayer/vacuum interface plus the epilayer/substrate interface (fe + fi) and the free energy of the substrate/vacuum interface (fs), decides the "wetting" behavior of the epilayers. The epilayers are supposed to cover onto the substrate homogeneously with a decrease of free energy, when fe + fi < fs. In case of fe + fi > fs, a 3-D island morphology is formed preferentially. The partial uncovering of the substrate decreases the total free energy. Looking to a system with lattice mismatch, we should take into consideration the strain from the lattice mismatch in the growth model. The build-up of strain energy at the interface increases with the initial "wetting" growth of the epilayer, and the increased fi leads to 3-D islands formation. For different systems, a competition between different strain relaxation mechanisms was experimentally found, resulting in either 3-D islands formation without dislocations (coherent islands) or the formation of dislocations [Joh97]. Controllable epitaxial semiconductor nanostructures can be synthesized by applying the growth mode of coherent islands, which provides a potential platform for many applications, such as quantum dots devices. For the Ge or GeSi alloy growth on Si (100) substrate, island formations with dislocations were observed [Eag90, Flo99].

The application of the low-dimensional semiconductor nanomaterials requires that, for convenient device integration and processing, position and orientation control over large scales are necessary. Table 1.1 shows a collection of various methods that have been reported so far to realize 1-D semiconductor nanowires at defined locations, with the corresponding scaling range and the literature references. The most common process for position control is based on electron or ion lithographic processing. Herein, for semiconductor nanowire growth, catalyst lithography is the most popular technique for position control. The substrate is patterned by electron-beam lithography, a processing with exposure of a resist layer, metal evaporation, and a lift-off step. Up to date, large area lithographic technologies are confined to scales larger than 32 nm. The growth direction of nanowire is influenced by a lot of factors and positioning of catalysts at well defined locations will not solve the task of controlling position and direction of nanowires. For these reasons, alternative means of down-scaling to small diameters (≤10 nm) are exploited. The surface template method was derived from the selective area growth on a lateral patterned surface. A quantum wire structure was produced on a GaAs(100) substrate with an etched pattern of parallel V-grooves [Bia98]. The epitaxial nanowires had a crescent shape, and with a core thickness in the 10 nm scale. Using the scanning tunneling microscopy (STM) approach with atomic resolution, ultra-thin Cu_3N nanowires with a width down to 1 nm were demonstrated grown lateral on a single crystalline Cu(110) reconstructed surface [Max09]. To realize vertically aligned nanowire arrays, reactive ion etching (RIE) and patterned metal-assisted etching methods were used, through a self-organized porous mask, decreasing the mean size of nanowire arrays down to the sub-10 nm scale [Hua08]. However, some top-down techniques produce surfaces of nanowires with a high density of defects, by the high energy ion bombardment at the bulk material. Although the crystallographic orientation could be confined vertically to the substrate, the nanowires were found to be tapering with increase of the length to diameter ratio. The surface programmed assembly method [Rao03] does not impose strong demands on the growth process, only proper selective alignment is crucial for well controlled structures. Nanowires & nanotubes are initially, without position control, grown with a fixed growth direction and size. Afterwards, they are collected by a lift-off process and placed on a pre-patterned substrate. A precise single unit alignment is, however, not easily achieved.

Catalyst lithography	**Masked Neutral-beam etching**	**Patterned Metal-assisted etching**	**Surface programmed assembly**	**Surface template**	**Porous template -assisted**
50-100 nm	Sub-10 nm	Sub-10 nm	Sub-10 nm	1-2 nm	Sub-10 nm
[Fan06], [Boo10]	[Kub07]	[Hua08]	[Rao03], [Lee06]	[Max09]	[Rya03], [Zsc07]

Table 1.1 Collection of methods to realize 1-D semiconductor nanostructures at defined locations, with the corresponding size scale and literature references.

The criteria periodicity, small diameter, and vertical alignment of the nanowires can be fulfilled by the assistance of self-organized porous templates. Either a liquid or a gaseous precursor can be

used for the growth. A supercritical fluid (SCF) inclusion technique combined with a mesoporous silica film was developed, which produced ordered semiconductor nanowire arrays with several nanometers in diameter [Col01, Wan07]. The high-diffusivity of the fluid enables a rapid transport of the precursor into the mesopores of the silica film. However, rigorous safety precautions should be taken into consideration in these experiments, because of the high pressures and temperatures used to allow nucleation and growth [Han03]. The ideal growth of semiconductor nanowires is supposed to be bottom-up epitaxial growth. Selective bottom-up filling in the vertical 1-D direction can be realized by a combination of VLS growth and porous template with catalysts at the tip of nanowires. This means no template sidewall deposition occurs or at least slow rate parasitic growth on the sidewall compared with the nanowire growth rate. Otherwise, cracks or voids affecting conductive properties of products would be inevitable. At this point, not only high-diffusivity of the source gas is required at the growth temperature, but also the templates have to satisfy the following conditions: (1) ordered pores fitting to the desired size of nanowire growth; (2) chemical stability against source gas and by-products during CVD at the growth temperature; (3) selective deposition of catalyst metal at the pore bottom to enable the epitaxy. Satisfying these conditions, the molecules of source gas can smoothly enter into the pore, being cracked only at the surface of the catalyst with direct contact with the substrate surface.

1.3 Heteroepitaxial Nanowire Growth and Crystalline Structure

An enormous amount of work has been focused on fabrication of heteroepitaxial nanostructures which could confine carriers to 1-D quantum wires or to 0-D quantum dots, since the first observation of confinement in a quantum well [Din74]. Compositionally modulated semiconductor nanowire heterostructures and doping modulated nanowire p-n junctions have been produced. The change of the density of states and the Coulomb interactions between carriers in low-dimensional semiconductor nanostructures cause their distinct optical and electric properties. For example, single-nanowire photoluminescence, electrical transport and electroluminescence measurements show the unique photonic and electronic properties of these nanowire heterostructures, and suggest potential applications ranging from nano-barcodes to polarized nanoscale LEDs [Gud02]. Axial heterostructure nanowires were first demonstrated in 1994 for the GaAs-InAs system [Yaz94]. Further development of axial InAs/InP superlattices with atomically perfect interfaces was realized, and a conduction band off-set of 0.6 eV was deduced from the electrical current measurement, due to thermal excitation of electrons over an InP barrier [Bjö02]. For a lateral heterostructure, spatial separation of subband energies leads to a carrier confinement and a reduced carrier scattering, due to confinement of carriers in the radial direction. For example, Lieber's group used band-structure design and controlled epitaxial growth to create a 1-D hole gas system in Ge/Si core/shell nanowire heterostructures, with ballistic transport through individual 1-D subbands and long carrier mean free paths at room temperature [Lau02, Luw05]. Furthermore, most of the interesting physical behaviors are only observed from true quantum heterostructures, in which their lateral size should be on the scale of 10 nm or less, to be comparable to the de Broglie wavelength of charge carriers. Geyer *et al*. have demonstrated that, by a top-down method, the diameter of Si nanowire arrays containing Si/SiGe superlattices could be scaled down to sub-20 nm [Gey09].

To create an abrupt carrier-confining potential, the interface between the two heteroepitaxial materials must have a high degree of definition. A proper combination of materials has to be considered, because the appropriate growth temperature for each material is generally different. If the traditional VLS mechanism using metal catalyst is responsible for the fabrication of heterostructures in free-standing wires, only a low solubility of the initial target material in the eutectic catalyst allows the growth of compositionally sharp interfaces. For the important two-material system Si-Ge with a similar growth temperature range, however, a sharp interface cannot be achieved by the VLS growth, because of the 19 % and 28% solubilities of Si and Ge, respectively, in the catalytic Au-Si and Au-Ge droplets [Mas90].

For III-V nanowires, experimentally, some combinations show straight nanowire morphology. Persson *et al*. proposed a vapor-solid-solid mechanism for GaAs nanowire growth [Per04], and Dick *et al*. demonstrated that InAs nanowires with Au seed particles grow only in the temperature range where the Au-In alloy was believed to be in a solid state [Dic05]. It was noted that the solid solubility of group V elements, such as As and P in Au is less than 1 at.% [Mas90]. Thus, for a heterostructure consisting of the combinations GaAs-GaP and InAs-InP, a high possibility of compositionally sharp heterostructure interfaces in nanowires is expected. However, by changing the growth order for the two materials, most combinations do not provide straight shape in each case. For example, GaP nanowires grown on InP nanowires were straight, but InP nanowires grown on GaP nanowires were kinked [Dic08]. Based on the thermodynamic "wetting" model, a similar behaviour of the crystallization at the initial stage for the epitaxial growth of nanowires can be deduced from the catalyst-free case. Instead of the surface free energy, the interfacial free energies between each of these materials and the catalyst alloy should be considered. Generally, layer growth beneath the catalyst leads to the straight morphology, while islands growth on the initial crystallization position results in the kinked structure. The model described here does not include the consideration of the strain accommodation from lattice mismatch. Without a thin enough mismatched interlayer to release the force by elastically surface deformation, islands tend to form to relieve the built-up strain after growth of a few layers, which finally results in a kinked heterostructure. Other effects, such as changes in catalyst composition affect the interfacial energies, and thus could potentially be used to tune heterostructure morphology by an appropriate choice of growth conditions.

Besides the occurrence of dislocations and kinked structures, we should take into account another special feature existing in III-V heteroepitaxy. The crystalline structure of III-V nanowires is quite different from its bulk counterpart or other low-dimensional heteroepitaxial structures (superlattices, quantum dots). Most III-V NWs have a strong tendency to adopt the hexagonal wurtzite (WZ) crystallographic structure, even though their bulk counterparts are strictly dominated by the cubic zinc blende (ZB) structure. For example, it is possible to grow InAs nanowires with WZ structure, however, WZ is non-existing in the corresponding bulk material where the ZB structure prevails [Kog92]. It is also necessary to find proper growth mechanism working on the heteroepitaxial growth of III-V nanowires in a certain crystalline phase, either in a WZ phase or dominated by the ZB phase. Commonly, the WZ nanowires in many samples contain parts of ZB structure, which show up as stacking faults or as continuous segments. A polytypic structure along the growth axis is even controllable with sharp phase transition [Alg08]. In reality,

nanowires with diameters of tens of nanometers usually appear with a polytypic structure along the growth axis. The phase transition between these two structures obviously affects its physical properties, such as symmetry of the band structure and electron or hole transport along the wire. Woo *et al*. demonstrated the strong impact of twin boundaries on the optical emission of a mixture of ZB and WZ domains in InP nanowires grown on Si(111), which were assumed to be efficient recombination centers [Woo08]. Pemasiri *et al.* published the quantum confinement of holes into the WZ sections and electrons into the ZB sections, which results in extraordinarily long recombination lifetime at energies below 1.5 eV [Pem09]. It will be of great interest to extend the investigation of phase stability with scaling-down of III-V nanowires on Si substrates.

Consequently, the heteroepitaxial growth and crystalline structure of semiconductor nanowires have to be investigated and understood before their electronic and photonic properties can be optimized. Based on experimental observations, several possible growth mechanisms have been discussed in order to better control the crystal phase, for both Ge/Si and III-V/Si heteroepitaxial systems.

1.4 Impurities & Defects

Practically, a small quantity of impurities has an obvious effect on the physical and chemical properties of all kinds of semiconductors, as well as on the devices. For example, taken one exotic atom like boron into 10^5 silicon atoms, the conductance of intrinsic Si increases by three orders of magnitude. In crystalline semiconductor materials, much more complicated phenomena are caused by crystallographic defects. The requirements for production of CMOS devices limit the density of dislocations to as low as 10^3 cm^{-2} [Mil73]. The introduction of impurities and defects destroys the symmetry of periodic potential in the host lattice, and changes the band structures consequently. Unintentional impurities can affect the carrier concentration. For example, the VLS process uses a metal catalyst, introducing the possibility of metal contamination. The catalyst gold in particular introduces deep levels in silicon and acts as a recombination centre for free carriers.

Impurities in semiconductors can be located on substitutional sites, interstitial sites, or are incorporated as impurity complexes. Examples for such impurities are group-III and group-V elements used in p-type and n-type silicon doping (P, B, As, Al and Ga), and group-Ⅳ elements in III-V doping (C, Si). These impurities are shallow, i.e. their ionization energy is comparable to the thermal energy kT. That is, at room temperature, the concentration of free carriers can be considered as similar to the density of impurities, ignoring recombination and compensation effects. Thus, shallow impurities are of great technological importance to determine the conductivities and the carrier types. For high-performance FETs, doping the source and drain contacts as high as possible is crucial to reduce the contact series resistances [Jav05]. Crucial issues for the realization of semiconductor nanowire-based electronic devices are the quantitative and spatial doping control in the wire and the implementation of effective methods to characterize electrically active impurities and their distributions. The in-situ synthesis of doped nanowires during a VLS growth is, depending on the gaseous doping sources, a high-controllable doping method [Zhe04, Sch09a]. In previous works, doped Si nanowires were characterized intensively

with conductance measurements, by placing an isolated Si nanowire between electrodes with the help of e-beam lithography [Cui00, Yuj00], or by contacting single NWs with conductive tips inside a scanning electron microscope (SEM) [Kan08]. In contrast, electron holography [Den09] and Raman spectroscopy are simpler and more reliable methods because no electrical contacts between NWs and electrodes are required. Imamura *et al.* reported that, by analyzing the Fano spectral shapes, the active boron concentrations could be characterized along the growth direction of single p-type SiNWs grown by a VLS process [Ima08]. The Fano resonance is due to the interference between scattering from discrete optical phonons and the photoexcited carriers [Gup03]. Disadvantages of this method are the small sensitivity below a doping level of 10^{19} atoms/cm^3, and almost no sensitivity to n-type doping because a minimum density of active donors of 4×10^{19} atoms/cm^3 is required to observe the Fano line-shape in n-type silicon [Nic00]. Limited spatial resolution is another hindrance for some applications, therefore, atom probe tomography was used to analyze the quantitative and spatial dopant concentrations in arbitrary position of a single nanowire [Per09]. This method displays atomic resolution, but is insensitive to electrical activity.

The impurities are introduced into III-V compound nanowires in a more complicated way. The growth of III-V nanowires by chemical-beam epitaxy (CBE) employs gas sources for both the group-III as well as the group-V elements. Although an ultra-high vacuum chamber is used to avoid further contamination, the precursors are metallorganics and the incorporated element is usually attached to three alkyl molecules. The alkyl groups most frequently used are derived from methane (CH_4) and ethane (C_2H_6). Veuhoff *et al.* reported the use of trimethylgallium (TMGa) and arsine for the growth of GaAs [Veu81], in which high p-type conductivity was obtained as a result of the carbon incorporation. Carbon is known as a stable p-type impurity in GaAs which makes the TMGa precursor an attractive choice for highly p-type doped GaAs. Furthermore, the impurity background concentration of $Al_xGa_{1-x}As$ was found to be very high, typically in the 10^{17}-10^{19} cm^{-3} range [Dee04]. Such high background impurity concentrations in $Al_xGa_{1-x}As$ are due to the high reactivity of Al which tends to form strong Al-C bonds (which are stronger than the Ga-C bonds). One should also consider that Si doping might occur in the heteroepitaxial growth of III-V nanowires on Si substrate using Au as catalyst. This is related to Au-Si alloy formation between the Au nanoparticle and the Si substrate working as a Si reservoir. Considering that all group-Ⅳ impurities are amphoteric, Si may autocompensate strongly at high doping levels. Even though, Si introduces predominantly n-type doping in III-V semiconductors, and is a shallow donor with 4-6 meV ionization energy in GaAs and InP [Sch93].

A specific challenge for obtaining compatibility of semiconductor nanowire growth with CMOS processing is, that the metal catalyst can behave as a deep-level impurity contamination in silicon. Au produces a deep level close to the middle of the silicon band gap with high recombination efficiency. Therefore, one of the most significant issues is the elimination of Au from the process. Since Au is difficult to remove completely after growth [Woo07], catalysts compatible with CMOS requirements or catalyst-free growth techniques must be developed. Several non-gold catalysts were successfully adopted for the growth of Si nanowires [Giv75, Kar00, Gar07]. The epitaxial growth of Al catalyzed Si NWs via VSS growth mechanism is a promising solution [Wan06]. The control of size, growth direction, and crystal quality using Al catalyst has been

demonstrated in Chapter 4. The new discovery of silver as catalyst for gallium phosphide nanowire epitaxy will be discussed in Chapter 6. Deep levels can be caused not only by impurities, but also by point defects or spatially extended defects. Examples for extended defects are dislocations and nanowire surfaces. The surface depletion region can compensate shallow dopants and, as a consequence, reduce the conductivity. Recombination happening on the nanowire surface can drastically degrade the performance of minority carrier devices such as light-emitting diodes, lasers, and bipolar transistors. The optical properties of semiconductor nanowires can be strongly affected by deep traps. Optical measurements of the sub-10 nm diameter GaP nanowires are analyzed with regards to the large surface-to-volume ratio in Chapter 6.

Still, our understanding of 1-D semiconductor nanowire growth mechanisms, as well as the effective characterization of their physical properties is incomplete. The state-of-the-art growth techniques offer limited control of structural and crystallographic properties and at doping. Efforts on improving synthesis techniques have stimulated 1-D nanomaterial research, and a proper understanding of their unique properties is the driving force behind the semiconductor nanowire-based device applications.

Chapter 2

Anodic Aluminium Oxide (AAO) Combined with Si Growth

In this chapter, first a short introduction on the development of anodic aluminium oxide (AAO) templates is given, and later its application as growth template for semiconductor nanomaterials is described. Our experimental setups for both the AAO template synthesis and the growth of semiconductor nanowires are specified here. Afterwards, two different methods for combination of AAO and Si substrate will be presented respectively, as well as a confirmation of the selective growth of Si inside the AAO templates.

2.1 Introduction

Porous AAO synthesized by electrochemical oxidization of aluminium has been studied and used in numerous fields for more than half a century [Kel53, Boo55]. Based on a two-step anodization process, in 1995, a self-ordered porous AAO membrane with 100 nm interpore distance was first reported by Masuda and Fukuda [Mas95]. The long time first anodization results in an equilibrium morphology at the oxide/metal interface, which shows a textured aluminium surface after removing the first oxide layer. The textured aluminium surface results in highly ordered hexagonal pore arrays in the second anodization step. Since this discovery, AAO can be used to provide ordered honeycomb nanopore arrays, perpendicular to the surface. Most importantly, the diameter of AAO pores can be controlled from a few nanometers to several hundreds of nanometers depending on the anodic voltage and acid species used for anodic oxidation. To date, the most popular model for the self-adjustment of ordering in AAO is based on the mechanical stress, which is associated with the expansion between neighboring pores during the oxidation process [Jes98]. Under conventional so-called ‘mild anodization’ (MA) conditions, AAO formation is described by a 10% porosity rule, corresponding to a volume expansion ratio of 1.2 between aluminum and alumina [Nie02]. Lee *et al*. reported that, by using the so-called ‘hard-anodization’ (HA) process, well ordered hexagonal pore arrays in AAO can be produced with a growth rate 25–35 times larger than with MA but a smaller porosity rule of only 3% [Lee06a].

Anodization can be carried out under constant voltage mode (potentiostatic) or constant current mode (galvanostatic). In general, a two-step constant voltage anodization is recommended (Fig 2.1). The experimental setup is quite simple as shown on the illustration of Figure 2.1. In order to get homogeneous reactions, the electrolyte is stirred. The structure of pore arrangement after the second anodization is characterized as a close-packed hexagonal pore array (top-view SEM image), and columnar cells containing elongated cylindrical nanopores are normal to the Al surface. Each nanopore is ended by a thin barrier oxide layer with approximately hemispherical shape (side-view SEM image, white insert). Typically, AAO films with different pore diameters and interpore distances ranging from 20 to 200 nm can be prepared, using three major inorganic

acid electrolytes: H_2SO_4, $H_2C_2O_4$, and H_3PO_4. The respective electrochemical parameters and dimensional measurements obtained by *ex situ* SEM characterization are shown in Table 2.1. We can conclude that, without further pore widening after the second anodization, the pore diameter after ordering in sulfuric acid is the smallest down to the 20 nm range. The pore density is increased with decreasing of constant voltage, similar to the reported approximately 2.5 nm/V linear relationship [Nie02]. On the other hand, the pore diameter and shape are influenced by the electrolyte temperature and the anodization time because of the chemical etching on the pore wall. For example, the sulfuric acid anodization at 25 V results in a minimum pore diameter of 20 nm at 1 ℃ rather than the 25 nm at 8 ℃.

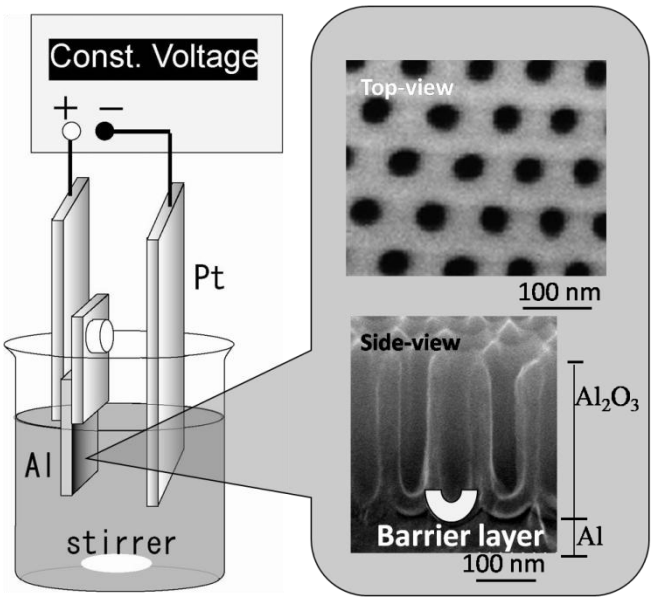

Figure 2.1 Simplified illustration of the experimental setup of a two-step constant voltage anodization. The structure of the AAO film was characterized by top-view and side-view SEM images.

Table 2.1 Recommended electrochemical parameters for ordered AAO preparation.

Electrolyte	Concentration	Voltage (V)	Temperature (℃)	1st anodization time (h)	Oxide etching T(℃)/t(h)	Pore diameter(nm)/ interpore distance(nm)
H_2SO_4	0.3 M	25	1 ~ 8	20 ~ 40	60/16	20/65
$H_2C_2O_4$	0.3 M	40	1 ~ 8	20 ~ 40	60/20	40/100
H_3PO_4	1.0 wt. %	195	1 ~ 2	16 ~ 20	45/24	180/500

AAO has been used as a template for fabrication of various nanomaterials since it has many advantages [Mar94], such as small pore diameter, high packing density and much lower cost compared with conventional lithographic techniques. Its application was a breakthrough in the preparation of ordered 1-D nanomaterials, such as in the fields of metal nanowire arrays [Sau02], carbon nanotube arrays [Iwa99], vertical ultra-high density magnetic storage media [Chu05] and

photonic crystals [Nak99]. In addition, thermal and chemical stabilities of AAO are high enough for VLS growth of Si NWs, since the main component is a stable material. Early experiments using AAO as templates to grow semiconductor nanowires have been done with free standing membrane without epitaxy [Xud00, Car01]. Ordered vertical nanowires would allow a higher packing density than the presently used lateral structures. If nanowires are grown epitaxially on the substrate from defined catalyst locations, for integration convenience, the wires can be left in place, and the contacts can be post-processed to the exposed top of the wires. One approach presented in literatures utilized a thin aluminum film on a conductive substrate [Chu02]: the electrochemical formation of aluminum oxide stops as soon as all Al metal is consumed, and the thinner AAO barrier layer formed on the conductive material can be removed by chemical etching. In this case, the AAO membranes are fitting and connected to the substrate. A big advantage of a fixed AAO membrane on a substrate is that the AAO nanopores can be used as template to control the epitaxial growth direction of semiconductor nanowires perpendicular to the substrate surface, even if the direction is not a preferred orientation of nanowire growth in free space.

2.2 Experimental Setup

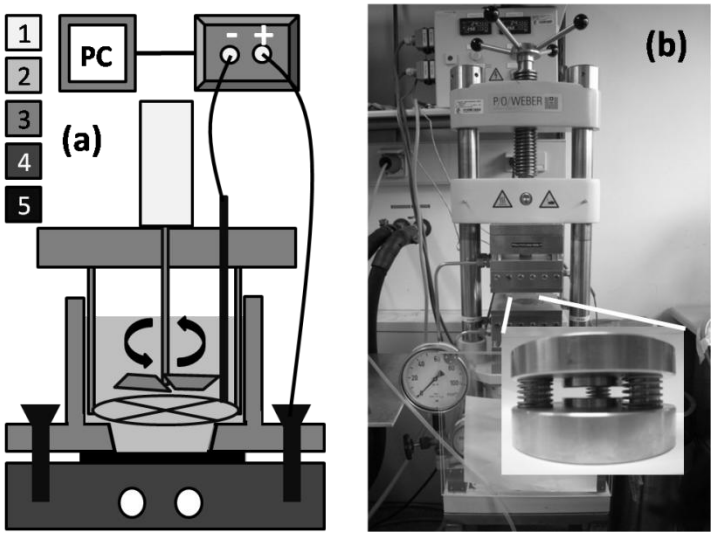

Figure 2.2 (a) Schematic drawing of the apparatus used for the AAO anodization. A computer (PC) controlled the potentiostat (Keithley Sourcemeter 2400). The different greyscales from 1 to 5 represent respectively: 1. Motor-controlled rotator for agitating the electrolyte; 2. Cooled electrolyte sealed in the cell with heat isolation by the thick Teflon walls; 3. Main electrochemical cell and rotating stirrer made of Teflon; 4. Copper plate working as electric conductor and cooling element; 5. Aluminum sheet, metallic screws for fixing the cell to the copper plate and connecting the anode, and Pt mesh working as counter electrode connected to cathode. (b) Photograph of a hot-plate manual lab press (PW 40 TEMPRESS; P/O/WEBER) used for bottom-imprint method. The insert shows a home-made counter-part designed for small samples.

Figure 2.2a shows a schematic drawing of our apparatus for electrochemical anodization. The Teflon made electrochemical cell consists of mainly two separate parts: one is the electrolyte

container which is fixed by screws to the copper cooling plate, and the Al sheet is sealed between the electrolyte and the conductive cooling plate worked as anode; the other part with platinum (Pt) mesh acting as the counter electrode (cathode), and a motor-driven agitator is used to stir the electrolyte. For effective cooling of the Al sheet during anodization, a combination of cooled electrolyte with thick Teflon wall sealing is employed. The sourcemeter for anodization is controlled by a computer, with a working capability of either 0-200 V (potentiostatic mode) or 0-100 mA (galvanostatic mode). Figure 2.2b shows a device used for the bottom-imprint method, which will be discussed in details in Chapter 4. The two pressing plates can be heated with controllable temperature, and the insert shows a home-made counterpart with ultra-flat surfaces of single-crystal sapphire wafers.

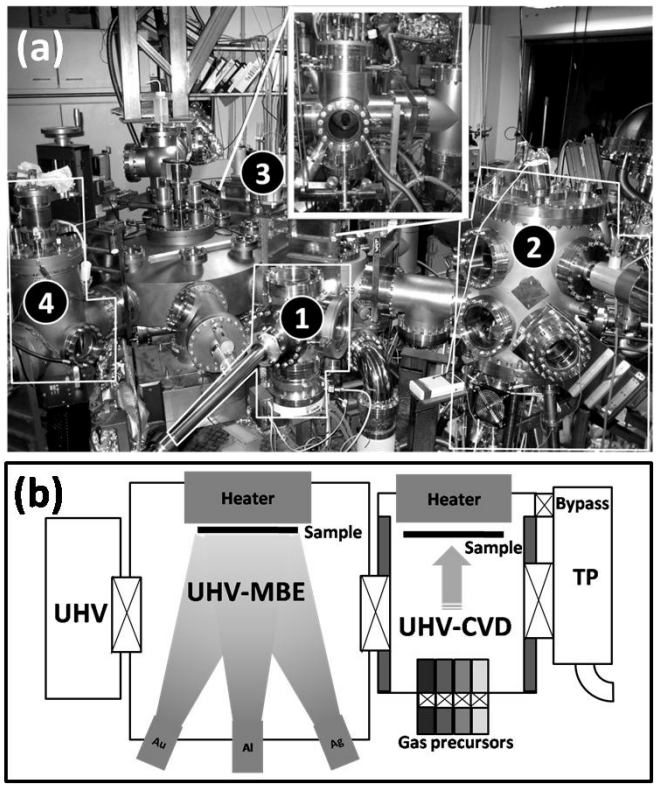

Figure 2.3 (a) Photograph of the main UHV system consisting of: No.1 load-lock chamber, No.2 MBE chamber, No.3 CVD/CBE chamber, No.4 heating chamber. (b) Schematic drawing of the MBE chamber for catalyst deposition, and the CVD chamber for nanowire growth.

Figure 2.3a shows our main UHV system for semiconductor nanowire growth. Several functionalized chambers are connected to the main vacuum chamber which has a background pressure below 1×10^{-10} mbar. No. 1 as outlined is the load-lock chamber for inserting samples into the UHV chamber. It also works as a pretreatment chamber for pumping away the remaining chemicals, especially absorbed inside the AAO pores, such as the volatile chloroform. One of the functionalized chambers for deposition of catalytic materials is No.2, an UHV-MBE system with multiple crucibles. A radiative heater with temperature control placed inside was designed to observe the growth of catalysts at certain temperatures with an *in situ* reflection high-energy electron diffraction (RHEED) characterization. This chamber is also used for the metal decoration

method to tremendously shrink the size of metal catalyst particles. The most important chamber is No.3 (enlarged as inset in Figure 2.3a), which can be either used in a CVD growth mode (total pressure in the range from 1×10^{-2} to 1×10^{1} mbar) or in a CBE growth mode (from 1×10^{-5} to 1×10^{-4} mbar). To enhance the efficiency of gas precursors, this chamber was designed with a dual-wall structure with water-cooling and compact volume. The heater with a PID controller (Eurotherm 216e) can be set from room temperature to 750 ℃. The temperature was calibrated by a measurement with five thermocouples glued on a standard 100 mm Si wafer. The flow rate of silane gas is controlled by a mass flow controller (MKS 647B), while the other gas precursors were introduced from the lower part of the chamber by manually adjusted gas dosing valves of separate channels. For phosphor doping during Si nanowire growth and gallium/indium phosphide nanowire growth, gaseous tertiarybutylphosphine (TBP) is pre-cracked by a tubular gas cracker settled inside the chamber. No.4 is a water-cooled dual-wall UHV-heating chamber used for the surface reconstruction of Si wafers, with a heating capability of 800 ℃ at 1×10^{-9} mbar. A simplified schematic cross-section drawing of the two main process chambers respectively for catalyst and nanowire growth is shown in Figure 2.3b. The sample (Si wafers in most cases) is first transferred from the main UHV chamber into the MBE chamber for catalyst growth. High purity (⩾99.999%) reservoirs of Au, Al, and Ag inside thermal evaporation crucibles are mounted with a fixed angle relative to the sample position. Afterwards, the sample with deposited catalyst can be *in situ* transferred into the CVD chamber for nanowire growth.

2.3 AAO Growth on Si

In order to use AAO as a scaffold that separates and aligns semiconductor nanowires or nanotubes for integration with Si-based CMOS technologies, AAO membranes connected directly to the Si substrates are desirable. As formed on bulk Al sheet, AAO films can be provided with highly ordered honeycomb nanopore arrays. They are produced by an electrochemical polishing of Al and a two-step anodization [Mas95]. If the thin Al film is deposited on the Si substrate and anodized, the ordering of AAO is difficult to be achieved due to the complicated surface roughness and nonuniform crystallite sizes [Hil08]. The surface condition of the Al film will directly affect the ordering of the grown nanopore arrays. However, with pore formation guided by lithographical or imprinted surface patterns, controlled pore ordering and independently controlled pore spacing can be realized [Rob07].

Figure 2.4a is a schematic illustration of Al anodization on Si substrate, the barrier layer formation, and the morphology of the AAO/Si interface after removal of the barriers. First, a thin Al layer (thickness < 1 μm) was sputtered onto the H-terminated *n*-type Si(100) substrate. A standard anodization for the fabrication of AAO with 40 nm pore diameter was performed. The pore formation process proceeds with a thick barrier layer underneath as shown in Figure 2.4b. The normal anodization stops as soon as the Al below the center of the pore is oxidized. The anodization can be continued until it consumes all of the aluminum beneath the barriers. When this process is continued, the resulting oxide barrier layer structure at the bottom of the pores is, as shown in Figure 2.4c, quite different from the morphology in the bulk aluminum. A void structure is observed beneath a thin arch-shape barrier layer bended upwards at the end of each pore. Forces

on already existing oxide by newly formed oxide combined with geometrical conditions produce the upward bending [Cro00].

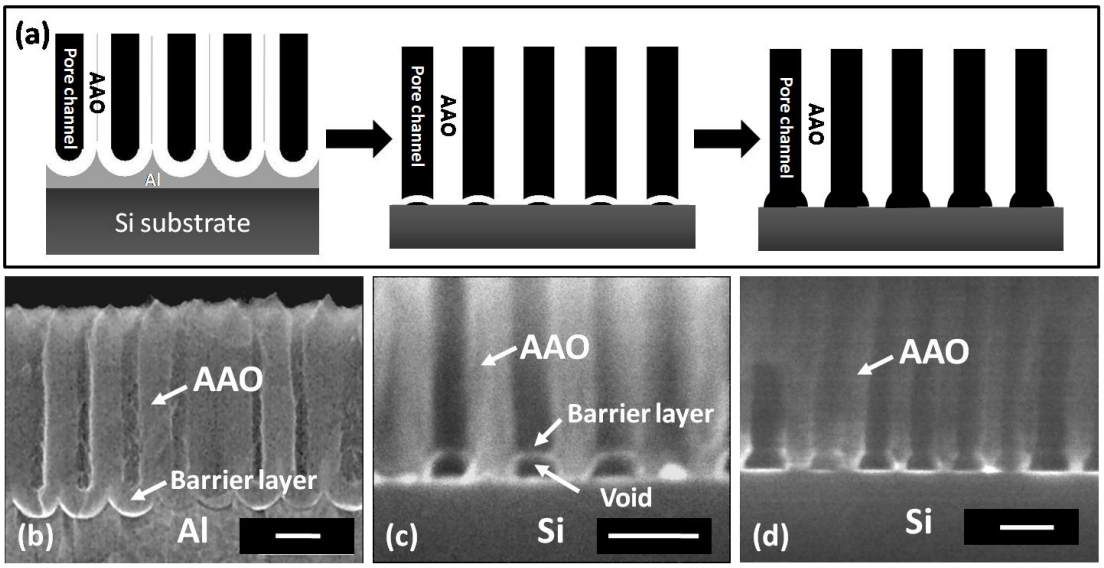

Figure 2.4 (a) Schematic illustration of AAO anodization on Si substrate, barrier layer formation, and the pore opening by etching off the barriers. (b) - (d) Side-view SEM images corresponding to each single process illustrated in (a), respectively. Scale bars are 100 nm.

To confirm the growth mechanism responsible for the arch-shape barrier layer formed on Si, further analysis of the current-time curve together with the microscopy of the interface is shown in Figure 2.5. The barrier layer touching the Si substrate is shown in Figure 2.5b, corresponding to the current point at A in the I-t curve in Figure 2.5a. Further anodization creates additional dissolution of the barrier near the Si, and the increase of current from point A to point B is explained by a resistance decrease. Schematic inserts illustrate the stresses at the interfacial region and the growth of silicon dioxide on Si surface, corresponding to point B and point C, respectively. In contrast to the anodization on the Al sheet, the residual Al on Si in between the neighboring pore-cell as confirmed in Figure 2.5b is firmly attached to the rigid Si substrate. Therefore, the stresses by volume expansion of alumina and silicon dioxide (the directions of stresses are shown by arrows) are accommodated with interfacial restructuring to create the void. During the oxidation of the residual Al, the inverted shape of the barrier layer becomes thinner with further bending. The electrolyte leaks into the voids, through cracks of the barrier caused by bending, and the aluminium oxide is dissolved inside the void as well as at the outside surface. The further anodization of Si instead of Al results in the decrease of current from point B to point C with prolonged SiO_2 growth. The thickness and shape of SiO_2 beneath the pores was investigated with HF selective etching (Figure 2.5d). We found that the Si surface had concave dimples at the position of pore bottoms after removal of the SiO_2 layer.

In conclusion, anodization of an Al film on a conducting Si substrate has two main peculiarities. First, the insulating arch-shape barrier alumina layer with void beneath, which is easy to remove without obvious widening of the pore diameter. Second, the Si surface reacts electrochemically in

a controllable manner, and its oxide thickness can be selected by monitoring the anodization I-t curve after the anodization of Al is complete. In this process, proper switch-off time is crucial in order to avoid the detachment of the AAO from the Si substrate after removing the SiO_2 layer. Inhomogeneities of Al metal film thickness and of current density during anodization result in different optimum anodization times required at different positions of the sample.

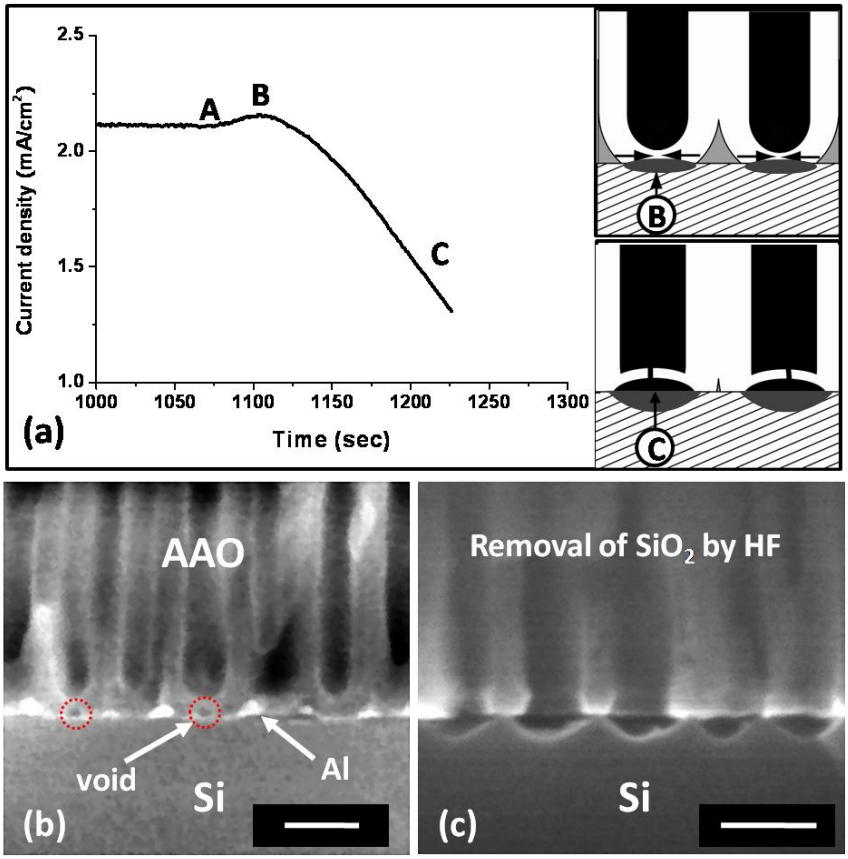

Figure 2.5 (a) The evolution of current during the last period of anodization of an Al film on a Si substrate using $H_2C_2O_4$ solution. The inserts depict the process flow of voids formation with curvature inversion of the thin barrier layer, corresponding respectively to the highest current point (B) and the lowest point (C) in I-t curve when the process is stopped. (b) Side-view SEM image of the AAO/Si interface when the Al beneath the barrier is completely consumed, corresponding to the current point (A) in (a), where remaining Al between neighboring AAO pore cells is visible with bright contrast and triangular shapes. (c) The SiO_2 formation can be confirmed from the concaves beneath each pore after the HF dipping. Scale bars are 100 nm.

2.4 AAO Bonding onto Si

As mentioned previously, the approach of anodizing an Al layer on the Si substrate has two main drawbacks. First a good ordering of AAO pores requires a long time etching and a thick and smooth Al film which could not be obtained with available equipment. Second the undesired anodization of Si leads to a rough Si surface with dimples beneath each pore bottom. A new

method was invented based on the idea of processing a freestanding AAO membrane and bonding the thin membrane onto a Si wafer. Instead of filling the pores with an etching solution and simultaneously etching pore walls and the barrier at the pore bottom, a freestanding AAO membrane can be floated on an etching solution, and only the barrier layer contacts to the chemicals.

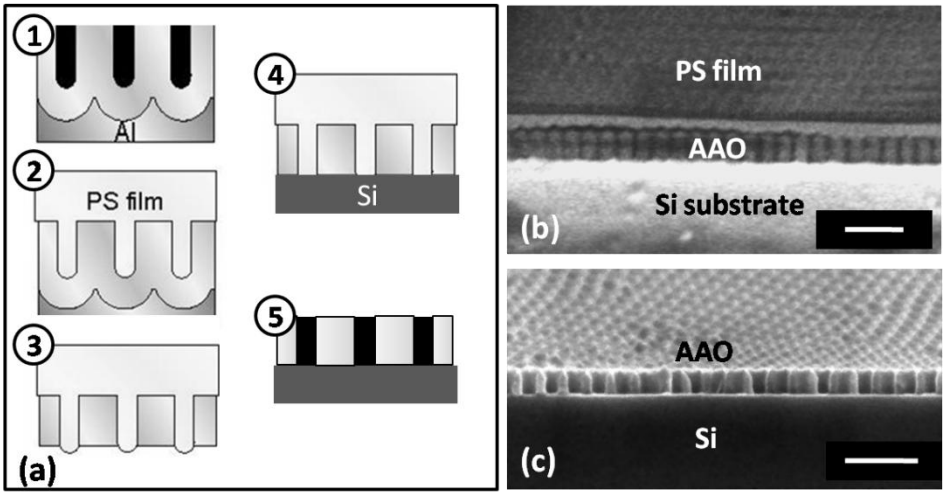

Figure 2.6 Thin AAO membrane bonded onto Si substrate. (a) Scheme for the fabrication: 1) thin AAO film on Al with high ordering, 2) spin-coating of PS film, 3) selective etching of Al substrate and barrier layer, 4) transfer of AAO membrane onto Si substrate, 5) removal of PS. (b) Tilted side-view SEM image of AAO/PS bonded on Si in step 4, scale bar is 100 nm. (c) Tilted side-view SEM image of sample (b) after step 5, scale bar is 150 nm.

In order to realize a freestanding continuously open AAO membrane bonded onto Si substrate, a polymer-assisted method was used as illustrated in Figure 2.6a. First, a thin AAO film was synthesized by the standard two-step anodization process as step 1. Here we show one sample as an example, because different electrochemical parameters correspond to different pore diameters and interpore distances. Applying a constant voltage of 25 V in 0.3 M H_2SO_4 acid (3 ℃), the first anodization lasted for 24 h. Then, the oxide layer was completely removed by wet etching (a mixture of 1.8 wt. % chromic acid and 6 wt. % phosphoric acid) at 45 ℃ to obtain a textured surface on Al. The second anodization was conducted with the same parameters as the first one, and only lasted for 180 s for an oxide thickness of about 100 nm. A spin-coating process (step 2) was used to fill into the pores a thin layer of polystyrene (PS), which attached homogeneously to AAO after spinning with 3000 rpm for 60 s using 1.5 wt. % PS/$CHCl_3$ solution, followed by a 90 ℃ solidification heating. The protection layer of PS enhances the buoyancy of AAO, and its hydrophobic nature enables the remaining Al substrate to be etched completely by floating on a mixture of $CuCl_2$ and HCl solutions. It should be pointed out that the thin PS film prevents the thin ceramic membrane from mechanical deformation. The integral structure can be retained during handling and transfer. After removal of Al, the barrier layer was selectively etched by changing the etching solution to 5 % H_3PO_4 at 30 ℃ for 15 min (step 3). Since the whole pores were filled by PS, the side-effect of pore widening was avoided. The whole PS/AAO membrane still floating on the surface of deionized water was transferred to a desired substrate such as Si

(step 4). One sample is shown in Figure 2.6b, a tilted side-view SEM image. The AAO has a thickness of around 100 nm with a homogeneous 30 nm thick PS film covering the surface. The pores are sealed and attached to the Si surface. The exterior PS film can be removed by a $CHCl_3$ washing, and the PS inside the pores can be further dissolved with an immersion into $CHCl_3$ or vacuum pyrolysis. This process (step 5) not only gets rid of the PS but also enables the conformal contact of the AAO bottom side with the flat Si surface (shown in Figure 2.6c). The pores are oriented along the normal of the substrate.

The van der Waals forces at the interface exhibit an excellent contact which can even survive evacuation. The thickness of an AAO film produced with sulfuric acid anodization should not exceed 250 nm, which corresponds to a pore length/diameter ratio of 10. The same ratio limitation was found in the case of oxalic acid, with a 40 nm pore diameter. Beyond this ratio, the PS always filled the pores only incompletely, and conformal contact was impossible because of surface roughness after selective etching. The analysis of pore morphologies of the two AAO/Si integration methods, as shown in Figure 2.7, shows the advantages of the new method. Using the direct growth of Al on Si substrate method (Figure 2.7a) with a short 1st anodization, the self-ordering is quite limited, and the pore diameters have a distribution factor (i.e. the ratio of FWHM/mean diameter) above 40 %. Partial pores are branched, and are not perpendicular to the substrate. The new method of thin AAO film bonded onto Si inherits the highly self-ordered pore arrangement caused by a long 1st anodization (Figure 2.7b). While keeping the mean diameter with the same potentiostatic voltage, the pore diameter has a narrow size distribution of about 10 %. Judged from the top-view SEM image, the pores are all perpendicular to the substrate and they form close-packed hexagonal array.

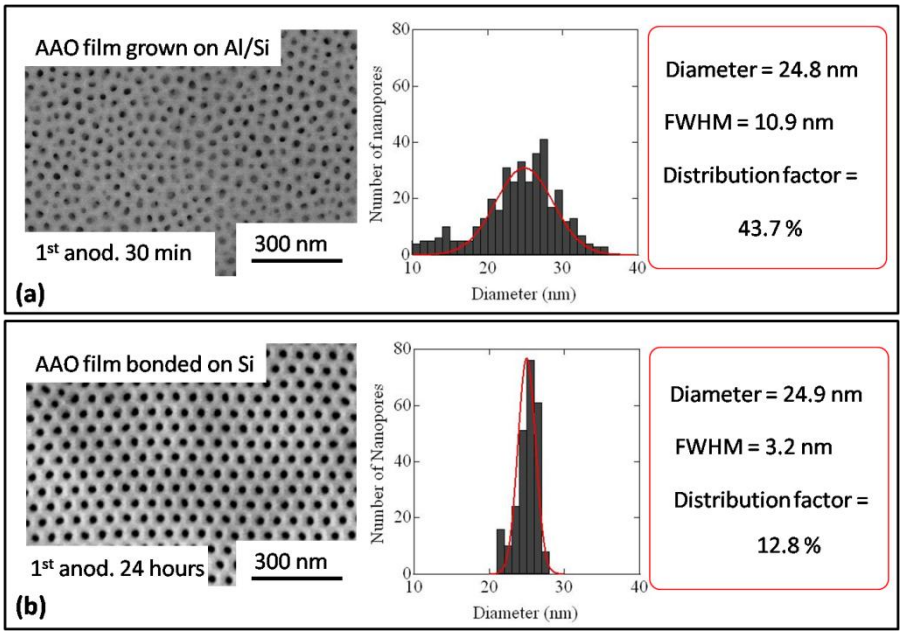

Figure 2.7 Comparison of two methods for AAO/Si integration: (a) Anodization of Al film deposited directly on Si substrate and (b) thin film of AAO bonded on Si substrate. Left top-view SEM images of pore morphologies with 1st anodization of 30 min and 24 h, right size distribution diagrams together with key parameters.

2.5 AAO-Metal-Assisted Chemical Etching

This subchapter describes a complementary method for the production of vertically-aligned semiconductor nanowire arrays. Among various fabrication methods, AAO-metal-assisted chemical etching has gained importance as a low-cost and versatile top-down method for fabricating Si and Si/Ge nanowire arrays [Hua08, Gey09]. In AAO-metal-assisted chemical etching, noble metals such as Au, Ag, and Pt with porous film morphology are used to catalyze etching of Si substrates, in a HF solution containing an oxidant. The noble metal could offer a path for hole injection from the oxidant to the Si substrate. The noble metal catalyzes reduction of the oxidant (such as H_2O_2), and therefore accelerates the chemical etching reaction [Tsu07, Lee08]. The Si substrate has a selective fast etching rate just below the noble metal coverage. Consequently, the morphology of the noble metal controls the morphology of etched Si nanostructures.

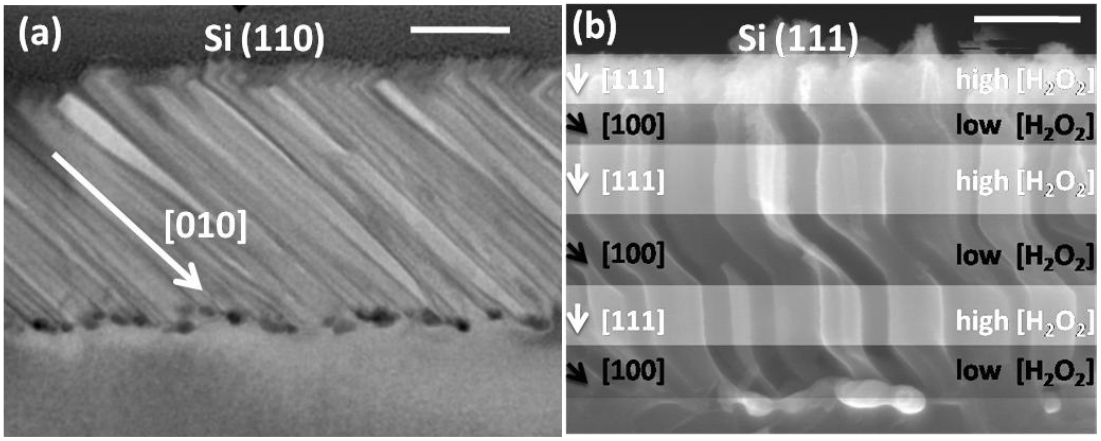

Figure 2.8 (a) Cross-sectional TEM image of Ag particles assisted etching of Si(110) substrate with [010] etching direction, the viewing is along the [001] direction, and (b) cross-sectional SEM image of orientation-modulated etching of Si(111) substrate by periodic control of oxidant concentration [Hua10]. Scale bars are 200 nm.

It was demonstrated that metal-assisted chemical etching is also influenced by crystallographic factors and the concentration of the oxidant. Etching prefers to proceed in the <100> directions, even if Si(110), and Si(111) substrates are used. Figure 2.8a is a cross-sectional transmission electron microscopy (TEM) image of Ag nanoparticles assisted etching of Si(110) substrate. The viewing direction is along Si[001]. We observed that all the Ag particles have a similar etching rate along the [010] direction. On the other hand, the etching behavior on Si(111) substrate remained confusing, since in the literature the preferred etching directions were reported as either <100> or <111> directions [Che08]. Illustrated in Figure 2.8b, a side-view SEM image, we found that the concentration of the oxidant allowed a highly controllable modulation of the etching direction of the Si(111) substrate between the [100] direction and [111] direction. In an etching solution with high concentration of oxidant (H_2O_2 0.5 M, HF 4.6 M), the etching occurred in the vertical [111] direction. Whereas in the solution with much lower oxidant concentration (H_2O_2

0.01 M, HF 4.6 M), the etching preferred the [100] direction. Based on this controllable etching, we can realize porous Si nanostructures with periodically modulated pore orientations.

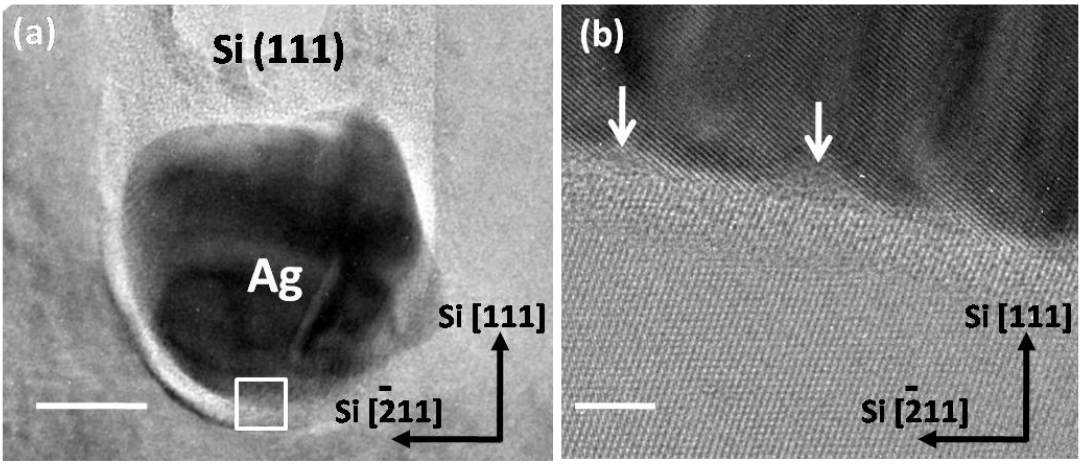

Figure 2.9 (a) Low-magnification of HRTEM image of an Ag particle etching front along Si[111] direction, the enlarged view (b) from the selected region gives the lattice patterns along the interface, with defect positions indicated by arrows. Scale bars in (a) is 20 nm, and in (b) is 3 nm.

In order to get insight into the crystallographic structure of the etching front (as illustrated in the low-magnification TEM image of Figure 2.9a), a high resolution transmission electron microscopy (HRTEM) image of the interface between Ag particle and Si(111) substrate is presented (Figure 2.9b). The Ag particle has an unsymmetric shape sitting on the top of a pore proceeding along the [111] direction. The etching front is a non-flat interface with a concave shape, where the bright contrast between Si and Ag might be due to the thinner Si or to amorphous oxide formed in between. HRTEM image gives details of crystalline lattice patterns from the selected region on the lowest position. The crossed lattice plans are Si{111} planes with a zone axis of [01$\bar{1}$] direction. The lattice of Si is tightly connected with the dark-contrast area corresponding to the lattice of the Ag crystal. From the lattice planes, we confirmed that the etching front was not porous but solid without a homogeneous oxide interlayer. We also found that along the interface, at random positions, there are amorphous voids between the two sets of lattice planes (as indicated by arrows in Figure 2.9b). We assume that this is a proof of oxidization of Si at the interface. However, it might be a result of damage caused by the ion-beam thinning process as well.

Experimentally, the Ag-particle catalyzed etching was carried out with Si(100), (110), and (111) substrates, and all SEM images showed that the <110> directions are not the crystallographically preferential etching directions. With the assistance of a thin AAO membrane bonded onto the Si substrate, the fabrication of highly ordered vertically aligned [110] Si nanowire arrays was realized by AAO-metal-assisted chemical etching [Hua09]. The schematic fabrication flow is shown in Figure 2.10a: (1) A thin AAO membrane was bonded tightly onto Si(110) substrate by the same procedures as illustrated in Figure 2.6a; (2) Subsequently, a thin (thickness around 20 nm) layer of Ag film was sputtered onto the surface of AAO/Si. With the AAO membrane as a patterned scaffold, the Ag formed a nanoporous film structure with the same pattern (as shown in

the top-view SEM image of Figure 2.10b). Meanwhile, Ag nanodots were also deposited onto the Si surface through the AAO pores (as shown in the tilted-view SEM image of Figure 2.10c); (3) Ag/AAO/Si was dipped into an etching solution, which was a water-based admixture of HF and H_2O_2. The AAO sandwiched between Ag and Si was dissolved rapidly by the HF etching through the porous Ag film. The integral Ag film fell onto the Si surface in the solution and started to assist the Si-etching process. During the Si-etching, the lateral vector of the crystallographically preferred <100> etching was suppressed by the interconnected 2-D Ag film. Therefore, the overall etching direction was restricted along [110]. The integral Ag film movement downwards into the Si(110) substrate resulted in the formation of vertically-aligned Si[110] nanowire arrays corresponding to the AAO pattern. Moreover, the isolated Ag particles at each pore bottom could etch into the Si slanting in <100> directions and drop out of the etching of the Si nanowire, leaving the top region of Si initially below the silver partially etched; (4) After the etching ceased, Ag was removed by a HNO_3-dipping. A Si[110] nanowire array was left, and the partially etched top of wires possessed inclined planes (indicated with the dashed circles in Figure 2.10d). Such details of the nanostructure also confirm that isolated Ag particles move freely in the crystallographically preferred <100> directions. The transition from step 2 to step 3 as illustrated in Figure 2.10a, can only work if the AAO is etched very homogeneously, otherwise it would result in bending and detaching of the Ag layer.

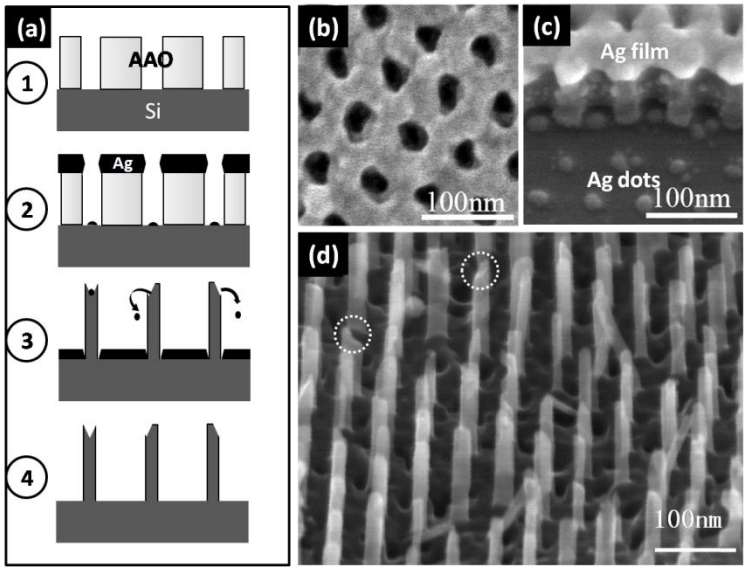

Figure 2.10 (a) Schematic fabrication flow of vertically aligned Si[110] nanowire array by Ag/AAO patterned film etching. (b) Top-view SEM image of the Ag porous film sputtered onto AAO/Si substrate, and (c) its tilted-view SEM image on which the AAO membrane was partly removed, in order to uncover the Ag dots on the Si surface. (d) Tilted-view SEM image of the etched Si[110] nanowire array after silver removal.

2.6 Conclusions

In this chapter, the electrochemical synthesis of ultrathin AAO membranes directly and indirectly

bonded on the Si substrates is studied, respectively. As a crucial part of the production of AAO directly grown on Si substrate, the growth mechanism responsible for the arch-shape barrier layer at the interface was modeled by analysis of the I-t curve combined with microscopy. The etching process of the barrier layer is inevitably accompanied by a pore widening and anodization of Si. This is a disadvantage for practical applications of AAO used as a template for nanowire growth. Therefore, in order to integrate AAO with Si, a polymer-assisted method of bonding a free-standing AAO membrane onto the Si substrate was used. The thin AAO film bonded on Si inherits a highly self-ordered pore arrangement due to a long time 1^{st} anodization. Combining the AAO/Si bonding with the metal-assisted chemical etching method, it was revealed that except for the influence of the concentration of oxidant, the crystallographic orientation of Si-etching can be well controlled by the design of interconnected Ag nanostructures.

Chapter 3

Epitaxial Growth of Semiconductor Nanowires

Integration of semiconductor nanowires on the Si platform is essential for device purposes. Therefore, it is highly required to control the crystallographic direction, positioning, diameter, and doping of large area nanowire arrays grown on Si. Innovative template-assisted bottom-up approaches to fabrication and integration of semiconductor nanowires compatible with conventional semiconductor processing will be the subjects of the following chapters. Through a detailed investigation of crystallographic relations in the well-defined nanostructures, we try to understand the different growth mechanisms and the related physics behind.

The previous chapter deals with the fabrication of ordered porous AAO nanostructures, as well as their integration with the Si substrates. This chapter will focus on the crystallographic direction control of Si and Ge epitaxial growth with the assistance of AAO templates. The growth mechanism responsible for Ge/Si wire-on-wire heteroepitaxy will be demonstrated. First, the understanding of VLS epitaxy was extended to isotopically enriched Si nanowire growth without template. Later, the growth direction control with AAO templates will be discussed related to the VLS growth mechanism. Finally, a growth mechanism for realizing a sharp interface between two different materials, Ge and Si, with a 4 % lattice misfit is presented, and the experimental results of the Ge/Si heteroepitaxy with a wire-on-wire nanostructure are shown.

3.1 Silicon Nanowire Epitaxy in Free Space

To realize the integration of Si-based 1-D nanoelectronics, the most promising approach is the epitaxial growth of Si nanowires directly on Si substrate with desired crystallographic orientation and doping. Technically, the most widely used method for the high-quality epitaxy is based on a VLS growth mechanism [Wag64, Wag65]. Especially, with the CVD growth technique, the essential concept is a metal/silicon alloy in the liquid-phase working as a medium to transform Si atoms from components of gaseous molecules into a solid crystal. The Si epitaxy is a continuous extension of Si lattice planes from the surface plane of a hydrogen-terminated single-crystal Si substrate.

3.1.1 Introduction

A typical VLS growth model using gold as catalyst is shown in Figure 3.1a. Gaseous molecules with Si components (such as diluted SiH_4, Si_2H_6, and $SiCl_4$) are introduced into a vacuum chamber, where an H-terminated Si substrate covered by a deposited thin Au film is heated above

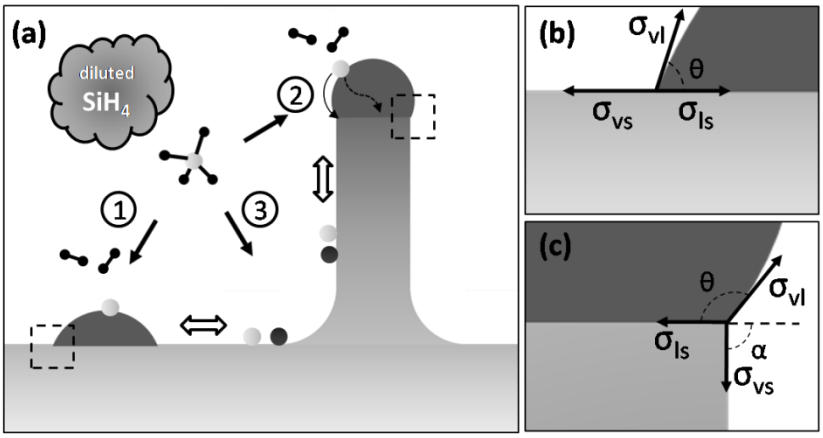

Figure 3.1 (a) Schematic of VLS growth mechanism with Au-Si droplet formation and Si nanowire epitaxy: (1) SiH_4 decomposed on Au-Si eutectic droplet; (2) Si atoms precipitate at the liquid-solid interface or at the edge at the three-phase line through bulk or surface diffusion, respectively; (3) Si atoms deposited from SiH_4 directly onto the Si surface. Expanded views of selected three-phase line junction areas in (b) initial droplet, (c) nanowire growth.

the Au-Si eutectic temperature of 363℃ [Mas90]. Let me first mention that, during the dewetting process, bigger Au-Si droplets always grow up at the expense of smaller ones in their neighborhood (Ostwald ripening) through a surface diffusion process [Fer09]. Meanwhile, traces of Au saturating the Si dangling bonds as a submonolayer film spread over the Si surface in between [Lel77]. Although studies of the wetting behavior observed a depression of Si surface where the droplets once stood [Fer08], we assume in the schematic that the liquid Au-Si alloy droplets are formed on a flat Si surface, i.e. the initial positions of Si epitaxy. With SiH_4 decomposed on both surfaces of the catalysts and the Si crystal, Si atoms can diffuse into the catalyst particle. At the same time, the by-product H_2 is taken away by the gas flow. In order to provide sufficient Si atoms to freeze out at the solid-liquid interface from a supersaturated Au-Si alloy droplet, the precursor species must decompose to some extent at the growth temperature. The nucleation model suggests that Si atoms nucleate at the edge at the three-phase boundary with propagation toward the center by the Burton–Cabrera–Frank mechanism [Bur51]. Experimentally confirmed [Sch05], the Si nanowire base during the initial phase of growth has an expanded shape as shown in Figure 3.1a. Surface thermodynamics was adopted to explain the interplay between droplet and nanowire in the VLS epitaxy [Neb03]. They presented a model of stable growth that predicts a limited range of possible contacting angles. Depicted in the expanded view of Figure 3.1b, forces at the three-phase line have mainly three components corresponding to the vapor-solid, liquid-solid, and vapor-liquid interfacial tensions, i.e. σ_{vs}, σ_{ls}, and σ_{vl}, respectively. It was pointed out that an additional line tension contribution should be considered if the contact radius is on the order of a few nanometers [Che96]. In equilibrium, the lateral driving forces for a three-phase boundary movement are balanced. Si atoms are nucleated at the growth interface by bulk or surface diffusion. In a typical VLS growth, the liquid diffusion pathways in the droplet dominate the transportation. Surface diffusion along the nanowire and on the Si substrate should be considered as well, since nanowire growth was experimentally found to be in an unsteady state [Ros05]. For example, faceting and tapering of Au-catalyzed Si nanowires were observed at

elevated growth temperatures due to surface migration of Si and Au [Sch08, Han06]. The competition between these two Si transportation processes, surface diffusion and bulk diffusion in the liquid, leads to a characteristic profile of the supersaturation as a function of the radius. The supersaturation at the rim has the highest value and thus the nucleation probability is highest at the three-phase line. If high supersaturations are used, nucleation will also occur with high probability at other positions at the interface of liquid and solid. This can result in a rough interface by polycentric nucleation. During the nanowire growth, depicted in the enlarged view of Figure 3.1c, the vapor-solid interface is inclined to the nanowire surface with an angle α, satisfying the force balance in the lateral direction as well.

One issue which is intimately connected with the Si nanowire epitaxy is the question of the relation between diameter and growth directions. In free space, metal-catalyzed Si whiskers grown by CVD prefer to grow in <111> directions [Wag64a]. Additionally, other growth directions such as <110> [Giv71], <112> [Giv75] and <100> [Sha04] were also experimentally found. A transition between different preferred growth directions was observed for epitaxial Si nanowires [Sch05a]. The preferred growth directions were <111> for large diameter (> 40 nm) nanowires, a mixture including <112> for intermediate diameters, and <110> for small diameters (< 20 nm) [Sch05a]. The influence of supersaturation on the growth direction using other conditions, like plasma excitation [Ael07], and pressure change [Lug08] were investigated to some extent. However, using the VLS growth mechanism, mainly three epitaxial growth directions on bare silicon substrates were obtained, which do not include the <100> growth directions. Considering that conventional Si micro/nanoelectronics is based on Si(100) wafers, it is meaningful to realize high-density epitaxial Si[100] nanowire arrays vertically grown on Si (100) wafers, especially for devices requiring vertical nanowire alignment. Compared with the growth in free space, it is possible to obtain controllable growth directions of embedded 1-D nanostructures with the assistance of porous templates. Lew et al. demonstrated successfully the use of AAO membranes as template for Si nanowire growth [Lew02]. The Si nanowires grown by this method had two gold tips at each ends, and the single grain Si nanowires were found with two growth directions, parallel to <100> and <211>. Shimizu *et al.* anodized an AAO membrane directly on a Si(100) substrate in order to realize the homoepitaxy of Si [Shi07]. After selective removal of the barrier layer and silicon dioxide, Au catalysts were electrolessly deposited on Si confined at the bottom of AAO pores, leading to an epitaxial growth of Si[100] nanowires perpendicular to the Si surface.

3.1.2 Epitaxy of Isotopically Enriched Silicon Nanowires

Previous works related to Si nanowire growth all referred to natural silicon (Si), which is composed of three stable isotopes: ^{28}Si, ^{29}Si, and ^{30}Si with atomic ratios of 92.28 %, 4.67 %, and 3.05 %, respectively [Ing45]. The superscripts indicate different neutron numbers in the isotopes, which could potentially change the physical properties of silicon nanowires, such as the dependence of lattice constant, phonon frequencies, and thermal conductivity on isotope content [Ple01, Cap97]. The growth of Au-catalyzed Si isotope nanowires was demonstrated by using isotopically purified precursors, and the atomic mass difference of isotopically enriched nanowires was confirmed by Raman investigation [Mou09].

The monoisotopic silane precursors $^{28}SiH_4$, $^{29}SiH_4$, and $^{30}SiH_4$ we used had an isotopic purity of (99.994 ±0003)%, (99.909 ±0.019)%, and (99.944 ±0.010)%, respectively. A 1 nm-thick Au film was deposited onto the H-terminated Si(111) substrate by the UHV thermal evaporation. Afterwards, the Si substrate was heated up to 620 ℃ and annealed for 20 min. The growth was initiated by the introduction of pure isotopic gas precursor into the CVD chamber with a steady total pressure of 0.1 ～ 0.2 Torr. Compared to growth with natural silane, the gas throughput was reduced by a factor of about 100 by closing the throttle valve between CVD chamber and turbopump almost completely. During the nanowire growth, the composition of the gaseous precursors was monitored *in situ* by a mass spectrometer, which confirmed the presence of monoisotopic molecules [Mou09]. The morphologies of isotopically enriched nanostructures were characterized by SEM.

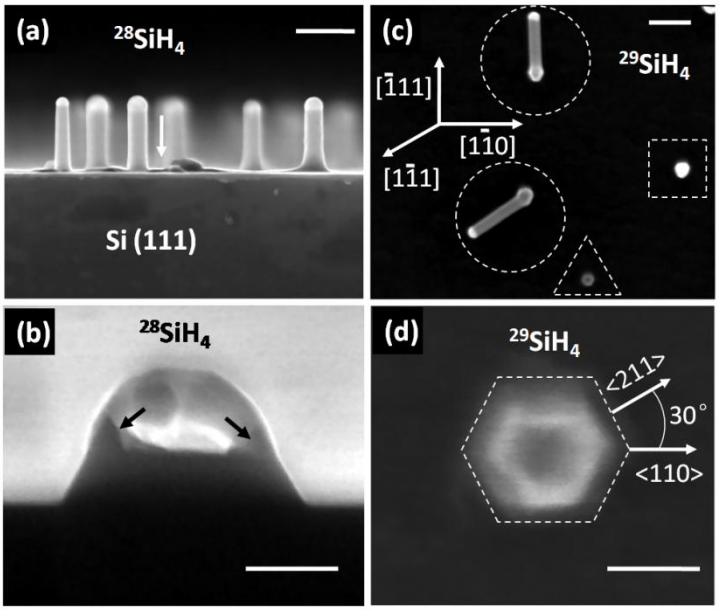

Figure 3.2 Epitaxial growth of ^{28}Si and ^{29}Si nanowires on Si(111) substrates. (a) Side-view SEM image of ^{28}Si nanowires grown in the vertical [111] direction, and (b) a typical wire observed in the initial stage of growth, the cracking line is along the Si[1$\bar{1}$0] plane. (c) Top-view SEM image of ^{29}Si isotope nanowire epitaxy. The inset scheme shows a projection of directions. The nanowires within dashed circles grew along inclined <111> directions. A vertical [111] oriented nanowire is indicated by a dashed square. (d) The enlarged view of the nanowire within the dashed triangle without Au droplet shows the {112}-type faceting of the sidewalls. Scale bars in (a), (c) are 500 nm, while scale bars in (b), (d) are 100 nm.

Figure 3.2a shows a representative side-view SEM image of ^{28}Si nanowires. The viewing direction is perpendicular to the wafer cracking plane along the [1$\bar{1}$0] direction. In this sample, the ^{28}Si nanowire exhibits epitaxial growth in the vertical [111] direction with a hemisphere Au catalyst sitting on the top. The high growth temperature (> 600 ℃) causes relatively larger Au-Si droplets, which result in nanowire diameters above 200 nm and parasitic silicon growth on both the substrate and wire side walls. We found a thin film detached from the substrate by the cracking force (indicated by a white arrow in Figure 3.2a), and some of the nanowires had tapered shape

with either increased or decreased diameter. Both observations can be explained by the surface diffusion of Au during the high temperature anneal and the growth. The silicon surface surrounding the Au droplets acts as a diffusion path for Au atoms which catalyze the Si growth. The volume variation of the Au droplet also leads to the change of its liquid-solid interface. We also found the expansion of nanowire base which is typical for the initial stage of VLS growth. A special case when the cracking of the substrate just happened in the wire, revealed a cross-sectional morphology in the SEM (Figure 3.2b). The wire base on the Si substrate has a diameter of 270 nm which is almost double of the diameter on the top-side. Instead of a completely flat interface beneath the Au droplet parallel to the Si[111] plane, the interface was found to be uptilted at both sides. The additional facets could correspond to other Si{111} planes. However, we assume that a concave shape of the liquid-solid interface was formed during the fast cooling process from 620 ℃, which is considered as a thermal equilibrium process with a decreasing Si compositon inside the Au-Si liquid (i.e. approximately from $Au_{73}Si_{27}$ to $Au_{81}Si_{19}$ [Mas90]). Note that quenching the sample is critical to maintain the composition of the droplet core close to the value reached upon annealing [Fer08]. Extra Si atoms were expelled out only in the outer region of droplet, and nucleated on the surface as a Si shell or at the edge of interface as a tapered Si ring with a decreased growth rate. Such a phenomenon was not observed experimentally with small Au droplets or at lower growth temperatures.

Figure 3.2c shows a top-view SEM image of the ^{29}Si nanowires grown on the Si(111) substrate with the same growth conditions. The bright hemispheres at nanowire tips are the Au catalysts. The diameters of the two wires within dashed circles are 200 nm and they are kinked along the [$\bar{1}$11] and [1$\bar{1}$1] directions with a rotation angle of 120 °. The wires initially grew along the [111] direction perpendicular to the substrate surface (like the ones within the dashed square and triangle), and then they switched their growth direction spontaneously to one of the other <111> growth directions [Wes97]. The faceting of sidewalls of the wires should be determined by the lowest surface energy. The nanowires observed in Figure 3.2c all exhibit the same faceting type. A top-view vertical wire without Au catalyst on the tip was enlarged in Figure 3.2d. The crystal directions of the sidewalls could be determined to be perpendicular to the {211} directions, relative to the [1$\bar{1}$0] direction of the cracking flat of the Si(111) wafer as indicated by the white arrows.

Compared with the ^{28}Si and ^{29}Si nanowires, most of the ^{30}Si nanowires observed in the 25 ° tilted side-view SEM image are grown vertically and have partially (or completely) lost their Au tips with short growth heights (Figure 3.3a). Ostwald ripening between the Au catalysts on the Si substrate results in large Au droplets, which also catalyzes the Si growth at the initial stage. However, the bigger ones continue to collect Au from the neighboring smaller ones which are consecutively consumed with Si islands or short straight tapered Si wires remaining on the substrate. Upon the extensive SEM investigations, we classified the longer ^{30}Si nanowires into mainly four types of morphologies (Figure 3.3b-e): (b) rod-like straight wire with Au tip, (c) tapered wasp-waisted wire with Au tip, (d) cone-shaped wire without Au tip, and (e) flat-top wire without Au tip. Compared with the wire in (c), the wire in (b) grew straight without obvious base expansion, due to a different coarsening process of the Au catalyst. That is, the droplet on the wire in (b) grew up at the initial growth stage which compensated the base expansion, while the droplet

on the wire in (c) grew up after the base expansion and gained Au continuously during growth with the obvious diameter increase. From the contrast patterns seen on the catalyst tip after fast cooling, the surface exhibits a disconnected Si outer shell expelled from the Au-Si alloy (indicated with a white arrow in the zoomed image shown as insert in Figure 3.3a). The wire in (d) has a shape similar to the *in situ* observation by Hannon *et al.* [Han06], that cone-shaped nanowires often had no catalyst tips with continuous loss of Au during growth. These results clearly show that Au can migrate from one nanowire tip to another at the different growth stages or in different diffusion directions during the growth. The wire in (e) is a direct proof that the droplet can first gain and then lose catalyst halfway during growth, and with the droplet coarsening away abruptly even just before the cooling stage. The flat growth front is indicated by a white arrow, while its surrounding edges (indicated by black arrows) have a strange tilt because of the rapid shrinkage of the Au-Si droplet.

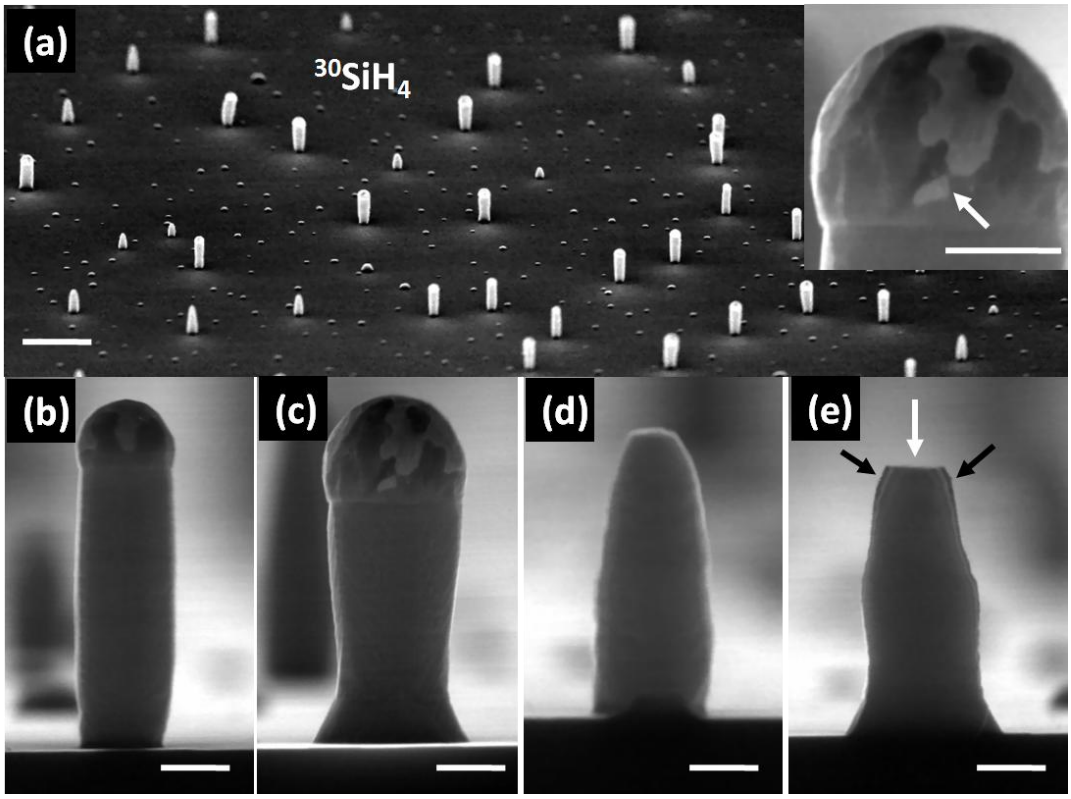

Figure 3.3 (a) 25 ° tilted side-view SEM image of ^{30}Si nanowires grown on the Si(111) substrate, bright dots dispersed on the substrate are corresponding to the short height of ^{30}Si growth with the loss of Au tips, scale bar is 1 μm, insert is a zoomed image of catalyst tip in (c). Classification of nanowire morphologies: (b) rod-like straight and (c) tapered wasp-waisted wire with Au tip, (d) cone-shaped and (e) flat-top wire without Au tip, from left to right, scale bars are 100 nm.

We have shown that all the three Si isotopes (^{28}Si, ^{29}Si, and ^{30}Si) can be grown epitaxially on Si(111) substrate with nanowire structures by a VLS mechanism, which results in growth phenomena similar with the natural Si nanowire growth. The observed Au diffusion on Si at high growth temperature, fundamentally limits the shape, length, and sidewall properties of Si isotope

nanowires. In general, these observations extend the understanding of the VLS growth mechanism into the isotopically purified semiconductor nanowire growth, although thinner Si nanowires are grown routinely using natural Si precursors at lower growth temperatures with higher densities and constant diameters. The reason for the necessity of the high growth temperature might be a detrimental effect of impurities in the isotopically enriched silanes, or that the natural silicon wires usually grow from disilane, even if the label of the container says “silane”.

3.2 Si Growth with AAO Template

Porous AAO membranes were used as templates to control the VLS-growth of Si nanowires. This technique results in both single crystal Si nanowires and polycrystalline Si nanotubes with well-controlled diameters and growth directions. Such a template-assisted synthesis provides a convenient platform to study the effect of diffusion from the catalyst surface to the growth front since the three-phase line is covered by the sidewalls of AAO different from the growth in free space. The sidewalls also change the force balance with enforcement of growth along the pores. In this study, the effect of smaller pore diameters ($25 \sim 40$ nm) of AAO on the growth of Si nanowires with or without epitaxy was investigated. The experimental results are compared with those previously reported for AAO templates with bigger pore diameters above 100 nm [Lew02, Lew03].

3.2.1 Nonepitaxial Si Nanowire Growth

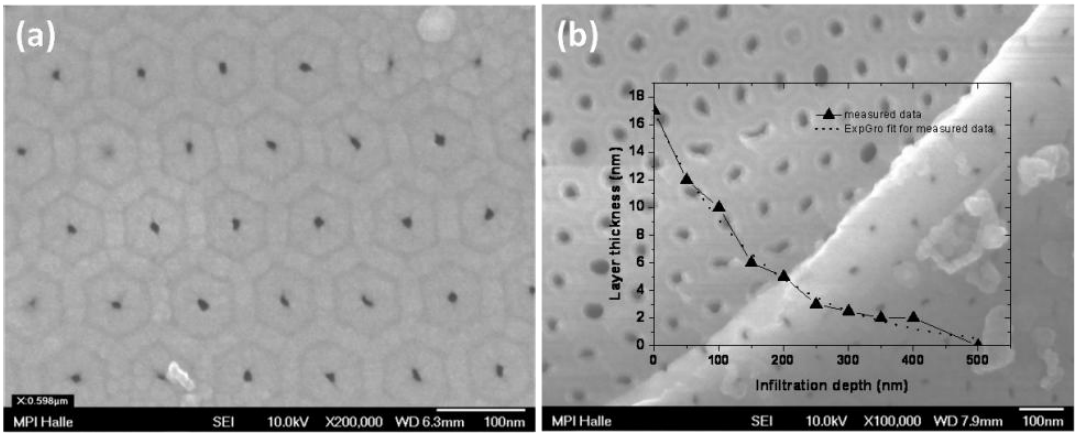

Figure 3.4 (a) Top-view SEM image of AAO (40 nm pore diameter) surface after CVD growth with SiH_4, which was covered by a Si layer, and (b) of a tilted crack surface with an insert showing the dependence of Si layer thickness inside the pores on the infiltration depth.

We adopted an electrochemical procedure to insert short Au segments inside the pores of a AAO membrane, which has been reported by Lew *et al.* [Lew03]. 40 nm pore diameter AAO membranes were synthesized by a two-step anodization, with a thickness around 20 μm [Zha10]. Au nanowires with length less than 100 nm were electrodeposited onto the Ag nanowires, which were selectively removed by 40 wt.% nitric acid afterwards. The position of Au is decided by the

length of the Ag nanowire electrodeposited inside the pore. The Au inserted AAO was transferred into the UHV-CVD system for Si growth. Due to the embedment of Au catalysts deep inside the pores, it is anticipated that such a technique can be extended to the synthesis of smaller diameter nanowires only in case that the SiH_4 molecules diffuse far into the pores and preferentially react with the Au rather than the internal sidewall or the top surface of AAO. Therefore, a search for the proper set of CVD conditions was carried out. A model of gas phase diffusion and reaction in a cylindrical pore was considered [Fit91]. Lew *et al.* predicted the SiH_4 concentration profile within a 200 nm diameter pore as a function of temperature and pressure, and suggested that lower growth temperature (< 500 ℃) and SiH_4 pressure are required for AAO with smaller pore diameter [Lew03]. However, we should also consider the time-dependent pore sealing process with a smaller pore diameter (i.e. a diameter of 40 nm as revealed in Figure 3.4). Figure 3.4a is a top-view SEM image of an AAO surface after 2 h CVD growth at 500 ℃ with SiH_4 partial pressure of 0.25 Torr. The 40 nm diameter pores were almost sealed by Si growth, with remaining inlets in the sub-5 nm scale. A tilted crack surface was checked, as shown in Figure 3.4b. The thickness of Si growth on the internal walls decreased with the depth increased. A diagram of the measured Si layer thickness at certain depths beneath the surface is shown as an insert. The measured data was fitted by the exponential growth (ExpGro of the software Origin 7.0) curve ($y = y_0 e^{+az}$, $a = 0.006$, $y_0 = 17.2$). In this case the thickness decreases with depth and the parameter of the exponential growth a was negative (unit of a -nm^{-1}).

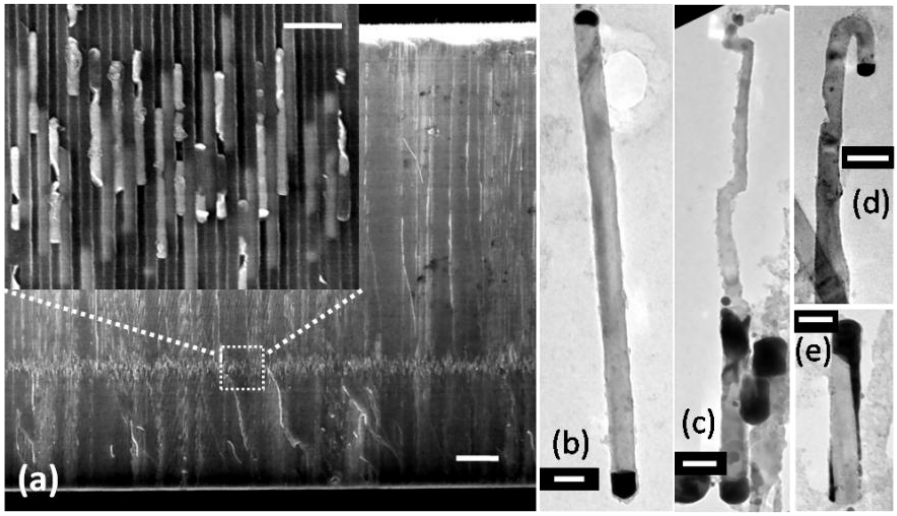

Figure 3.5 (a) SEM images of a cross-sectional 20 μm thick, 45 nm pore-diameter AAO membrane after the Si growth, the enlarged view shown as insert was selected from the dashed square region, scale bars are 2 μm and 500 nm, respectively. (b) – (e) TEM images of Si nanowires released from the template, dark black contrast corresponds to the Au catalyst with a high z value, scale bars are 50 nm.

Figure 3.5a shows the SEM image of a cross-sectional 20 μm thick, 45 nm pore-diameter AAO membrane after the Si growth, where the bright contrast layer corresponds to the Si nanowires, indicating the positions of initial Au catalysts as well. Since the shortest pathway for SiH_4 diffusion is approximately 6 μm away from the bottom surface, we optimized the CVD conditions

with a decreased growth temperature to 450 ℃, a lower SiH_4 partial pressure of 0.1 Torr, and a growth time of 30 min. Confirmed by the insert enlarged image taken from the bright layer within the dashed square region, the Si nanowires grown along the pores were capped by Au tips. Almost all the pores along the cross-sectional surface were filled with Si, seen by SEM observation. The nanowires were released from the template by a wet chemical etching in 1.0 M NaOH at room temperature, and were collected on the carbon film of special Cu grids for TEM observations. Figures 3.5b-e are a collection of diverse Si nanowire structures produced by our templated VLS growth. The initial Au segment was around 60 nm long and the length of the Si nanowire varied in relation to the Au catalyst shape. As shown in (b), a typical nanowire consists of an approximately 700 nm long central region of Si with short caps of Au at both ends. Such a nanostructure is the most abundant one produced in this process. Several wires were found with anomalous nanostructures, such as the second separation of Au catalyst during the Si growth shown in (c). Au was used partially, and a small Si nanowire grew within the confinement of the straight walls in a zigzag shape, which indicates an offset between preferred growth directions and the pore axis. A very unusual case is that the growth direction turned around oppositely inside the pore as shown in (d). The growth front beneath the Au cap is tilted with a Au layer on the Si side wall in (d), while the other Au end detached away. The structural diversity indicates that Si can nucleate at different positions of the Au–Si liquid alloy confined within the AAO pores and the growth along the pore axis is a compromise between the preferred growth directions of the nanowires and the constraint set by the wall. The observation of [100] oriented nanowires in [Car01, Lew02] is the result of this random selection process.

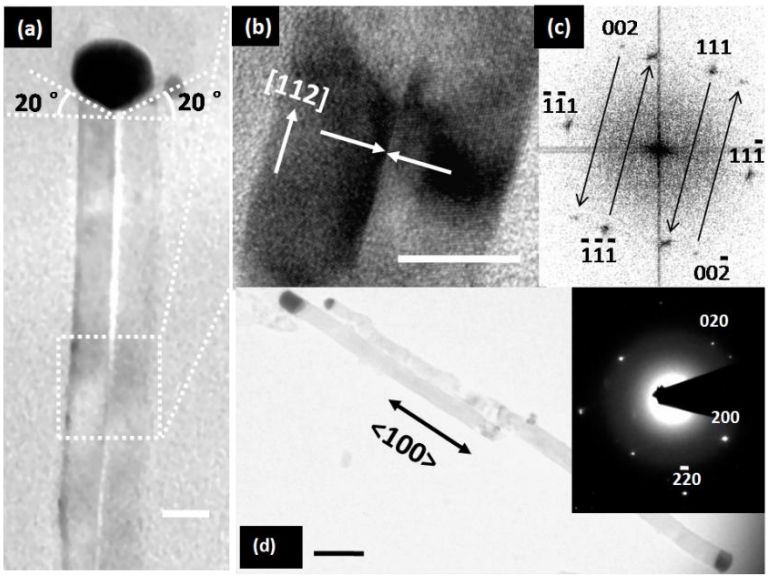

Figure 3.6 (a) Low-magnification TEM image of a bicrystalline Si nanowire connected with the Au catalyst cap, the Au/Si interface was denoted by two dashed lines with a symmetric 20 °tilting relative to the normal of the twin plane, and (b) HRTEM image of highlighted dashed square region in (a) together with (c) its indexed FFT pattern, it reveals a (11$\bar{1}$) twin plane along the [112] growth axis indicated by the white arrows in (a), scale bars are 20 nm. (d) Two wires with relatively flat Au/Si interfaces, and the inset shows SAED pattern taken from the single body of the longer one, scale bar is 100 nm.

Here we demonstrate the crystallographic orientations of Si nanowires grown in the AAO template with a smaller pore diameter (40 nm). A low-magnification TEM image of a bicrystalline Si nanowire connected with the Au catalyst cap is shown in Figure 3.6a. The diameter is 40 nm, being consistent with the pore diameter. The long bright contrast line near the central axis of the wire corresponds to a single (11$\bar{1}$) twin plane along the [112] growth direction. This was revealed by the HRTEM image in Figure 3.6b, highlighted within the dashed square region in Figure 3.6a. Its fast Fourier transformation (FFT) pattern is shown in Figure 3.6c. The contrast difference is probably caused by the bending of the wire after its removal from the AAO template. In addition, the cross-shaped Au/Si interface with a symmetric 20 ° tilt relative to the normal of the twin plane is indicated in Figure 3.6a. If this cross-shaped interface was formed as the growth front of the Si nanowire inside the pore, the Si atoms prefer forming a nucleus at an interface with a low-index crystallographic plane (such as the {111} planes). In this special case two {111} growth fronts are connected by the twin plane, while the general case is a single (111) growth plane. Thus, an axial twin plane is expected only for specific growth directions, like the [112] direction shown in Figure 3.6b. Besides, a crystalline Si nanowire belonging to the <100>-oriented type is shown in Figure 3.6d. Both wires have relatively flat Au/Si interfaces, and the inset shows an SAED pattern taken from the single body of the longer one. Indexing the diffraction pattern after calibrated rotation revealed that this wire has a growth direction of [100] with defects along the growth axis. Other growth directions, such as <111> and <110> observed frequently in free space with the similar diameters, were not observed to be dominant by both TEM and XRD characterizations. Especially, XRD has not shown a strong orientational preference, instead an almost ideal random distribution of orientations.

3.2.2 Synthesis of Polycrystalline Si Nanotubes

Using the confinement effects of the sidewalls, in the last few years, AAO template-assisted synthesis of polycrystalline Si nanotubes have been reported, such as the catalyst-assisted CVD method [Sha02], the molecular-beam epitaxy method [Joe03], and the chemical reductive deposition method [Par09]. Smaller diameters and controllable structures are still remaining challenges. A UHV-CVD method combined with a transition metal as catalyst was used to fabricate Si nanotubes with cobalt silicide ends. The growth length, diameter, and thickness of tubewalls can be well controlled by the high-quality AAO templates.

Figure 3.7 schematically illustrates the proposed growth mechanism by sketching three main procedures, i.e. step (1), step (2), and step (3). First, in step (1), a gold film was sputtered onto one side of the AAO membrane as a contacting electrode. Cobalt nanowires with a defined length were electrodeposited into the pores. The overall cross-sectional structure is shown in the SEM image of Figure 3.7(4). The average pore diameter and thickness of the as-prepared AAO templates were 45 nm and 40 μm, respectively. The electrodeposition of cobalt was performed in a galvanostatic mode with a current density of 1.5 mA cm^{-2} with an electrolyte consisting of 200 g/l $CoSO_4$ $7H_2O$ and 20 g/l H_2SO_4. A thin gold film about 300 nm in thickness covered one top-surface of the AAO template as the cathode, and a platinum mesh was employed as the anode. The different contrasts in the SEM image of Figure 3.7(4) correspond to the Co nanowires and the remaining pore spaces with Si nanotubes. Subsequently, in step (2), the AAO template with embedded Co nanowires was

transferred into the UHV system. The annealing was performed at 600 ℃ for 2 h, resulting in a homogeneous decoration of Co nanoclusters on the sidewalls and the other top-surface of the AAO template. It is well-known that the sidewalls of AAO templates contain electrolyte anions after anodization [Tho81]. These anions would attract the positively charged metallic ions on the sidewalls during the exposure to the Co-sulfate solution. During the UHV annealing process, the linked OH^- anions could reduce Co^{2+} to the metallic nanoclusters (Equa.1).

$$2Co^{2+} + 4OH^- \rightarrow 2Co + 2H_2O + O_2 \quad (1)$$

Simultaneously the byproducts (H_2O and O_2) are pumped away with a vacuum pressure less than 1×10^{-9} mbar. Such a metal decoration is similar to the Ag nanoparticles immobilized on the pore walls of AAO membrane by a spontaneous reduction process [Lee05].

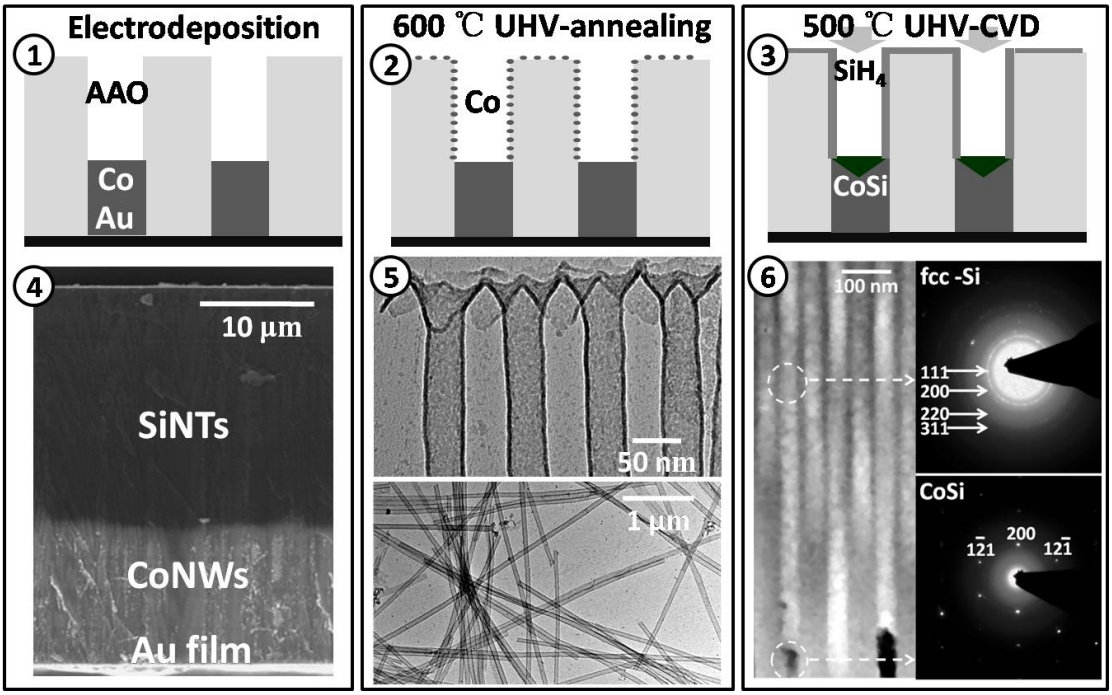

Figure 3.7 Schematic illustration of the growth mechanism of Si nanotubes by three main procedures: step (1) electrodeposition of Co nanowires into AAO pores with a Au film as counter electrode, (4) cross-sectional SEM image of a sample after CVD process; step (2) UHV-annealing produces Co nanoclusters decorating the surface of AAO, (5) TEM images of the Si nanotubes after removal of the AAO template; step (3) growth at 500℃ with SiH_4, (6) cross-sectional TEM image of as-prepared heterostructures within AAO and its selective-area diffraction patterns with indexing.

An indirect proof of a homogeneous Co decoration on the surfaces of AAO is the homogeneous Si growth. A flow rate of 20 sccm 5% SiH_4 gas was fluxed into the UHV chamber with controlled partial pressures, from 0.1 to 0.75 Torr and a fixed growth temperature of 500 ℃, the growth lasted for 30 min. The TEM image of Figure 3.7(5) was taken from a sample grown at 0.1 Torr partial pressure. It confirms the Si growth with a homogeneous thickness, even at the pore opening. The AAO was selectively etched by a 5% H_3PO_4 solution. The lower insert indicates that the nanotubes can grow up to several micrometers long with a homogeneous thickness inside the pore.

This can be understood if Co nanoclusters formed with a high density/uniformity and then worked as catalytic nuclei for the Si growth during step (3). The Si grains grown at each nucleus will get connected and will get thickened with the continuous SiH_4 decomposition. Finally, a polycrystalline Si nanotube attached tightly to the sidewalls. Meanwhile, SiH_4 reached the top-surface of the Co nanowires, resulting in the formation of cobalt silicides connected with the end of the Si nanotubes. The silicides are shown in the cross-sectional TEM image (Figure 3.7(6)) of the structures embedded in AAO template. The SAED patterns which were taken from one tube body and the end of this tube were indexed as polycrystalline Si and CoSi, respectively.

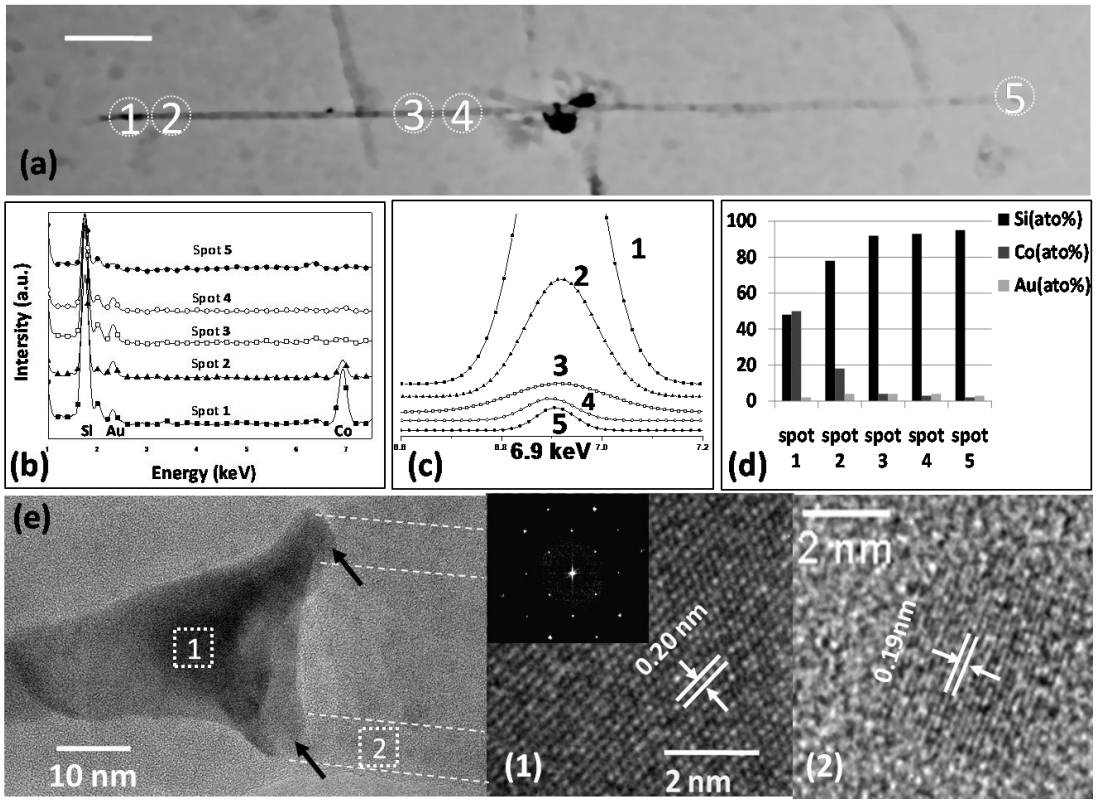

Figure 3.8 (a) TEM image of a single nanotube with one end sealed characterized by compositional measurements, the encircled numbers highlight the areas that the electron beam was focused on. (b) EDS spectra taken from the five positions, and (c) enlarged view around 6.93 keV, of the Co peak. (d) The histograms of the atomic ratio of Co, Si and Au. (e) HRTEM image of the solid end and the tube wall with enlarged inserts from selected regions, respectively, the dashed lines mark the Si tube wall [Zha10].

Selective-area energy-dispersive X-ray spectroscopy (EDS) was used to determine the compositions, at five different positions (spot1 - spot5), along one nanotube of 10 μm length, as shown in Figure 3.8a. Si, Co, and Au are all found in the EDS spectrum taken from these five spots (Figure 3.8b). An enlarged view near 6.93 keV shows the Co Ka1 peaks with higher sensitivity (Figure 3.8c). The histograms of the atomic ratio of Co and Si (Figure 3.8d) confirm that the tip consisted of Co and Si with a stoichiometric ratio of about 1:1, whereas the concentration of Co was almost constant in the tube body. It was also revealed that the observed

Au was from the background contaminations, i.e. being constant in Figure 3.8d, and the spot2 was interfered by the nearby silicide with a higher Co atomic ratio. The crystallographic structure at the end of the tube was further investigated by a high-resolution TEM image. Figure 3.8e reveals a crystalline cone at the end of the nanotube, the shoulder edge of which is connected with the Si nanotube (indicated by the black arrows). Inserts are the enlarged views of the selected dashed squares: (1) the tip consists of a single-phase CoSi with CsCl structure (ICSD database, space group pm-3m with a lattice constant a=2.816 Å), of which the calculated interplanar spacing of 0.20 nm is very close to that of the CoSi(110) plane (1.99 Å) [Kän95]; (2) the nanotube with a wall thickness of about 6 nm consists of 1～2 nm thick amorphous oxide layers and polycrystalline core, where the (220) lattice planes (d = 0.19 nm) of the crystallized silicon regions are still observed. As we know, several Co-Si alloy phases are expected to appear in sequence according to the thermal equilibrium phase diagram of Co-Si [Mas98]. In such a case, Co_2Si, CoSi and $CoSi_2$ will be formed with increasing temperature [App85]. It was reported that for a thin-film Co/Si couple, the phase appearing first at the Co/Si interface will be Co_2Si when the annealing temperature is above 350 ℃. With longer time and higher temperature, CoSi will form when additional Si is available. When the temperature is increased up to 500 ℃, the $CoSi_2$ phase can be observed [Com96]. In our experiment, the CoSi phase should be the dominant compound since it is more stable in thin films than Co_2Si and $CoSi_2$ at 500 ℃.

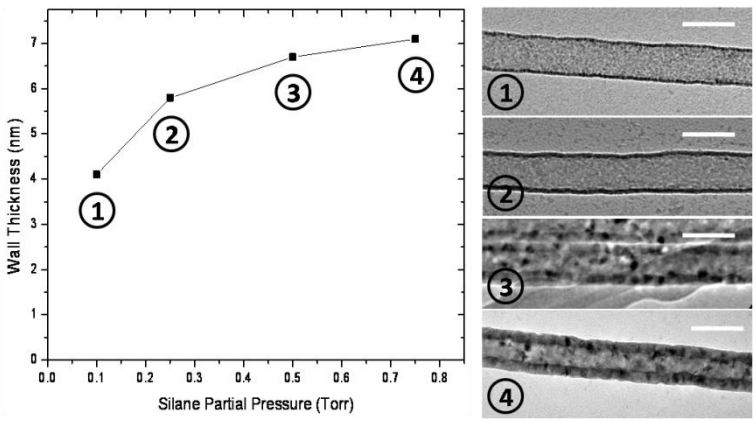

Figure 3.9 Variation of the wall thickness of SiNTs versus silane partial pressure at 500 ℃. TEM images of Si nanotubes grown at pressures from 0.1 Torr to 0.75 Torr. Scale bars are all 50 nm.

Control of wall thickness of polycrystalline Si nanotubes was achieved experimentally in 45 nm pore-diameter AAO by adjusting the partial pressure of SiH_4 at a given temperature (500 ℃) and using a fixed growth period (30 min). Obviously, there is an increase of the wall thickness with increasing pressure, shown as the measured curve and corresponding TEM images of each measured sample in Figure 3.9. With the other conditions unchanged, an increase of the SiH_4 partial pressure increases the growth rate. With the highest partial pressure of 0.75 Torr, the thickness of the Si was approaching 10 nm. The growth might be explained analogically to the experiments by Kamins *et al.*, who used a silicide forming metal as catalyst for nanowire growth [Kam00]. Initially, the metal (Ti or Co) reacts to form a silicide. With the Si supply continued, the Co nanoparticles are consumed with a higher Si supersaturation required. It is possibly related to

the limited diffusion rate of Co into the Si at a given temperature with the Co/Si system as well [Lau78]. No more Si could be catalyzed from the precursor when the wall of Si nanotube approaches its maximum thickness. The wall thickness was found to be homogeneous, although the thickness of the self-catalyzed Si growth was confirmed to be a function of distance to the AAO surface in the previous chapter.

3.2.3 Epitaxial Si Nanowire Growth

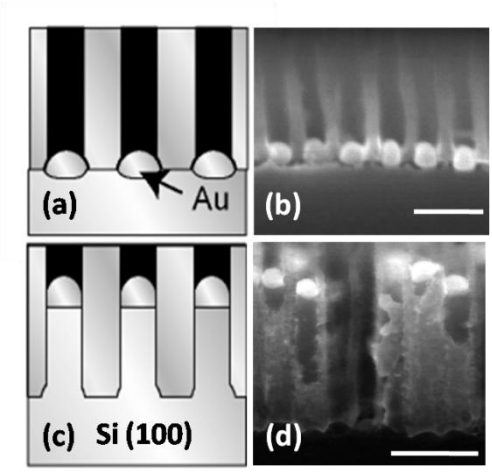

Figure 3.10 (a) schematic drawing of Au electroless plating and (c) Si nanowire epitaxial growth in an AAO template, corresponding to cross-sectional SEM images of (b) Au nanoparticles sitting on the pore bottom and (d) Si nanowires grown inside the template with Au caps, respectively. Scale bars are 100 nm.

One specific target is the realization of epitaxial Si nanowire growth on Si substrate with controllable growth direction. Moreover, the diameter of the nanowires has to be as small as possible, in particular less than 25 nm. Previous work done by Shimizu *et al.* demonstrated that homo-epitaxial growth of Si [100] nanowires on Si(100) substrate was accomplished using a combination of AAO template and UHV-CVD growth [Shi07]. The mean diameter of Si nanowires was about 60 nm, caused by a 40 V oxalic acid anodization with following pore opening process. Here, we adopted a 25 V sulfuric acid anodization for fabrication of the AAO template with smaller pore diameter. At first a AAO template was made from a Al film deposited on the Si(100) substrate. The alumina barrier layer that existed at the bottom of the nanoholes and the native oxide on the Si substrate were selectively removed by a chemical etching without losing the connection between AAO and Si, as described in chapter 2. Using the sulfuric acid, the barrier layer is thinner. It requires only 8 min pore widening, resulting in a mean pore diameter of 25 nm. Then, Au nanoparticles for the VLS growth of Si nanowires were deposited onto the Si substrate at the pore bottom of AAO by electroless plating. Figure 3.10a shows a schematic drawing of the Au electroless plating in an AAO template, and the corresponding cross-sectional SEM image (Figure 3.10b) of Au nanoparticles sitting separately at the pore bottom. The Si nanowires were synthesized by an UHV-CVD method using SiH_4 as a gaseous precursor. The growth temperature was 450 ℃, the SiH_4 partial pressure was 0.1 Torr, and the growth time was 20 min. During the growth, the Au catalysts would be fitting to the pore shape and guide the growth of Si along the pore, as illustrated in Figure 3.10c. Figure 3.10d shows a cross-sectional SEM image after the

growth with a cracked side-surface. We can distinguish arrays of Si nanowires capped by the Au catalysts on the top side, being oriented along AAO pores vertical to the Si(100) substrate.

The epitaxial growth of vertically aligned Si[100] nanowires, together with its smaller diameter less than 25 nm, has been confirmed by the analysis of HRTEM images. Figure 3.11a shows a cross-sectional HRTEM image at the base of a Si nanowire with a diameter of 25 nm. The dashed lines highlight the outlines of the nanowire on the substrate. We found an expansion on the base with a diameter of about 35 nm, which is caused by the barrier removal (see chapter 2). The FFT insert confirms its epitaxial growth along the Si[100] direction. Moreover, Figure 3.11b is an enlarged image of the interfacial area including the Si substrate and the base of Si nanowire at the position indicated as a red box in Figure 3.11a, which looks quite clear without any amorphous layer or remarkable defect. This result suggests the effective removal of oxide layers at the pore bottom on the Si substrate. The HF acid contained in the electroless Au plating solution helps to make a direct contact between Au and Si. The diameter of the Si nanowire estimated form the lattice constant of Si is around 25 nm. One problem which should be mentioned here is that, when this anodization process is done with a thin evaporated film of Al on *p*-type Si(100) wafer with a doping level up to 0.001 Ωcm, the pore formation process proceeds until it consumes all of the Al and stops at the Al–Si interface. Afterwards, both of the oxalic and sulfuric acid solutions will react unfavorably with such *p*-type Si at any anodization voltage and anodic silicon oxide is produced unless an intermediate layer was used to protect the substrate before the Al deposition. However, such a protective layer needs to be thin and homogeneous, which is technically difficult to be achieved.

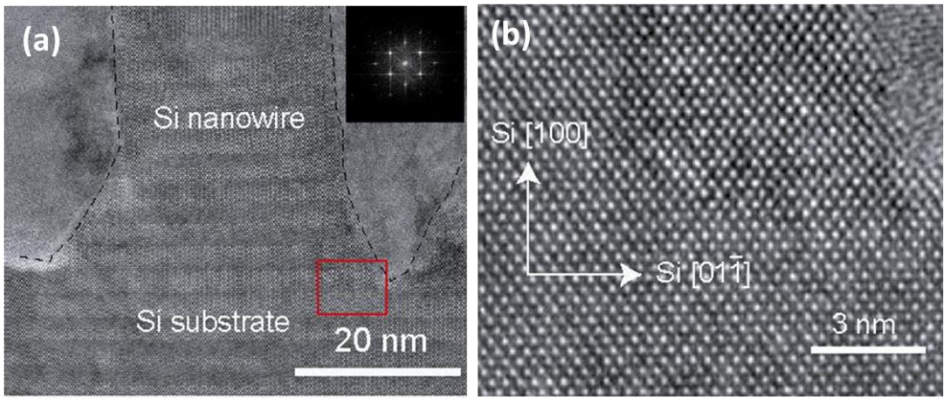

Figure 3.11 (a) Cross-sectional TEM image of Si nanowire in the bottom of AAO template viewed along the [011] zone axis, in which the dashed line shows the interface between Si and Al_2O_3, and the inset shows the FFT pattern. The area of the red box is shown in (b), an enlarged HRTEM image of the interface of Si substrate and deposited Si demonstrating high-quality homo-epitaxial growth along the [100] direction.

3.3 Ge/Si Wire-on-Wire Heteropitaxial Growth

A vertically aligned Ge/Si wire-on-wire heterostructure grown epitaxially on Si(100) substrate was achieved using a UHV-CVD method with the assistance of AAO templates. An

n-butylgermane (NBG) vapor was employed as a new safer precursor for Ge nanowire growth instead of germane. First a Si nanowire epitaxy was performed by the Au-catalyzed VLS growth described in the last section. The second step was the heteroepitaxial growth of Ge nanowires on top of the Si nanowires. The method presented here will allow producing epitaxially grown vertical nanowire arrays consisting of axial heterostructures on an arbitrary substrate, avoiding undesired lateral growth.

3.3.1 Growth Mechanism

Typically, in order to produce Ge nanowires using the VLS mechanism, GeH_4 is employed as Ge source gas, in spite of its toxicity and highly hazardous nature. The lack of an inherently safe growth process is known as one of the major limitations of commercial Ge production using CVD processes. Searching for a safer Ge source gas instead of GeH_4 is, therefore, important and highly desirable for Ge nanowire growth via VLS. In addition, a Ge/Si heterostructure on a Si substrate would be interesting if a compositionally sharp transition at the interface could be realized during the nanowire epitaxy. In this study, the epitaxial Ge nanowires inside AAO template are grown by a less toxic Ge source gas. We employed n-butylgermane (ABCR GmbH & Co. KG, $C_4H_{12}Ge$, 95 %) as source gas to grow Ge nanowires in consideration of the following properties: substantially less hazardous and less toxic compared to GeH_4, easy to handle liquid with acceptable vapor pressures at room temperature, and good thermal stability [Shi09].

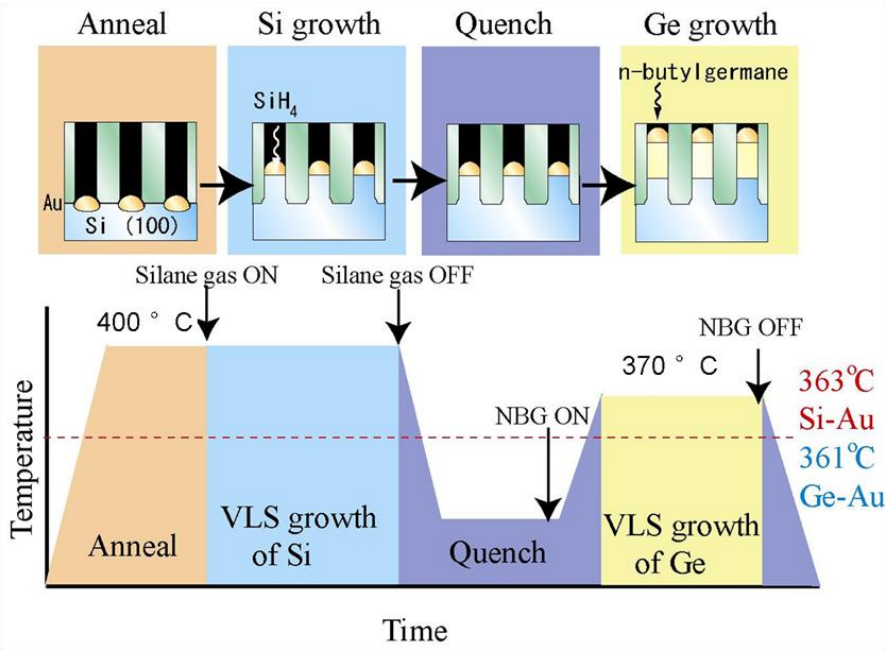

Figure 3.12 Schematic flowing chart of axially aligned heteroepitaxial growth of Ge/Si nanowire with AAO template. The dashed line indicates similar eutectic temperatures of Si-Au and Ge-Au at 363 ^{o}C and 361 ^{o}C.

The axially aligned heterostructure of Ge[100] nanowire epitaxial growth on Si[100] nanowire was realized using AAO templates. The two-step UHV-CVD procedure is illustrated in Figure

3.12. First, the AAO template was grown directly on Si(100) substrate and the catalyst particles filled in by Au electroless deposition. Then it was transferred into the UHV-CVD system. The temperature was raised up to 480 ℃ for annealing. The Au deposited at each pore bottom on the Si surface was used for the growth of Si segments. It was carried out at a temperature of 400 ^{o}C for 10 min using SiH_4 with partial pressure of 0.1 Torr. After the growth of Si, the SiH_4 gas flow was stopped. The growth chamber was evacuated down to a UHV condition again. The setting of the heater was changed to a nominal temperature of 370 ℃. Actually, the temperature of the Si substrate was decreased to a small value far below the eutectic temperature of about 360 ^{o}C by increasing the distance between substrate and heater from 1 mm to 10 cm. The quenching process is critical due to the Si solubility inside the molten Au catalyst. Subsequently, NBG vapor was introduced into the chamber, up to a pressure of 0.1 Torr. Meanwhile, the substrate was moved up to approach the heater again, and the growth of Ge nanowires continued for 7 minutes.

The phase diagram of Ge-Au (Figure 3.13a, see also Fig.A1) allows not only the VLS growth mode, but also at temperatures below the eutectic temperature Ge can be dissolved in solid Au. Wang *et al.* pointed out that the VSS growth using Al as catalyst was related to the characteristic feature of the pocket region in the Al-Si phase diagram [Wan06], which resembles the shape of Ge-Au phase diagram. Such a pocket implies that Ge can be dissolved with a small concentration in solid Au according to the temperature dependent phase boundary. At the end of the quenching process, NBG gas was introduced with moving the sample up to approach the heater until the growth temperature was higher than the eutectic temperature of Ge-Au. The transition region (indicated as dark black in Figure 3.13b) leads to the VSS growth of Ge on Si with a low Si solubility in the Au catalyst, which allows a compositionally sharp interface between Si and Ge. The continued Ge nanowire growth was in the VLS mode. Such a two-step design is in contrast to experiments using VLS growth only, where the Si dissolved in the liquid catalyst is replaced continuously by Ge and the interface is smeared out with a Ge_xSi_{1-x} interlayer formed.

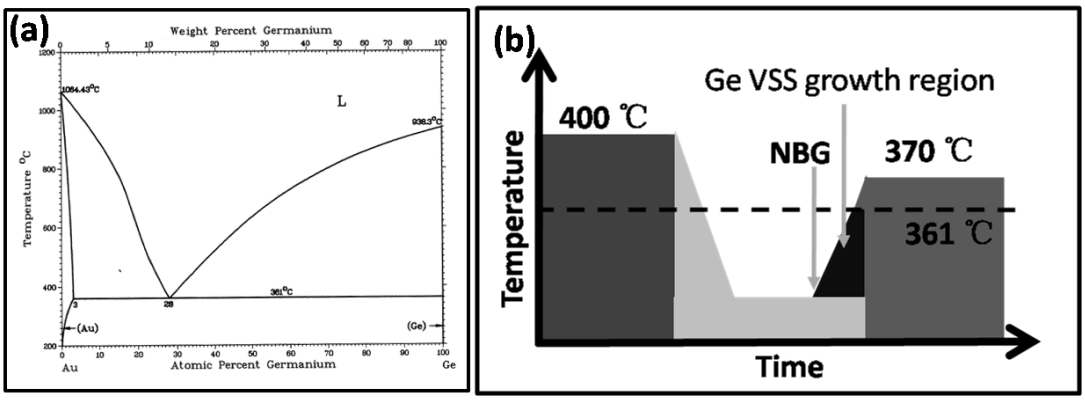

Figure 3.13 (a) The binary phase digram of Ge-Au [Mas98], the solid-solution pocket is on the very left side, the eutectic temperature is 361 ^{o}C. (b) Schematic drawing of Ge VSS growth region below its eutectic temperature, and the successive VLS growth at 370 ^{o}C.

3.3.2 Results and Discussions

Figure 3.14a shows a cross-sectional TEM image of the Ge/Si nanowires grown in the 650 nm-thick AAO template. Each nanowire has a Au cap with strong dark contrast on the top, and the wires were grown perpendicular to the Si(100) substrate. They fit to the pores with a diameter of about 80 nm, and tapered growth was not observed. Along the wire direction, there are two segments, which can be distinguished simply by material contrast in the nanowire. The interfaces between different segments were indicated with dashed lines. These segments were recognized as Au, Ge (upper wire), Si (bottom wire), and Si substrate by EDX with an energy range from 0.3 to 3 keV shown in Figure 3.14b. Although we expected a small amount of Si contained in the Ge parts, the Si peak was not observed within our limit of resolution. O and Al peaks originating from the AAO template were observed in the spectra except for the substrate part, due to the growth of the nanowires inside the pores of an AAO template. The advantage of template growth is not only controlling of growth direction and diameter of nanowires, but also avoidance of tapering and lateral heteroepitaxy during growth.

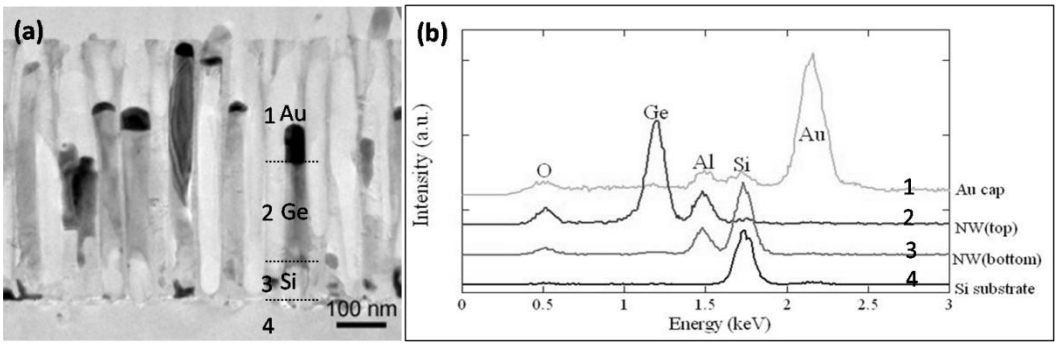

Figure 3.14 (a) Cross-sectional TEM image of the Ge/Si nanowires grown in AAO template. (b) Segments of Au, Ge (upper wire), Si (bottom wire), and Si substrate in a single nanowire were characterized by EDX with peaks marked in the spectra.

Figure 3.15a shows a HRTEM image of the interface between the Si and the Ge region. The upper part with dark contrast is Ge and the lower part is Si, respectively. The interface of every nanowire investigated showed a convex shape, which is quite unusual. The interface of axial Ge/Si nanowire heterostructures grown in free space was reported to be flat [Wen09]. The strong dark contrast at the left edge of the interface is a Au particle remaining after Ge growth. Figure 3.15b shows an image obtained by Fourier transformation filtering of an enlarged view of the area indicated as a box in (a). The Si part in the nanowire was homoepitaxially grown on the Si(100) substrate, and its growth direction was [100]. Moreover, we could observe that Ge[100] is parallel to Si[100], and the Ge part of the nanowire was grown heteroepitaxially on the Si[100] nanowire. The lattice constant of the Ge nanowire estimated from the image and using the image of the Si substrate as a reference was 0.56 nm. This is in good agreement with the bulk Ge lattice constant of 0.567 nm. The dislocations are indicated as “T” symbols. We observed two different types of dislocations at the interface, which were the expected dislocations relaxing the lattice misfit and dislocation loops. Therefore, the overall observed dislocations showed a complicated pattern, and were difficult to distinguish from each other. We think that the dislocation loops were introduced by an imperfect surface of Si due to remaining Au. Distortion contrast can be seen around such

dislocations in Figure 3.15b as dark or white contrast region.

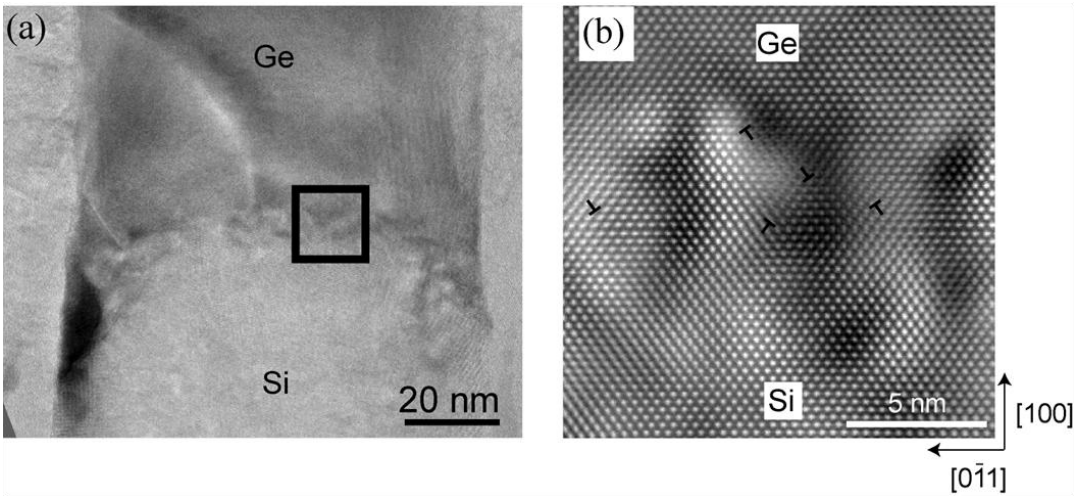

Figure 3.15 (a) HRTEM image of the interface between the Si and the Ge region, and (b) an enlarged view of the area indicated as a box obtained by Fourier transformation filtering. The "T" symbols indicate the dislocations. [Shi09]

The origin of the convex interface might be understood as a result of the special temperature sequence used during growth, which was plotted in Figure 3.12. The Si dissolved in the Si-Au eutectic is precipitated during quenching below the eutectic temperature. Supported by TEM image of Si/Au interfaces made after the growth of Si nanowires in AAO template, we found that Si atoms prefer nucleations at interfaces with low-index crystallographic planes, such as the Si{111} surfaces as shown in a cross-sectional TEM image of in Figure 3.16. The result might be a truncated pyramid of Si at the interface consisting of {111} side surfaces and a flat (100) top surface. The relative angle measured from the image is similar to the theoretical value of 55 °. The Ge starts to grow on top of the truncated Si pyramid replacing Au, as illustrated in the schematic drawing, after introducing the Ge precursor with the temperature rising again.

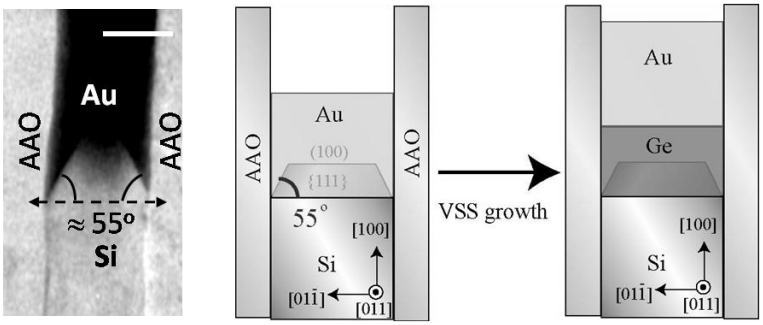

Figure 3.16 A cross-sectional TEM image of Si/Au interface after quenching in AAO template, and schematic illustration of a truncated pyramid at the Si/Au interface consisting of {111} side surfaces and a flat (100) top surface with the Ge VSS growth. Scale bar is 50 nm.

3.4 Conclusions

In conclusion, we have successfully demonstrated that Si isotope nanowires (^{28}Si, ^{29}Si, and ^{30}Si) can be grown epitaxially on Si(111) substrate with Au as catalyst by a VLS mechanism. The growth direction is similar to the natural Si nanowire epitaxy in free space. In addition, the Au surface diffusion phenomena were investigated in the high temperature growth mode. With usage of porous growth templates, Au-catalyzed Si nanowire growth inside the AAO was extended down to the 40 nm pore-diameter range, and the growth directions of non-epitaxial nanowires were found to be independent of the pore-diameter of AAO. A low-pressure CVD method combined with transition metal catalysis was used to fabricate polycrystalline Si nanotubes connected with cobalt silicide ends inside templates. The growth length, diameter, and thickness of tube walls can be well-controlled by using highly ordered AAO templates. Controllable Si nanowire homoepitaxy with 25 nm diameter was realized by Au electroless plating inside AAO pores onto a Si(100) substrate surface. The growth direction of the epitaxial wires was forced perpendicular to the substrate along the Si[100] direction. At last, a Au-catalyzed vertical Ge/Si nanowire heterostructure was grown inside an AAO membrane on the Si(100) substrate, using lowly toxic n-butylgermane as precursor. Ge nanowires could be grown at a temperature lower than the eutectic temperature, due to a VSS growth mechanism, and a compositionally sharp Ge/Si interface was prepared. The interface between Ge and Si has a distinct convex shape which was not reported in other studies of Ge/Si nanowire growth.

Chapter 4

Epitaxial Growth of Semiconductor Nanowire Arrays with Structural Control

Highly-ordered vertically aligned epitaxial Si nanowire arrays are of utmost importance for many practical applications. Especially small diameters, large-area ordering and narrow size distribution of such nanowire arrays are still challenges. In the following chapter, an innovative template-assisted bottom-up approach called Bottom-Imprint (BI) to fabricate epitaxial semiconductor nanowire arrays will be described. This new approach has several advantages compared with the direct AAO synthesis on Si substrate. Both growth directions and shapes of Si and indium phosphide (InP) nanowires could be well controlled with the BI method, which was also successfully extended to the growth of Al-catalyzed Si nanowires in the vapor-solid-solid (VSS) growth mode.

4.1 Introduction

We have used AAO membranes as the templates either isolated from Al foils or grown directly on Si substrates. Au segments were embedded at the middle (or the end) of pores by chemical methods, which were used as catalysts to crack Si precursor gas and grow non-epitaxial nanowires. Later Si nanowires were grown directly on a Si substrate with selective electroless Au plating, through which epitaxial growth of Si[100] nanowires was realized. However, the previous work in Chapter 2 had shown that the structural properties of the AAO could be strongly influenced by those two fabrication methods. For example, with anodization of thin Al films that were deposited directly onto Si substrate, the self-ordering of pores was quite limited, and the pore-diameter had a size distribution above 40 %. Partially pores were branched, and not perpendicular to the substrate. In order to remove both the barrier layer and the SiO_2 layer before Au embedment, pore widening and enlargement of pore bottom radius were inevitably introduced. In order to obtain the epitaxial growth of well-aligned semiconductor nanowire arrays on Si substrate, a highly ordered AAO membrane can be used as shadow mask during metal evaporation to form catalyst nanoparticle arrays directly on the substrate. Lombardi *et al*. prepared Au nanodot arrays on a Si(111) substrate by this method [Lom06]. They utilized the Au dots as catalysts for the VLS growth of Si after removal of the AAO membrane from the substrate, and succeeded in preparation of vertically grown epitaxial Si[111] nanowires on Si(111) substrate. Using optimized parameters (see Table 2.1) a AAO membrane usually has a perfect self-ordering with domain size of some microns after 24 h of first anodization, and is also suitable as template for nanowire epitaxy. The catalyst needs to be properly fixed at the pore bottom without any oxide layer between metal and Si substrate before CVD growth. Furthermore, although Au has dominated as the catalyst for growing

semiconductor nanowires via the VLS mechanism, it should be avoided in the CMOS fabrication. Au traps electrons and holes in Si and poses a serious contamination problem for Si CMOS processing. Therefore, CMOS compatible catalysts or catalyst–free growth techniques are required to replace Au. Epitaxial growth of silicon nanowires using an aluminium catalyst via VSS growth was already reported in the free space case [Wan06].

4.2 Bottom Imprint (BI) Method

The central idea of our approach is to bond a AAO thin-film directly onto the Si substrate with a pre-deposited catalyst film, forming tight and conformal contact. Under proper temperature and load, it is possible to imprint the bottom structure of the AAO template into the metal film to form homogeneously separated nanoparticle arrays. Finally, with a UHV-CVD process, Si nanowires grow epitaxially inside the pores with the same ordering and size distribution as the template.

4.2.1 What is Bottom Imprint?

The bottom imprint (BI) method used to synthesize ordered Si[100] nanowire arrays is schematically depicted in Figure 4.1: (ⅰ) An H-terminated Si substrate was covered with a homogeneous catalyst film through UHV thermal evaporation. The thickness of this metallic deposit is adjusted according to different pore-sizes of AAO templates. Au and Al films with about 10 nm thickness were realized with negligible surface roughness at room temperature. Thus, the Si beneath the catalyst layer is protected against the oxidization when it is taken out of the UHV chamber temporarily. (ⅱ) An AAO template with a PS protective layer is bonded onto the desired substrate as described previously in Chapter 2. The pores are filled with PS completely in order to prevent pore widening during the selective etching of the barrier layer. For an imprint purpose, the fragile AAO thin-film must be partially elastic to enable conformal contact on the substrate surface, which means that it must adapt elastically without leaving voids created by the natural roughness of the substrate and itself. A polymer material can play such a role to increase the conformal contacting area. (ⅲ) The big hardness difference between AAO and plastic metals (such as Au, Al and Ag) allows using AAO as imprint stamp. Both Young's modulus and hardness of the metals decrease as the temperature and indentation load increase and the process was optimized by slightly heating the press [Liu07]. During the hot-embossing process, only the bottom side of the press was heated, and the temperature of the sample was slightly lower than the melting point of PS (240 ℃). Thus, the metal can enter and occupy the space inside the pores by deforming the softened PS at the base. With the help of the polymer filling, the extruded metallic catalysts are isolated from each other by the alumina. The polymer prevents the oxidization of the Si surface beneath the metal layer during the whole process. Finally, the surrounding alumina wall is connected with the silicon substrate tightly, and the metal film is patterned exactly into the hexagonally ordered porous structure of the AAO template. (ⅳ) The PS is removed by organic solvents, and then the sample is inserted into the UHV system. Specific care should be taken of the removal of PS. High purity (99.9%) chloroform was used to prevent oxidation at the metal/Si interface, and the sample was transferred into the load-lock chamber immediately after the chloroform dipping. (ⅴ) The metal nanoparticles sitting at the bottom of the pores act as catalyst

to crack the precursor gas, which finally forms the epitaxial semiconductor nanowire arrays along the pores with catalyst tips. (vi) AAO can be removed with selective chemical etching, thus we finally get the vertically-aligned epitaxial nanowire arrays directly on Si substrate with the same ordering and size distribution as the template.

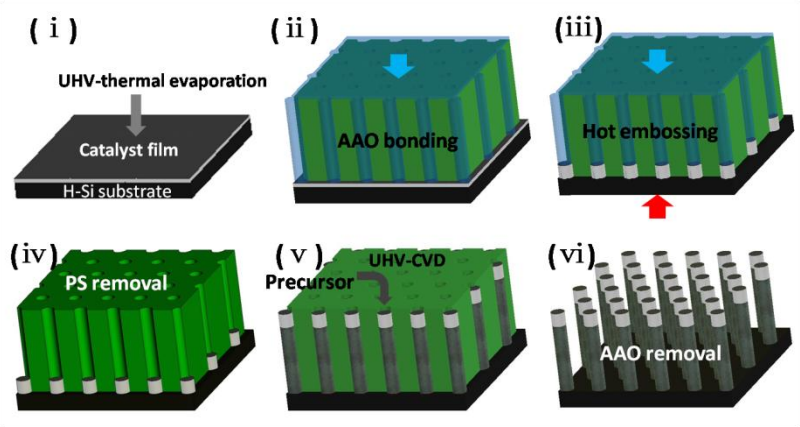

Figure 4.1 Schematic diagram of the bottom imprint method work flow: i) covering the H-terminated single-crystal Si substrate with catalyst film by UHV-thermal evaporation; ii) bonding the PS filled AAO membrane onto the catalyst film; iii) hot-embossing of the catalyst film into separated nanoparticle array by imprinting with the bottom pattern of AAO; iv) removal of the PS inside the pores by organic solution; v) epitaxial growth of semiconductor nanowire arrays inside the template with catalyst tips; vi) removal of the AAO template by selective chemical etching.

4.2.2 BI for Au-catalyzed Si Nanowire Arrays

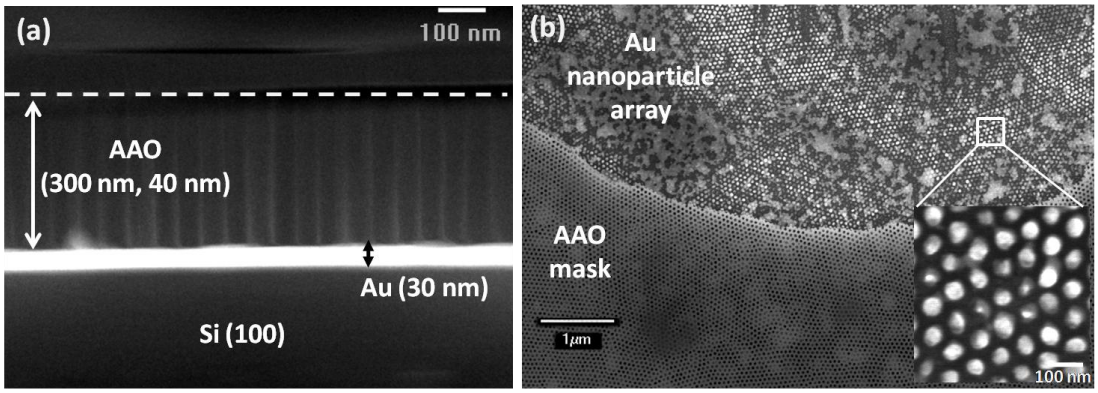

Figure 4.2 (a) Cross-section SEM image of bonded AAO thin-film on Au/Si(100) substrate before BI, the dashed-line indicates the top side of the AAO sealed by PS layer. (b) Top-view SEM image of Au nanoparticle array with AAO film partially detached by an adhesive tape, insert is an enlarged view of the selected area.

Figure 4.2a shows a cross-sectional SEM image of a bonded AAO template on Si(100) substrate before the imprint. The PS has been removed from the side surface by an O_2-plasma etching to enhance the contrast of the pore structure of AAO with SEM characterization. From the distinct contrast difference, we identify that a 300 nm thick, 40 nm pore-diameter AAO film tightly bonds with a homogeneous 30 nm thick Au film on Si substrate. No voids or remaining barrier layers were observed in between of these two bonded surfaces. After imprinting and removing of the PS from the surface, part of the AAO was detached by an adhesive tape to reveal the Au morphology underneath (Figure 4.2b). Caused by the force used during lift-off of the adhesive tape, some PS pillars are left over from the pores, remaining on the substrate as milky areas. The insert is an enlarged top-view image, of which the bright contrast corresponds to the Au catalysts formed inside the base of AAO pores, and the dark one in between is the bare surface of the Si substrate. It was confirmed that, working as a stamp, the AAO imprints on the Au film with its hexagonally close-packed pattern, and the Au nanoparticles were separated from each other since the AAO was connected with Si directly by the indentation.

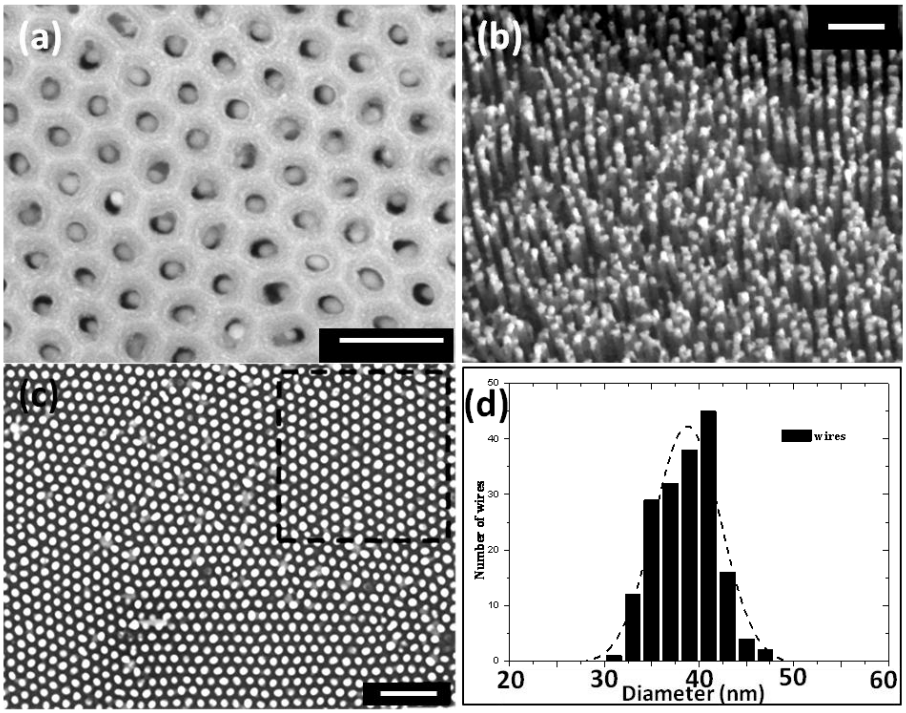

Figure 4.3 (a) Top-view SEM image of Si nanowire arrays after CVD process within AAO template, scale bar is 200 nm. (b) Side-view SEM image with 50 ° tilt and (c) Top-view SEM image of Si nanowire arrays with Au tips on Si(100) substrate after selective etching of the AAO template, scale bars are 500 nm. (d) The size distribution diagram of nanowires selected by the rectangular black dashed-line box in (c), the Gauss fit corresponds to a FWHM of 9 %. [Zha09]

In a steady VLS process, the small Au-Si liquid droplet moves upward from the Si surface along the vertically-aligned pore of AAO. For a 40 nm pore diameter and a 300 nm thick AAO template, the growth rate of Si was 10～12 nm/min at a growth temperature of 400 ^oC and a total pressure of 1.0 Torr which contained a gas mixture of 5 % SiH_4 and 95 % Ar. Figure 4.3a is a

top-view SEM image of Si nanowires grown within the template for 20 min, which almost grew out from the pores with a good ordering and a 100 % filling factor in one single domain area of the AAO template. The growth temperature should be as low as possible to avoid the parasitic deposition of silicon on the AAO surface. At 400 ^{o}C, we demonstrated that there was no obvious diameter shrinkage of the pore opening on the top surface of AAO. The black contrast in some of the pores is caused mainly by the shape of the Au tips on top of Si nanowires, which deviates from the typical hemispheres of Au-Si droplets in free space. After removal of the template, we find a high-density array of Si nanowires with various shapes of Au tips. The nanowires are grown vertically on the Si(100) substrate and some of the Au tips have cone shapes, observed by tilted-view SEM with the bright contrast in Figure 4.3b. An ordered alignment of the nanowires with a similar height was achieved by the homogeneous imprinting of the Au film into an array of separated Au nanoparticles. The tight and conformal connection of the bottom side of AAO with the Si surface prevents the agglomeration of Au-Si droplets during the heating process, which caused some problems in an earlier experiment [Shi07a]. A top-view image of the vertically aligned Si nanowire array after removing of the AAO template is shown in Figure 4.3c. We can extract the information about the size distribution from the statistics of the spot size. The diameter size distribution of the nanowires in one single ordered domain, which contained about 200 nanowires arranged in a perfect hexagonal ordering, was used to plot the diameter distribution in Figure 4.3d. The average diameter was 39 nm while keeping the 100 nm wire spacing distance unchanged, which are exactly the values of the template used. We approximated the distribution by a Gauss fit and obtained a FWHM of 9 %.

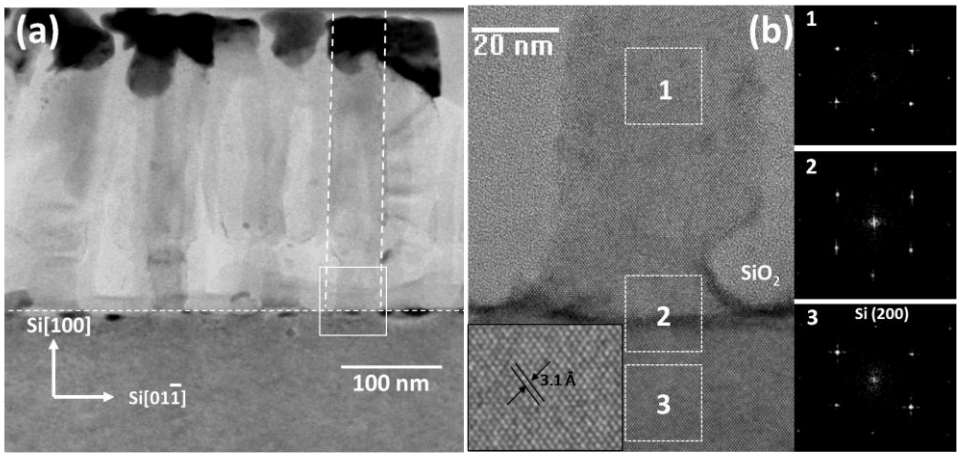

Figure 4.4 (a) Cross-sectional TEM image of the Si nanowire array after removal of the AAO template. The horizontal dashed line indicates the surface of the Si(100), and the two parallel lines outline an integral nanowire. (b) The HRTEM image shows the bottom side connected with the Si substrate, the insets from 1 to 3 are the FFTs of the numerically corresponding square regions.

Figure 4.4a shows a cross-sectional TEM image of the Si nanowire array after removal of the AAO. The horizontal dashed line indicates the surface of the original Si(100) substrate. From the contrast difference between Si and SiO_2 which was deposited as a protection layer during the focused ion-beam (FIB) sample preparation, the two parallel dashed lines indicate the sidewalls of one single Si nanowire with Au cap. All the nanowires revealed in this image have similar growth

height of about 220 nm, and are all connected to Au caps in dark contrast at the top-side. Moreover, some small Au nanoparticles were observed on the substrate, under the bottom surface of AAO (black contrast at the horizontal dashed line in Figure 4.4a), but no obvious Au was visible in the Si nanowires. The interfacial region is revealed by a HRTEM image in Figure 4.4b. The FFT patterns from three representative regions along the wire are shown as inserts, respectively: region 1 is from the growth of Si nanowire, region 2 refers to the interface between the wire and the substrate, and region 3 is from the Si substrate beneath the wire. It was confirmed that the Si nanowires grew epitaxially on the Si(100) substrate, and the growth direction was parallel to the [100] direction, since the FFT in each insert is exactly the same viewed along a [011] zone axis. A deformation observed at the bottom part of the nanowire was caused by the indentation of the AAO on Si. Thus, there is a smaller diameter at the base of nanowire, being opposite with the situation observed in AAO grown directly on Si substrate. Whereas 20 nm above the interface it grows with constant diameter during the whole VLS process with the Au tip moving up along the pore. The insert is an enlarged HRTEM from the interface, in which the Si{111} lattice planes are continuous with a measured lattice distance of 3.1Å, and no dislocations were observed.

4.2.3 BI for InP Nanowire Arrays

Most of the III-V compounds intrinsically have direct bandgaps and high electron mobilities, whereas Si has a high thermal conductivity, favorable mechanical properties, and is a relatively inexpensive substrate. Indium phosphide (InP) is a direct bandgap material with energy gap of 1.34 eV, being suitable for optoelectronic applications. Well-aligned vertical epitaxial growth of InP nanowire arrays on Si(100) substrate might be interesting for both fundamental studies and device applications. However, the principal difficulties with the integration of InP nanowires on Si substrate are differences between (100) and (111) growth, potential formation of antiphase domains and the large lattice mismatch of 8.1% between these two semiconductors. These properties resulted in non-vertical wire growth and a high density of defects which degraded the device performance [Woo08]. The growth of InP(100) nanowires on Si(100) substrate was reported [Kri04]. The density of this wires was relatively low and the positioning was random. In the following text, the BI approach is extended for the integration of III-V nanowires onto silicon substrates with a superior structural control.

A low-pressure CVD (LPCVD) method was used for the growth of InP. UHV electron-beam evaporation was used to deposit Au with a thickness of about 1 nm onto an H-terminated Si(111) substrate. The substrate was then transferred *in situ* into the UHV-CVD chamber with a background pressure less than 1×10^{-9} mbar. In order to form Au catalyst islands (30 ~ 60 nm in diameter), the sample was annealed at 550 ℃ for 15 min. For the VLS growth, the substrate temperature was then lowered to a calibrated value of 450 ℃. The group-V and group-III precursors were tertiarybutylphosphine (TBP) and trimethylindium (TMI). They were introduced successively to initiate InP nanowire growth with partial pressures of 0.01 Torr and 0.25 Torr, respectively. The growth continued for 3 min. At the end of the process, the TMI was first shut off with at the same time moving the sample far from the heater, and then the TBP was shut off with pumping down to the UHV again.

Figure 4.5 shows SEM images of InP nanowires produced by the Au-catalyzed growth on Si(111) substrate. In the top-view image (Figure 4.5a), small sphere-shaped Au particles are found at the tips of the nanowires with smaller diameters. Hexagonal {110}-type sidewall facets were observed by comparison with the cracking line along the Si($\bar{1}$10) plane. The schematic insert shows the tilted-view of a InP[111] nanowire exhibiting hexagonally-arranged {110}-type facets normal to the Si(111) plane, with a smaller diameter of Au catalyst sitting on the top. No cylindrical nanowires were found to grow with Au tips having diameters smaller than 60 nm. The tilted-view image of Figure 4.5b shows that the growth in the free space resulted in either tapered nanowires with Au on their tips or geometrically misaligned nanowires on the Si surface. Krishnamachari *et al.* reported rectangular cross-section (001)-oriented defect-free zinc blende and <111>B-oriented homoepitaxial InP nanowires with stacking faults [Kri04]. They found that the annealing of the Au droplet at the InP surface reduced the yield of InP[001] nanowires strongly. The samples we attempted to grow on Si(100) substrate with the same growth conditions as for Si(111) all failed without any distinguishable nanowire growth.

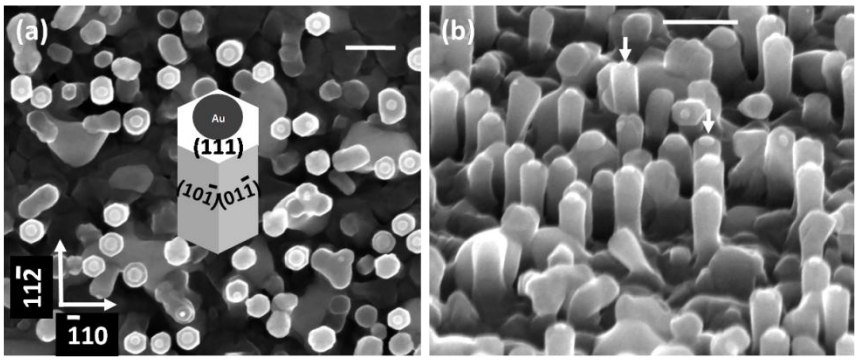

Figure 4.5 (a) Top-view SEM image of Au-catalyzed InP nanowires grown on Si(111) substrate, schematic insert of tilted-view InP nanowire with Au catalyst tip and hexagonal {110} sidewall faceting, and (b) Tilted-view SEM image with arrows indicating the Au tips. Scale bars are 200 nm.

The BI method combines the control over size, shape and ordering of the III-V nanowires with the [100] growth direction on a Si(100) substrate. With the same parameters as used for InP LPCVD growth in the free space case, a BI AAO/Si(100) substrate with Au film of 15 nm thickness was used. Figure 4.6 shows SEM images of a Au-catalyzed InP nanowire array on Si(100) grown within AAO template. The tilted top-view image of Figure 4.6a shows that, after a growth time of 2 min, the tips of the nanowires reached the pore openings with a growth length identical to the AAO thickness. The InP nanowires lost their confined shape after growing out of the pores, recognized by the increased diameter (from 50 to 70 nm). The catalyst sitting on the tip of a outgrown nanowire is in its thermal equilibrium shape as shown in Figure 4.6b. Figures 4.6 c and d show the effect of the Au film thickness on the shape of InP nanowires grown inside the AAO template which was removed by the selective chemical etching. Wires in (c) were catalyzed by a 10 nm thick Au film before BI, and the growth time was again 2 min. After removing the template, the InP nanowires had a uniform growth length of 200 nm, and a cone-shaped trunk without obvious Au tip. Whereas, using a 15 nm thick Au film with other parameters fixed, the

growth length increased to 300 nm being almost equal to the pore length, and the nanowires had a uniform diameter connected to bigger Au tips. With a low V/ III partial pressure ratio like 10, the growth ceased due to the insufficient P absorbed into the catalyst. Only islands were found sitting at the bottom of the pores, whose composition was determined to be an In-rich Au-In alloy by EDS in SEM. The lateral growth and corresponding strong tapering present after freestanding growth could be avoided by the confinement inside the AAO template.

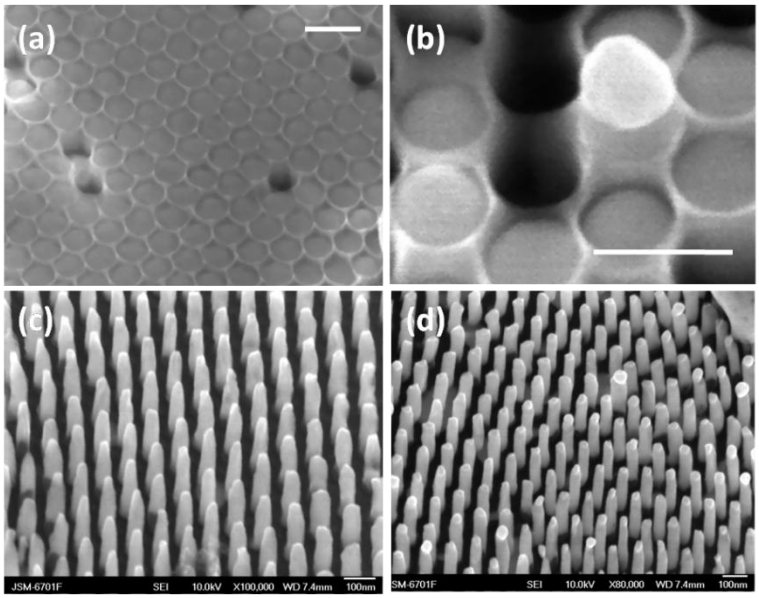

Figure 4.6 25° tilted side-view SEM images of Au-catalyzed InP nanowire arrays grown on AAO/Si(100) substrates, AAO was of 50 nm pore diameter and 300 nm thickness, at 450 ℃, V/ III partial pressure ratio of 25, and growth time of 2 min. (a), (b) Au film of 15 nm thickness, with AAO remaining after growth, scale bars are 100 nm. (c), (d) Ordered nanowire arrays after removing the template with initial Au film thickness of 10 nm and 15 nm, respectively.

4.3 BI with Al as Catalyst

In terms of device compatibility, low-temperature growth (< 450 ℃) using the solid-phase Al catalyst is very promising. Meanwhile, a well-arranged structure and a controllable crystallographic orientation are required. The discussion of the VSS growth mechanism in the publication [Wan06] was based mainly on the phase diagram Al-Si and an experimental confirmation of a solid catalyst would support the model. Freestanding Si nanowires could be grown with Al catalyst only on (111) substrates with high structural quality. The BI method uses a highly ordered AAO membrane as an imprint stamp and in principle it can be combined with other plastic metal catalysts like Al. Using the BI method, any crystallographic orientation of Si substrate can be used, and the epitaxial Si nanowire arrays are expected to be perpendicular to the substrate in a good ordering.

4.3.1 Al-catalyzed Si Nanowire VSS Growth in Free Space

For Al-catalyzed Si nanowires grown epitaxially on bare Si(111) substrate at 450 ℃, the crystallographic orientation mainly depends on their diameter. Experimentally, high-purity Al was deposited directly onto a hot Si(111) surface at 400 ℃ with a nominal thickness of 0.8 nm by MBE, and then transferred *in situ* into the UHV-CVD chamber. The growth of Si was performed with 5% SiH_4 (40 sccm), 5.0 Torr total pressure. The sample was directly heated to 450 ℃, and growth continued for 30 min at this temperature. Figure 4.7 shows that, wires of diameters greater than 20 nm prefer the perpendicular [111] growth direction, whereas wires with diameters less than 20 nm are mostly <112>-oriented. The top-view SEM image (Figure 4.7a) shows that, except for the [111]-oriented wires, as depicted schematically as insert, the <112> growth directions can be identified. {112} has two possible tilts, only one family could be observed in a cross-sectional sample. Other wires had stacking faults. The cross-sectional TEM image of Figure 4.7b confirms the <112> orientations kinked ±19 ° with respect to the normal of Si(111), in which wires with relatively smaller diameters are labeled by black dashed circles. Otherwise, wires of bigger diameters grow perpendicularly in [111] direction as in the white dashed circles. A <112>-oriented wire was investigated with HRTEM. The images with different magnification are shown in Figure 4.7c and d. It is apparent that the growth of Si nanowire is along [112] direction with a 71 ° tilt relative to the surface of Si(111) substrate. Although the wire was slightly tapered, the diameter at the base is still smaller than 20 nm. The FFT pattern obtained from the tip corresponds to an Al crystal with a planar defect visible from the contrast difference (see Figure 4.7d).

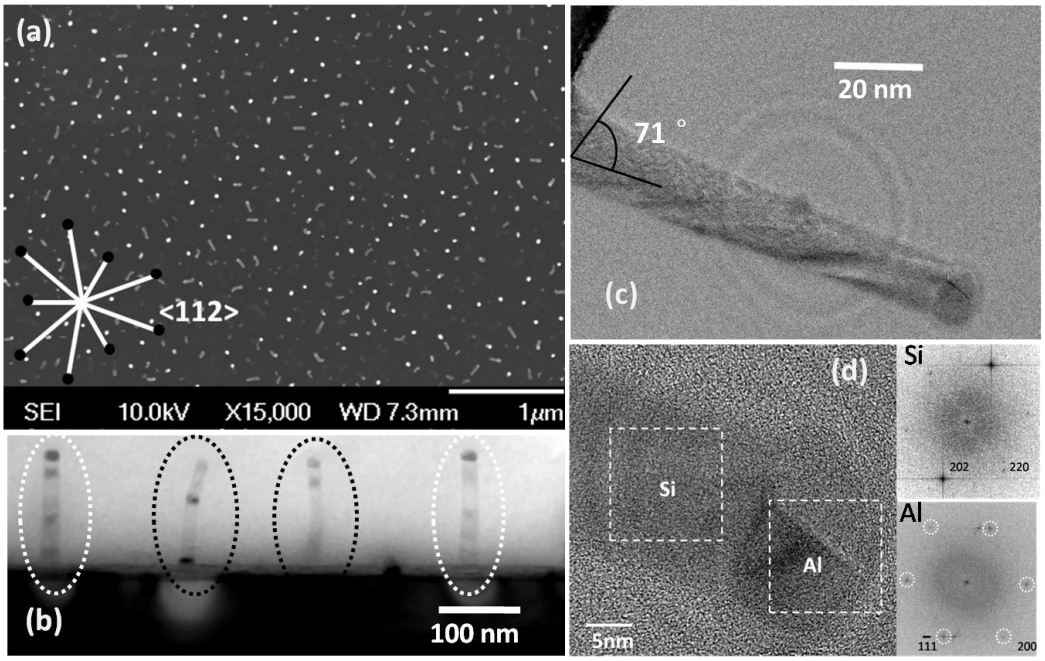

Figure 4.7 (a) Top-view SEM image of Al-catalyzed Si nanowires and schematic <112> orientations on Si(111) substrate. (b) Cross-sectional TEM image of labeled wires with <112> and [111] epitaxial directions in black and white dashed circles, respectively. (c), (d) HRTEM images taken from Si and Al crystals, respectively, and the corresponding FFT patterns from the selected square regions are shown on the right side.

We have also investigated Al-catalyzed Si nanowire growth on a H-terminated Si(100) substrate (n-doped with Phosphor, 0.001～0.005 Ωcm). Al catalysts were formed through a annealing

process at 600℃ with a 1 nm thick Al film, which resulted in diameters between 30～70 nm of the Al nanoparticles distributed on the Si surface. The growth was performed at 450℃ with the aforementioned growth conditions, and a tilted-view SEM image viewed along the {111} cracking plane is shown in Figure 4.8a. Clearly, the worm-like wires exhibit a non-straight growth behavior, presenting a lot of structural defects. No dominant vertical [100] wire was recognized. Furthermore, the top-view image of Figure 4.8b demonstrates that the Al catalysts are faceted on the tips of Si nanowires after growth. In a typical VLS growth with Au as catalyst, such faceted-shape of catalyst after growth was not observed previously. The observation of a faceted catalyst was used as an evidence of the VSS mechanism during growth [Wen09]. A large wire with 50 nm diameter shown as insert kinked and continued growth along a <111> direction, behaving similar to Au-catalyzed wires with diameters more than 40 nm [Sch05a].

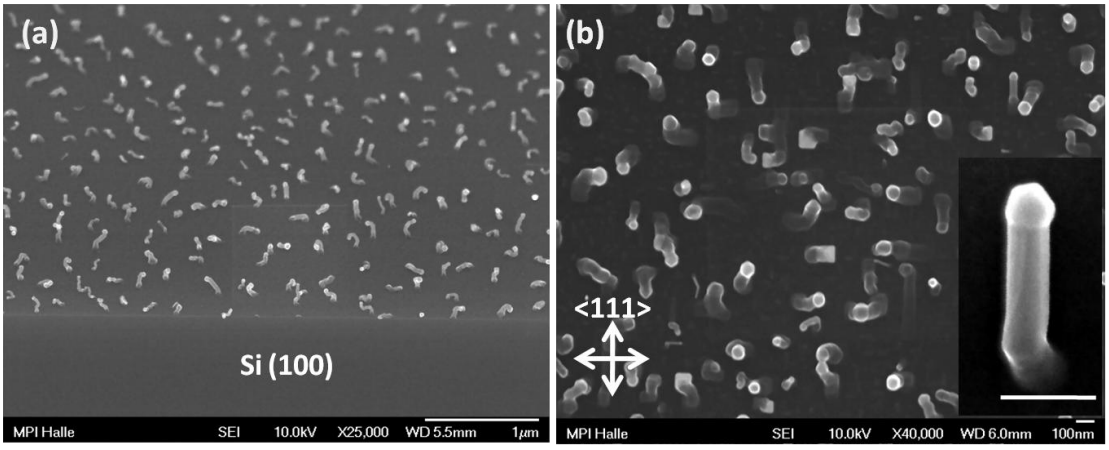

Figure 4.8 (a) Side-view with 25 °tilt and (b) top-view SEM images of Al-catalyzed Si nanowire grown on Si (100) substrate, of which the enlarged top-view of a kinked wire in <111> orientation with faceted Al tip as an insert, scale bar is 100 nm.

4.3.2 Electrical Characterization of Si Nanowires

It is well known that Au is detrimental to the performance of minority carrier electronic devices, because it drastically enhances electron-hole recombination in Si by creating deep energy levels. Recent research provided the observation of single Au atoms in Au-catalyzed Si nanowires [All08]. In contrast, Al only creates an impurity level close to the valence band of Si with better compatibility to the standard CMOS process lines although it is accompanied by a *p*-type doping [Sze68].

Electrical measurements of individual Si nanowires with both Au-catalyst and Al-catalyst grown on n-type Si(111) substrates at 450℃ were carried out by contacting them with a Pt/Ir tip, which was fitted to a micromanipulator inside a SEM at room temperature. Manipulation details can be found in reports about similar work done with Au-catalyzed Si nanowires grown by MBE method [Kan08, Bau07]. Remarkable differences in the I-V characteristics observed are revealed in Figure 4.9, on highly doped (0.001～0.005 Ωcm) *n*-type Si substrates. Both measurements showed non-linear current-voltage relations. The measured Al-catalyzed Si nanowire shows a

diode-like behavior, whereas the Au-catalyzed one shows a very weak *p*-type doping compared with other nondoped wires. The current at a forward voltage of 1 V increased from 40 nA for the Au-catalyzed wire to 2.5 μA for the Al-catalyzed one. Assuming volume conduction through the entire wire (70 nm of diameter and 250 nm length measured in SEM) without considering surface depletion, from the linear part of the I-V curve of the Al-catalyzed wire (from 0.7 to 1.0 V), the resistivity was estimated to be 0.3 Ωcm, corresponding to *p*-type Si doping with a concentration of 10^{17} /cm^3. The measured curve can be modeled by a combination of a non-ideal diode with a series and a parallel resistor, details are shown in the appendix. The measured effective doping level at room temperature is about one magnitude below the Al dopant concentration level of about 3×10^{18} /cm^3 after solid-phase epitaxy at 450℃～530℃ [Maj77], since not all of the acceptors contribute to the current flow. The Si nanowires we measured are above 60 nm in diameter, therefore, the effect of dielectric confinement [Seo06] is not discussed here. The theoretical prediction of the effect of surface states in [Sch09] can be combined with our result and delivers an order of magnitude estimation of the surface state density of 1×10^{12} eV^{-1}cm^{-2}.

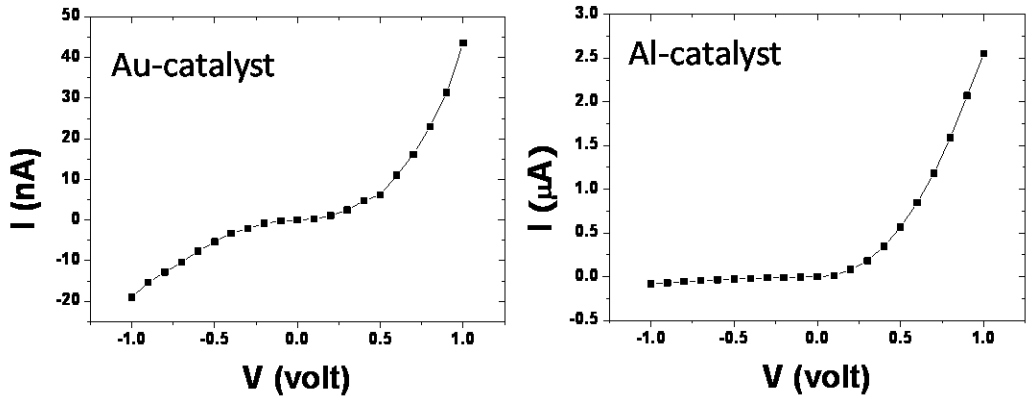

Figure 4.9 Comparison of I-V curves between Au-catalyzed and Al-catalyzed single Si nanowires grown at 450 ℃ on highly doped *n*-type Si(111) substrates. The characteristic of the Al-catalyzed Si nanowire corresponds to a diode behavior with *p*-type doping.

4.3.3 Al-catalyzed Nanowire Growth in AAO Template

Whether the *p*-type doping introduced into the Al-catalyzed Si nanowire growth is an advantage or disadvantage depends on specific applications, however, further advancement to control over the shape and crystallographic structure of these nanowires is highly essential since the electrical and optical properties strongly depend on these parameters. Vertically oriented, well-ordered nanowire arrays with Al as catalyst grown at low temperature can be potentially used in ultrahigh density nanoscale devices compatible with CMOS processing.

Figure 4.10a shows a homogeneous Al film of 20 nm thickness that was deposited onto an H-terminated Si substrate by MBE under a vacuum of 5×10^{-10} mbar. The AAO membrane with a pore-diameter of 20 nm was bonded tightly onto the Al film. The BI method is especially suited for highly reactive metals such as Al. The surface of the metal Al film is covered by a thin native

oxide layer after exposure to air, beneath which the Al and Si are protected from further oxidization after taken out of the UHV chamber temporarily. With the BI, the bottom surface of AAO is pressed into the Al layer on Si surface, and the Al film is transformed into an array of Al islands. Shown in Figure 4.10b, the AAO was removed by a gluing tape in order to reveal more morphologic details. The hexagonal imprint mark on Si is a copy pattern of the AAO bottom surface with sharp edges by the indentation. The low-magnification view shows that the homogeneous imprint area can reach up to a 10×10 μm^2 (Figure 2c). The VSS growth can start directly at the low temperature (400 ℃). This avoids the annealing above the eutectic temperature, and thus the Al remains solid throughout the growth. Compared to the bulk system Al-Si, the melting temperature of the eutectic is reduced for a diameter of 20 nm by a few Kelvin, and the formation of a metastable undercooled liquid as proposed by Wacaser [Wac09] would require heating to above 550 ℃.

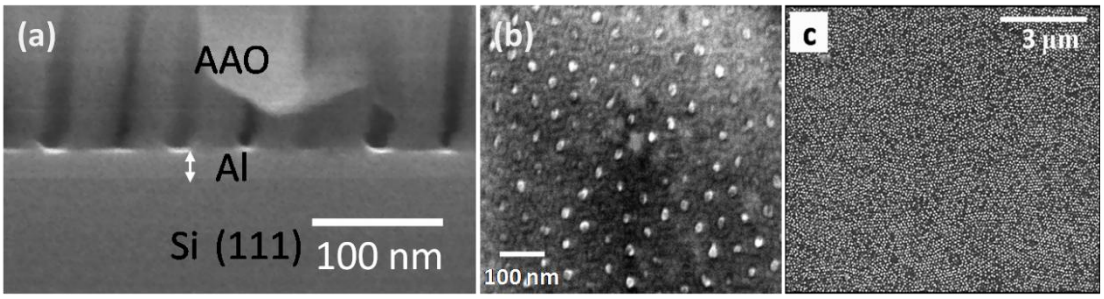

Figure 4.10 (a) Cross-sectional SEM image of sample before BI, a homogeneous Al film is sandwiched between AAO with 20 nm pore-diameter and Si(111) substrate. (b) Top-view image with AAO partially removed by adhesive tape after BI. (c) Low-magnification view of Al nanoparticle array imprinted by 45 nm pore diameter AAO with a homogeneous imprint area of 10×10 μm^2.

Figure 4.11 presents the epitaxial growth of vertically-aligned Si nanowire arrays using Al catalyst by BI on both Si(111) and Si(100) substrates. Both the positioning and crystallographic orientation are well-controlled by the AAO templates. In order to show more structural details, the AAO was selectively removed after the nanowire growth by a 5% H_3PO_4 solution, which can also partially etch away the Al remaining on the tips as well. In both the tilted-view and top-view images, the growth directions were confirmed to be perpendicular to the Si substrates. Resulting from the template confinement, close-packed hexagonal ordering of the nanowire arrays was achieved. Mean diameters of 20 ± 2 nm and 42 ± 3 nm with 10% and 8% half-width of the size distribution are shown as the insert histograms on the right side of Figure 4.11c and 4.11d, respectively. Besides the controllable diameters, another important advantage is the avoidance of lateral growth in nanowires. It was observed that there was no obvious tapering in contrast to the case of free-standing ones.

The native aluminium oxide layer hinders the Si diffusion into the catalyst. However, such a thin oxide film could be cracked by the rapid heating up to the growth temperature. The epitaxial relationship between the Si substrate and Al-catalyzed Si nanowires was substantiated by using

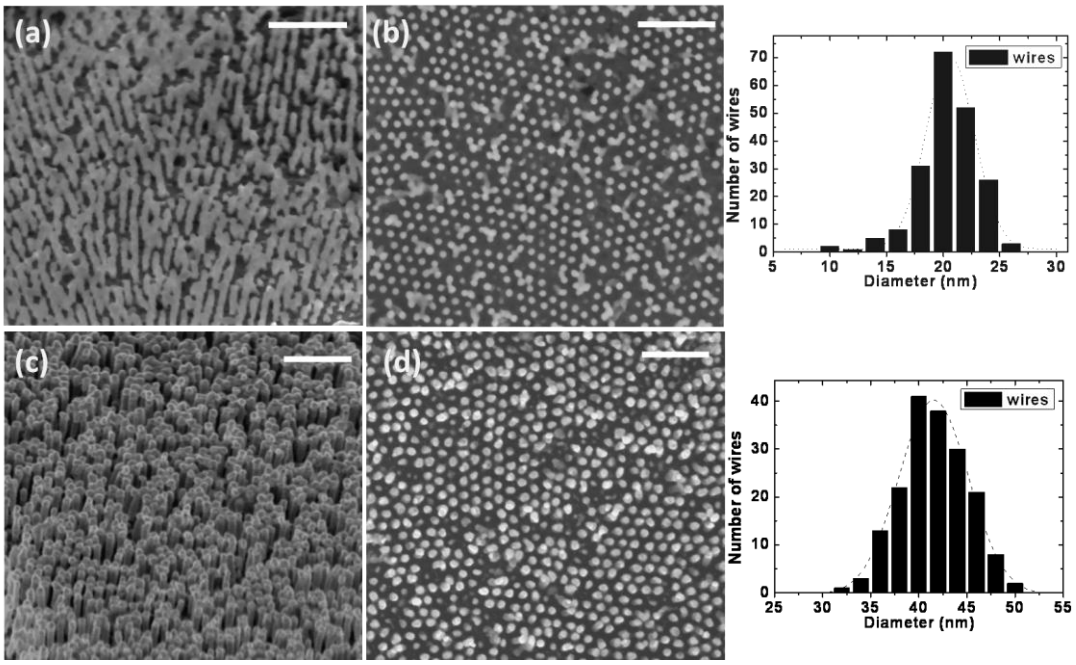

Figure 4.11 Tilted-view (a), (c) and top-view (b), (d) SEM images of Al-catalyzed Si nanowire arrays after selective etching of the AAO templates. (a), (b) are with 20 nm pore diameter AAO, 10 nm Al film on Si(111) substrate, (c), (d) are with 45 nm pore diameter AAO, 20 nm Al film on Si(100) substrate. The size distribution diagrams of 200 SiNWs measured in (b), (d) are shown on their right sides, respectively.

HRTEM microscopy. The wire-substrate and the wire-catalyst interfaces from individual wires on both (111) and (100) substrates were investigated, and shown in Figure 4.12, respectively. The wire on the Si(111) substrate has a uniform diameter of about 19 nm, and a little shrinkage of the diameter happens at the base caused by the indentation of the AAO bottom edge (Figure 4.12b). From the identical selected-area FFT patterns, it is apparent that the nanowire was grown epitaxially on Si(111) substrate in [111] direction. The wire grown vertically on the Si(100) substrate had a uniform diameter of 45 nm, which is the same as the pore-diameter of the AAO template. FFT pattern from the interfacial area also shows the epitaxial relationship between the wire and the substrate in Figure 4.12d. Distinguished from the surrounding SiO_2 amorphous layer, the tips are outlined in Figure 4.12 a and c. The absence of remaining Al catalysts on the tips was probably caused by the chemical etching of AAO. No direct proof of the lattice planes belonging to Al could be observed in both images. Nevertheless, the FFT pattern close to the tip in Figure 4.12a reveals that a twin defect exists. Comparing with wires grown in free space [Wan06], we believe that the defects are on the top-side of the wires due to the final cooling procedure. If we assume that the defects were caused by the stress difference between Al and Si due to the VSS process, such defects should be found along the whole wire, not only on the top-side. In contrast, in Figure 4.12c, two planar twin defects with a cross-angle of 71°are observed, identical with the angle between two {111} planes in [011] viewing direction. These two defects extend from the tip to the surface of the wire body, which are $(11\bar{1})$ and $(1\bar{1}1)$ twin planes marked with the arrows. We checked other wires on the TEM samples, and more twin defects were observed in the [100]-oriented Si nanowires compared with the [111]-oriented ones. Without the template

confinement, these defects cause the worm-like free-standing epitaxial growth of Si nanowire on Si(100) substrate. Stresses are caused by the lateral forces on the solid Al catalyst extruding through the inner walls of AAO while moving up along the pore. However, in the Au-catalyzed VLS growth on Si(100) using BI, as shown in Figure 4.12e, as long as the liquid Au/Si tip is inside the template, the shape of the catalyst is confined to the diameter of the pore. In this wire, the interface of Au and Si has a 22 °tilt parallel to the substrate, which is perpendicular to the [110] direction of the Au crystal estimated by the FFT patterns from Au tip in the selected region. The stresses accumulated by the confinement of AAO could be released through the deformation of liquid Au/Si alloy without introducing more structural defects into the Si growth.

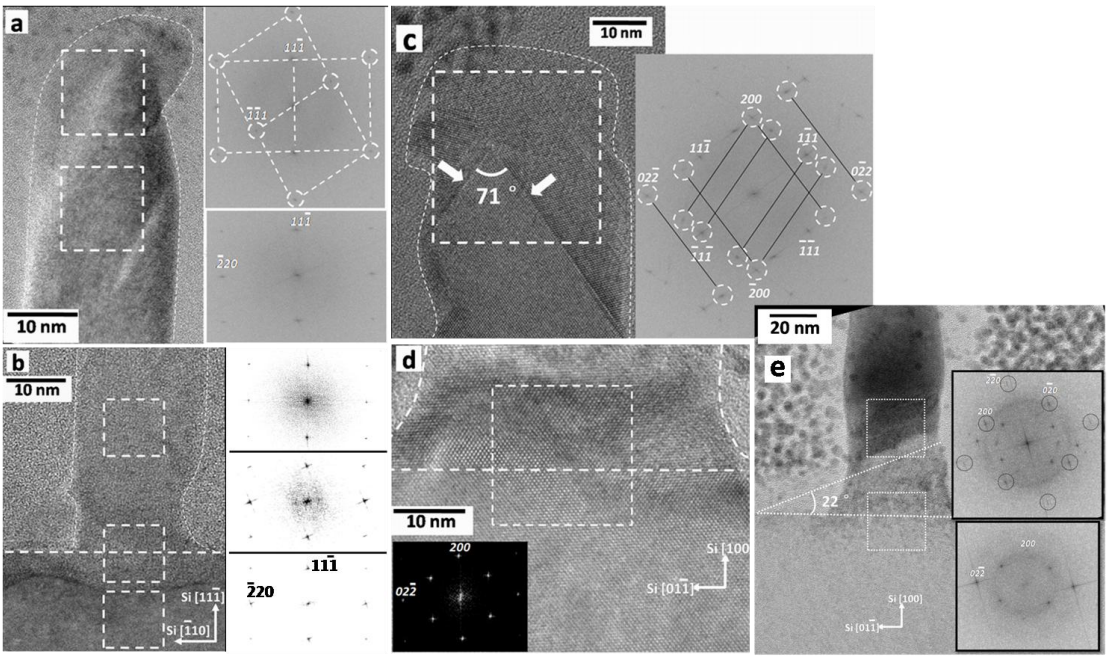

Figure 4.12 Cross-sectional HRTEM images taken with the electron beam parallel to the [112] and [011] directions of the Si(111) (a, b) and Si(100) (c, d, e) substrates respectively. Inserts of FFT patterns in all these figures are from the selected dashed square regions respectively. The outlines of wires are profiled by the dashed curves, the horizontal dashed lines at the base of wires indicate the surface position of Si substrates.

An important experimental phenomenon indirectly supporting the solid phase of Al catalyst during growth is the consistency of diameter when the nanowire grew out of the pore openings. Otherwise, the liquid catalysts always change their shapes to fit to the minimum surface energy according to the VLS mechanism. An AAO template with 45 nm pore-diameter was imprinted on a relatively rough 20 nm thick Al film on Si(100) substrate. The roughness of the Al film caused an inhomogeneous Al height distribution at the pore bottoms after BI. Therefore, some of the Si nanowires reach the pore openings first seen as the bright contrast spots in the top-view SEM image of Figure 4.13a. Figure 4.13b illustrates the morphologies of nanowires after getting rid of the support from the template on Si(100). Although the Si nanowires lost their [100] growth direction perpendicular to the substrate, and changed to worm-like shapes as the free standing ones, their diameters remained almost constant similar to the pore sizes. In contrast, a control experiment with catalyst exchanged to Au confirms that, shown in Figure 4.13c, the liquid

catalysts change their shapes into the equilibrium ones, like hemispheres, after growing out from the pores. Some of the Si nanowires with larger volume of Au at the tips increased their diameters, preferring the <111> directions instead of the [100] epitaxial growth direction inside the template. The Al catalysts, revealed by the bright dots seeing the top-view image in Figure 4.13d, keep their diameters and the vertical [111] growth direction after growing out of the pores on Si(111). These two growth mechanisms are quite different with template-control as shown schematically in Figure 4.13e. We can distinguish the difference between the VLS and VSS growth mechanisms when the wires grow out without the support of AAO. The Al catalyst tip exhibited a behavior as expected if it stayed in the solid phase with the shape preservation, as shown in the images (Figure 4.13b, d), whereas the liquid one had completely different behavior (Figure 4.13c). Therefore, we conclude that at the growth temperature of 400 ℃, the Al catalyst tip was present in its solid-phase. As long as the growth front is inside the template, only the top surface of the Al catalyst is exposed to the gas precursor. According to the model presented earlier, the VSS mechanism well explains the transport of Si atoms through the solid Al catalyst [Wan06].

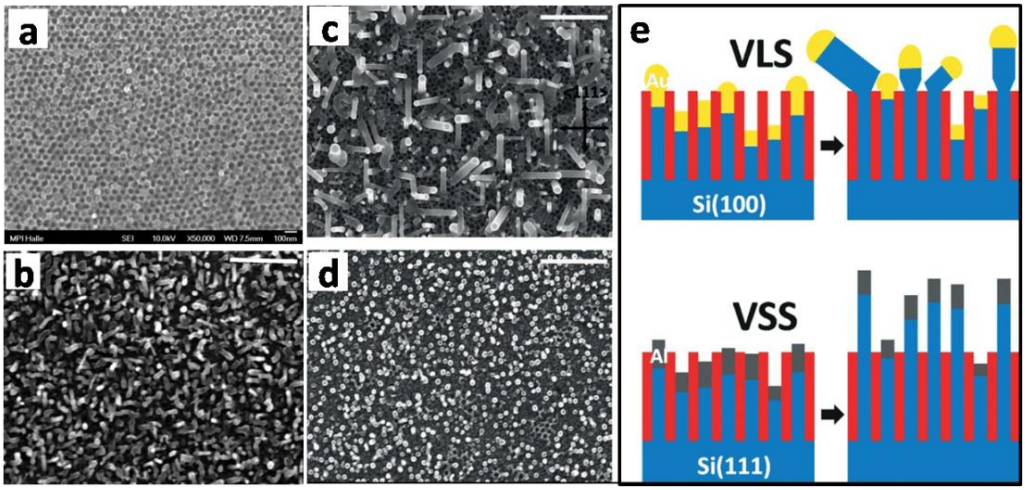

Figure 4.13(a), (b) Top-view SEM images of Al-catalyzed Si nanowire arrays grown inside and out of template on Si(100) substrate with different growth times; (c) top-view SEM images of Au-catalyzed Si nanowire arrays grown out of the template on Si(100) substrate, compared with the Al-catalyzed ones on Si(111) with same roughness of catalyst films. (e) The illustrations of the cross-sectional view on the right side show the difference between the nanowires grown out of the templates with VLS and VSS growth mode respectively, corresponding to the samples in (c) and (d). The scale bars are 1 μm.

4.4 Conclusions

The previous chapter was dealing with a technological problem, the vertical growth of epitaxial [100] silicon nanowires on (100) silicon wafers. In the present chapter, a much more controllable method to grow epitaxially high-quality semiconductor nanowire arrays on Si substrates was described. This new approach has several advantages:

1). A well-arranged positioning and control of the crystallographic orientation of the vertically

standing epitaxial semiconductor nanowire arrays on Si, and avoiding any annealing process of the AAO which was above 900 ℃ [Shi07];

2). Adjustable diameter of nanowires from 20 nm to 45 nm with a narrow size distribution (< 10%) according to specific pore diameter in the AAO template;

3). Low-temperature growth (400 ℃) of Si nanowire arrays via a solid-phase Al catalyst with diameter and crystallographic orientation control.

Controllable growth of semiconductor nanowire arrays has attracted much attention because of its importance to the physical properties of potential nanodevices. For freestanding epitaxial nanowire arrays, their growth axes are often kinked with decrease of diameters. Using BI, the ordering and crystallographic structure of vertically grown epitaxial semiconductor nanowire arrays on Si substrates can be well controlled. Using this technique, the metal catalyst film can be simply changed from Au to Al. Furthermore, evidence that the Al catalyst is in the solid state during the Si nanowire growth is also presented using BI.

Chapter 5

Templated Sub-10 nm Si Nanowire Epitaxy

The previous chapters focused on the structural control of epitaxial semiconductor nanowire growth. As promising building blocks, Si nanowires are of special interest for their potential applications in future post-CMOS technology with shrinking down the diameters to the sub-10 nm scale. If they are grown epitaxially on a suitable Si substrate, the diameter and crystallographic orientation are crucial to the nucleation and growth kinetics of Si nanowires. In this chapter, we focus on the size control of Si nanowires below 10 nm diameter, and provide crystallographic explanations for different nucleation and growth behaviors of sub-10 nm diameter Si nanowire epitaxy on Si(111) and (110) substrates.

5.1 Introduction

Using the conventional VLS free-standing growth, epitaxial Si nanowires using gold as catalyst prefer the <111> direction with larger diameters, otherwise, the <112>, <110> directions are dominant with smaller diameters [Sch05a]. In addition to the diameter effect, Hyun *et al.* showed that Au-catalyzed Si nanowires synthesized on Si(111) substrates at a total pressure of 3 mbar grew along <111> directions, while the ones grown at 15 mbar favored <112> directions with a diameter of 80 nm [Hyu09]. In general, Si nanowires of diameters below 20 nm are mostly in the <110> and <112> directions.

As usual, the diameters are scaled down when smaller catalytic seeds are used. Cui *et al.* reported non-epitaxial growth of Si nanowires catalyzed by Au nanoclusters with diameters as small as 3 nm and their growth direction was [110] [Cui01a], which was considered to approach the thermodynamically allowed minimum diameter in the VLS growth mode [Tan04]. They also suggested that the nucleation of Si happened at {111} planes which are the lowest-energy liquid/solid interfaces in both <111> and <110> growth directions [Wuy04]. However, for the epitaxial growth on a Si substrate, a high-density of sub-10 nm Si nanowires with a uniform size distribution is difficult to achieve starting from a Au thin film. One specific reason is the conventional process for the Au/Si eutectic droplets formation by annealing the Au film, during which the bigger Au/Si droplets always grow up at the expense of smaller ones in their neighborhood (Ostwald ripening). It is also difficult to achieve a uniform dispersion of Au colloids directly on an H-terminated Si substrate without using substances contaminating the substrate like lysine. Furthermore, a low-temperature and plasma-enhanced CVD process was used to fabricate Si nanowires of small diameters [Akh08, Hof03]. This technique did not yield high-quality Si nanowires with sub-10 nm diameters, since the plasma also enhanced the parasitic decomposition of gaseous precursors and introduced structural defects. The control of epitaxial growth directions for sub-10 nm diameters is missing as well. In this chapter, both bio-template of

Apo-ferritin and a hot-surface MBE method are investigated for scaling down the Au catalyst into the desired size scale. The size distributions of specific epitaxial directions on different Si substrates were analyzed using HRTEM data.

5.2 Apo-ferritin as Bio-template for Si Nanowire Growth

Different from artificial porous templates, proteins are synthesized according to the information stored in DNA. In nature, a large number of identical protein molecules can be harvested at a relatively low cost. Owing to this feature, proteins are investigated as highly efficient bio-templates to synthesize nanostructures with sizes of only a few nanometers. Some proteins have an ability called "biomineralization" that creates inorganic materials on their surfaces. Ferritin is a large globular protein used for iron storage and is present in many organisms. Hollow spheres called apo-ferritin can be easily prepared by releasing the iron containing core from the cavity. The sphere consists of 24 subunits with an outer diameter of 12 nm and an inner cavity of 7.6 nm. The junctions of the subunits provide 14 channels, 0.3-0.4 nm in diameter, which perforate the protein shell and serve as pathways between the exterior and interior [For84]. This feature enables us to use apo-ferritin molecules as highly accurate templates to synthesize metallic nanoparticles which could potentially be used as catalyst for sub-10 nm diameter Si nanowire growth. Ge nanowires were grown via the biotemplating of very small sized (5-20 nm) Au nanoparticle catalysts [Sie08].

5.2.1 Integration of Au-apoferritin on Si Substrate

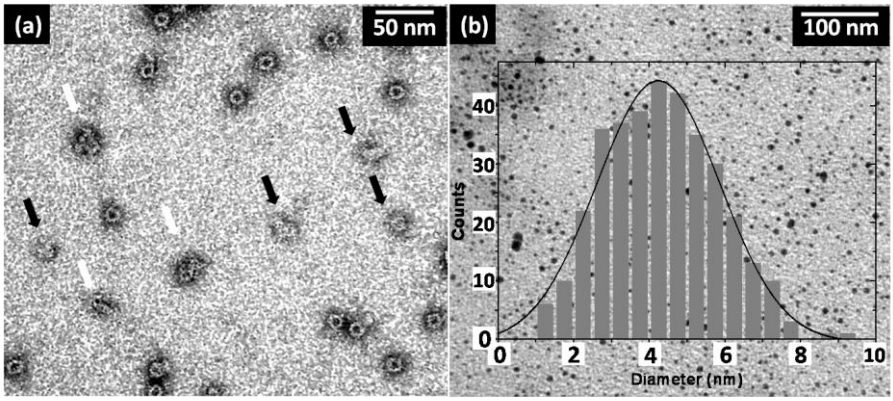

Figure 5.1 (a) TEM image of Au nanoparticles synthesized in apo-ferritin cavities stained negatively by uranyl acetate, and (b) the size distribution of the obtained Au nanoparticles calculated from a non-stained TEM image.

To synthesize metallic nanoparticles inside the apo-ferritin molecules using an aqueous solution-base method, additions of metal ions together with reductants are required. 5 mg/ml apo-ferritin was incubated with $HAuCl_4$ in a buffer solution at pH = 7.4. The solution was mixed in darkness at 30 ^{o}C for 1 hour to transport Au ions into the cavity, then excessive salt was removed with a Desalt Spin Column (Thermo Scientific Pierce) to prevent the formation of metal

particles outside the protein shell [Zha07]. Afterwards, the desalted apo-ferritin was immediately mixed with $NaBH_4$ and stirred for 30 min at 30 ^oC. This reduced the Au(III) ions inside the cavity to yield the Au nanoparticles. The excessive reducing agents were removed with spin columns after the reduction.

Low-voltage TEM (JEOL JEM-1010) was used to characterize the structure of bio-templated Au nanoparticles, due to the stronger contrast of low atomic number materials at low voltage. The molecules were dropped onto a carbon-coated copper grid. Figure 5.1a shows a TEM image of the Au-encapsulating apo-ferritins, which were stained with 1.5% uranyl acetate. The uranyl acetate was excluded from the cavity, and introduced a negative contrast difference to identify the protein of apo-ferritin. It confirms that the small Au nanoparticles were reduced inside the cavity, corresponding to the black dots with ca. 4 nm in diameter. It is worth mentioning that a treatment of the solution with spin columns prevents forming of Au nanoparticles outside the apoferritin. This procedure was previously reported by Zhang *et al.* [Zha10a]. However, even with optimal conditions, the filling factor is not 100 %. As marked by the black arrows, in some apo-ferritins the Au cores were absent. The ones indicated with the white arrows showed a cavity filled with much smaller Au nanoparticles (1～2 nm). However, the outer surfaces were all free of reduced Au. With increased incubation time within Au ion solution, we postulate that more Au ions would be transported into the cavities with increased filling factor, but also augment the competition of Au ions binding onto the outer surface. Thus, in order to avoid the formation of exterior the Au nanoparticles the incubation time needs to be limited. The non-stained TEM image shown in Figure 5.1b was used to calculate the size distribution of Au nanoparticles. The insert histogram of particle size gives a broad size distribution with mean diameter of 4.4±1.1 nm. This value appears reasonable. Assuming a saturation of the cavity with the hydrated gold complex and the larger volume of the complex compared to atomic gold, after reduction an approximate particle size of around 4 nm is expected. In nature, the iron(III) oxyhydroxide nucleated inside ferritin was found to be hydrophilic [Pie01]. Therefore, within the confinement of the ferritin cavity, the nucleation of $NaAuCl_4 \cdot xH_2O$ ($x \geq 2$) was assumed to occupy the whole space. The unit cell volumes of $KAuCl_4$ and Au are 674.96 $Å^3$ (PDF 70-1363) and 67.85 $Å^3$ (PDF 04-0784), respectively. The volume ratio between the dihydrate Au salt and the reduced Au is approximately 10:1. Considering the cavity of apoferritin having an inner diameter of 7.6 nm, the size of the synthesized Au nanoparticles is expected to be around 4 nm ($7.6/10^{1/3}$). The process related size limitation can be circumvented with lower precursor concentrations for smaller particle sizes or repeated steps for larger ones. Therefore, with a refined size of Au nanoparticles as catalysts, we tried to grow the diameter-controlled Si nanowires directly on Si substrate in sub-10 nm scale.

For the immobilization of Au nanoparticles as catalysts onto a Si substrate, a high-density of Au-apoferritin molecules were first adsorbed onto the pretreated surface by the modified bionanoprocess, as reported by Yoshii *et al.* [Yos05] and Oliveira *et al.* [Oli07]. In this bionanoprocess, illustrated in the schematic fabrication-flow of Figure 5.2, a *p*-type Si(111) substrate was passivated with Piranha solution (1:3 H_2O_2/H_2SO_4) for 2 h. Then, after cleaning with deionized water and drying with nitrogen, the surface was silanized with 10% 3-aminopropyltriethoxysilane (APTES) in toluene for 12 h at room temperature. To bind with dehydroascorbic acid, it was put into saturated solution of L-ascorbic acid (Vitamin C) in 90%

ethanol and 10% methanol. After 30 min the sample was washed with ethanol and dried in air. For the immobilization of Au-apoferritin, the dried wafer was incubated with aqueous solution of Au-apoferritin over night at 4^{o}C. The sample was then washed with flowing deionized water to remove non-bonded Au-apoferritin.

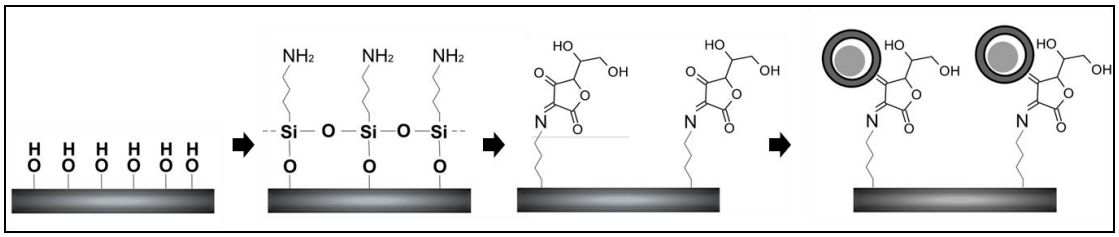

Figure 5.2 Schematic flow chart of immobilization of Au-apoferritins on Si substrate: 1. oxidative activation of silicon wafer surface with Piranha solution; 2. silanization with 3-aminopropyltriethoxysilane; 3. binding dehydroascorbic acid; 4. immobilization of Au-apoferritin.

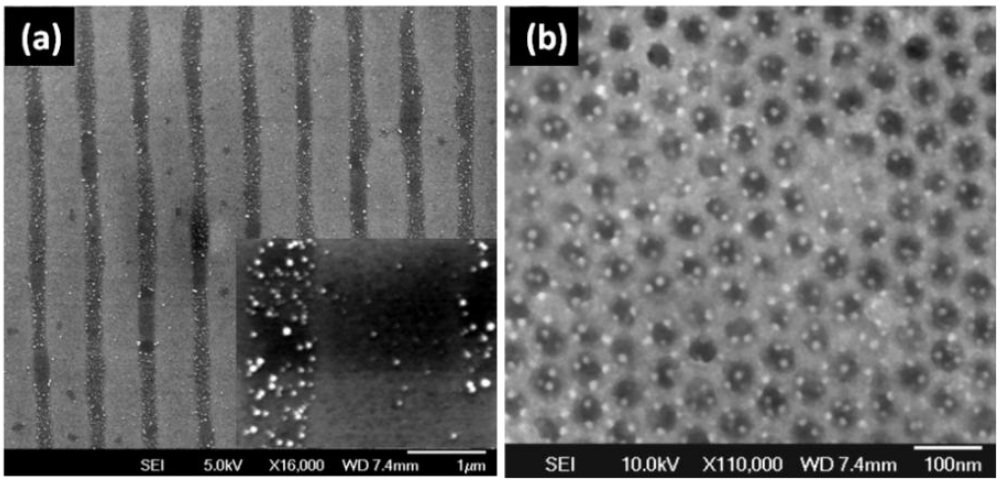

Figure 5.3 Top-view SEM images of Au-apoferritins absorbed on (a) a linear and (b) a hexagonal pre-patterned Si substrate, respectively, by a Polydimethylsiloxane (PDMS) and a thin-film of AAO imprint.

Pre-patterned Si substrates with different morphologies were used for the analysis of the selectivity of our modified immobilization method. Figure 5.3 shows the absorption behaviors of Au-apoferritin on a linear and a porous patterned Si substrate, respectively, by a Polydimethylsiloxane (PDMS) and a thin-film of AAO imprint. The regions with a bright contrast correspond to the passivated Si surfaces without modified by ATPMS and L-ascorbic acid, where Au-apoferritin molecules were scarcely found. In the case of sample (a), in which the density of the bright spots corresponding to Au cores increased dramatically at the linear edge (insert of Figure 5.3a), whereas only a few ones were dispersed on the passivated Si surface. This is because the negatively charged silicon dioxide surface repels Au-apoferritin molecules which are negatively charged at approximately pH 7. Although the local density of Au-apoferritin is still

inhomogeneous in each region, both samples demonstrate that a patterned monolayer of Au-apoferritin molecules can be selectively immobilized on a Si substrate after a surface modification.

5.2.2 Au-apoferritin-catalyst Si Nanowire Growth

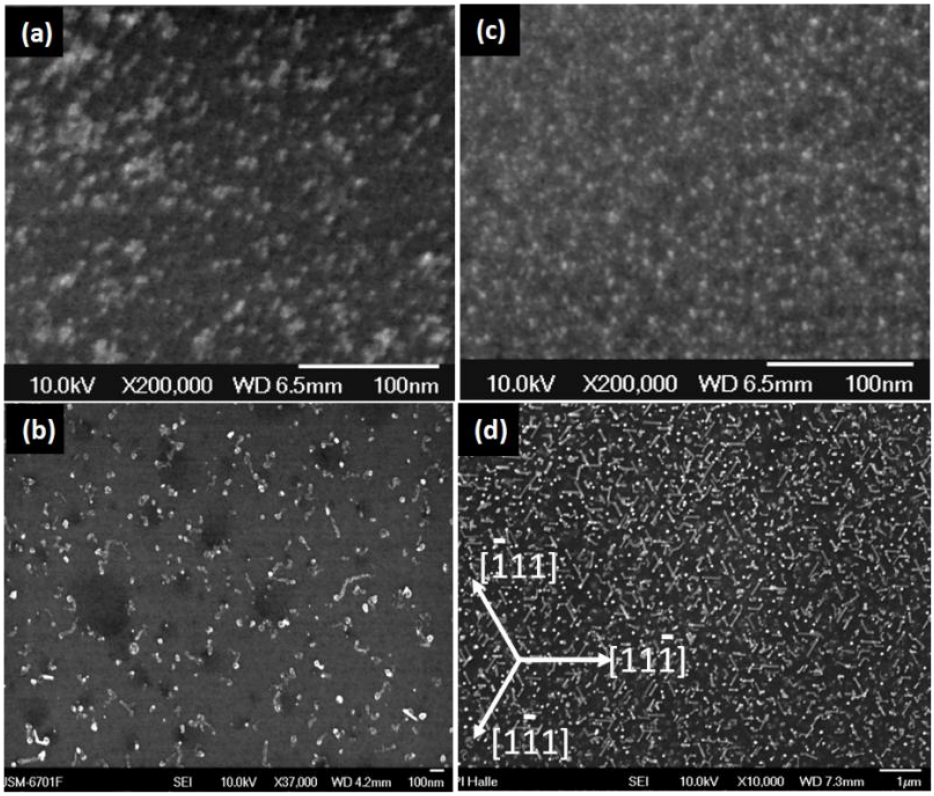

Figure 5.4 Top-view SEM images of (a) Au-appoferritins immobilized on pretreated Si(111) substrate and (b) Si nanowires grown after UHV-CVD, whereas (c) is the Au nanoparticle array on Si(111) with HF-steam treatment and (d) after Si nanowire growth with the same CVD conditions.

Figure 5.4a is a top-view SEM image of Au-apoferritin molecules immobilized on Si substrate. Each of the nanodots with bright contrast shows a Au nanoparticle inside a apo-ferritin molecule. This bionanoprocess has not yet been completed for a homogeneous space required monolayer in a large area on Si surface. Several clear blank spaces correspond to the molecules filled with less Au or completely empty ones. Si nanowires were grown by the UHV-CVD method with SiH_4 as gas precursor. A preheating at 110 ℃ in the UHV environment was performed for 2 h, removing the remaining water and anchoring the molecules to avoid aggregation during growth. Afterwards, the temperature was raised up to 450 ℃, and a 5% SiH_4 mixture gas with Ar was flowed into the chamber with a total pressure at 5 Torr, the growth continued for 20 min. Figure 5.4b shows a top-view SEM image after the Si nanowire growth catalyzed by Au-apoferritin. The observed nanowires were grown with a worm-like shape and a low growth density. This is explained by a combined effect of carbon contamination from the protein shell and the underlying SiO_2. For confirmation, the Au-apo, immobilized on Si, was exposed to a HF-containing steam in a sealed Teflon beaker for 30 min. Figure 5.4c reveals the Au nanoparticle assembly after the HF-steam

treatment, which appears better resolved due to the lack of non-conductive covering. The HF will also attack the SiO_2 underneath, and after the CVD growth as shown in Figure 5.4d, the Si nanowires grew on the Si(111) substrate with a straight shape and a high density. However, without the protein shells and SiO_2 in between, the Au could diffuse on the substrate surface to form Au/Si eutectic droplets with a larger diameter. Most of the Si nanowires measured were with diameters larger than 20 nm, and grew in the three kinked epitaxial <111> directions.

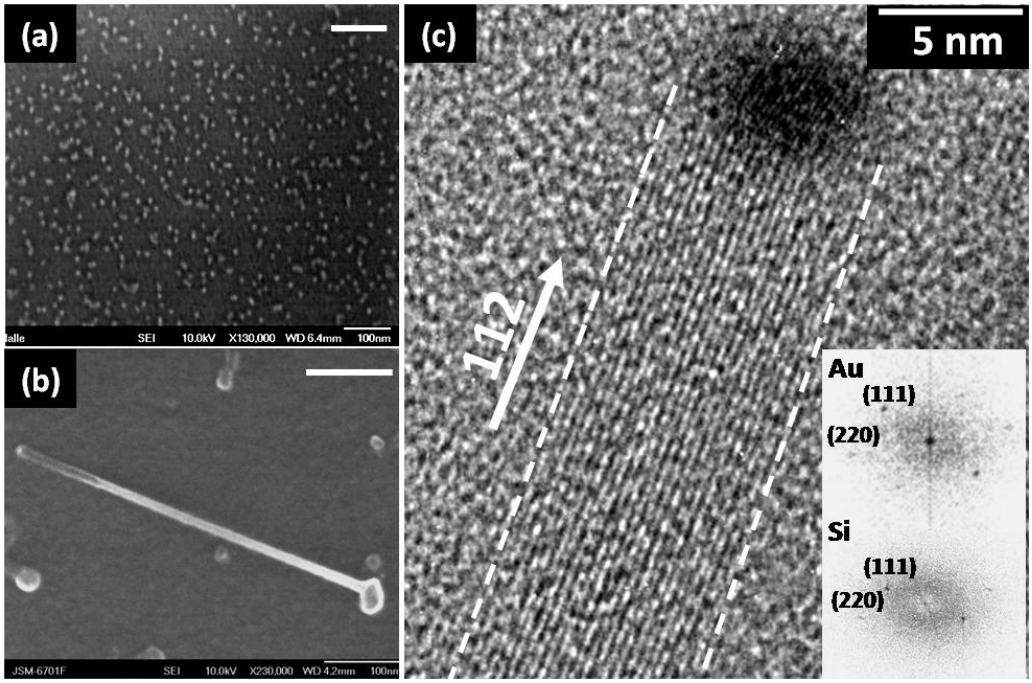

Figure 5.5 Top-view SEM images of Au-appoferritins (a) immobilized on pretreated Si(111) surbstrate after O_2-plasma treatment, (b) High-magnification of Si nanowires grown by UHV-CVD. (c) HRTEM image of a top part including both Si and Au catalyst lattice planes, inserts are FFT patterns from Au and Si, respectively.

To remove the protein covering, the sample was first treated with O_2-plasma for 2 min (0.9 Torr, 100 W, technics plasma 100-E, TePla). As a result, the Au nanoparticles were attached onto the Si substrate which was still covered by a thin SiO_2 layer. Figure 5.5a shows top-view SEM images of Au nanoparticles on Si substrate after O_2-plasma treatment. We found no aggregation of Au nanoparticles happened after the treatment. Although straight Si nanowires with sub-10 nm diameter were grown on Si substrate after the CVD process (see Figure 5.5b), the growth density was much lower than the density of Au seeds, and no obvious epitaxial relationship between the growth direction and Si(111) substrate was observed. The Au catalyst was found on top of the nanowire as a bright dot. The wire had a diameter below 10 nm, was uniform along its length, and had a disc-shaped base, which is a typical feature observed for semiconductor nanowires grown on an oxide surface. The bright spots with a weak contrast on the Si surface are presumably remaining Au nanoparticles, which did not induce Si nanowire growth. Considering the effect of Si supersaturation on the growth, it appears that Au nanoparticles larger than 4 nm can more easily catalyze the growth of Si nanowires [Sch09]. To investigate the crystallographic structure of both Si and Au parts, TEM investigations were performed of Si nanowires collected onto a carbon film

covered Cu grid. Figure 5.5c is a HRTEM image taken from the top part of a Si nanowire. The electron beam was adjusted close to the [1$\bar{1}$0] Si zone axis. The FFT pattern (lower inset) shows both Si(111) and (220) planes, corresponding to a nanowire with a [112] growth direction. The (111) planes are easily visible being parallel to the sidewalls marked with dashed lines. The diameter of the Si nanowire was about 7 nm. The black contrast in the upper part of the nanowire corresponds to Au with a cubic lattice. The upper inserted FFT pattern is derived from the Au along the [1$\bar{1}$0] zone axis. The Au tip is around 6 nm in diameter, slightly smaller than the Si beneath.

5.3 Surface Template for Sub-10 nm Si Nanowire Epitaxy

Au-appoferritins, together with other Au colloids as catalysts can realize the Si nanowire growth with several nanometers in diameter. However, in order to achieve a high-density of sub-10 nm diameter nanowires grown epitaxially on Si substrate with a uniform size distribution, small catalytic seeds on Si with a uniform size distribution should be maintained at the growth temperature above its liquid eutectic in a VLS growth mechanism.

5.3.1 Synthesis of Sub-5 nm Au Nanoclusters

The size distribution of nanowires grown by the VLS mechanism can be in a good accordance with the one of the catalytic seeds [Kan08a]. In order to maintain small catalytic Au seeds with a uniform size distribution, further annealing should be avoided. The condition of the Si surface has a strong influence on the formation of nanoclusters [Zha97]. Steps and other surface defects on Si substrates can be responsible for the formation of small Au nanoclusters after a deposition of a few atomic layers. Before the deposition of Au, the H-terminated Si(111) or Si(110) wafer were heated in the UHV-heating chamber at a temperature of 900 ℃ for 30 min with a background pressure of 1×10^{-9} mbar. The preheating was intended to form a reconstructed surface, working as a surface template for the formation of metal nanocluster arrays [Kot02, Ant98]. The MBE growth rate of Au was 50 pm/min calibrated at room temperature. The backside of the Si wafer was heated up to 350 ℃ in the MBE chamber during the deposition. After the Au deposition, the Si wafers were removed away from the heater and then transferred *in situ* into the UHV-CVD chamber for the Si growth.

Figure 5.6 a and b are 25 °-tilt top view SEM images of the Au nanoclusters formed on Si(111) and Si(110) substrate, respectively, by the hot-surface MBE method. The small Au nanoclusters formed directly on the Si surface with a high density and a small size distribution. It was shown by Gaussian fitting of the diameter distribution (insert diagram of Figure 5.6a) that the Au clusters had a mean diameter of 4.5 ± 1.1 nm with a nominal deposition thickness of 0.15 nm. With the same growth conditions, Au nanoclusters formed on a Si(110) substrate had similar sizes. The insert AFM measurement in Figure 5.6b shows the Au cluster had a width of about 5 nm and a height less than 2 nm. The measured mean diameters of Au clusters on Si(111) substrate increased with the nominal thickness of Au deposition at 350 ℃, the curve is plotted in Figure 5.6c. The

sub-5 nm diameter Au seeds on both Si(111) and (110) were used as catalysts for the sub-10 nm Si nanowire epitaxy.

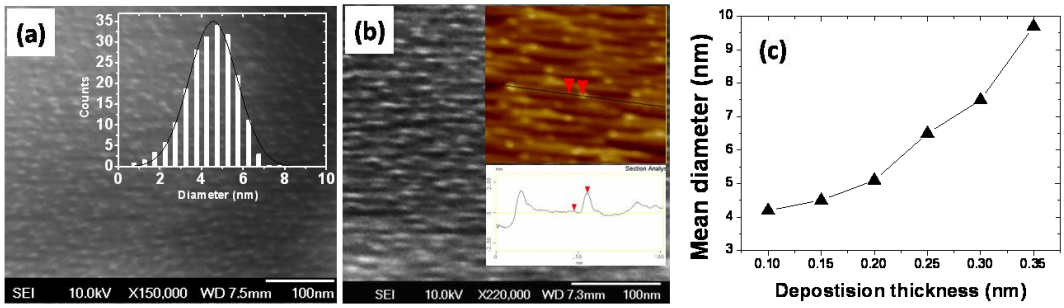

Figure 5.6 25 °-tilt top-view SEM images of the Au seeds formed on (a) Si(111) substrate, with an insert diagram of Gaussian fitting of the size distribution, and on (b) Si(110) substrate. The insert shows an AFM characterization of the surface. The Au clusters have a height smaller than 2 nm and sub-5 nm diameters. (c) Mean diameters of Au nanoclusters measured by SEM for different Au nominal deposition thickness with substrate heating at 350 ℃.

5.3.2 Sub-10 nm Si Nanowire Epitaxy on Si(111)

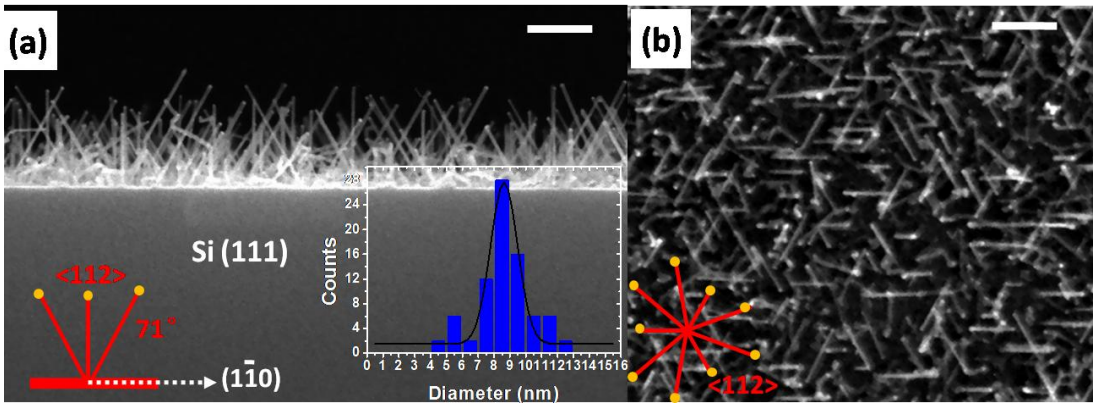

Figure 5.7 (a) Side-view SEM image of the Au-catalyzed Si nanowires grown epitaxially on Si(111) substrate. Scheme of growth directions of <11$\bar{2}$> SiNWs with the side-view orthographic projection along the [112] direction, and diagram of Gaussian fitting of the diameter distribution are shown as insets. (b) Top-view SEM image with the inset of corresponding orthographic projection along <112> growth directions. Scale bars are 100 nm.

The Au nanoclusters formed on Si substrates with a mean diameter of 6.5 ± 1.3 nm (i.e. Au thickness = 0.25 nm) were directly used as catalytic seeds without annealing process. Thus, when the calibrated temperature of the Si substrate approached 370 ℃ in case of Au as catalyst, a 40 sccm 5 % Silane (SiH_4) + Ar mixture gas was fluxed into the chamber to a total pressure of 15 Torr. The growth temperature was fixed at 370 ℃ for 5～10 min, and stopped by pumping off the precursor gas and moving the sample far from the heater.

The SEM images in Figure 5.7 illustrate the influence of the substrate orientation and catalyst size on the epitaxial growth direction of Si nanowires, showing the side-view and the top-view of nanowires grown on a Si(111) substrate respectively. The growth time was 10 min. In the side-view image (Figure 5.7a), the viewing direction is perpendicular to the cracking plane along Si[1-10] direction. Most of the straight nanowires show tilts of 71° and 90° relative to the Si substrate. These tilts are predicted for <112>-oriented nanowires, as shown in the schematic insert of Figure 5.7a. The <112> wires are tilted by 19° with respect to the normal of the substrate. The orthographic projection on the Si(111) substrate in the top-view image (Figure 5.7b) shows a triangular network. However, there are a few bright spots which correspond to the Au-catalyst tips of some Si[111] nanowires grown perpendicular to the substrate, or the Au nanoclusters remained on the surface without catalyzing Si nanowire growth. The insert diagram of Figure 5.7a shows a Gaussian fitting of the narrow diameter distribution. The <112>-oriented nanowires have a mean diameter of 8.4 ± 0.9 nm, and a wide distribution of growth length from 10～150 nm. According to the growth model presented by Lew *et al.* [Lew03], the growth rate at 370℃ and 0.65 Torr SiH_4 partial pressure was about 20 nm/min for a 200 nm diameter Au-catalyzed Si nanowire. If the base nucleation process caused a short delay, the reported growth rate should outrange our observed maximum Si nanowire growth rate in sub-10 nm diameter. A diameter-dependent reduction in growth rate has been reported by Schmidt *et al.* which was attributed to the Gibbs-Thomson effect [Sch09a]. The <110> growth directions were prevalent for diameters below 10 nm grown epitaxially on a Si(100) substrate [Sch05a] and non-epitaxially in the free space case [Wuy04]. However, according to our observations, the Au-catalyzed sub-10 nm diameter Si nanowires grown epitaxially on Si(111) substrate preferred <112> orientations.

Figure 5.8 shows HRTEM images taken from the cross-sectional specimens, a growth time of 5 min was used. The Au catalyst can be distinguished from silicon by a much higher atomic number z which results in a dark contrast. A shorter wire with a diameter of about 6.5 nm is shown in Figure 5.8a. The Au catalyst is not shaped in the typical equilibrium hemisphere as shown for the free standing nanowires in chapter 3. The interface is probably affected by the oxidization of Si surrounding the small Au tip during storage in air at room temperature [Xie08]. Distinguished from the crossed {111} lattice planes, side surfaces of the nanowire base are curved as a result of typical VLS homoepitaxial growth. Estimated from the difference of curvatures on both side surfaces, the left one tends to be parallel to the {111} lattice planes with [112] growth direction, the diameter is decreasing from 10 nm to 6.5 nm. To confirm it, a longer wire with a height of 40 nm is shown in Figure 5.8b. Obviously, it was along the [112] growth direction with a tilt of 70.5° to the Si(111) surface. By counting of the lattice planes, the wire has a diameter of 10 nm. A step-like 1 nm shrinkage happened on the left sidewall at a growth length of 11 nm. The diameter increase at the base could be a result from the lateral growth of Si besides the expansion of the nanowire base happened during the initial VLS growth. Together with the initial stage of Si nanowire epitaxy shown in Figure 5.8a, notably, the Si[112] epitaxy originates from the interface between the original Si(111) with a defect-free interface. The base expansion is corresponding to the liquid phase of Au-Si catalyst at the growth temperature of 370 ℃. Other growth directions such as <110> directions were not found during the TEM observations. With different nominal thicknesses of Au deposition, but thinner than 0.3 nm, Si[112] nanowire epitaxy with sub-10 nm diameter was dominant on Si(111) substrates.

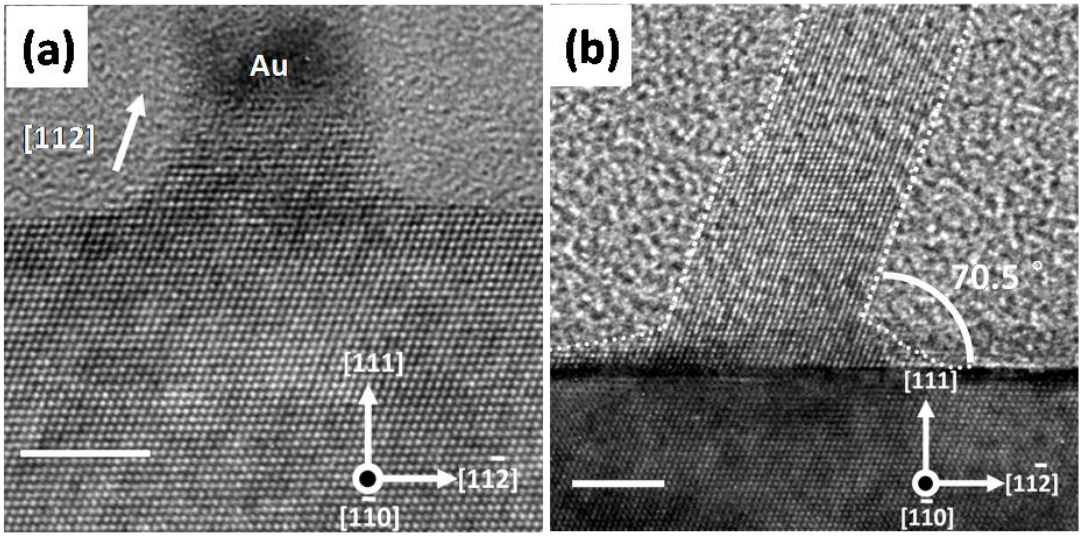

Figure 5.8 Cross-sectional HRTEM images of Si nanowires grown epitaxially on Si(111) substrate with different growth heights: (a) 4 nm and (b) 40 nm growth height with a diameter of 6.5 nm and 9 nm, respectively. The zone axis is along the Si[1$\bar{1}$0] direction for both samples, scale bars are 5 nm.

Now we consider nucleation and growth behavior of sub-10 nm Si nanowires. Ideal would be an *in situ* experiment in a high resolution TEM with gas injection possibility. High resolution investigations of Si surfaces covered by Al or Au were performed by the group Saka [Sak05]. The work presented in this thesis was limited to the use of a room temperature HRTEM. During cooling the Si dissolved in the Au catalyst precipitates and the images obtained at room temperature show the frozen in state after this precipitation. The nanowires discussed here showed a [112] growth direction. The interface between solid catalyst and Si was usually flat and a Si(111) plane terminated the Si nanowire. The growth of a nanowire is believed to be a dynamic process [Sch05]. The theory of crystal growth from a liquid predicts a close relation between surface roughness and nucleation behavior [Jac74]. The Si(111) plane has a low interface energy to the catalyst droplet and some models of the growth discuss a layer by layer growth at (111) planes [Wuy04]. This model requires the nucleation of a new plane, as soon as one plane was completed. Experiments with solid silicide as catalyst for nanowire growth or about the growth of a silicide on a Si surface showed a ledge flow mechanism. Hesse et al. [Hes93] published HRTEM images of a Ni-silicide/Si interface with ledges. The height was three Si(111) planes. Later Hofmann et al. used Pd-silicide in an *in situ* TEM to grow Si nanowires and observed again ledges with a height of three or more Si(111) planes [Hof08]. A low resolution *in situ* TEM investigation of the growth of Si nanowires using a liquid catalyst showed a moving contrast at the interface [Kim08]. The low resolution of the images did not allow to quantify the height of the moving step. The precipitation of Si from the catalyst during cooling will usually result in a completed Si(111) plane at the interface to the catalyst. For large droplets also some Si decorates the surface (see Fig 3.3). Only for small diameter wires it might happen that a new layer nucleates just before cooling down, and the amount of Si stored in the catalyst is so small that the layer is not completed during cooling.

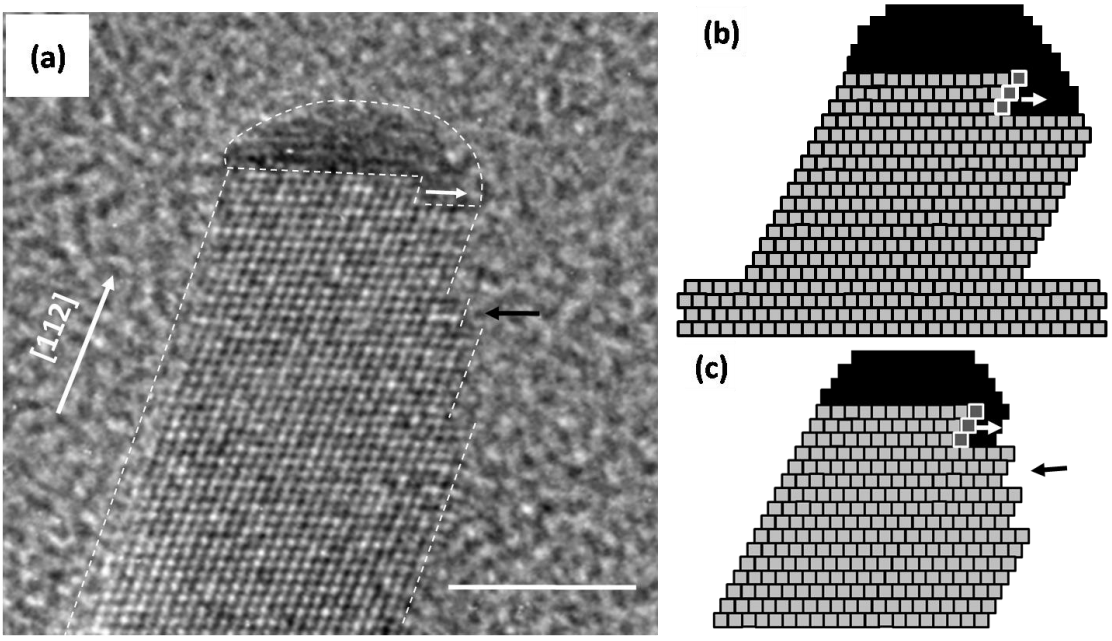

Figure 5.9 (a) Cross-sectional HRTEM image of top side of a Si nanowire grown epitaxially on the Si(111) substrate, the growth direction is illustrated as [112], viewing along the Si[1$\bar{1}$0] zone axis, scale bar is 5 nm. (b) Illustration of the growth model with a ledge-flow propagation direction indicated by the white arrow shown in (a), the Si atoms with white outlines are the growth front of the ledge consisting of three Si(111) planes, which results in the [112] growth direction. (c) Modified growth model with considering the steps of the right sidewall indicated by the black arrow shown in (a).

For the Au-catalyzed Si nanowire epitaxy on the Si(111) substrate, we observed that the solid-liquid interface with diameter above 40 nm was always perpendicular to the growth direction. However, for Si nanowires grown epitaxially on Si(111) with sub-10 nm diameters, the interface of the Si[112] nanowire was observed to be a Si(111) plane as well (shown in Figure 5.9a). This Si nanowire grew epitaxially on Si(111) with a diameter of 8 nm. The growth direction is illustrated as [112]. A gold cap remained on the tip with a dark contrast, outlined by the dashed curves. The Si-catalyst interface is atomically flat with a Si(111) interface plane. It contained a ledge consisting of three Si(111) planes. The ledge-flow direction was indicated by a white arrow in Figure 5.9a. The nucleus started from the left sidewall and stopped at the right one, which resembles the lateral propagation process from one sidewall to the other as reported for *in situ* solid-catalyst growth [Hof08]. However, it contradicts to the interfacial morphology on a liquid-catalyst interface proposed with two symmetric ledges from both sidewalls [Wac09a]. Thus, we postulated a ledge-flow growth mechanism for the Si[112] nanowire epitaxy on Si(111) in the sub-10 nm diameter scale, even with a liquid-catalyst. A simplified 2-D cross-sectional growth model is depicted in Figure 5.9b, according to the HRTEM image shown in Figure 5.9a. Initially, a Si nucleus formed at the left sidewall, on the three-phase boundary, as birth of the ledge-flow. Accompanied by the propagation of that ledge-flow to the other sidewall, three Si(111) planes formed on the solid-liquid interface of Si nanowire with the tilted sidewalls along the [112] direction. The sidewall of the nanowire in Figure 5.9a is terminated at the left side by a Si{111}

plane. This gives some hint to develop a model of nucleation. The nucleus of a three layer thick ledge could be formed by extending the {111} plane at the left side. As soon as a height of the nucleus of three layers (one unit cell) is reached, the ledge flow can start, and the new ledge propagates from left to right, shown by the white arrows in Figure 5.9. This nanowire was somehow special with a small thickness of the Au catalyst on top. Perhaps the nanowire has lost Au by surface diffusion during growth. This would also explain the steps at the right sidewall, which decreased the diameter during growth. This model is supported by the observation of a step at the right sidewall with a height of three (111) planes, marked in Figure 5.9a by a black arrow. The nanowire seems to grow preferentially by extending existing {111} planes.

5.3.3 Sub-10 nm Si Nanowire Epitaxy on Si(110)

The observed epitaxial growth in the <112> directions on Si(111) suggests that the surface construction plays an important role. One can assume that, during the initial Si growth, the small surface energies of the Si{111} planes may influence the nucleation behavior. Another key factor is the interface energy of the solid-liquid interface, with the lowest interfacial energy being believed to be on Si{111} planes. A higher supersaturation of the Au-Si alloy is required with smaller volume [Sch09] and the mobility of Au increases with higher SiH_4 partial pressure [Den08]. Other aspects in nanowire epitaxy may contribute to determine the growth direction, such as the surface energies of multiple faceting types. Cai *et al.* assumed that a preferential growth direction may reflect the competition between the surface energies of solid-liquid interface and nanowire facets, although additional analysis will be needed referred to the nonequilibrium nucleation processes [Cai06]. Considering the different start nucleation behaviors caused by the Si surface conditions [Kri04], we investigated the influence of different orientation-types of Si substrates on sub-10 nm Si nanowire epitaxy.

Figure 5.10 shows side-view and top-view images of Si nanowires grown epitaxially on Si(110) substrate. The growth conditions were the same with the experiment described in Figure 5.7. In the side-view image (Figure 5.10a), we observed that most of the nanowires were grown vertically to the Si(110), which was confirmed by the bright spots in the corresponding plan-view orthographic projection (Figure 5.10b). Furthermore, the viewing direction is perpendicular to the cracking plane along Si($1\bar{1}2$), most of the straight nanowires show tilts of $30\,°$ and $60\,°$ relative to the Si(110) surface. The tilts are predicted for <110>-oriented nanowires, as shown in the schematic insert of Figure 5.10a, which have a $30\,°$ angle with respect to the normal of substrate. The plan-view orthographic projection on the Si(110) shows two types of growth directions: the <110> family with a percentage of more than 98%, and the possible <111> directions (white lines inset of Figure 5.10b) with only a small percentage. Compared with the one illustrated in Figure 5.7a, measured from the <110>-oriented Si nanowires, the Gaussian fitting of the diameter distribution shows a smaller mean diameter of 5.6 ± 1.2 nm in Figure 5.10a. As a result of that the Au nanoparticles formed on Si(110) were smaller than the ones on Si(111) with the same Au deposition condition, the mean diameter of nanowires was smaller than the one characterized in Figure 5.8 as well. The average growth length was longer than the epitaxial growth on Si(111) substrate. Obviously, on the Si(110) substrate, the <112> growth directions seem to be forbidden completely, replaced by the <110> growth directions. Considering the similar diameters and

growth rates on both substrates, during the initial stage of nucleation, the competition of different surface conditions affects the epitaxial growth direction in the sub-10 nm scale. However, a few exceptions with unknown growth directions could be seen in the SEM observations. We need further support from the HRTEM analysis.

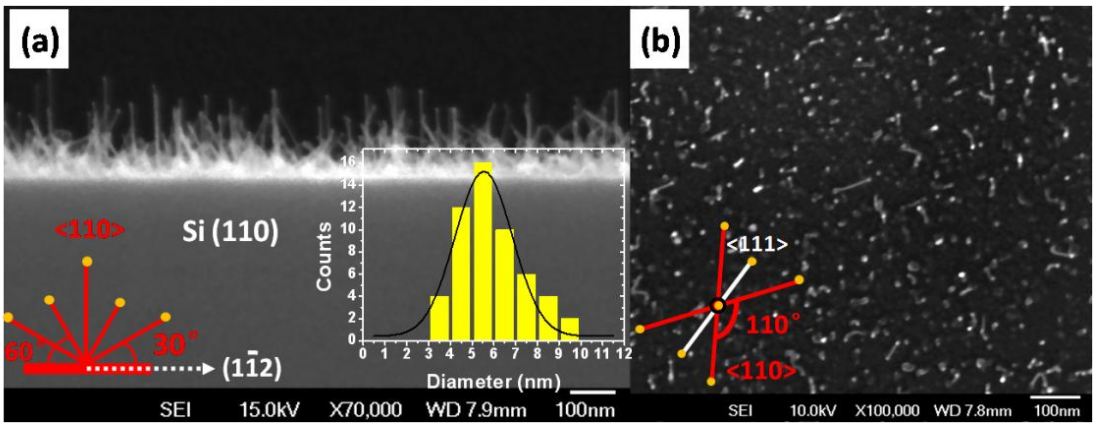

Figure 5.10 (a) Side-view SEM image of the Au-catalyzed Si nanowires grown epitaxially on Si(110) substrate, schematic growth directions of <110> SiNWs with the side-view orthographic projection along the [$\bar{1}$11] direction, and diagram of Gaussian fitting of the diameter distribution are shown as insets. (b) Top-view SEM image with the inset of corresponding orthographic projection along <110> and <111> growth directions.

Figure 5.11 are cross-sectional HRTEM images taken from Si nanowires grown epitaxially on Si(110) with a decreased growth time of 5 min. In [1$\bar{1}$2] viewing direction, only the vertically aligned Si[110] nanowires could be observed. Figure 5.11 a-c show Si nanowires with a sub-5 nm diameter. The nanowires in [110] growth direction have continuously grown {111} planes parallel to the normal of Si(110) surface, with a [1$\bar{1}$2] viewing direction. The base expansion implies the VLS epitaxial growth since the start nucleation. By counting the numbers of {111} lattice planes, the one shown in Figure 5.11a has a diameter of 4.4 nm and a growth length of 5 nm, whereas the one in Figure 5.11b has a smaller diameter of 4.1 nm and a smaller length of 2 nm. The minimum diameter observed was confirmed to be 2.8 nm in Figure 5.11c. We can distinguish the Si[110] nanowire from the connected Au catalyst. It consisted of 9 Si{111} lattice planes continuously stretched from the substrate to the Au cap with a length of 10 nm. When the epitaxial growth was catalyzed by a bigger Au droplet, as shown in Figure 5.11d, a much faster growth rate of about 7 nm/min was observed with a diameter of 7 nm. Moreover, due to the mobility of the Au-Si droplet, the initial growth was in an unsteady state. We observed a lateral movement of the growth interface and a decrease of diameter in Figure 5.11d. The sidewalls of the nanowires are highlighted with the dotted outlines.

The interface between [110] oriented Si nanowires and the catalyst particles was not flat, as observed for [112] wires, but showed a considerable roughness. The growth model for [112] wires assumed a stacking of (111) planes to build a wire. If also for [110] wires the {111} planes would be planes of rapid growth, two different growth scenarios can be expected. First the ($\bar{1}$11) and ($\bar{1}\bar{1}$)

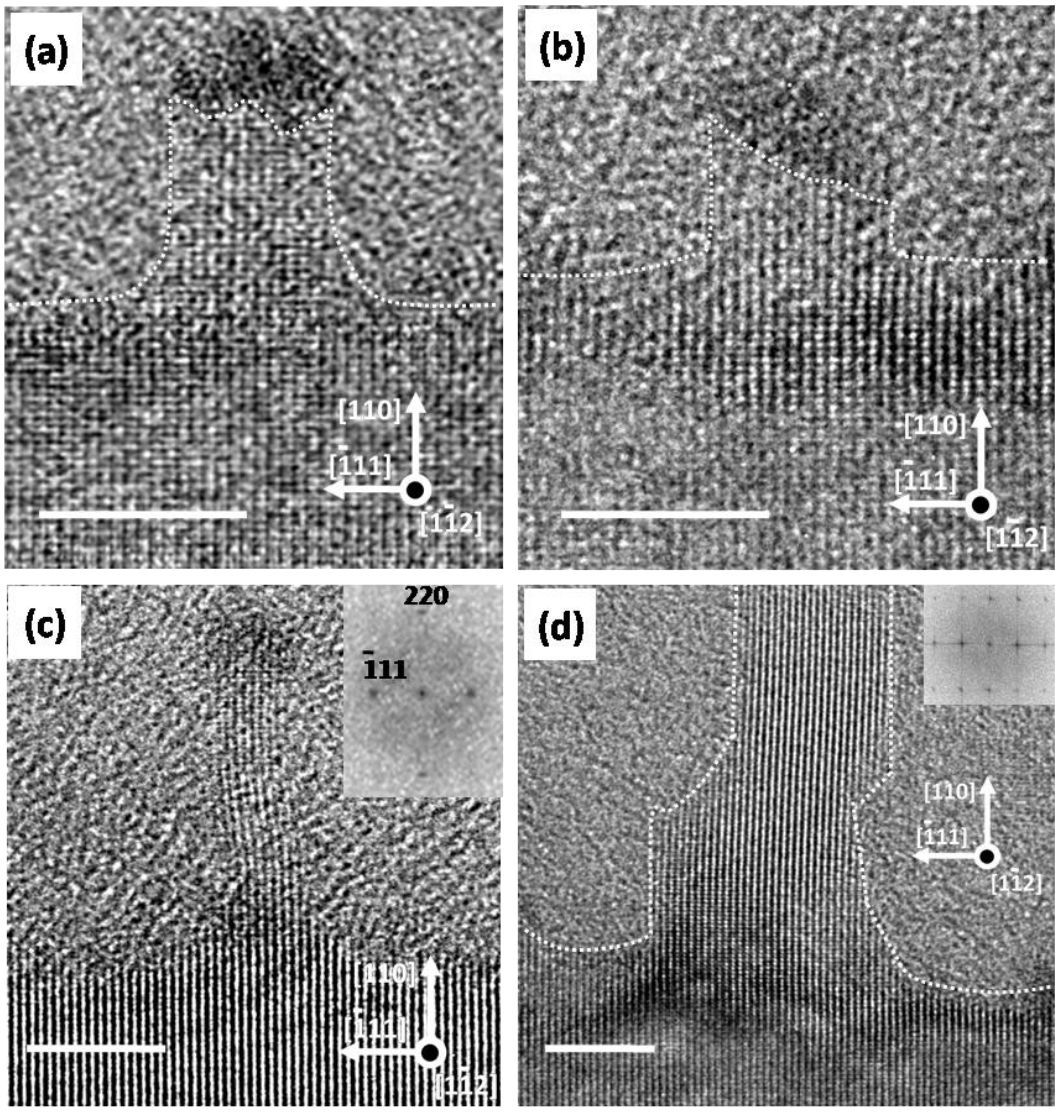

Figure 5.11 Cross-sectional HRTEM images of Au-catalyzed sub-10 nm diameter Si nanowires grown epitaxially on Si(110) substrate for 5 min. (a) Rough interface between Au and Si, (b) inclined interface between Au and Si. (c) The smallest [110] SiNW found with a 2.8 nm diameter. (d) Cross-sectional HRTEM image reveals a segment tilted away from the [110] growth direction during growth, the inset shows the FFT diffraction pattern taken from the tilted region. Scale bars are 5 nm.

planes perpendicular to the [110] wire axis could be growth planes. This would allow a continuous growth of {111} planes without breaks in between for nucleation of new layers. A second possibility would be a growth using (111) planes with 35 ° tilt relative to the (110) plane. Figure 5.11b shows an inclined interface which might be the result of the second growth mode. The first mode seems to be dominant and was observed in all other TEM images. As already discussed, the TEM images show the situation after precipitation of Si dissolved in the catalyst. The concave shape of the interface shown in Figure 5.12a might be the result of such a precipitation. This is shown schematically in Figure 5.12b. The schema in Figure 5.12c explains the idea of a continuous growth by adding material to all perpendicular {111} planes.

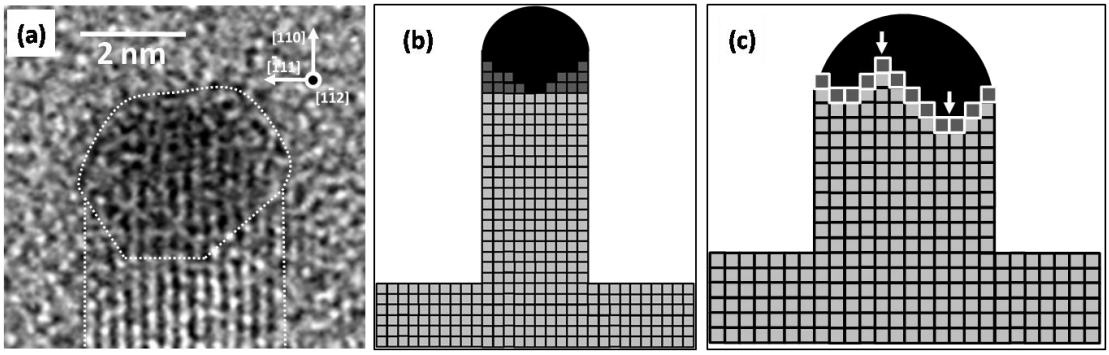

Figure 5.12 (a) Cross-sectional HRTEM image of top side of a 3.8 nm diameter of Si nanowire grown epitaxially on Si(110) substrate, the growth direction is illustrated as [110], viewing along the Si[1$\bar{1}$2] zone axis, the interfaces are outlined with dotted lines. (b) Schema of growth with precipitation during cooling, (c) continuous growth of vertical Si(111) layers, the white arrows point to the last added atoms.

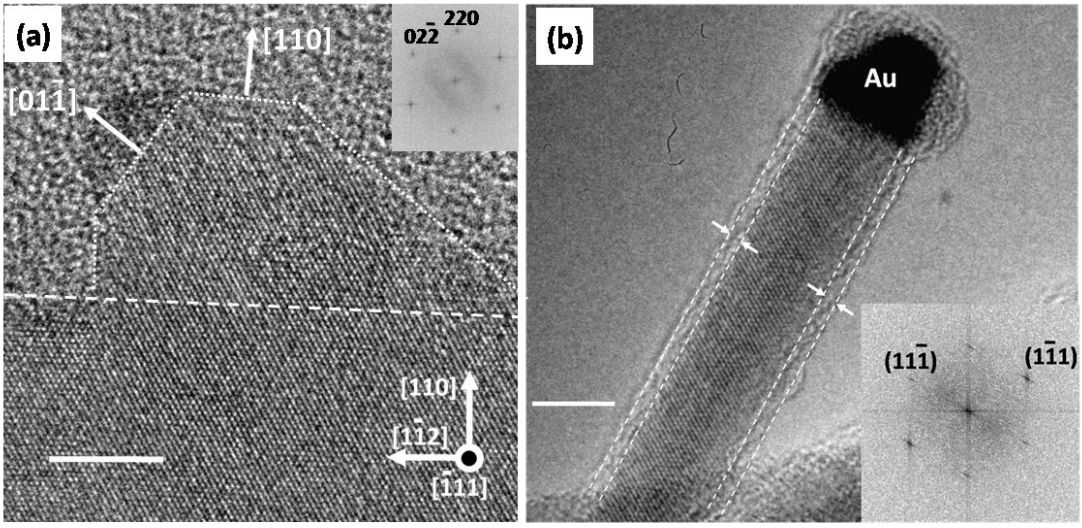

Figure 5.13 (a) Cross-sectional HRTEM image reveals the kinked growth direction from a [110] growth direction to the [01$\bar{1}$] growth direction, the surface of Si(110) substrate and outlines of grown Si are indicated with a dashed line and dotted lines, respectively, the inset shows the FFT diffraction pattern taken from [$\bar{1}$11] zone axis. (b) HRTEM image of Si nanowire collected on carbon grid with 7 nm diameter and 1 nm thick amorphous oxide outer layer, the inset FFT diffraction pattern shows two crossed Si{111} lattice planes. Scale bars are 5 nm.

According to the configuration of the <110> family epitaxial growth directions, inclined <110> nanowires are grown beside the vertically aligned [110] ones on Si(110) substrate. A cross-sectional HRTEM image prepared along another viewing direction than Si[1$\bar{1}$2] could observe the specific growth directions. Figure 5.13a shows a cross-sectional sample viewed along the [$\bar{1}$11] zone axis. From the inset FFT diffraction pattern, a growth front of 6 nm diameter connected with Au catalyst corresponds to the [01$\bar{1}$] growth direction, for which the growth axis deviates 60 ° from the [110] growth direction. Figure 5.13b shows the top-side of a Si nanowire

collected on a porous carbon film, which contains a single crystalline Si core of 7 nm in diameter, and around 1 nm thick amorphous oxides outer layer. The two crossed {111} planes seen in the inset FFT diffraction pattern taken from the wire can be explained by a [011] viewing direction. Other growth directions such as <112> and <111> directions were not found in the extensive TEM observations. In general, in sub-10 nm diameter, <110> growth directions are dominant for Si nanowires grown epitaxially on Si(110) substrate.

5.4 Conclusions

In summary, we demonstrated that small Au catalyst particle can be synthesized by both bio-templated and surface-templated method, with a mean diameter of sub-5 nm and a small size distribution. Using apo-ferritin, in order to avoid the Au nanoparticles reduced exteriorly, a modified bionanoprocess resulted in a high selectivity of Au nanoparticle encapsulated into the cavity and a high-density of Au-apoferritin molecules immobilized on Si substrate. The sub-10 nm diameter Si nanowires can be catalyzed by Au nanoparticles after removing the protein cells, although a dilemma exists regarding diameter control and good epitaxy. Using reconstructed Si surfaces as template for the formation of metal nanocluster arrays, on both Si(111) and (110), Si nanowires were grown epitaxially with uniform size distributions in sub-10 nm diameter, and the epitaxial growth direction was strongly affected by the orientation-type of the Si substrate. The dominant <112> growth directions on Si(111) substrate were confirmed, whereas on Si(110) most of the Si nanowires grew vertically in [110] direction. Based on crystallographic analysis, a ledge-flow growth mechanism was presented for the Si[112] nanowire epitaxy on Si(111). A ledge-flow consisting of three Si(111) planes was assumed to be responsible for the step-shaped sidewall. A step with a height of three Si(111) planes at one interface was interpreted as evidence for the growth of a complete unit cell, contrary to the usually discussed layer by layer model. The smallest observed epitaxial Si nanowire had a diameter of 2.8 nm and a growth direction [110]. The roughness at the interface between catalyst and nanowire was different for [112] and [110] wires, with smooth interfaces for [112] nanowires. Two growth models were presented, a three (111) layers ledge flow model for [112] wires, and a continuous growth model for [110] nanowires. The ability to grow epitaxially sub-10 nm diameter Si nanowires should open up new opportunities for fundamental research in post-CMOS applications.

Chapter 6

III-V Nanowire Heteroepitaxial Growth on Si

Heteroepitaxial growth of III-V nanowires on Si substrates with sub-10 nm diameters is of importance for both fundamental research on crystal growth as well as for the integration into the established Si-based technology. In this chapter, sub-10 nm diameters III-V nanowire heteroepitaxy on Si was realized with diverse catalysts. The Ga supersaturation-dependent phase transition from zinc blende to wurtzite has been confirmed in the sub-10 nm scale. Furthermore, in order to expand the range of possible nanodevices, diverse morphologies of axial and branched nanowire heteroepitaxy have been investigated.

6.1 Introduction

The vapor-liquid-solid (VLS) growth mechanism has been widely employed in III-V nanowire growth [Bar65]. Gold is commonly used as catalyst and combined with an epitaxial growth method, such as MOCVD [Joy07], MOVPE [Sei04], or MBE [Lug07]. The size and the distribution of catalysts on substrate play an important role in nanowire epitaxy. Other growth conditions, such as the III/V flux ratio, the substrate temperature, and the growth duration, all have a strong influence on the shape and crystallographic structure in an interdependent manner. Particularly, it is difficult to integrate vertically aligned III-V nanowires onto a Si substrate with an annealing process for formation of Au droplets [Roe06]. Considering the sensitivity of growth to several parameters, well-controlled heteroepitaxial growth of III-V nanowires on a Si substrate is still a challenge.

The main crystallographic difference between III-V and Si or Ge is that most III-V nanowires have a strong tendency to adopt the hexagonal wurtzite (WZ) crystallographic structure, even though their bulk counterparts are strictly dominated by the cubic zinc blende (ZB) structure. In reality, III-V nanowires with diameters of tens of nanometers usually appear with a polytypic structure along the growth axis [Alg08, Car09]. The WZ structures in many nanowires contain parts with ZB structures, which shows up as stacking faults or as continuous ZB segments. The phase transition between these two structures obviously affects its physical properties, such as electron and hole transport along the wire [Pem09, Bao08]. Based on both theoretical and experimental observations, several possible growth models have been discussed in order to better control the crystal phase. One explanation given by Akiyama *et al.* leads to a critical diameter below which the nanowire favors the WZ formation, possessing a lower surface energy than that of the ZB structure [Aki06]. With the experimental result of WZ phase formation in considerably thicker diameter nanowires than the predicted critical value for the same compound, another possible explanation in terms of the liquid supersaturation was developed by Glas *et al.* [Gla07],

which is based on the classical nucleation theory at the solid-liquid interface. Accordingly, WZ nucleation is favored at a high liquid supersaturation, which is related to lower interfacial energies at the three-phase boundary. Several reports on the growth of epitaxial GaAs NWs present a transition from WZ to ZB during the final cooling process [Gla07, Sht09]. Such a ZB neck region under the Au particle is regarded as a result of the gallium remaining in the droplet being consumed (hence a decreasing supersaturation). The corresponding diameter is the same as the connected WZ segment, eliminating the size effect. However, at the time of writing this thesis, there was no report on the phase formation during initial heteroepitaxial growth with a considerably decreased diameter in the sub-10 nm scale. Also experimental evidence of the influence of the Ga-concentration on the phase formation during the initial stage of heteroepitaxial growth was missing. The Ga concentration in the catalyst droplet increases during initial growth up to a steady state value, and a transition from ZB to WZ could be expected. The strain caused by the lattice mismatch could influence the initial phase formation as well. Gallium phosphide (GaP) has a lattice mismatch of less than 0.4% relative to Si, and is thus the best candidate of the binary III-V compounds on Si for investigating the initial heteroepitaxial phase with little strain effect. Otherwise, III-V nanowires with structure control down to 10 nm (the requirement of post-CMOS), offer a higher possibility of defect-free heteroepitaxial growth with a big lattice mismatch. Another fundamental problem is that, considering that GaP has two nonequivalent atoms in the unit cell, if GaP is grown on Si, antiphase boundaries can be produced. The usual growth direction of III-V nanowires is along (111)B, but on Si theoretically also (111)A could nucleate [Hol84]. In addition, III-V nanowire growth with catalyst other than Au is required for CMOS processing and will be presented in chapter 6.3.

6.2 UHV-CBE Growth of GaP Nanowires on Si

To achieve a homogeneous distribution of Au seeds with sizes of only several nanometers, we adopted an approach partially based on a specific observation in previous Si nanowire growth experiments: homogeneous ultra-small Au clusters decorated the Si surface if the Si nanowire growth was followed by a surface migration [Sch06, Doe08]. Thus, a homogeneous distribution of gold nanoclusters with a size of a few nanometers on the Si surface was realized by a controlled post-growth annealing process. Subsequently, a high density of GaP nanowire arrays of sub-10 nm diameter could be catalyzed with the Au clusters, heteroepitaxially growing both on the Si(111) substrate and the sidewalls of the epitaxial Si[111] nanowires. Crystallographic analyses of the phase control in the ultrathin GaP nanowires and the branched heterostructure on the Si nanowire are also presented here.

First, a thin Au film (1 nm) deposited on H-terminated Si(111) substrate was adopted for the Si nanowire epitaxial growth. The annealing for Au droplet formation was performed at 500 ℃ for 30 min. Then, Si nanowires were grown at 450 ℃ with a 0.1 mbar SiH_4 partial pressure. Finally, the gas was pumped out after achieving the desired growth length. The post-anneal process was heating at 550 ℃ for 10 min, in order to get a homogeneous distribution of Au nanoclusters on both sidewalls of Si nanowires and Si substrate in between. Right after the substrate temperature had been decreased to 470 ℃, the TMG and TBP were introduced successively with partial

pressures of 1×10^{-5} mbar and 1×10^{-4} mbar respectively. The CBE growth was kept for about 5 min.

6.2.1 Au-catalyzed GaP/Si Nanowire Heterostructures

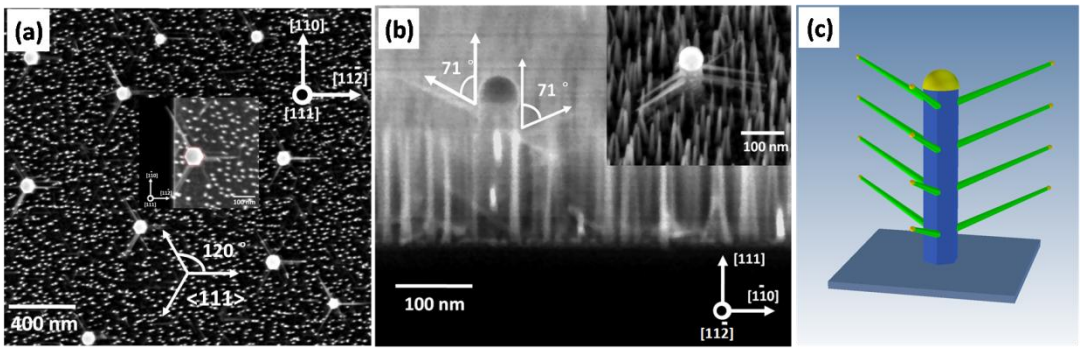

Figure 6.1 (a) Top-view SEM images (see Fig.A10) of GaP nanowire heterostructures on Si(111) and Si[111] nanowires. On Si(111), the GaP nanowires are vertically aligned, otherwise, on sidewalls of Si[111] nanowires, they are all oriented in a three-fold symmetry of orthographic projection along the <111> directions, the insert shows a magnified top-view SEM image of a single GaP/Si nanowire heterostructure. (b) Side-view SEM image of the GaP nanowirs perpendicularly grown on Si(111), and the GaP branches have a 71 ° tilt relative to the Si[111] nanowire, insert is a top-view image with 15 ° tilt. (c) Illustration of the GaP nanowire heterostructure on Si[111] nanowire catalyzed by Au with a 3-D ideal branch alignment model.

SEM images of a well-controlled heteroepitaxial growth of sub-10 nm diameter of GaP nanowires on both the Si(111) substrate and the side walls of vertically aligned epitaxial Si[111] nanowires are shown in Figure 6.1. Measured from the top-view image (Figure 6.1a), the diameters of the Si[111] nanowires alter between 60 nm to 90 nm with a 500 nm mean distance. Each one has the same set of vertically arranged hexagonal facets. From the insert of a magnified top-view along the [1$\bar{1}$0] cleaving edge, it was verified that the Si nanowire had a hexagonal {110}-type faceting, and the GaP branches grow on the two-facet edges. The branches are all along the three tilted <111> epitaxial directions of the Si(111) substrate in a three-fold symmetry, as labeled with a 120 ° orthographic projection angle in between. For the GaP nanowires grown vertically on the Si substrate (corresponding to the bright spots in top-view image), the diameter was below 10 nm and the mean distance was around 30 nm, corresponding to a wire density around 5×10^{11} cm^{-2}. Moreover, most of the GaP nanowires were grown perpendicular to the substrate, the other kinked <111> growth directions are restrained or completely avoided. Figure 6.1b is a side-view SEM image, with the [11$\bar{2}$] viewing direction perpendicular to the cleaving edge. It is obvious that the sub-10 nm GaP nanowire branches connect with the Si nanowire core, having a homogeneous length of 150 nm, similar to the ones grown vertically on the Si substrate. On the {112} facet-edges visible from [11$\bar{2}$] viewing direction, the branches extrude with a 71 ° deviation from the Si[111] growth direction, exactly along the three kinked <111> epitaxial directions of the Si(111) substrate. From the opposite viewing direction with a 15 ° tilt shown as an insert, it is evident that the branches align along the three facet-edges with a homogeneous spacing, which is illustrated as an idealized 3D model in Figure 6.1c.

Therefore, we propose the following nucleation and growth scenario: After the post-anneal, the growth of GaP nanowires was catalyzed by the Au nanoclusters distributed along the {112} facet-edges of Si[111] nanowire with a three-fold symmetry, as well as on the Si substrate in between. The Au catalyst tip for the Si nanowire growth was directly observed in the SEM images. However, it was not directly confirmed that the Au nanoclusters formed by the post-anneal catalyzed the sub-10 nm GaP nanowire growth. There is also the possibility of self-catalyzed growth by the group-III metal itself [Tom08]. Different sidewall facets of Si nanowire existed after the VLS growth: {110}-type as shown in Figure 6.1 and the typically observed {112}-type faceting [Ros05], which probably has a relationship to the wire diameter [Zha05].

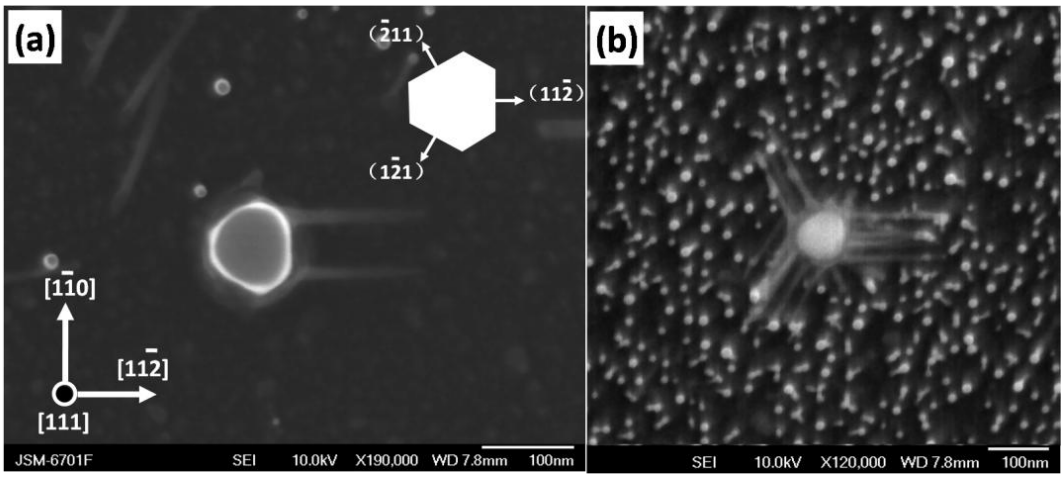

Figure 6.2 Relationship of the GaP nanowire growth to the Au diffusion on the Si[111] nanowires with {112}-type faceting. Top-view SEM images of GaP NWs grown on the {112}-type facets (a) without post-anneal and (b) with post-anneal process. A schematic representation of the cross-section of the {112}-type faceting in (a) is marked with the three wider facets.

Using the UHV-CVD method, we found that the indexing of side facets of Si[111] nanowires is dependent on the SiH_4 partial pressure. Shown in the top-view SEM images of Figure 6.2, Si nanowires were grown at a lower SiH_4 partial pressure of 0.05 mbar, without changing other conditions. We noticed that, at half of the pressure used for the {110}-type faceting, the sidewalls changed to the {112}-type with similar nanowire diameters. To exclude the possibility of self-catalyzed growth of GaP nanowires by gallium, the post-anneal process was selectively either used or not used. The result is quite obvious, from the comparison between Figures 6.2a and b. Without any post-anneal, only at a few random positions, some GaP nanowires grew out (Figure 6.2a). The delay time of the phosphorus source we adopted was not long enough for gallium droplet formation, which works as catalyst for the self catalyzed growth. In addition, most of the Au was probably still dissolved in the Si bulk [All08], or formed a thin cover layer on the surface of Si [Den08]. Implementing post-annealing as described above, a high density of GaP nanowires on both the Si substrate and the sidewalls of Si nanowire was observed (Figure 6.2b). Thus, the post-anneal was responsible for the formation of the desired size of Au nanoclusters, which nucleate at positions having higher surface energy. Nevertheless, it should be mentioned that the alignment of the GaP branches grown on the three broader {112} facets (illustrated in Figure 6.2a)

was less homogeneous, than observed for the {110}-type faceting. Instead of the linear confinement along the facet-edge, on the {112} facets, Au nanoclusters were dispersed with about half of them sitting at facet-edges, and the others distributed randomly in between. The gold diffusion on the Si nanowire can be influenced by the silane partial pressure, the growth temperature, and the wire diameter [Den08]. Lugstein *et al.* demonstrated GaAs nanowire branches grew perpendicularly on each {112} facet with a six-fold symmetry, and a few cases with a quasi three-fold symmetry suggested a minimal facet size for whisker nucleation [Lug07]. In the higher silane partial pressure mode we used, the Au diffusion was probably rapid on the {110} facets. Otherwise, the narrow {112} facets have a higher surface energy and are preferential nucleation sites for the parasitic GaP growth. Accordingly, ultra-thin GaP branches prefer growing along the three-fold symmetry facet-edges in the {110} faceting case as well as on the broader {112} facets.

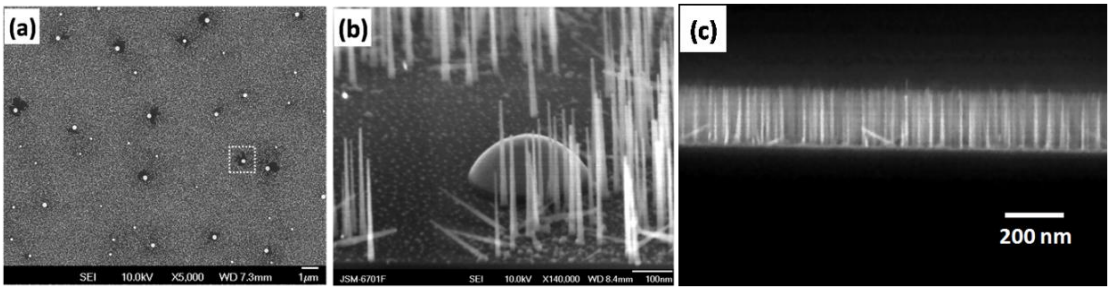

Figure 6.3 Influence of increase of Au droplet size and post-anneal temperature on the Au diffusion for the different GaP NW heterostructures, shown as top-view (a), 15 ° tilt (b) and side-view (c) SEM images. Without changing other growth conditions, a 60 min annealing at 500 ℃ for Au droplet formation, and a post-anneal with 600 ℃ were adopted. (b) The neighborhood of the 250 nm diameter Si NW is magnified from the area selected in (a). Most of the GaP NWs grow on the Si(111) perpendicular to the substrate with a homogeneous length (c).

We now focus on the effects of the initial Au droplet size and the post-anneal temperature on the Au nanoclusters formation. Except for these two parameters, the experiments were performed under equal growth conditions as those mentioned above. After a 60 min annealing at 500 ℃, the Au droplets possessed a distinct size distribution ranging from tens of nanometers to hundreds of nanometers in diameters, and large mean distances (several micrometers) between the large islands. The milky grey area in Figure 6.3a is covered by a high density of GaP nanowires. The white dots are large diameter Au islands. Some of them are surrounded by a black region. Figure 6.3b shows a very short Si nanowire with about 250 nm diameter covered by a Au hemisphere. The substrate on the left side of the large nanowire is empty. The Au droplet might have moved around on the surface and removed Au from the black area. It was reported that Au could move within its diffusion length depending on the temperature and the diameter of nanowires [Den08]. Moreover, the collection also happens on the surface of the substrate, within an area with a radius determined by the diffusion length [Bor07]. A collection of Au by surface diffusion during the 600 ℃ anneal after the silicon nanowire growth should have produced symmetrical Au depleted areas.

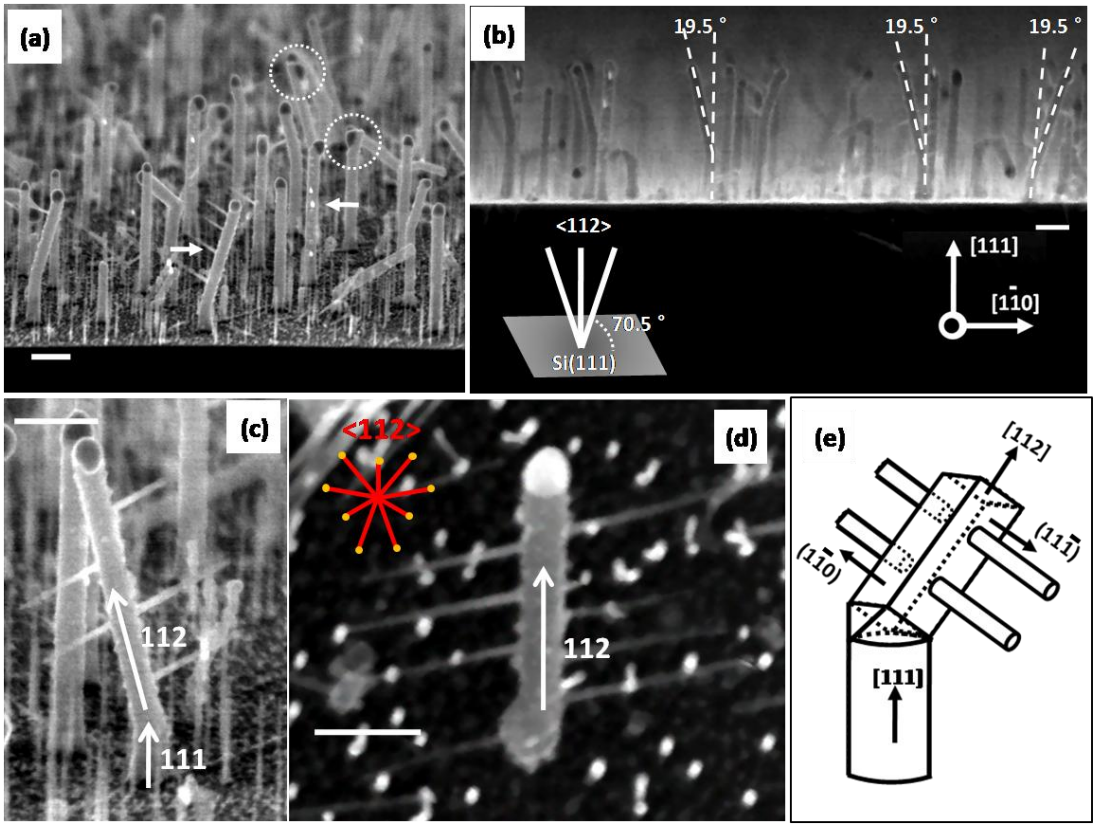

Figure 6.4 Influence of decrease of Au droplet size and post-anneal temperature on the growth of GaP nanowire heterostructures. (a) 15 ° tilted and (b) 0 ° tilted side-view SEM images of GaP/Si nanowire heterostructures. A 15 min annealing at 500 ℃ for Au droplet formation, and a post-anneal with 500 ℃ were used. (c) The 15 ° tilted side-view and (d) top-view SEM images of GaP nanowire branches grown oppositely on the sidewalls of kinked Si[112] nanowires. (e) 3D principle sketch illustrating the GaP branches grown perpendicularly on the two opposite (111) facets of a Si[112] nanowire, the growth directions and indices of the rectangular faceting are indicated with arrows. Scale bars are 100 nm.

It was confirmed that a higher post-anneal temperature enhanced the Au diffusion on the Si substrate, and we expected that if the parameters would be changed the other way round, the Au diffusion should be reduced. Figure 6.4 presents the Si-GaP nanowire heterostructures grown after a 15 min annealing for Au droplets formation at 500 ℃. The post-anneal temperature was decreased to 500 ℃. Figure 6.4a is a tilted side-view SEM image along the Si[1$\bar{1}$0] cracking line. The Si nanowires have a diameter of 30 nm and a height of 400 nm. Some of the catalysts tend to sit on the sidewalls of nanowire tips or tend to kink, as highlighted with dashed circles. It is obvious that the GaP nanowires grown on the Si substrate have a lower density, as well as a smaller diameter and a shorter length compared to Figure 6.1. Along the sidewalls of vertically grown Si{111} nanowires, almost no branches could be observed. However, indicated by the white arrows, a few GaP branches were grown vertically on the kinked sidewalls of Si nanowires in a linear alignment. The side-view SEM image of Figure 6.4b shows that the kinked Si nanowires first grew epitaxially in [111] direction, and changed to the <112> directions during growth. Viewed along the [11$\bar{2}$] zone-axis, the measured kink angle of 17 ° away from Si[111]

orientation corresponds to <112>-oriented Si nanowires with tilt of 70.5 ° relative to the substrate surface (illustrated in the inserted schematic drawing). It was observed that the GaP nanowire branches were mainly grown oppositely along two sidewalls of <112>-oriented segments, in both side- and top-view SEM images (Figure 6.4c-d). Zhang *et al.* demonstrated that <112>-oriented Si nanowires were characterized by a single configuration of a rectangular cross section enclosed by two (111) and two (110) facets, by low Miller index surfaces [Zha05]. Considering the absence of Au nanoclusters on the (110) facets observed in the {110}-type faceting of Si[111] nanowires, a growth model is illustrated in Figure 6.4e to visualize the crystallographic relationship of the GaP branch heteroepitaxially grown on the <112>-oriented Si nanowire. Si[111] wires could have similar facets with {112} and {110} segments while the connected Si[112] wire was a rectangular prism with opposite (110) and (111) facets. There are in principle three inclined <112> growth directions with an angle of 19.5 ° relative to the vertical [111] direction. It is also clear that some intermediate facets in the kinked region connect the [111] column with the [112] rectangular prism. Although Hyun *et al.* proposed a transition faceting based on a regular Thompson tetrahedron with three inclined-type {111} planes [Hyu09], we use a simplified intermediate faceting with a rectangular (112) plane as the basal one for the [112]-oriented growth. The GaP nanowire branches grow perpendicularly on the opposite (111) facets. The previous discussion assumed ZB GaP, if the GaP was grown in the WZ phase, the growth direction would be indexed [000$\bar{1}$].

6.2.2 Phase Transition in Sub-10 nm GaP Nanowires

It is well known that III-V nanowires typically have an additional lateral growth resulting in a tapered shape. On the Si(111) substrate, most of the sub-10 nm GaP nanowires grew vertically with a slight tapering according to our low growth temperature. Now, let us consider the interfacial crystal structures of the sub-10 nm diameter GaP nanowires grown heteroepitaxially on Si(111) substrate, i.e. the initial stage of growth. Cross-sectional HRTEM images taken along the [1$\bar{1}$0] zone axis (shown in Figure 6.5) are analyzed here. We found two types of different crystal structures in the bases of the wires illustrated in Figure 6.5a and b, respectively. Both of them contain a short ZB structure involving lateral stacking faults in between. All observed GaP nanowires grew heteroepitaxially on Si(111) with first a short ZB segment and later a continuous WZ structure along the [0001] direction perpendicular to the substrate. Moreover, instead of the vertical [111] growth direction observed for large diameter GaP nanowires with ZB structure [Mar04, Bak07], the thin ZB section had several different growth directions. Illustrated in Figure 6.5a, the wire measured at the base has a diameter of 9 nm. The first 35 ° tilt relative to the vertical [111] direction equals to the [110] growth direction, and the second 19 ° tilt corresponds to the [112] direction. Otherwise, with the diameter increased to 11 nm, an initial growth direction [001] was revealed (Figure 6.5b). Due to the experimental delay of introducing phosphorus, the catalyst should be in a state of high Ga supersaturation before the growth. The heating resulted in Au-Si eutectic droplets. Ga can be dissolved easily in the Au-Si eutectic [Kuz74]. After switching on the Ga precursor, an Au-Ga-Si eutectic was formed. The ZB structures with a lot of twins on the {111} planes, verified by the FFT patterns taken from the GaP/Si interface, were probably caused by the separation of Si out from the initial Au-Ga-Si ternary eutectic. According to the observation of a diameter-dependent growth direction of Si nanowire epitaxy by the VLS mechanism, the <110> and <112> orientations are preferred for sub-10 nm diameters. Cai *et al.* reported that ZnSe

nanowires had a diameter-dependent growth direction [Cai06]. However, the observed changes of growth direction and phase of sub-10 nm diameter III-V nanowires have not been reported at the time of writing the thesis. In the following text A, B, C has a meaning of labeling (111) planes with lateral offsets.

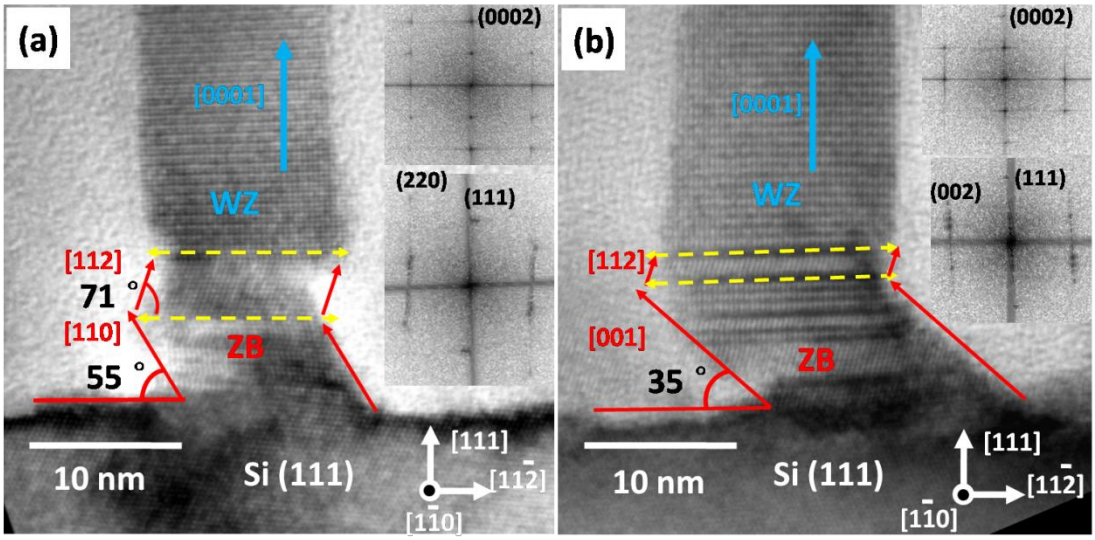

Figure 6.5 Cross-section HRTEM images of two GaP nanowires heteroepitaxially grown on Si(111) substrate and viewed along the [1$\bar{1}$0] zone axis: (a) one with a smaller diameter of ZB base (9 nm), heteroepitaxially grown in the [110] direction relative to the Si(111), (b) the other one with a larger ZB base (11 nm) with [001] base orientation. The upper dashed lines indicate the transition interfaces from ZB to WZ, the lower ones are according to direction change, and the FFTs from the interfaces of the GaP/Si and the WZ structure of GaP are respectively inserted on the corresponding right side in (a) and (b).

In general, we note that the GaP NWs changed to the pure WZ structure with a sharp transition on the (111) plane. The lateral stacking faults in the ZB structure, plus the atomic-level transition line, all suggest that the growth of the ZB structure proceeded in a layer-by-layer growth mode on the (111) plane. The catalyst droplet has a low energy interface to the (111) ZB plane and (0001) WZ plane during the whole process. This feature of the solid-liquid interface can be applied to the ZB structure growth model with different faceting. The projected side surface of <110>, <112>, and <100> ZB wires is not parallel to the growth axis. Figure 6.6a is an enlarged HRTEM image to illustrate the growth process at atomic level. The preferred growth direction of III-V A-B compounds is usually reported in literature as (111)B. In this experiment first the Ga source was opened and a first layer of Ga should have grown. This results in a top surface of (111)B. In the ZB phase, the stacking sequence is illustrated (Figure 6.6b) as C-B-A stacking, and the side surface corresponds to a [112] growth direction. A stacking fault plane, such as a B plane on top of C-B-A in the ZB phase, can result in a new B-A-B-A sequence of the WZ phase, which leads to the growth of WZ in <0001> direction. In order to produce such a structure, we can assume an asymmetric nucleation at the side surface of the wire. In analogy to the mechanism reported in an *in situ* solid catalyst growth experiment [Hof08], the growth might proceed in a ledge-flow mode

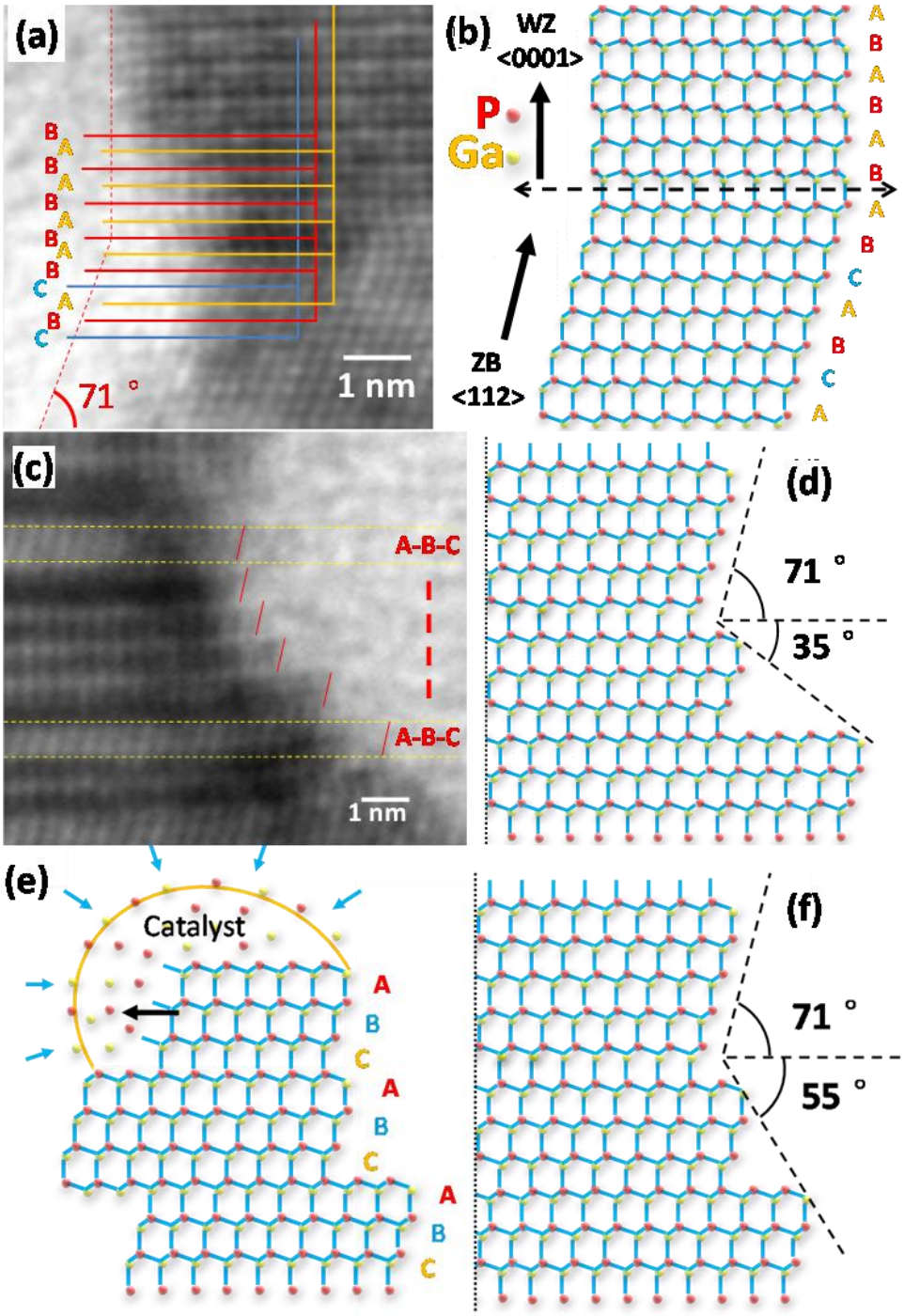

Figure 6.6 Enlarged HRTEM images and 2D atomic models in the <1$\bar{1}$0> viewing direction. (a) Transition from ZB to WZ, (b) the side surfaces of ZB nanowire are (111)A and (111)B planes, respectively, and atomic planes of stacking sequences during the transition are illustrated from C-B-A to B-A-B-A stacking. (c) The side surfaces of ZB nanowire are sawtooth-shaped with stacking unit of C-B-A within dashed yellow lines, the right edges of the respective nucleus are marked by red lines. (d) Scheme of atom position at the right edge, a shift of 5{111} layers is responsible for the [001] direction depicted in the 2D atomic model. (e) The catalyst covers a nucleus of C-B-A layers with a lateral ledge-flow growth direction as marked with the black arrow, (f) the side surface of ZB phase corresponds to the [110] (55 °) and [112] (71 °) growth directions.

from one sidewall to the other. The important difference to a layer by layer growth is that in this case a complete unit cell with a height of three (111) planes (for ZB) is nucleated and the growth front builds three layers. As shown in Figure 6.6b, the nucleation would have a stacking sequence of C-B-A for the tilted ZB structure in [112] growth direction, and a sequence of B-A for the vertical WZ nanowire.

During the growth of the ZB phase, the nucleus at the outer edge of the Au catalyst contains a layer of the complete C-B-A stacking sequence. After the nucleation the growth continues in a ledge-flow growth mechanism (as illustrated in the 2D atomic model in Figure 6.6e). We assumed for the drawing that nucleation started from the right P-rich side surface and ended at the left Ga-rich side surface. Thus, we postulate a ledge-flow growth mechanism for the GaP nanowires of sub-10 nm diameter in the VLS epitaxial growth on Si(111) substrate. The transition from the tilted surface of the ZB segment to the parallel surface of the WZ nanowire can be understood by the change of the nucleus. During the ZB nanowire growth, the nucleus has a more complicated C-B-A stacking with a stepped side surface (Figure 6.6c). Such a nucleus requires more atoms and this results in the observed high density of stacking faults in the ZB phase. The lattice of WZ is a simple two-layer stacking sequence resulting in the <0001> growth direction. In a nonequilibrium VLS nanowire growth, different lateral shift widths of the nucleus lead to the different growth directions. As illustrated in Figure 6.6d, a lateral shift of 5 {111} planes of the nucleus results in the observed [001] growth direction. Similarly, a shift of 3 {111} planes is responsible for the [110] direction (Figure 6.6f).

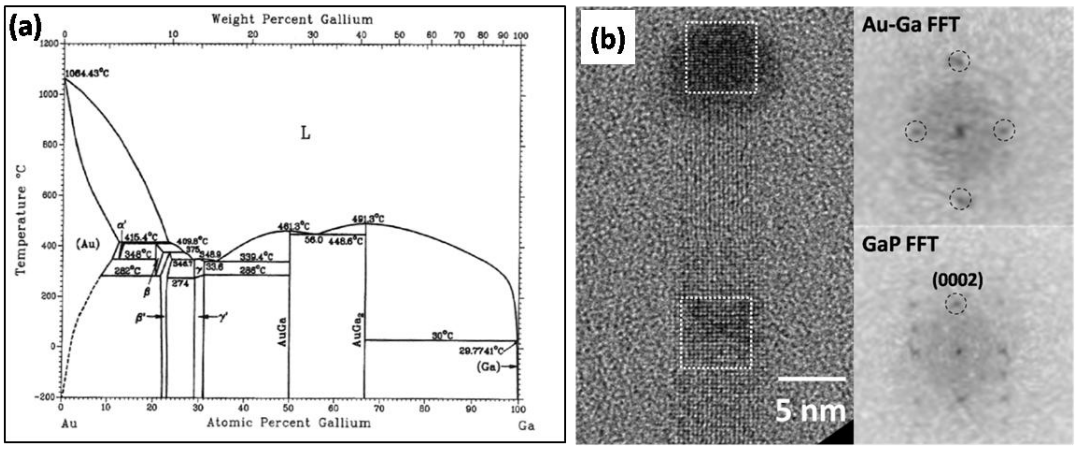

Figure 6.7 (a) Binary phase diagram of Au-Ga [Mas98]. (b) HRTEM image of a GaP nanowire with catalyst tip, in which the WZ structure GaP ends with a Au-Ga tip with two perpendicular lattice planes, and the FFTs are shown respectively taken from the dashed square boxes on the left side.

To understand the phase transition between ZB and WZ structure in more detail, we combined the crystallographic information included in the catalyst after growth with the phase diagram of Au-Ga (shown in Figure 6.7a). The GaP WZ nanowire continued growth to the final end with a diameter of 5 nm (Figure 6.7b). The metal catalyst had a spherical shape with a larger diameter (8 nm) connecting to the GaP. The selective-area FFT patterns were taken from the square regions marked in Figure 6.7b, taking the FFT pattern from the WZ GaP as a reference. In an attempt to

identify the phase of the catalyst particle, the image was compared with several possible Au-Ga phases with increasing content of Ga (see also table A1 in appendix). The result was $AuGa_2$ as the most probable phase. The calculated images (see figure A1 in appendix) compared with the real HRTEM image using the software JEMS (P. Stadelmann, CIME-EPFL, CH-1015 Lausanne, Switzerland). Only the phase $AuGa_2$ viewed in [11$\bar{2}$] direction fits. At a growth temperature of 470 ℃, during growth the catalyst was probably a liquid within a broad Ga-concentration range. The bulk phase $AuGa_2$ has a thermal stability range from 0-491 ℃ as illustrated in the bulk phase diagram. For a particle with diameter 8 nm, a considerable shift of the phase diagram to lower temperatures is expected [Kim09a] and during cooling the phase $AuGa_2$ was formed. We used a fast cooling process from the growth temperature of 470 ℃, and simultaneously pumped off the precursors back into the UHV condition. The experiment was performed under Ga-rich condition. During cooling the small amount of P dissolved in the catalyst was used up rapidly and a Ga-rich liquid remained. Upon further cooling the undercooled liquid nucleated and the solid $AuGa_2$ was formed. At the initial stage of heteroepitaxial growth on the Si substrate, the liquid catalyst contains silicon as a Au-Si eutectic. If it would start from pure gold, the Au-Ga eutectic liquid would occur with some delay, since the Ga supersaturation needs to increase initially. Si may dissolve into the GaP and cause doping, but with an amphoteric character of the doping [Dix08]. The very initial ZB phase of the GaP nanowire with stacking faults changes to a pure WZ phase, when the Ga supersaturation is above some critical value. That the WZ formation is favored by a high gallium supersaturation, is also supported by our crystallographic analysis of gallium-rich catalysts after the growth.

The crystallographic details of the GaP branch grown on the Si nanowire sidewalls are revealed in Figure 6.8. In order to observe the integral branched structure, considering the orientation relationship of branches to the Si nanowire faceting (shown in Figure 6.1), which has a three-fold symmetry of branches on the {112}-type facet edges, the TEM sample was cut along the [11$\bar{2}$] direction. From the low-magnified cross-section image (Figure 6.8a) it can be seen that one integral branch was still connected to the Si sidewall sealed in the protective glue. The dark contrast at the tip indicates a higher atomic number Z at the catalyst end. The magnified HRTEM image taken from the connection, which is marked by the black dashed square, is shown in Figure 6.8b. The dotted lines are the outline of the branch base. The 8 nm diameter GaP branch grew epitaxially on the sidewall of the Si[111] nanowire, although the branch was bent by the spin-coating of the protective glue layer, and the lattice planes show only weak contrast. Initially, the ZB GaP grew heteroepitaxially in the Si[11$\bar{1}$] direction, with a 71° rotation from the Si[111] direction, and it shows several twins. A flat twin plane perpendicular to the growth axis is marked with a white dashed line (Figure 6.8b). We have to consider that the Au droplet could have sunk into the Si surface during the annealing for Au/Si alloy formation, thereby wetting {111} facets [Roe06]. During the post-anneal under a high-vacuum condition, the Au clusters sitting on the facet-edge should sink into the {211} facet-edge, creating narrow facets. From the contrast difference between GaP and Si at the interface in Figure 6.8b, the [11$\bar{1}$] facet was identified. Several smaller catalyst particles were found along the edge without GaP branch growing. Figure 6.8e shows a Au-Ga nanocluster of about 6.5 nm diameter sitting on the Si [11$\bar{2}$] edge. It sank into the Si with a stepped [11$\bar{1}$] interfacial facet seen in high resolution. It was confirmed that, as shown in the selective-area FFT pattern (insert of Figure 6.8e), this Au-Ga nanocluster was also in

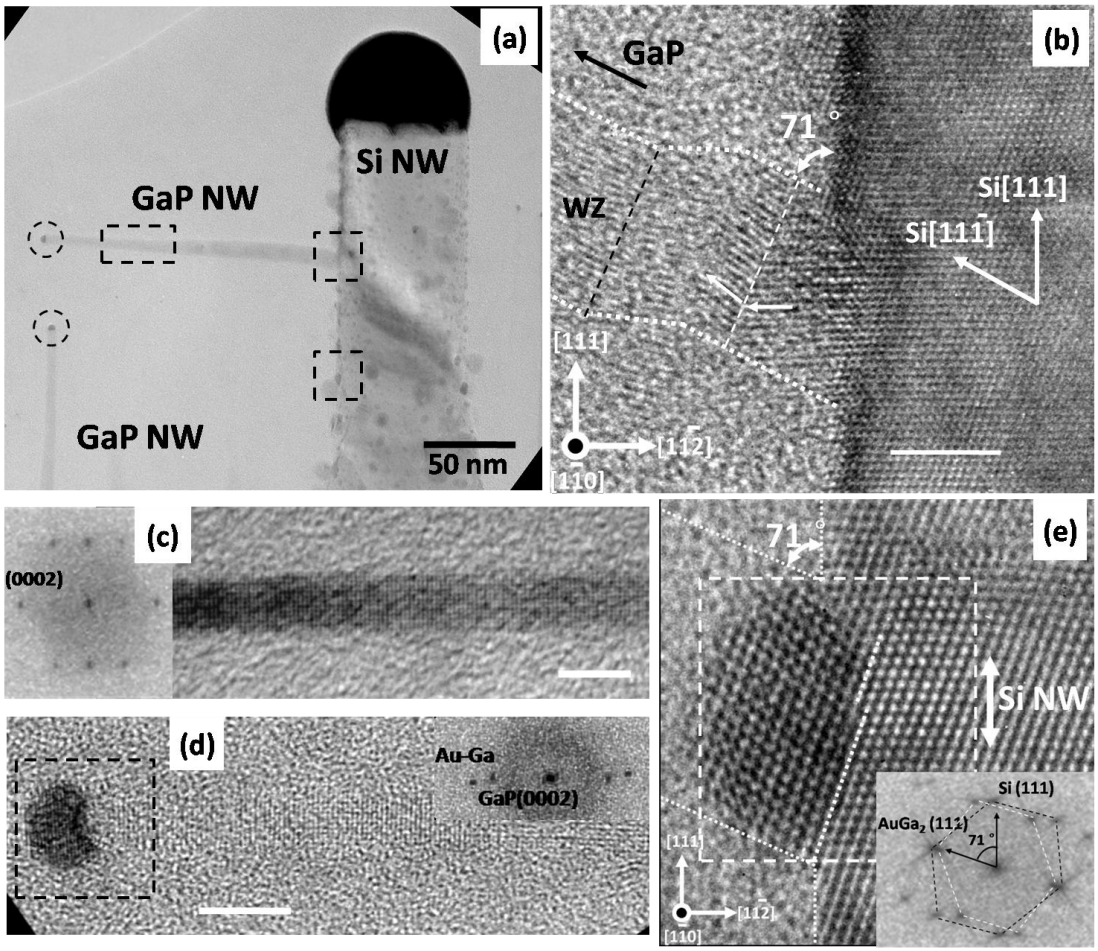

Figure 6.8 Visualization of the heteroepitaxial growth of the GaP NW branch on the Si[111] nanowire sidewall. (a) Overview TEM image with the catalyst tips of the GaP NWs grown on both Si substrate and Si NW indicated with dashed circles. (b) HRTEM image of the hetero-interface on the Si[11$\bar{2}$] edge viewing along the [1$\bar{1}$0] zone axis, which is taken from the selected dashed square box in (a). The branch base is along the Si [11$\bar{1}$] direction with 71 °tilt relative to the Si[111] direction, a twin plane at the base is marked with a white dashed line. (c) HRTEM image and FFT pattern taken from the dashed rectangular box in (a) show a pure WZ GaP branch with a diameter of 4 nm. (e) HRTEM image and FFT pattern of a $AuGa_2$ particle formed on the sidewall of Si the nanowire, at a different position marked in (a). The scale bars are 5 nm.

the $AuGa_2$ phase. The created [11$\bar{1}$] facet is a twin plane, and the measured lattice misfit of 11.5% is quite close to the 11.8% lattice misfit between $AuGa_2$ and Si. Due to the high misfit, several dislocations were observed along the interface. Similar to the already presented growth of GaP nanowires on the substrate surface (Figure 6.5), the branch shown in Figure 6.8a started to grow with a ZB segment. After growing to a length of 10 nm with several twin planes, the ZB wire changed to the pure WZ structure as a result of increase of Ga supersaturation. The transition is indicated by a black dashed line in Figure 6.8b. The body of the WZ GaP branch (black dashed rectangular box in Figure 6.8a) has a slight tapering with a sub-5 nm diameter (shown in Figure 6.8c). The explanation for the phase transition here is the same as for the GaP nanowires grown on the Si(111) substrate. By the crystallographic analysis from the HRTEM image at the tip (Figure

6.8d), we found lattice planes probably being the {220} planes of $AuGa_2$ as well. This analysis was based on heteroepitaxial structures of linearly aligned GaP branches on the facet edges of Si nanowire with {110}-type faceting. It is possible that for samples grown under other conditions, different types of faceting and heteroepitaxial directions may be observed (Figure 6.2 and Figure 6.4), which will not be discussed in more detail here.

6.2.3 Optical Characterizations

GaP is a popular semiconductor material, due to its large energy band gap (*E*g = 2.26 eV at 300 K) and good thermal stability [Lor68]. However, the indirect band gap nature usually limits its applications in optoelectronic fields. One promising approach to overcome the indirect nature of optical transitions in GaP is by the quantum confinement effects in low-dimensional nanostructures. Nanotube and nanowire structures have been introduced into traditional III-V materials, due to their unique optical properties distinctive from those of the bulk materials. Thus, vertically-aligned high-density sub-10 nm diameter GaP heteroepitaxial nanowires on Si would be ideally suited to investigate the role of dimensionality and size on the optical properties.

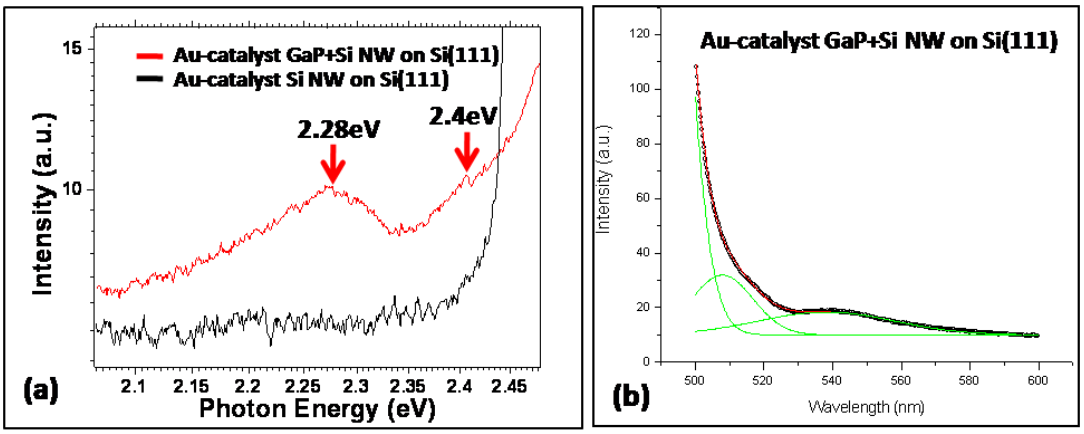

Figure 6.9 (a) PL spectra of the Au-catalyzed GaP + Si nanowires on Si(111) substrate and Au-catalyzed Si nanowires on Si(111) substrate at room temperature, the excitation wavelength was 475 nm. The Gaussian peak analysis of PL of sample with the GaP + Si nanowires on Si(111) substrate is shown in (b), one emission peak was at 508 nm, another one was at 539 nm.

The photoluminescence (PL) spectroscopy was measured by a Hitachi F4500 fluorescent spectroscope with the excitation at a wavelength of 475 nm. The spectral resolution of the detection system was 0.2 nm. The optical excitation was generated by an OPO laser pumped by a mode-locked high-energy Nd:YAG laser (PL2143) with a repetition rate of 10 Hz. The laser pulse duration was 20 ps and the excitation wavelength could be selected from 450 nm to 540 nm. Time-integrated emission spectra were recorded by a synchroscan streak camera connected to a monochromator. The excitation picosecond laser pulse was focused on the sample by a lens with focal length of 150 mm with a grazing incidence between the incident light and the normal of the sample plane. The light emission from the sample was collected with a home-built lens system into the spectroscope which was connected to the streak camera. The whole detection system gives

a time resolution of about 20 picoseconds and spectral resolution of 2 nm, respectively. The experiment was performed at room temperature.

The PL spectra of the as-grown high-density GaP + Si nanowires on Si(111) substrate (shown in Figure 6.9a) and the same sample before CBE (i.e. Si[111] nanowires on Si(111) substrate within the same diameter range) were measured and two PL peaks are distinguishable at about 2.4 and 2.28 eV only from the sample with GaP nanowire heterostructures. From the Gaussian peak analysis of the PL spectra (Figure 6.9 b) we can find that the sample with GaP + Si nanowire heterostructures showed the most significant light emissions at a wavelength of 539 nm (2.28 eV) with a half width of about 20 nm and at 508 nm (2.4 eV) corresponding to a smaller half width of about 10 nm, while the control measurement gave no light emission for wavelengths from 500 nm to 600 nm. Comparing the two curves in Figure 6.9a, it is obvious that the two light emission peaks did not originate from the silicon nanowires with the Au catalysts on top or the Si substrate. Indirect energy gaps of 2.26 eV at room temperature for bulk GaP material have been reported [Lor68]. Assuming that the sub-10 nm diameter of GaP nanowires changed the character of the indirect band structure towards a direct band structure, the light emission efficiency of ZB GaP would be increased. A recently published calculation by De and Pryor [Dep10] predicts for WZ GaP a direct band gap at 2.25 eV, slightly smaller than the indirect band gap of ZB GaP. For the compound WZ InP a direct band gap layer than the ZB InP band gap was predicted [Dep10], which matches to an experiment with InP nanowires [Pai09]. In the ZB parts of the GaP nanowires a high density of structural defects such as stacking faults and twins were observed. The WZ parts were bent by the glue, but all positions which allowed lattice plane imaging showed a defect free WZ stacking. The surfaces of the wires were covered by native oxide. The surface defects strongly influence the physical properties of the sub-10 nm diameter nanowires due to the large surface-to-volume ratio. Moreover, Si and C impurities act as shallow dopants and will introduce new energy states into the band gap. Therefore, it is possible that the PL peaks are attributed to band-to-band recombination channels caused by the impurities and defects, and a red shift would occur. The quantum confinement causes a blue shift of PL signals from small GaP particles [Kim02]. The combined effects of blue and red shifts are measured. The peak at 2.4 eV might arise from WZ GaP, the broader peak at 2.28 eV from ZB GaP.

We have also measured the time-resolved properties of the two different heterostructures described above, which is an important tool for understanding how the emission changes as the electron-hole pair density changes in the nanowire. In the experiment we have found that the excitation at 490 nm (2.54eV) was rather better that other ones between 450 nm to 540 nm. From Figure 6.10a, we can find that the Au-catalyzed GaP heterostructures and both Au-catalyzed and Al-catalyzed Si nanowires grown epitaxially on Si(111) undergo an ultrafast light emission under our picosecond laser excitation, although the lifetimes and emission intensities are quite different. From the curve of the sample including GaP nanowires, it is apparent that, after the initial fast decay (i.e. about one order of magnitude intensity drop in less than 100 ps), a slower decay process extends to a nanosecond time scale. However, the other samples with only Si nanowires exhibited only fast light emission processes. Moreover, the logarithmic plots of the emission intensity decay curves are shown in Figure 6.10b. The lifetime is defined as the decay time from the peak to 1/*e* of it. The fast decay processes fit the single exponential decays with lifetimes of 16

ps and 100 ps for Si nanowires and GaP nanowires, respectively. It was suggested by Maly *et al.* that there were two kinds of decay components: the slow one with several nanoseconds to microseconds was attributed to confined carrier processes in localized surface states, while the fast process of picosecond order has been assigned to the nonradiative recombination process of free carriers [Mal96]. In addition, both Paiman *et al.* and Pemasiri *et al.* demonstrated that InP nanowires which appeared to be mainly WZ phase exhibit recombination lifetimes an order of magnitude larger than their ZB counterpart with significantly higher quantum efficiencies [Pai09, Pem09]. At room temperature, a high density of free carriers created by the high excitation density of laser pulse at 2.54 eV recombined nonradiatively within a short time through recombination centers on the surface. The measured decay process of Si nanowires is close to the 20 ps of our time resolution. The Si decay was assumed to be in the sub-10 ps range actually. Otherwise, the slower decay in the recombination of GaP nanowires is attributed to the radiative lifetime of the carriers localized at impurities or defects of GaP [Dim83]. Especially, the sub-10 nm GaP nanowires have a larger surface-to-volume ratio compared with the Si nanowires. The slower decay process can be attributable to the recombination of confined carriers in localized surface states. Besides, Au atoms were found in grown III-V nanowires catalyzed by Au [Per06]. Au can cause unintentional doping of the nanowires, or work as trap center for recombination of electron-hole pairs. To verify this influence on the emission decay process at room temperature, Al-catalyzed Si nanowires were used as a reference sample. The decrease of emission intensity is mainly due to a nonradiative recombination of electron-hole pairs trapped into deep impurities or defects, reducing the radiative efficiency via Shockley-Read recombination processes [Sim71]. However, from Figure 6.10, it is obvious that the catalyst impurity had little influence on the lifetime. This can be explained by the dominant effect of surface states. In general, the carrier lifetime of sub-10 nm GaP nanowires was much higher than the ones for Si nanowires with larger diameters.

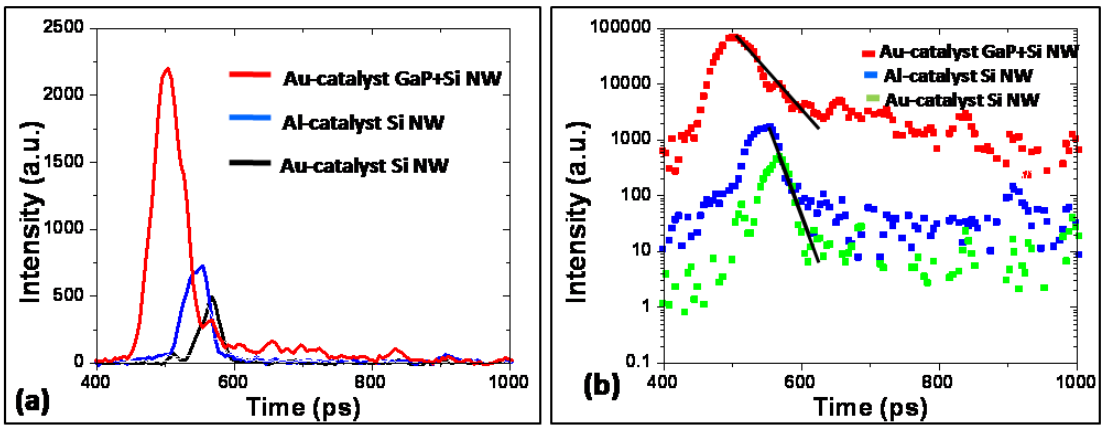

Figure 6.10 (a) Time-resolved spectra of the corresponding Au-catalyzed GaP + Si NW heterostructures, Au-catalyzed and Al-catalyzed Si NW on Si(111) substrates, respectively, and (b) logarithmic plot of the emission decay curves excited at 490 nm, the solid lines were fit to the exponential decays corresponding to each sample.

6.3 Non-gold Catalyst Heteroepitaxy on Si

The most commonly used metal catalyst for VLS growth of nanowires is gold. One relevant concern about the use of catalysts is whether the catalyst is incorporated into the wires during growth and changes their physical properties. Direct observation of Au atom impurities incorporated into III-V nanowires by Au-catalyzed VLS growth has been reported [Per06]. Moreover, the use of Au should be avoided for integration with Si substrates, in order to produce devices compatible with Si-CMOS technology.

6.3.1 Al as a Catalyst

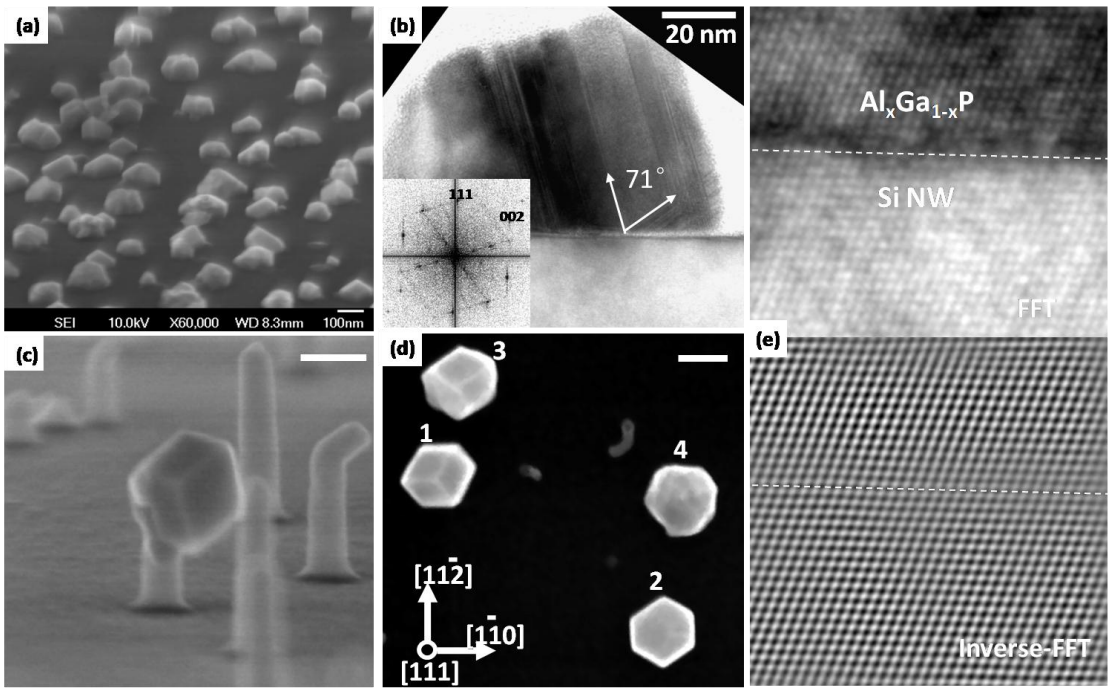

Figure 6.11 (a) Tilted top-view SEM image of the Al-catalyzed $Al_xGa_{1-x}P$ nanoislands grown on a Si(111) substrate. (b) Cross-sectional HRTEM image of a single $Al_xGa_{1-x}P$ nanoisland viewing along the [1$\bar{1}$0] zone axis, insert is its FFT pattern corresponding to twin planes with a 71 ° angle. (c) Tilted side-view and (d) top-view images of Al-catalyzed $Al_xGa_{1-x}P$/Si nanowire heterostructures on Si(111) substrate, scale bares are 50 nm. (e) A HRTEM image and corresponding Fourier-filtered pattern of the interfacial area formed on top of the Si nanowire, the dashed lines indicate the same interface.

Previously, we have discussed Al as a CMOS compatible catalyst for Si nanowire epitaxy. Furthermore, the ternary compound $Al_xGa_{1-x}P$ has the potential to extend the light emission range of the GaP-based material system into the blue-green portion of the optical spectrum [Cho00]. Another major advantage for integration with Si is that $Al_xGa_{1-x}P$ is lattice matched to GaP for all Al mole ratios, and thus has a low misfit to Si, which is essential to decrease the lattice mismatch-associated structural defects during initial stage of epitaxial growth. The nucleation and growth of Al-catalyzed GaP by CBE on both Si(111) substrates and the tip of [111]-oriented Si nanowires was studied by microscopy and PL spectra.

The H-terminated Si(111) wafers were covered by a Al film of 1 nm thickness in the UHV-MBE chamber without intentional heating of the substrate. Then, the wafer was *in situ* transferred into the UHV-CVD chamber with the annealing for Al droplet formation performed at 600 ℃ for 20 min. With partial pressures of 1×10^{-5} mbar and 1×10^{-4} mbar, respectively, TMG and precracked TBP (1000 ℃) were introduced successively. The CBE growth was continued for about 10 min at 600 ℃. Tilted top-view SEM images were used to illustrate the $Al_xGa_{1-x}P$ nanoisland morphology on Si substrate. Formation of discrete nanoislands was observed at each Al droplet site and no hemisphere-shaped Al remained after CBE growth in Figure 6.12a. The islands appeared to be faceted and fairly uniform in height (50～100 nm), and no typical catalyst droplets were observed on the nanoislands. However, the $Al_xGa_{1-x}P$ nanoislands were found to be quite unique in both size and faceting. An investigation of GaP islands reported {111}-type faceting at each growth temperature and effect was especially pronounced at 550 ℃ [San96]. Faceting and structural defects of a single nanoisland were analyzed, as shown in the cross-sectional HRTEM image of Figure 6.11b. It is obvious that no remaining Al cap existed on the surface. Defects in the islands, introduced at the early stage of heteroepitaxial growth, were identified to be stacking faults and planar twin dislocations from the inserted FFT. Defects in heteroepitaxial films are commonly due to lattice mismatch and thermal expansion mismatch stresses between the film and substrate during growth. However, as reported by Ernst *et al.* in the case of growing GaP islands on Si(001), the mismatch stresses played only a minor role in the formation of the planar defects and the dominant formation mechanism were atomic positioning errors on {111}-facets in the early stage of heteroepitaxy [Ern89]. Again, anti-phase defects are important. III-V compound semiconductors have polar (111) surfaces with either group III or group V elements terminating the lattice. A general relationship of planar defect formation mechanism and faceting cannot be obtained by investigations of a single island, but it was observed that the planar twin defects originate from the interface to the surface with two directions of {111} twin planes with a cross-angle of 71 °(as marked in Figure 6.11b). We believe that these defects were produced from interfacial defects caused by Al-Si alloy formation on Si substrate. In order to testify the influence of the Al/Si interface, the III-V growth was performed on top of the Al-catalyzed Si nanowires with the same growth parameters. Figure 6.11c shows the cubic morphology of an $Al_xGa_{1-x}P$ nanocrystal grown on the top of a Si nanowire. If it would be really a simple cube, indexing of side surfaces should be given as {100}. The shape of nanocrystals can be the result of multiple nucleation events: smaller initial crystals grow together and special interfaces between this partial crystals lead to a complicated surface morphology. From the top-view image shown in Figure 6.11d, several surface morphologies of $Al_xGa_{1-x}P$ were observed: No.1 as numerically marked had a cube-like morphology; with an in-plane rotation relative to No.1, the surfaces of the cube-like No.3 involved small facets; No.2 corresponded to a rod-like crystal with a six-fold symmetry of {110}-type sidewall faceting; No.4 partially lost its symmetry with a complicated morphology. Although several surface morphologies coexisted in our investigation, a decrease of morphological complexity compared to the nanoislands was caused by the smaller Al/Si interface area at the nanowire tip. A perfect hetero-interface was confirmed in a HRTEM image taken from the nanowire interfacial area, illustrated in Figure 6.12e. From the contrast difference, the interface between $Al_xGa_{1-x}P$ and Si was schematically indicated by a dashed line. The ZB $Al_xGa_{1-x}P$ was heteroepitaxially grown on the Si[111] nanowire, and its lattice constant estimated from the corresponding inverse-FFTs by Fourier transformation filtering was in

good agreement with the one of Si. No dislocation was found at the interface. Compared to Figure 6.11b, the density of planar defects was decreased considerably in the nanoparticle grown on a Si wire.

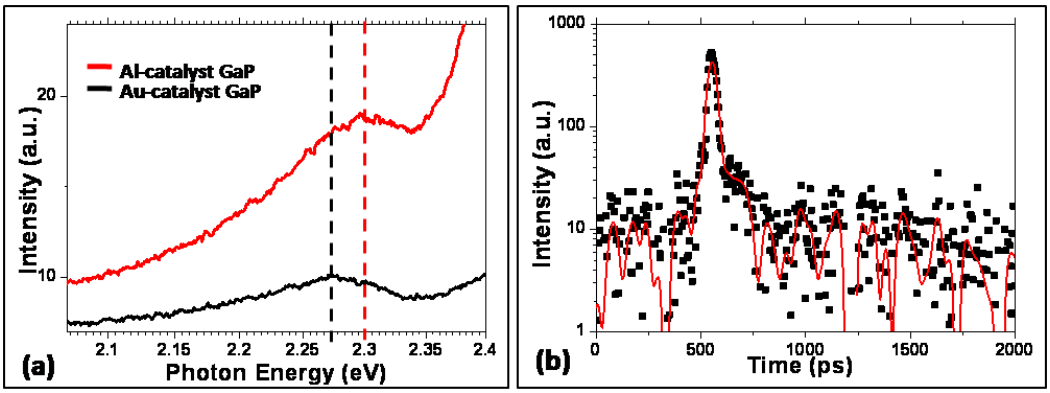

Figure 6.12 (a) PL spectra of the Al-catalyzed and Au-catalyzed GaP nanostructures on Si(111) substrates at room temperature, corresponding to an emission peak at 2.30 eV and 2.275 eV, respectively, and (b) a logarithmic plot of the emission decay curve of $Al_xGa_{1-x}P$ nanoislands. The excitation energy was 2.54 eV.

The PL spectra of the as-grown Al-catalyzed GaP nanoislands compared with Au-catalyzed GaP nanowires on Si(111) substrates is shown in Figure 6.12a. It is obvious that the two light emission peaks have different maxima. Similar to the previous result, Au-catalyzed GaP nanowires had an emission peak at 2.28 eV, whereas a blue-shift of about 20 meV was observed for the Al-catalyzed GaP nanoislands. The increase of the band gap energy confirmed the formation of an $Al_xGa_{1-x}P$ alloy instead of binary GaP. Estimation of Al concentration from the 20 meV blue-shift suggested that only a very small portion of Al was incorporated ($x \approx 0.02$) [Cho00]. Furthermore, a logarithmic plot of the time-resolved emission decay curve is shown in Figure 6.12b. It consisted of a fast decay process with a lifetime less than the time resolution of 20 picoseconds of the detection system. The mean size of nanoislands was larger than 100 nm and quantum confinement effects can be neglected.

6.3.2 Ag as a Catalyst

Recently, silver has been successfully used as catalyst for Si nanowire growth at a growth temperature far below the Ag-Si eutectic temperature [Wit10]. In particular, Ag creates two relatively shallow energy levels within the silicon band gap. Gallium arsenide (GaAs) and GaP are more prone to trapping effects than Si and Ge, caused by deep energy levels and defect levels [Mil73]. Au- and Ag-doped GaP have been studied by Ikizli *et al.* [Iki71]. The influence of Ag was manifested by a quenching of the red and an enhancement of the green luminescence when the concentration of Ag was increased. To our best knowledge, no author published the use of Ag as catalyst for GaP growth before. In our experiments, Ag (Alfa-Aesar; purity: 99.9%) was evaporated onto a H-terminated Si substrate (at 300 ^{o}C). Elevating the substrate temperature increases the surface mobility of Ag atoms, so that instead of a thin-film, Ag nanoparticles readily

formed. By that, an additional high temperature annealing step to break up the metal film can be circumvented. Then, the samples with the Ag nanoparticles were moved *in situ* into the UHV-CVD chamber to carry out the GaP growth. The CBE growth was kept for about 5 min at 480 ℃ with TMG and precracked TBP (1000 ℃) partial pressures of 1×10^{-4} mbar and 3×10^{-4} mbar, respectively.

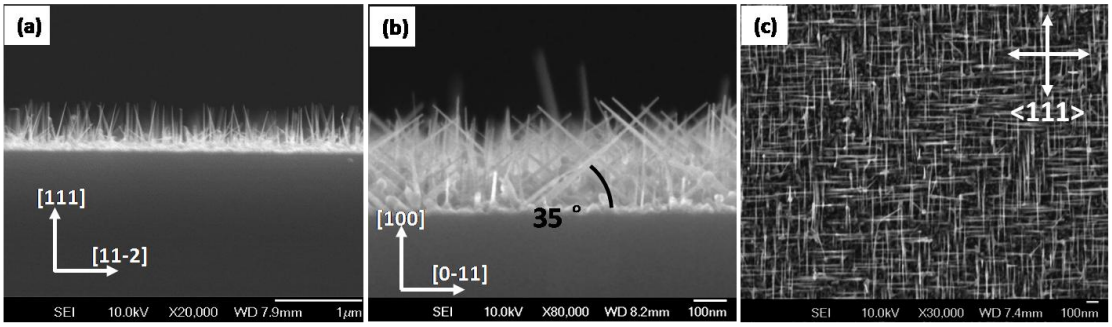

Figure 6.13 (a) Side-view SEM images of Ag-catalyzed GaP nanowires on Si(111) substrate taken with a cleavage along Si<112>, and (b) on Si(100) substrate taken with a cleavage along Si<011>. (c) Top-view SEM micrograph of the as grown sample on Si(100) substrate.

Figure 6.13a shows a side-view SEM image of Ag-catalyzed GaP nanowires grown on Si(111) substrate, cleaved along Si[11$\bar{2}$]. The mean diameter of the GaP nanowires was estimated to be tapered from 15 nm at the base to sub-10 nm at the top with a growth length of about 500 nm. Furthermore, most of the straight nanowires showed tilts of 20 °, 36 °, 55 °, 71 ° and 90 ° relative to the Si substrate. In this image the nanowires were projected on the plane perpendicular to the [1$\bar{1}$0] viewing direction. The observed angles can be explained by a growth mainly in <110> and <111> directions. The nanowires grown vertically along the [111] axis are projected perpendicular to the horizontal in the side-view image, and the nanowires oriented along the other tilted <111> directions have projections with either 36 ° or 20 ° to the horizontal. In contrast, the nanowires oriented along the <110> directions have projections with either 55 ° or 71 ° to the horizontal. Compared with the Au-catalyzed GaP nanowires grown on Si(111) in a similar diameter range, Ag-catalyzed ones had more tilted heteroepitaxial directions besides the perpendicular [111] direction. One can relate this to the solid state of Ag-Si during growth instead of the liquid Au-Si droplet, which has a direct influence on the nucleation. A control experiment was done on a Si(100) substrate. From the side-view image (Figure 6.13b) obtained with electron beam incident along the normal of the cleavage plane in [011] direction, the mean diameter, growth length, and even tapering of nanowires grown on these two substrates are almost the same. However, most of these wires were grown at 35 ° tilt or perpendicular to the horizontal of the Si(100) substrate seen from the side. Furthermore one can relate the stereographic projections of the Si(100) surface to the observed growth directions shown in the top-view (Figure 6.13c) micrograph. Hence, the Ag-catalyzed GaP nanowires were mainly grown along Si<111> directions on Si substrates.

Both annealing and growth temperatures (<500 ^{o}C) being far below the bulk Ag-Si eutectic temperature of about 830 ^{o}C, solid-phase catalysts may have been responsible for the nucleation of Ag-catalyzed GaP nanowires. Considering the phase diagrams of both Ag-Ga and Ag-P, a

considerable solid solubility range of Ga exists in the Ag-rich end with a maximum solubility of approximately 19 at.% Ga at 611°C, whereas, the solid solubility of P in Ag is less than 0.07 at.% [Mas98]. The change of the phase diagrams by the size effect does not influence the orders of magnitude and the content of Ga in the catalyst particles will be far higher than the amount of P. Its crystallographic characteristics were analyzed by TEM investigations. Figure 6.14a shows a TEM image of the top-side of a GaP nanowire with a diameter of 12 nm. The catalyst tip has a hemisphere shape sitting on the top of WZ GaP nanowire. Along the growth axis, the WZ wire had a sharp structural change at the catalyst-nanowire interface (marked by a dashed line in Figure 6.14a). Considering the delay of P input, we assumed that the catalyst mainly consisted of Ag and Ga. According to the published phase relations and crystal structures in the Ag-Ga system, at a growth temperature of about 480 ℃, the catalyst could be in the Ag-rich Ag_2Ga phase [Gun00]. Silver diffusion was studied in bulk and epitaxial GaP [Dzh81]. Within the limit of our EDX measurements, no Ag in the nanowire was detected. From an HRTEM image shown in Figure 6.14b, the Ag-rich catalyst could be distinguished from the contrast difference by the higher atomic z-value and had a cubic structure. The connected GaP is in its WZ phase with a diameter of about 17 nm. A further investigation of a nanowire with a sub-10 nm diameter is shown in Figure 6.14c. A crystalline Ag nanoparticle which had a diameter of 6.5 nm was connected with the WZ structure of the GaP nanowire. There are no obvious twin defects inside the catalyst compared with the larger one shown in Figure 6.14b. We assume the defects inside the catalyst particle have been induced by the precipitation of Ga during cooling.

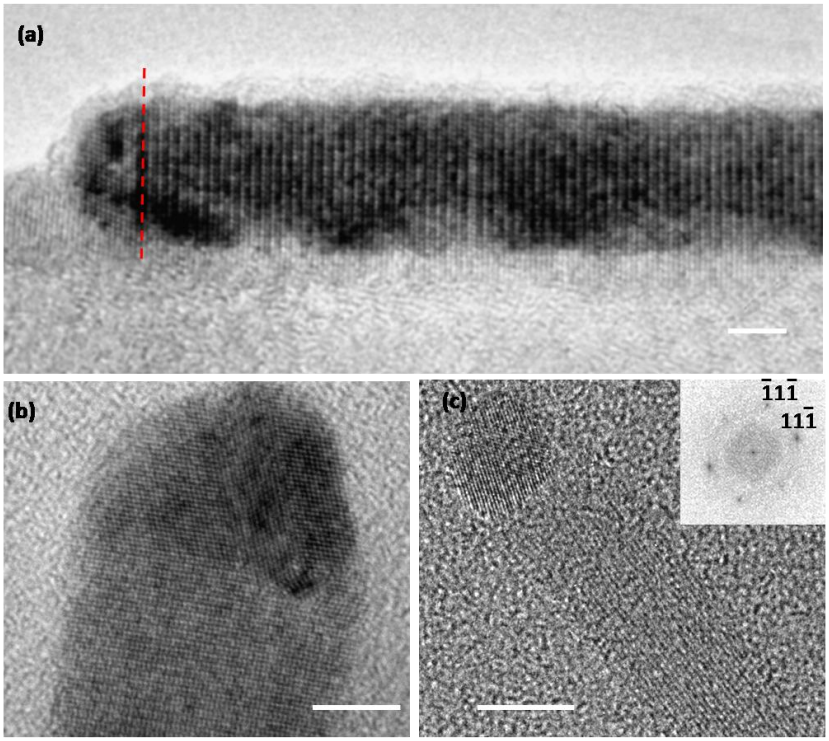

Figure 6.14 TEM investigations of Ag-catalyzed GaP nanowires. (a) A GaP nanowire connected with Ag catalyst tip with a sharp interface marked by a dashed line. (b) A nanowire tip with larger diameter showing a sharp interface between the WZ GaP and cubic fcc Ag catalyst with twin defects. (c) A smaller GaP nanowire showing a crystalline catalyst tip, insert is a selective area FFT from the Ag catalyst. Scale bars are all 5 nm.

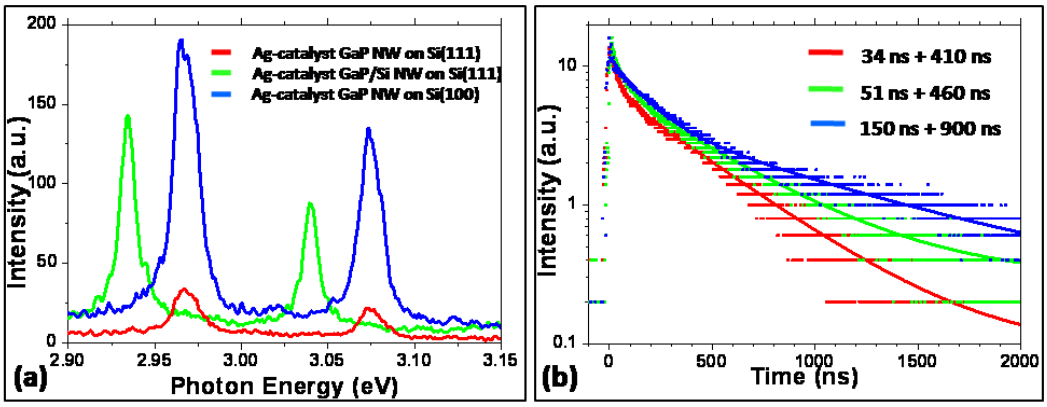

Figure 6.15 (a) PL spectra of the Ag-catalyzed GaP and Si/GaP nanostructures on Si substrates at room temperature, showing two emission peaks, respectively. (b) Logarithmic plots of the time-resolved decay curves, the solid lines are the exponential fitting results to the experimental data. The excitation energy was 3.49 eV.

We characterized the optical properties by analyzing PL and time-resolved emission spectroscopy at room temperature. It was the intention to show the effects of the silver catalyst on the structural and optical properties of GaP nanowires. Thus, the principal result of photoluminescence study with Ag as catalyst is the discovery of two unknown emission peaks in the blue range (blue and green curves shown in Figure 6.15a) instead of the well-known yellow-green ones in the PL spectra of bulk GaP. Both the samples grown heteroepitaxially on Si(111) and Si(100) substrates have two sharp emission peaks at 2.97 eV and 3.07 eV with narrow full-width at half-maximum (FWHM) of 12 ~ 17 meV. The intensity on Si(100) was one magnitude larger than on Si(111). We believe this was caused by the relatively large surface area of GaP nanowires with regards to the grazing incidence between the incident light and the normal of the sample plane. However, the GaP nanowires grown heteroepitaxially on Ag-catalyzed Si nanowires with similar sub-10 nm diameters showed a red-shift of about 40 meV to both peaks with a smaller FWHM of 10 meV. The narrow PL linewidth is particularly critical as its broadening often results from structural fluctuations and defects. The red-shift from Si/GaP hetero-nanowires can be interpreted as the influence of incorporating more Si atoms into the GaP, which were smeared out from the Ag-Si alloy after the Si nanowire growth. The Si atoms worked as shallow impurities, introducing new energy states into the bandgap of GaP. The optical properties of the nanowires were investigated in more detail by time-resolved measurements. The lifetime is related to the free carrier dynamics and allows one to estimate the contribution of radiative and nonradiative recombination of the free carriers. Since surface states are usually considered as the nonradiative recombination centers, the extracted lifetime of the decay curve can be used to assess the surface quality of nanowires. The corresponding time-resolved emission spectra are plot logarithmically in Figure 6.16b. All their decay curves have lifetimes (t1/t2) of 34/410, 51/460, 150/900 (ns), respectively, by fitting to the biexponential luminescence decay. The biexponential curve is associated with two slow decay processes with relatively long decay times. Previously observed fast decay processes in Au- and Al-catalyzed GaP nanostructures were all with picosecond time scale. We assumed that it was related to nonradiative surface recombination being dominant because of large surface-to-volume ratio and a lot of surface

defects. However, the longer decay time components observed in Ag-catalyzed GaP nanostructures with lifetimes of several tens to several hundreds nanoseconds are attributed to radiative recombination introduced by Ag.

Hence, the novel Ag-catalyzed GaP nanowires exhibited extraordinarily different PL and time-resolved characteristics, which can be probably attributed to: (1) a modified crystal lattice in which the impurity Ag is an intrinsic component to substitute the host Ga atom, i.e. a new type of (AgGa)P crystal was catalyzed by Ag. The two peaks and lifetimes of t1/t2 belong to its ZB and WZ structure, respectively; (2) Incorporation of either Ag^{+} or Ag^{0} in the oxide layer formed on the nanowire surface after exposure to atmosphere, which could cause additional energy levels in the band gap of the surface oxide, the intense PL emissions in the blue range of the spectrum and the long lifetimes are due to the radiative recombination of free carriers located at these surface states.

6.4 Conclusions

In this chapter, we realized controllable sub-10 nm diameter III-V nanowire heterostructures on Si substrate, by a variety of catalysts. Based on the analysis of the crystal structures at the base of the GaP nanowire and the Au catalyst tip, we concluded that, in the sub-10 nm diameter range, the initial catalyst contains Si, the growth direction of the initial ZB phase depends on the ledge-flow mechanism, and the WZ formation is favored by a high Ga supersaturation. The combination of small radius and high supersaturation leads to formation of the relatively large nucleus with A-B-C stacking of the ZB phase. The GaP NW branches grew heteroepitaxially on the Si with a fixed direction, i.e. in a controllable way. Optical characterization suggests that the sub-10 nm GaP nanowires grown epitaxially on Si substrates may be applicable to photoelectronic integrated devices. Especially, non-gold catalysts were successfully introduced into the growth of small III-V nanostructures. Al catalyst resulted in $Al_xGa_{1-x}P$ nanocrystal growth on both Si substrate and Si nanowire, optical characterization confirmed its bandgap enlargement and nonradiative recombination process of free carriers. For the first time, Ag-catalyzed GaP nanowires were grown on Si substrate. The influence of Ag on the GaP nanowire was studied. It was related with intense PL emissions in the blue range of the spectrum and long lifetimes due to the radiative recombination of free carriers. The method presented here can potentially be extended to other functionalized III-V materials integrated on Si nanostructures, and may play an important role in photoelectronic device design and the corresponding fabrication.

Summary

As the last part of the thesis, it is time to sum up the results and illustrate the connections between the chapters. Most of the content in this thesis is related to the study of template-assisted growth of semiconductor materials as indicated by the title "Epitaxial Semiconductor Nanostructure growth with Templates". The initial motivation and interesting aspects of this research area are stated as a general introduction in Chapter 1. The experimental results start with integration of ordered 1-D porous templates (AAO) with Si substrates in Chapter 2. Issues on AAO-assisted 1-D semiconductor nanowire & nanotube growth are presented successively in Chapter 3 and Chapter 4. In order to study size effects on nanowire growth, both bio-template and surface-template are developed in Chapter 5 and Chapter 6, the first is focused on Si nanowires while the other is on III-V. The thesis emphasized growth issues, such as growth mechanism and nucleation behavior, and controllable homo- and hetero-epitaxy of semiconductor nanowires on Si platforms. Chapter 2-5 mainly dealt with group Ⅳ materials while Chapter 6 described III-V materials.

As a multifunctional porous template, the synthesis of ultrathin AAO membranes directly and indirectly combined with Si substrates was studied in Chapter 2. Ordered AAO templates with pore diameters of 40 nm and 20 nm, and interpore distances of 100 nm and 65 nm, respectively, were produced. Specifically for AAO directly grown on Si substrate, the growth mechanism with upward bending of the barrier layer and the effect of subsequent HF-treatment was studied. The drawbacks of this approach, widening of the pores and anodizing the surface of Si, stimulated the development of a polymer-assisted method to bond a free-standing AAO membrane onto the Si substrate. This technique was also successfully extended to the metal-assisted chemical etching of large-scale Si nanowires arrays, and the influence of oxidant concentration and metal morphology on the etching mechanism was studied as well.

Integration of semiconductor nanowires on the Si platform is one of the essential issues for device applications. Therefore, control of the growth direction, positioning, diameter, and catalytic material of semiconductor nanowire arrays were studied in the following chapters. AAO thin film has the potential to be integrated with Si substrates, thus, in chapter 3 it was used for the growth direction control of epitaxial Si and Ge nanowires. The understanding of the VLS growth mechanism was extended to silicon isotopic (^{28}Si, ^{29}Si, and ^{30}Si) nanowire epitaxy in free space. The growth was influenced by the Au surface diffusion which was initiated by the high-temperature growth. By applying AAO as a growth template, Au-catalyzed Si nanowire nucleation and growth inside of AAO pores was extended down to the 40 nm diameter range, and the growth directions were found to be independent of the pore size of AAO. Furthermore, with a better understanding of the diffusion of the gaseous precursor within AAO, a transition metal such as cobalt was used as catalyst to fabricate polycrystalline Si, covering the inner surfaces of AAO pores by small amount of the metal cobalt. It was possible to fabricate polycrystalline Si nanotubes, which were connected at one end to a silicide crystal. The growth length, outer

diameter, and wall thickness of these Si nanotubes were well-controlled by a highly ordered AAO template and a UHV-CVD process. With Au electroless plating in AAO directly anodized on Si(100) substrate, controllable Si nanowire homoepitaxy was realized with the growth forced along the Si[100] direction vertical to the substrate. The growth of axial Si-Ge nanowires using VLS growth of freestanding nanowires resulted usually in Si-SiGe nanowires with compositionally graded interfaces. A new approach combining VLS and VSS growth inside a AAO template allowed to grow an epitaxial Ge on Si nanowire with a compositionally sharp interface.

Although Si[100] nanowires were grown before epitaxially on Si(100) substrate with the use of electroless Au plating and AAO templates, however, non-gold catalysts, smaller diameters, large-area ordering and a narrow size distribution were still challenges. In chapter 4, a new method was presented. Highly-ordered AAO thin films were used as both porous pattered mold and growth template. This improved the controllable growth of ordered epitaxial semiconductor nanowire arrays. This bottom-imprint (BI) approach has several advantages compared with direct AAO synthesis on Si substrates, such as well-arranged ordering, adjustable diameter of nanowires as small as 20 nm with a narrow size distribution, and low-temperature growth without an annealing. Most importantly, it was successfully extended to the growth of Al-catalyzed Si nanowires in the low-temperature vapor-solid-solid (VSS) growth mode. A I-V measurement showed that the Al catalyst introduced a highly *p*-type doping into the Si nanowire, with diode behavior on a *n*-doped Si substrate. Using this technique, the metal catalyst can be simply changed and optimized for different nanodevice applications. As an example to show the versatility of the BI method, vertically-aligned indium phosphide (InP) nanowire arrays were grown heteroepitaxially on Si(100) substrate by BI, a semiconductor which has potential applications in photoelectric devices.

The related physical properties would dramatically change with further shrinkage of nanowire diameters into the quantum-effect region, such as bandgap and optical behavior. Previous chapters focused on the controllable growth of semiconductor nanostructures using AAO as template. However, such techniques did not yield semiconductor nanowires with sub-10 nm diameters, the regime that is required for future post-CMOS technology. Since the self-ordered AAO has a minimum pore size around 20 nm, even further shrinkage of pore diameter could be done by a complicated and costly atomic layer deposition (ALD) method. More conveniently, the diameters can be scaled down if smaller catalytic seeds are used with confined positions. Therefore, in the last two chapters, we studied the size effects on both sub-10 nm diameter Si and GaP nanowire epitaxy, and provided crystallographic interpretations for different nucleation behaviors on Si substrates. Both bio-templating with apo-ferritin and surface-templating with *in situ* molecular beam epitaxy (MBE) methods were investigated for scaling down the catalysts. With both approaches, semiconductor nanowire arrays with sub-10 nm diameter could be produced, with a small size distribution. Au-encapsulated apo-ferritin has the advantage of being highly accurate as template and available in large amounts, although the immobilization of the proteins onto the Si surface limited their ability of catalyzing epitaxial nanowire growth. In order to achieve a high-density of sub-10 nm diameter nanowires grown epitaxially on Si with a uniform size, a reconstructed silicon surface was used as template for the nucleation of metal nanocluster arrays.

Such an *in situ* hot-surface metal deposition avoids further annealing before nanowire growth, and the direct deposition of catalytic seeds onto both the reconstructed Si(111) and Si(110) wafers allowed epitaxial growth of nanowires. On both Si(111) and Si(110), the epitaxial growth direction of Si nanowires was strongly affected by the orientation of the substrate for the sub-10 nm diameter nanowires. The [112] growth direction was dominant on Si(111), whereas most of the Si nanowires grew vertically in the [110] direction on Si(110). In the case of Si[112] nanowire epitaxy, VLS growth through a ledge-flow mechanism was proposed. The height of the observed step was three Si(111) planes. For the first time, Au-catalyzed Si nanowire homoepitaxy was extended down to a minimum diameter of 2.8 nm experimentally. Comparing Si[112] and [110] small diameter nanowires, it was assumed that different nucleation behaviors are important. [112] nanowires seem to grow by nucleation at the three-phase boundary with nucleus propagation along the Si(111) planes, while [110] wires nucleate at the perpendicular Si($1\bar{1}1$) planes across the whole solid-liquid interface.

In the last chapter, GaP nanowire heteroepitaxy with sub-10 nm diameter on Si was studied. It provided diverse morphologies, such as a high-density of perpendicular nanowires grown on Si substrate and branched nanowire heteroepitaxy, expanding the range of possible devices. A ZB phase was formed at the initial growth stage of GaP nanowires. Later, with the Ga supersaturation increasing, a phase transition from ZB to WZ was observed. Furthermore, a nonequilibrium multilayer ledge-flow mechanism was developed to explain the tilted growth directions of the ZB phase. Optical characterization revealed that a band-to-band recombination occurred with an energy similar to the indirect bandgap energy of bulk GaP with a short lifetime around 100 ps. Furthermore, non-gold catalysts were successfully introduced into the III-V nanostructure growth. Al catalysts resulted in $Al_xGa_{1-x}P$ nanocrystal growth on both Si substrate and Si nanowire, optical characterization confirmed its bandgap enlargement and a dominant nonradiative recombination process caused by the increased number of structural defects. For the first time, Ag-catalyzed GaP nanowires were grown epitaxially on Si substrate. Intense PL emissions in the blue range of the spectrum and long lifetimes were caused by the incorporation of Ag into the GaP growth. It opens up a promising synthesis step towards functionalized III-V compounds engineering. More characterizations are required to be done to understand the role of the new catalyst and the size reduction onto the optical and electrical properties of GaP nanowires.

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Appendix

Appendix for page 59:

The current I through an ideal diode is an exponential function of the applied voltage u:

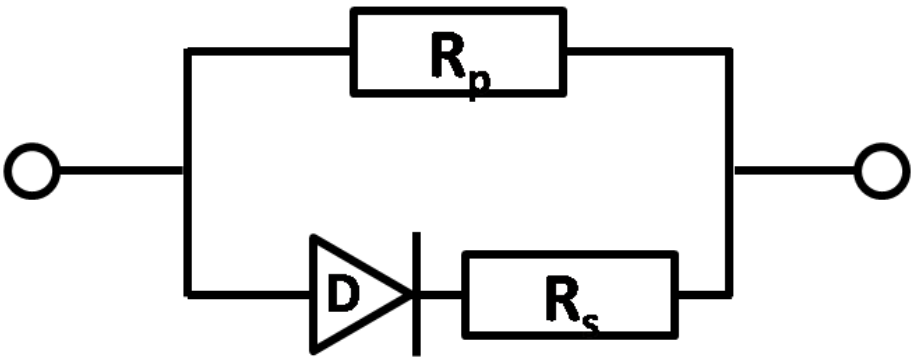
$$I = I_0 [\exp(e\,u/kT) - 1]$$

In this function, e is elementary charge, k is Boltzmann factor, T is temperature. A real diode has some contribution to the charge transport process by recombination. This is expressed by introducing the ideality factor n:

$$I = I_0 [\exp(eu/nkT) - 1]$$

The nanowire diode D (Figure 4.9 right side) showed a slower increase of current for voltage above 0.5 V. This is attributed to a series resistance R_s. The reverse current can be described roughly by a parallel resistance R_p, as shown in the schema.

The I-V curve of the Au-catalyzed nanowire showed a strong non-linear behavior. It cannot be fitted with this simple model.



	Au_7Ga_2	Au_2Ga	AuGa	$AuGa_2$
Sys.	**Hexagonal**	**Orthorhombic**	**Orthorhombic**	**Cubic**
a;b;c (Å)	**7.724;7.724;8.751**	**18.02;3.199;6.999**	**6.266;3.421;6.399**	**6.075**
3.4 (Å)	**3.53;3.53;3.34 {111;121;200}**	**3.50;3.44;3.26;3.20 {002;102;202;501}**	**3.20;3.42 {002;010}**	**3.51 {111}**
2.2 (Å)	**2.16;2.19;2.20;2.23 {301;004;203;300}**	**2.15;2.17;2.19;2.20;2.25;2.26; 2.26;2.28;2.28 {801;303;610;312;800;203; 511;212;602;}**	**2.13;2.17;2.19;2.24; {003;211;112;202}**	**2.15 {220}**
90 (°)	**{200}-{004} 90**	**{002}-{800} 90**	**{010}-{202};{003} 90**	**{111}-{220} 90**
Dir.	**[010]**	**[010]**	**[10-1];[100]**	**[11-2]**

Table A.1: Comparison of lattice parameters for different Au-Ga phases with the measured values (in bold) of the sample. For the two measured planes, considering the limited resolution, all the real planes within the $\pm 5\%$ errors of the measured values are listed respectively. All the possible combinations of the two planes possessing the observed $90°$ in between were listed below the thick line. The calculated viewing directions are listed in the last line.

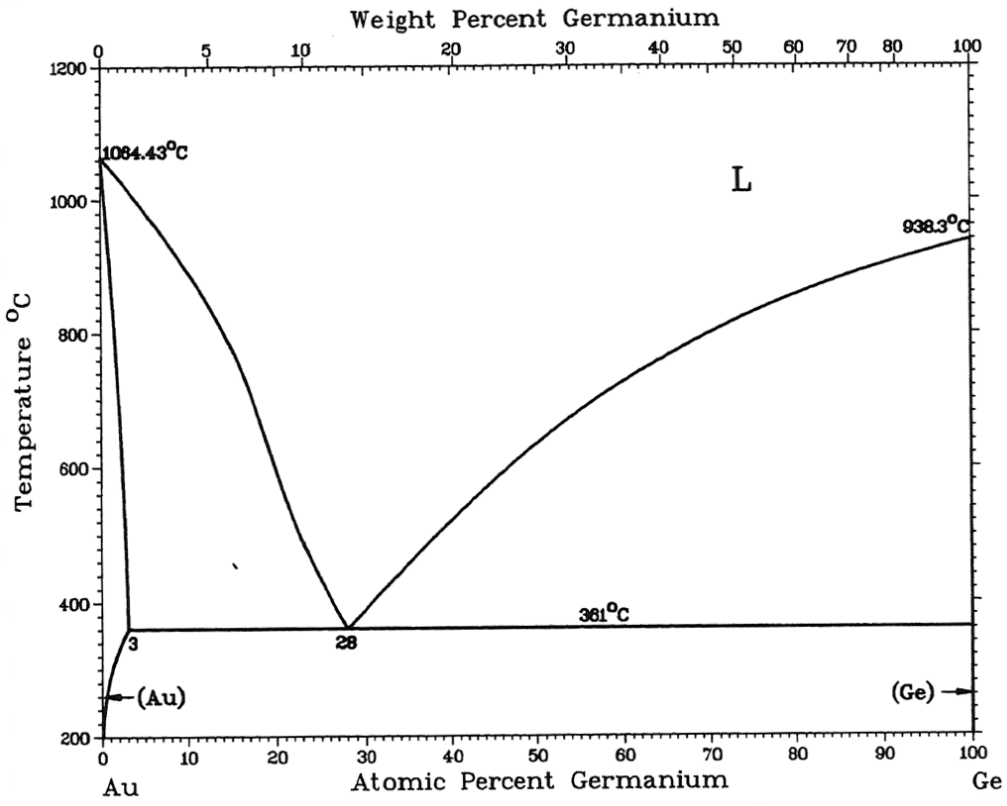


Figure A.1: The binary phase digram of Ge-Au [Mas98], the solid-solution pocket is on the very left side, the eutectic temperature is 361 °C, Figure 3.13a magnified.

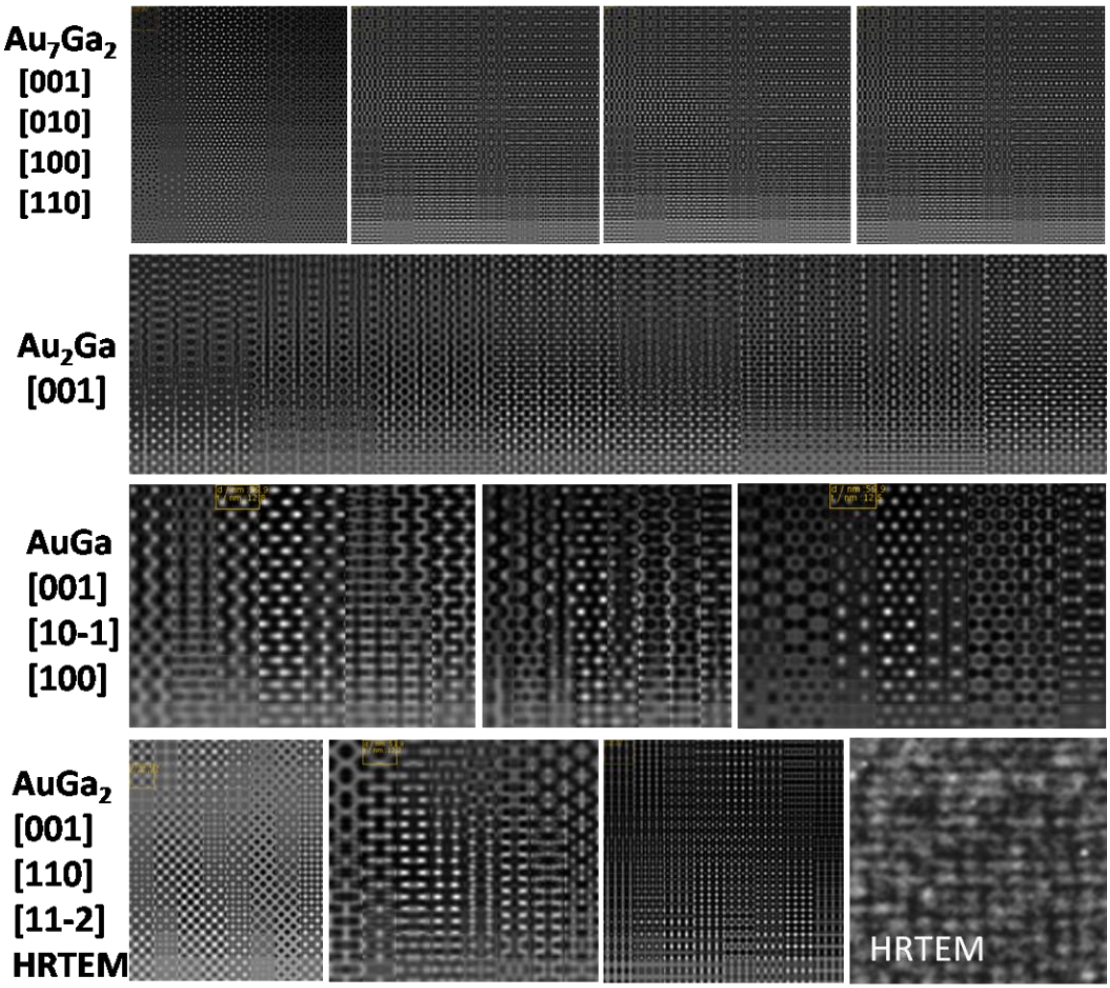


Figure A.2: The calculated images of different Au-Ga phases to compare with the real HRTEM image, the view directions are listed under the possible phase in accord with the images sequentially from left to right side.

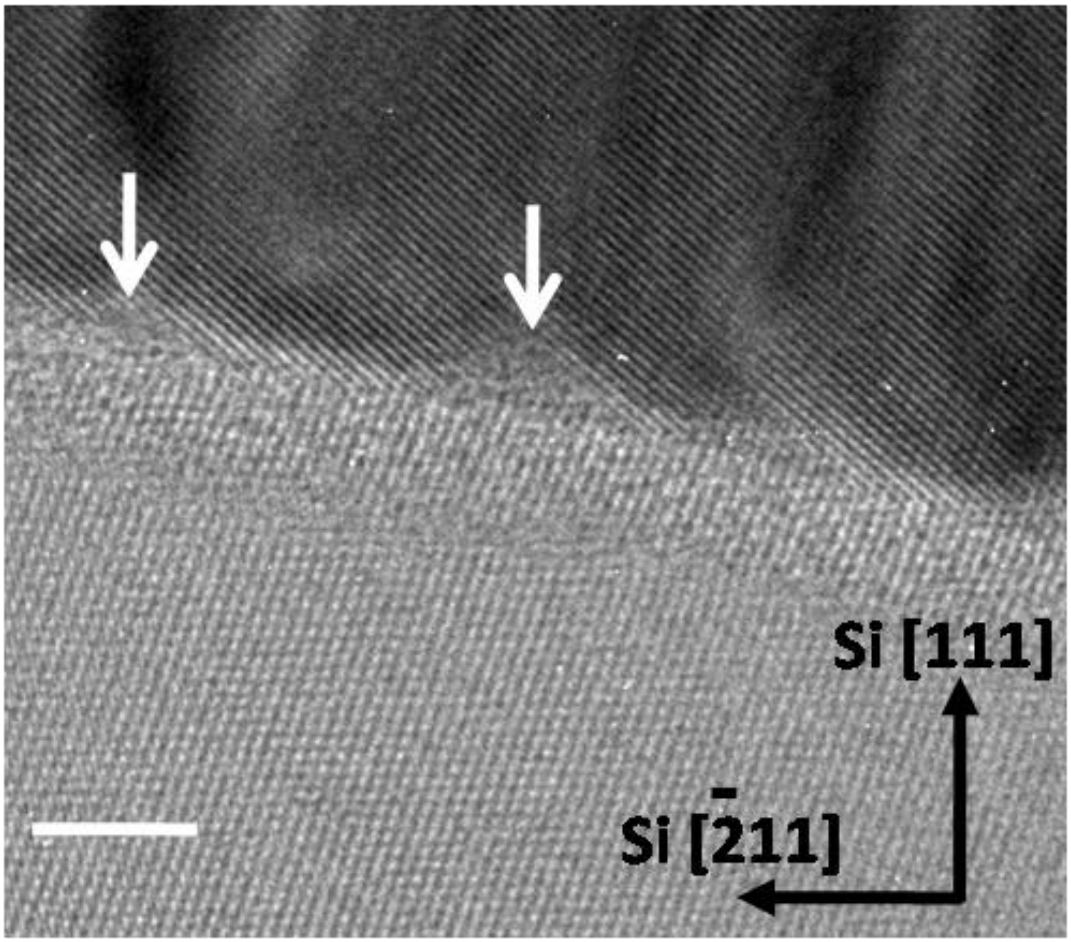


Figure A.3: HRTEM image of the Ag particle etching front on Si(111) substrate, with defect positions indicated by arrows, Figure 2.9b magnified.

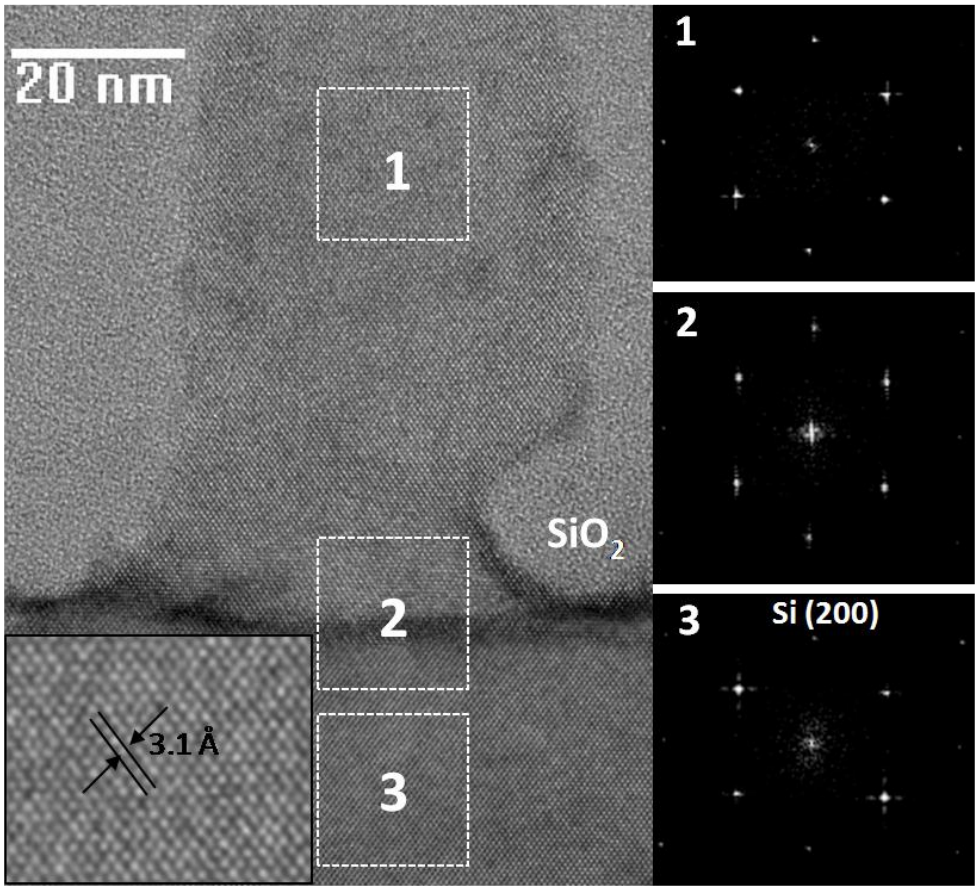


Figure A.4: Cross-sectional HRTEM image and FFTs of the Si nanowire epitaxy on Si(100) using BI method, Figure 4.4b magnified.

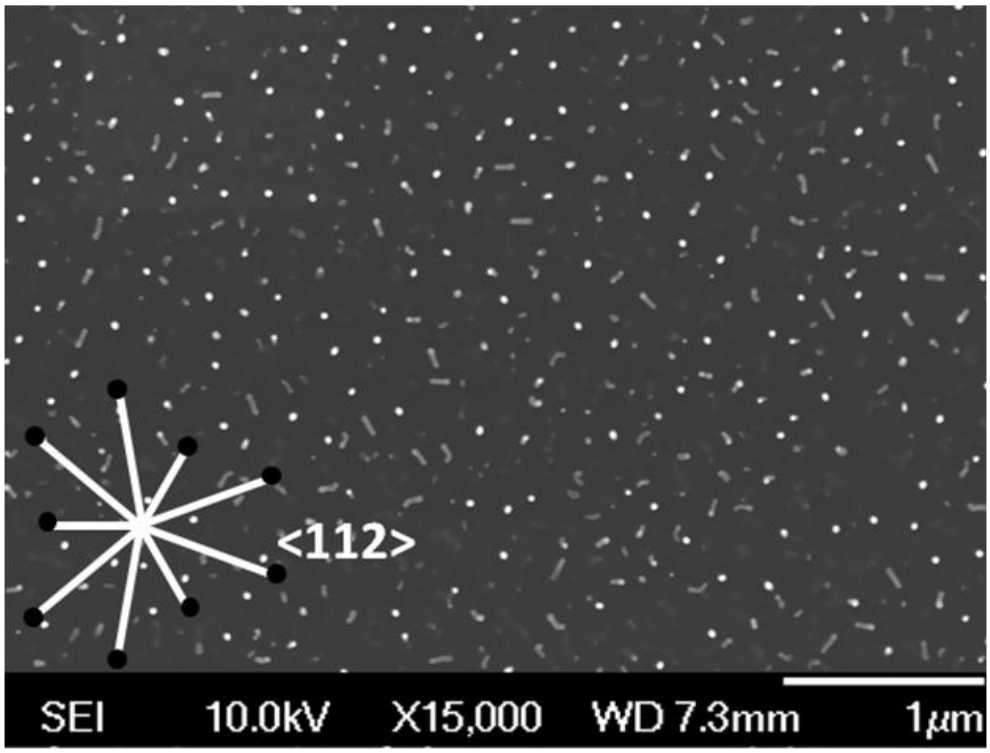


Figure A.5: Top-view SEM image of Al-catalyzed Si nanowires and schematic <112> orientations on Si(111) substrate, Figure 4.7a magnified.

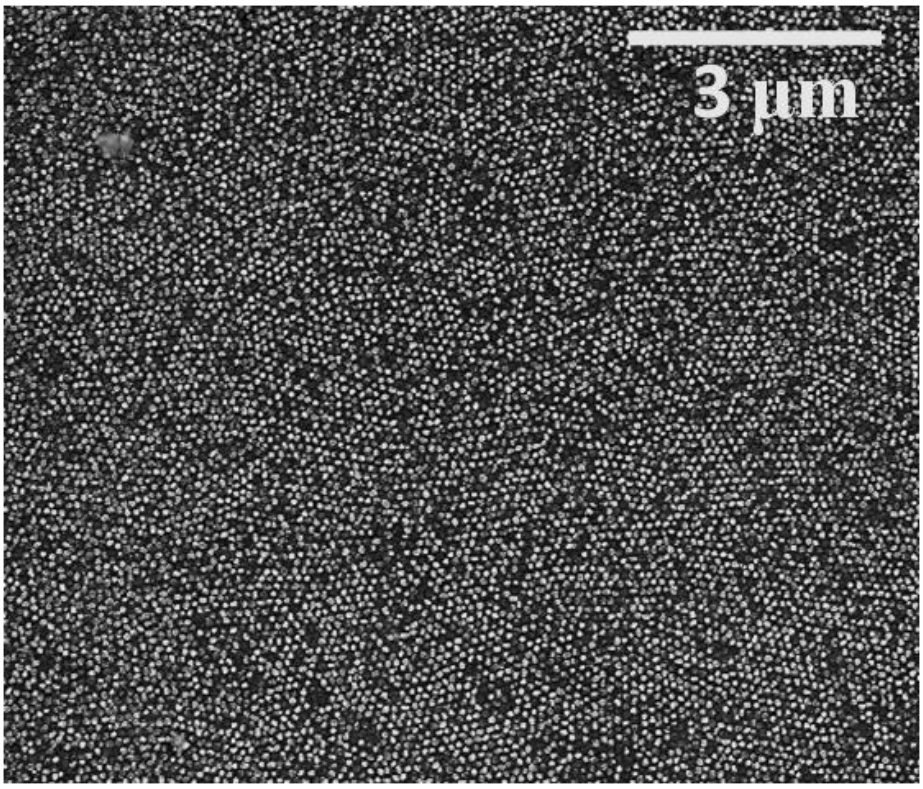


Figure A.6: Low-magnification SEM top-view of Al nanoparticle array imprinted by 45 nm pore diameter AAO with a homogeneous imprint area of 10×10 µm^2, Figure 4.10c magnified.

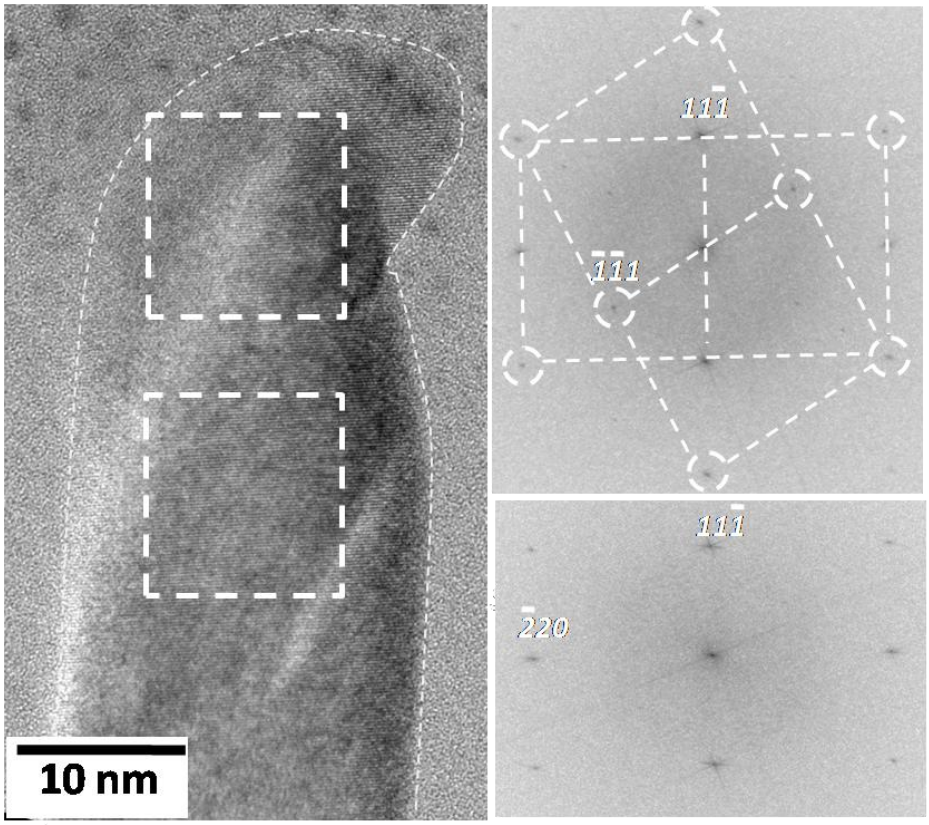


Figure A.7: Cross-sectional HRTEM image and FFTs of top-side of Al-catalyzed Si nanowire taken with the electron beam parallel to the [112] direction of the Si(111) substrate, Figure 4.12a magnified.

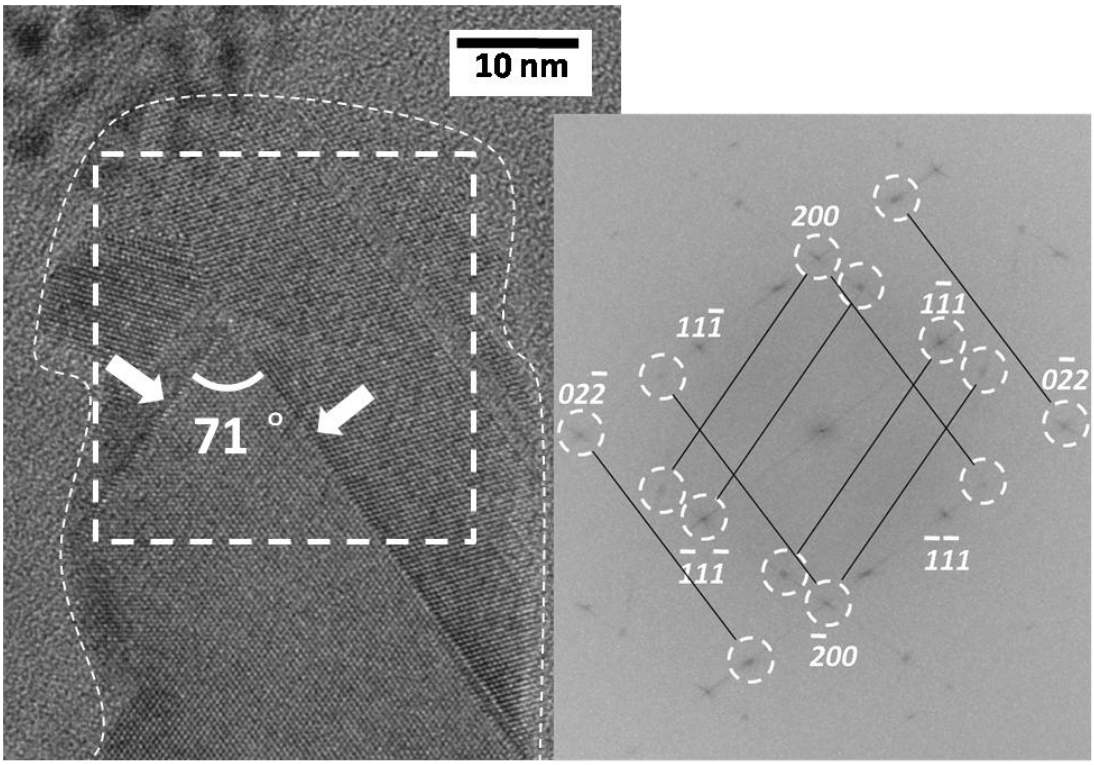


Figure A.8: Cross-sectional HRTEM image and FFT of top-side of Al-catalyzed Si nanowire taken with the electron beam parallel to the [011] direction of the Si(100) substrate, Figure 4.12c magnified.

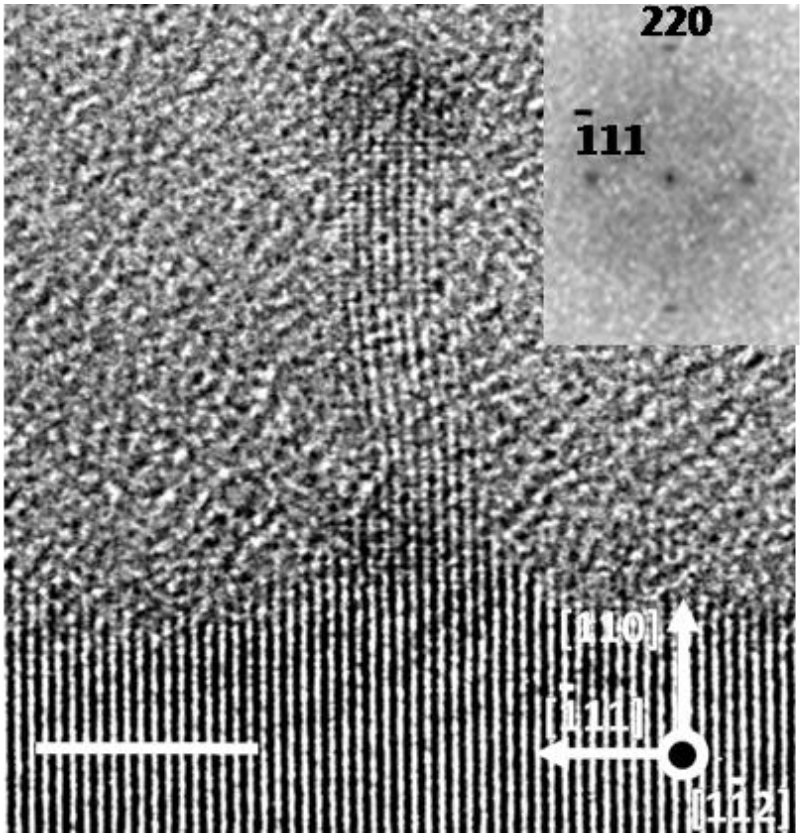


Figure A.9: Cross-sectional HRTEM image and FFT of Au-catalyzed Si nanowire grown epitaxially on Si(110) substrate with a 2.8 nm diameter, Figure 5.11c magnified.

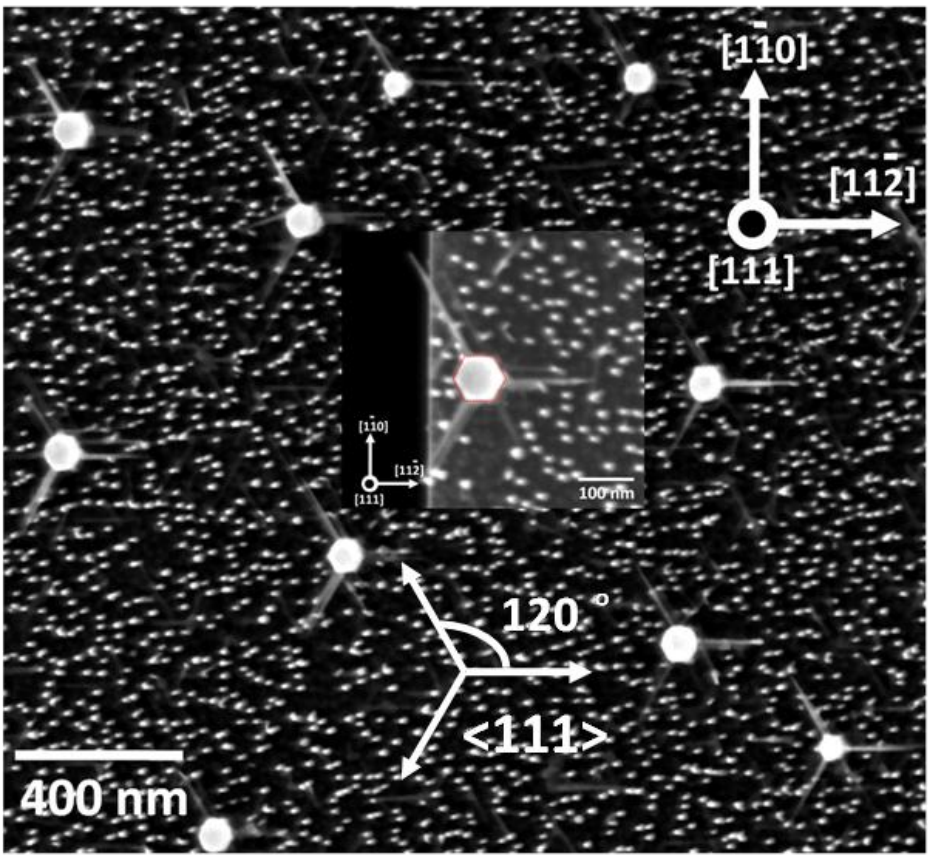


Figure A.10: Top-view SEM image of GaP nanowires heterostructures on Si(111) and Si[111] nanowires, Figure 6.1a magnified.

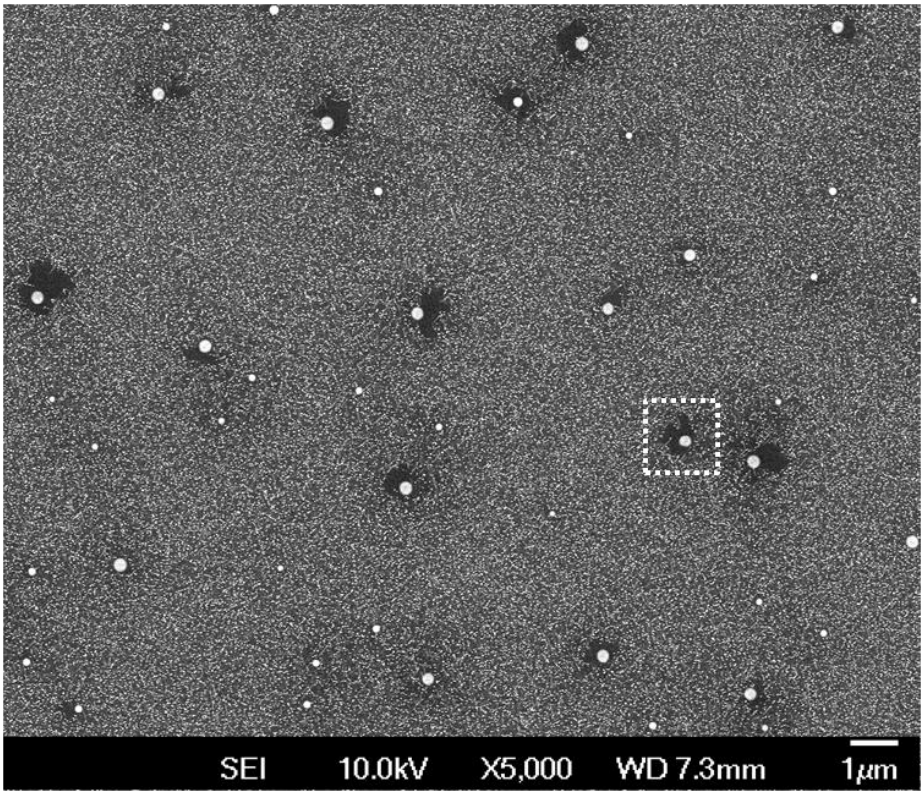


Figure A.11: Top-view SEM image of the GaP heteroepitaxial growth on the Si(111), a 60 min annealing at 500 ℃ for Au droplet formation, and a post-anneal at 600 ℃, Figure 6.3a magnified.

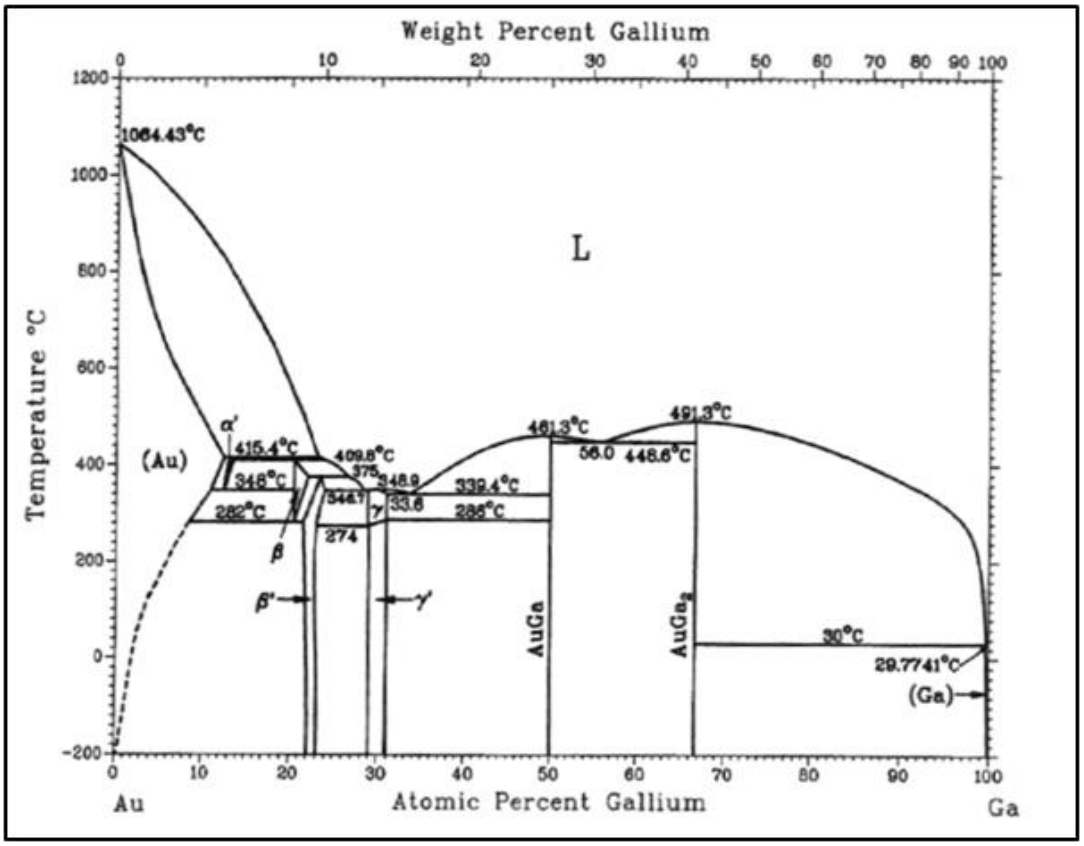


Figure A.12: Binary phase diagram of Au-Ga [Mas98], Figure 6.7a magnified.

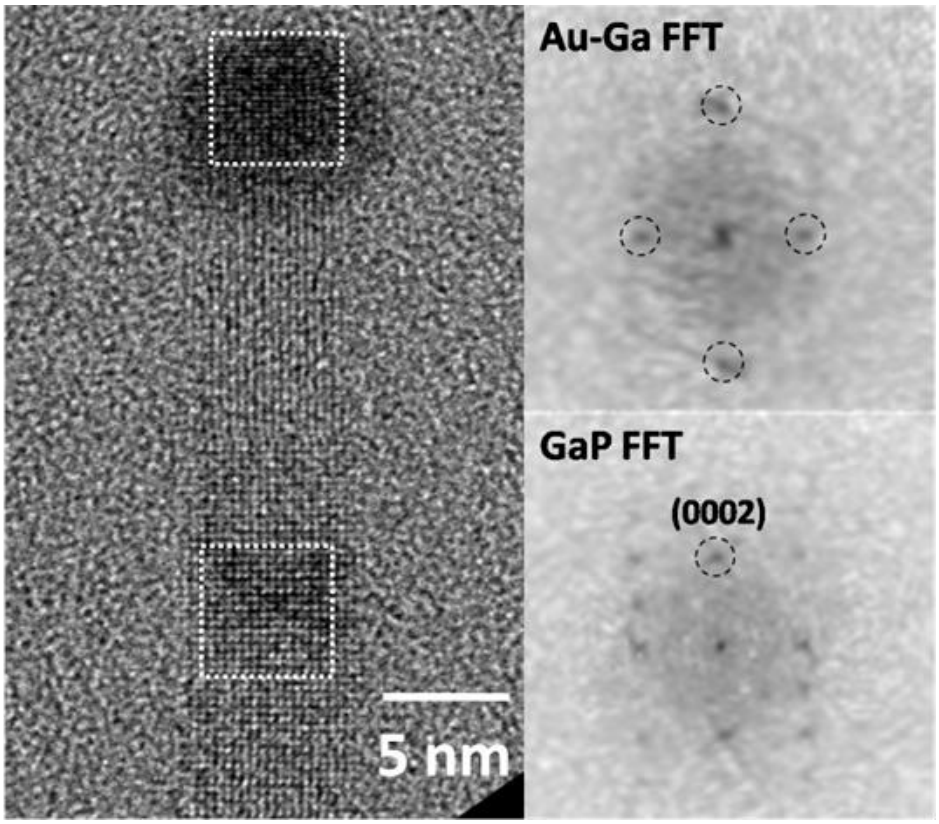


Figure A.13: HRTEM image and FFTs of a GaP nanowire with catalyst tip, Figure 6.7b magnified.

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Publikationsliste

1. Vertical Epitaxial Wire-on-Wire Growth of Ge/Si on Si(100) Substrate
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Tabellarischer Lebenslauf

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Halle (Saale), Jun 23, 2010

Erklärung

Ich versichere hiermit, die vorliegende Dissertation

Epitaxial Semiconductor Nanostructure Growth with Templates

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Erklärung

Ich versichere hiermit, dass ich mich an keiner wissenschaftlichen Hochschule im Geltungsbereich des deutschen Grundgesetzes bereits früher um den Doktorgrad beworben habe.

Halle (Saale), Jun 23, 2010 (Zhang Zhang)