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Common-Mode Current Reduction Technologies in Four-Wire Inverter-Fed Motors

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Zusammenfassung

Elektrische Antriebssysteme mit immer besserer Antriebsleistung und niedrigeren Kosten sind eine Notwendigkeit, um die Elektrifizierung des Verkehrs voranzutreiben, was derzeit als der bedeutendste Trend in Forschung und Entwicklung angesehen werden kann. Da die höhere Antriebsleistung jedoch auf den immer schnelleren Schaltvorgängen der getakteten Umrichter beruht, die zu elektromagnetischen Störungen (EMI) des Elektromotors und der umliegenden Geräte führt, wird auch die elektromagnetische Verträglichkeit (EMV) des Antriebes betroffen sein. Unter allen Arten von EMV-Problemen ist der Gleichtaktstrom die bedeutendste EMI des Antriebssystems.

Das Hauptaugenmerk dieser Dissertation liegt auf der Einführung zweier Technologien zur Gleichtaktstromunterdrückung für einen neuartigen Antriebssystem-Typ, dreiphasiger Vierleiter-Antriebssysteme, welche die Anwendung einer sensorlosen Steuerung und eines fehlertoleranten Betriebs ermöglichen. Anstatt empirische Formeln für die Analyse des durch den Motor fließenden Gleichtaktstrom zu verwenden, wurde eine theoretische Analysemethode vorgeschlagen, die auf der Übertragungsfunktion zwischen der Kabeleingangs- oder Neutralleiterspannung und der ursprünglichen Phasenspannung basiert. Darauf aufbauend werden die Optimierung des Pulsweitenmodulation-Algorithmus (PWM) sowie der Entwurf von Filtertopologien als die beiden wichtigsten Technologien zur Gleichtaktunterdrückung vorgeschlagen.

Für die PWM-Optimierung wird eine hybride Phasenverschiebungs-PWM vorgeschlagen, um den Gleichtaktstrom durch Entfernen der Nullsequenz in den Schaltzyklen zu reduzieren. Anders als herkömmliche Ansätze, werden damit die transienten bei den Sektorübergänge vermieden, und somit ein sanfter verlauf erreicht. Außerdem ist die variable Schaltfrequenz-PWM die zusätzlich zur hybriden Phasenschieber-PWM angewendet wird, um die Spitzen des Gleichtaktstromes bei ganzzahligen Vielfachen der Schaltfrequenz zu benachbarten Frequenzen weitgehend abzuschwächen. Zusammenfassend lässt sich sagen, dass die Verwendung dieser beiden PWM-Techniken zu einem neuartigen PWM-Algorithmus führt, der viel weniger Rechenaufwand erfordert, den Gleichtaktstrom stärker unterdrückt und somit besser die Standard-EMV-Prüfungen zu bestehen ermöglicht.

Für den Filterentwurf von Vierleiter-Antriebssysteme führt die Analyse der Übertragungsfunktion zu dem Ergebnis, dass ungefilterte Vierleiter-Topologie bereits ein Filternetzwerk bildet, das den Gleichtaktstrom reduzieren kann. Die Filterwirkung dieses Netzwerks wird auch durch die Impedanz des Motors beeinflusst. Darauf aufbauend wird ein neuartiges Auslegungeverfahren für Vierleiter-Antriebssysteme vorgeschlagen, bei dem nicht nur die Entwurfparameter wie Verlustleistung, Filtereffizienz, und Resonanz, sondern auch die Impedanz von Elektromotoren berücksichtigt werden. Die vorgeschlagene Filtertopologie hat bessere Filtereffekte, weniger Leistungsverluste sowie eine geringere Größe und geringeres Gewicht als die konventionelle Dreileiter-Topologie zur Folge.

Die Auswirkungen der Reduzierung des Gleichtaktstromes durch beide Technologien zur Gleichtaktunterdrückung wurden experimentell in einem praktischen Antriebssystem validiert. Darüber hinaus werden diese beiden Ansätze auch gemeinsam in einem Antrieb eingesetzt, das für die Traktion von Elektrofahrzeugen ausgelegt ist. Die Ergebnisse zeigten, dass eine einfache Kombination der beiden Ansätze nicht zu einem zusätzlichen Effekt der Gleichtaktstromunterdrückung führt, und weitere Forschungsarbeit notwendig ist, um eine Strategie zu entwickeln, welche die positiven Effekte bei einer kombinierten Anwendung optimal ausnutzt.

Abstract

Electric drive systems (EDS) with increasingly better drive performance and lower cost have been a necessity of boosting the transportation electrification, which currently has been regarded as the most significant trend of research and development. However, as the better drive performance always relies on the increasingly faster transition of the switch-mode inverters, which leads to a serie of electromagnetic interference (EMI) to the electrical motor and the surrounding equipments, the electromagnetic compatibility (EMC) of the EDSs must also be concerned. Among all types of EMC problems, the common-mode (CM) current is the most significant EMI to EDSs.

The primary focus of this dissertation is to introduce two kinds of CM current reduction technologies (CMCRTs) for a novel type of EDS, three-phase four-wire drive systems, which enables the application of sensorless control and fault-tolerant operation. Instead of using empirical formulas for the analysis of CM current flowing across the EDS, a theoretical analysis method has been proposed based on the transfer function between the cable input or neutral voltage and the original phase voltage. Based on this, optimization of pulse-width modulation (PWM) algorithm, as well as the design of filter topologies, are proposed as the two main CMCRTs.

For the PWM optimization, hybrid phase-shift PWM, which can implement the phase-shift more smoothly than conventional phase-shift approaches, is proposed to reduce the CM current through removing the zero sequence in switching cycles. Besides, variable switching frequency PWM is applied in addition to the hybrid phase-shift PWM to largely attenuate the peaks of CM current at integral multiples of the switching frequency to adjacent frequencies. In summary, utilizing these two PWM techniques results in a novel PWM algorithm requiring much less computational efforts, EDS with much less CM current and higher possibility of passing the standard EMC tests.

For the filter design of four-wire EDSs, the analysis of transfer function leads to a finding that unfiltered four-wire EDSs already consists of a filter network that can reduce the flowing CM current. The filtering effect of filter network is also influenced by the impedance of the motor. Based on this, a novel design procedure is proposed for four-wire EDSs with consideration of not only the design parameters like power loss, filtering efficiency, resonance, but also the impedance of electrical motors. Finally, the proposed filter topology results in better filtering effects, less power losses, as well as smaller size and weight than the conventional three-wire filter topology.

The effects of reducing CM current by both CMCRTs have been validated experimentally in practical EDSs. In addition, these two CMCRTs are also applied together in a EDS designed for the traction of electric vehicles. It is concluded that simply combining effective CMCRTs will not result in an added effect of CM current reduction, which provides hints of an more appropriate application strategy for the combined utilization of CMCRTs.

Contents

Nomenclature

α	overshoot of the resonance of transfer function
β	maximal percentage of the remaining CM current in the high-frequency range
ω	angular frequency
C	capacitance
d	duty cycle
f	frequency
i, I	instantaneous current
K	transfer function
k	ripple current slope
L	inductance
n	rotation speed
P	active power
R	resistance
T	torque
t	time
T_s	switching period
u, U	instantaneous voltage
Z	impedance

Subscripts

$1DC, 2DC$	variables of cable and motor impedance of 4wDC
$1EL, 2EL$	variables of cable and motor impedance of 4wEL

$3w$	three-phase three-wire drive topology
$3wF$	CMMF filtered three-wire drive topology
$4wDC\_F$	CMMF filtered 4wDC
$4wDC\_FCC$	choke filtered 4wDC
$4wEL\_F$	CMMF filtered 4wEL
$4wEL\_FCC$	choke filtered 4wEL
α, β	α-axis and β-axis variables under stationary reference frame
cm	variable of common-mode components
dm	variable of differential-mode components
L	parasitic components between power cable and ground
M	parasitic components between motor and ground
N	variables of neutral point of motor
n	variables of neutral phase of motor
U, V, W	variables of phase U, V and W

List of Acronyms

ACC Active Common-Noise Canceler

AZS-PWM Active Zero-state PWM

CM Common-Mode

CMCRT Common-Mode Current Reduction Technology

CMMF Common-mode Filter for Three-wire Electric Drive System

DM Differential-Mode

D-PWM Discontinuous PWM

EDS Electric Drive Systems

EMC Electromagnetic Compatibility

EMI Electromagnetic Interference

EMF Electromotive Force

FE Finite Element

FOC Field-Oriented Control

HPS-PWM Hybrid Phase-Shift PWM

NS-PWM Near-State PWM

PWM Pulse Width Modulation

PS-PWM Phase-Shift PWM

PMSM Permanent Magnetic Synchronous Machine

R-PWM Random PWM

SV-PWM Space-Vector PWM

S-PWM Sine-Triangle PWM

SCR Silicon Controlled Rectifier

TRIAC Triode for Alternating Current

VSF-PWM Variable Switching Frequency PWM

VSI Voltage Source Inverter

List of Figures

List of Tables

1 Introduction

1.1 Background and Motivation

Three-phase electric drive systems (EDS), consisting of inverter and motor, have been widely used in the field of electrified transportation among others. The operation of these drive systems relies on the proper design of pulse width modulation (PWM) algorithm and related switch-mode inverters. However, there always exists negative influences of PWM switch-mode inverters on electrical motors and surrounding equipments [1] [2].

Recently, highly integrated electronic systems of multifunctional electronic products can be quite sensitive to external electromagnetic fields, resulting in a number of problems like inaccurate action, malfunction or even damage to individual components or the whole system. To ensure their reliability, various test standards were established for a comprehensive inspection of thier Electromagnetic Compatibility (EMC) [3]. According to the methods of coupling electromagnetic energy from a source to a receptor, Electromagnetic Interference (EMI) can be classified as radiated and conducted interference [4]. Common-mode (CM) current, resulting from fast changing CM voltage, is a kind of conducted interference. As shown in Fig. 1.1, in three-phase EDSs, the high-frequency switching of IGBT results in extremely high voltage rise, which is delivered through power cables. Due to the transmission route of parasitic capacitance between the drive topology and ground, mainly through the cables and the machine, the CM current is then produced and can flow back to the inverter and DC-bus. The CM current is then defined as the sum of the phase currents ($I_{CM} = I_U + I_V + I_W$). This process causes great disturbances to the whole system, leading to the physical damage or unwanted tripping of ground fault relays [5]. This situation becomes even worse by faster switching devices with the use of SiC. In order to eliminate these negative influences, different CM current reduction technology (CMCRT) have been studied.

One widely used solution is building filter topologies. Passive filter, composed of passive components (resistors (R), inductors (L) and capacitors (C)), has been studied extensively and proved to have advantages of low cost and high operational reliability. In the meantime, active filter, a type of analog circuit implementing an electronic filter using active components, can improve performance and predictability of a filter. Besides, an active filter can have complex poles and zeros without using a bulky or expensive inductor.

Another solution is the optimization of PWM algorithm. Phase-Shift PWM (PS-PWM) can reduce the peak of CM voltage through shifting one of the three phase of the EDS.

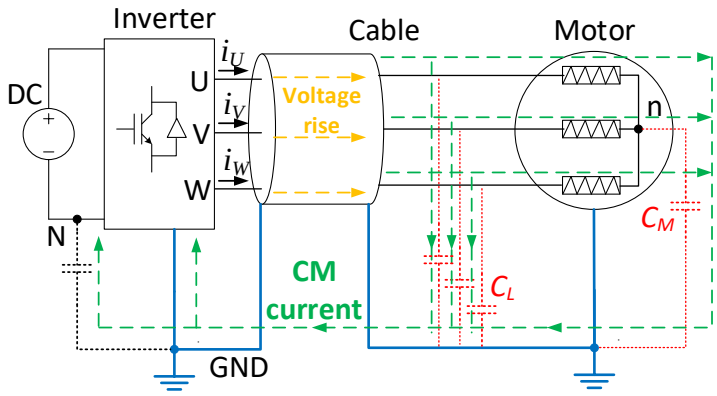


Figure 1.1: The origin of CM current.

Variable Switching Frequency PWM (VSF-PWM) can lower the the peak of CM current and reallocate them to adjacent frequencies.

EDS with four-wire inverter-fed topologies are an extension from traditional three-wire EDS and implemented through connecting the neutral of the motor to the mid of DC-link (4wDC), or to the fourth leg of the inverter (4wEL). Four-wire EDSs are favourably for position sensorless control [6], as well as for fault-tolerance operation [7] [8]. These features can contribute to higher reliability and lower-cost manufacture proposed to applications like electric vehicles, wind generators, etc.

However, the situation of CM current in the four-wire EDS has not been analyzed seriously. Thus, in view of increasingly more studies of the Four-wire EDS, a general evaluation of the flowing CM current in this kind of EDS is required. Besides, the traditional ways of reducing CM current in the three-wire EDS also need to be re-analyzed in the Four-wire EDS. Modifications and optimizations of the traditional CMCRT when applied in the Four-wire EDS are also expected to maintain or further enhance its effects of CM reduction.

1.2 Objectives of the Dissertation

While lots of researchers have kept making great efforts in developing novel CMCRTs, most of them are targeted on conventional three-wire EDSs. Meanwhile, as four-wire EDSs have shown increasingly greater potential in realizing new functions, the necessary CMCRTs for the application of this special topology in the field of electric drive have been seldom studied.

This dissertation aims to explore effective CMCRTs for four-wire EDSs from two aspects: filter design and advanced PWM technique. For the aspect of filter design, a theoretical method based on the analysis of relevant transfer functions is used for the determination of type and corresponding parameters of the filter. Besides, the availability of the PS-PWM and VSF-PWM is validated in the four-wire EDS, and also adjusted for reducing CM

current in a more effective way.

To be mentioned, all the obtained results are validated in two experimental EDSs. Some selected CMCRTs are applied in a practical EDSs used for driving an EV, which paves the path for the application of developed CMCRTs in practical situations.

1.3 Outline of the Dissertation

The dissertation is divided into 7 chapters.

Chapter 1 is the introduction of the research background in the field of CMCRT in EDS, along with the motivation of analyzing, applying and improving the CMCRT in Four-wire EDSs.

Chapter 2 gives an overview and the state of the art of the most significant CMCRT including filter-design and PWM-optimization, along with the representative useful functions that can be realized in Four-wire EDSs. Besides, the high-frequency lumped-parameter model of EDS are introduced specifically.

Chapter 3 introduces the research methodology utilized in this dissertation. Firstly, the theoretical analysis of the Three- and Four-wire EDS is illustrated specifically. Secondly, the simulation approaches used to verify the theoretical analysis are described. Furthermore, two practical EDSs consisting of a permanent magnetic synchronous machine (PMSM) with the power of 2.2 kW and 60 kW, respectively, are introduced and used as the experimental set-up in this dissertation.

Chapter 4 illustrates the effort of optimizing PWM algorithm for CM current reduction. This part also includes both types of four-wire EDS, 4wDC and 4wEL. PS-PWM and VSF-PWM were selected for analysis according to their success in the CM current reduction of Three-wire EDSs. For the application in the four-wire EDS, both advanced PWM technique were analyzed in terms of CM current reduction, switching loss and calculation effort of the micro-controller. Furthermore, the selected advanced PWM technique was optimized due to new features brought by the four-wire EDS. The optimized PWM algorithms was validated experimentally as well.

Chapter 5 investigates the way of reducing CM current through proper design of filter topology. For both types of four-wire EDS, 4wDC and 4wEL, the filter-design procedure was studied and summarized. Firstly, the filtering effect of the traditional CM filter used for three-wire EDSs was analyzed when it is used in the corresponding four-wire EDS with the same parameters. Secondly, new filter topologies were proposed considering the potential benefits brought by the four-wire topology. Lastly, a specific design procedure according to the practical condition was summarized. All theoretical analysis was verified by the proper experimental setup.

In chapter 6, the new CMCRTs proposed for four-wire EDSs in this dissertation were applied together in a prototype EDS designed for driving the electric vehicle. The obtained

CM current reduction were shown, along with the other performance (like the power loss, space required for the filter topology, etc.). These performances were also compared with the situation before applying one or both CMCRTs.

The main findings of this dissertation are concluded in chapter 7, along with the discussion of remaining challenges and potential future work in this field of study.

2 Overview of CMCRT and Four-wire inverter-fed motors

The development of CMCRT is always along with the fast growth of the power electronic technology in the last two decades. As a significant technology for the efficient and stable operation of EDS, CMCRT keeps adjusting and optimizing due to the widely use of new PWM technology, such as new IGBT design, new electric machine design, etc. Many research efforts have been conducted form both industry and academia, which promotes the continuous development of CMCRT. This part gives an overview of the two main CMCRTs, filter design and PWM optimization, along with the state of the art of each technology.

2.1 Design of Filter Topology

2.1.1 Passive Filter

Currently, the most commonly used passive filter is the RLC filter. Conventional output RLC filter is often connected at the inverter output with long leads to the motor, which usually uses a differential mode three-phase inductance. In this case it does not suppress CM. The resistance is only introduced to add some damping and so avoid over-voltages due to resonance. If decoupled inductances are used, it will suppresses mainly DM voltage due to the serial inductance and parallel capacitance. The CM suppression is limited to the action of the series inductance.

Developed from conventional RLC filter that leaves its capacitor neutral point floating, an optimized RLC filter connects its filter star point to the mid of dc-link (Fig. 2.1) and is able to considerably reduce motor terminal overvoltages, leakage current to ground and induced shaft voltage [9]. This filter topology can also be installed within the inverter enclosure and thus can enhance bearing life and improve reliability of drive systems. Here decoupled inductances have to be used to avoid current peaks in the inverter switches.The fundamental current component determines the flux and consequently the size of the inductors.

However, until now, the midpoint of the dc-link capacitors is not accessible in many commercial inverters, and this results in the great obstacle to its commercial application. Thus, another topology is proposed by connecting the filter star point to the dc-link with two diodes. This connection can decrease the motor insulation stress by reducing overvoltages at motor terminal. In general, this output filter topology is very useful and cost effective especially in cases like retrofit installations or when motors without improvement

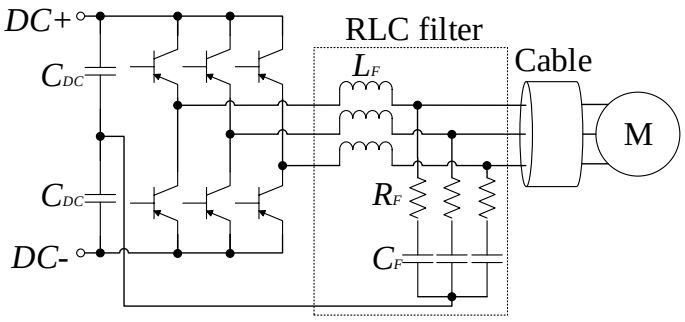


Figure 2.1: An optimized RLC filter

in insulation performance are fed from PWM inverters through long cables [10].

Switching harmonics is also a confronted problem in PWM drive systems. Using RLC filter, the magnitude of the voltage harmonics at any particular frequency depends on the cut-off frequency and amount of damping applied by the resistor. Normally, the filtering effect becomes better when the cut-off frequency reduces and the damping resistor increases, however, this also results in considerable reduction of the system efficiency. Using an LC trap filter cascaded with the RLC network (Fig. 2.2), effective filtering at and above the inverter PWM switching frequency can be obtained without the necessity of a low cut-off frequency and the associated high damping resistor value [11].

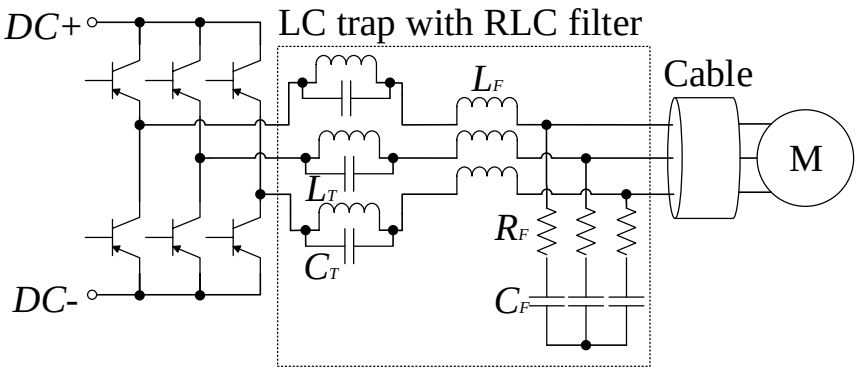


Figure 2.2: RLC filter with LC trap

Compared with RLC filter, LC filter is the most cost-effective type of inverter output filter. Under the condition that switching harmonics does not require to be suppressed, a small LC filter with a resonant frequency above the switching frequency is enough for the application. Due to the fact that the resonance in this type of filter topology cannot be damped with resistors practically, a diode bridge is used in addition to the LC filter (Fig. 2.3) to clamp the resonant voltage [12]. Besides, resistors are also required for dissipating the stored energy in the resonant circuit. Thus it is crucial for this type of LC filter to handle the additional loss through well selection of the inductor, capacitor and resistor values.

Due to the increasingly higher requirement for the safety and reliability of the PWM

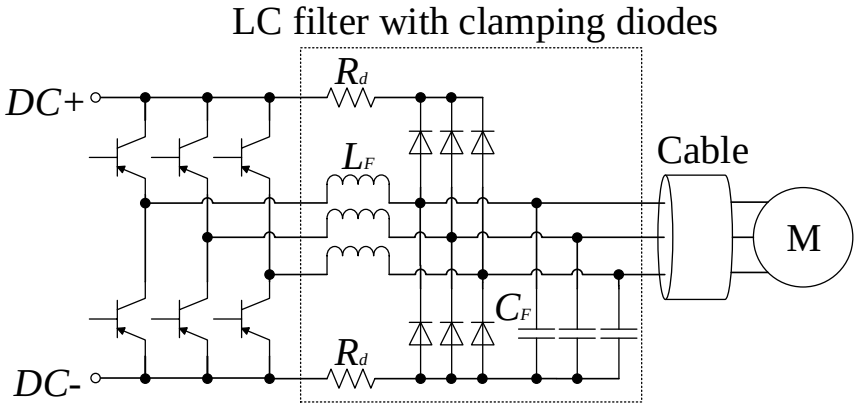


Figure 2.3: LC filter with clamping diodes

drive system, more and more development of filter topology emerges with not only the proper modification of the conventional RLC filter, but also the new type of topology. As an example, a filter topology combined with RLC filter and CM transformer is proposed (Fig. 2.4). This topology maintains the advantage of the ability to filter DM voltage and suppress CM voltage at the same time. The insertion of CM transformer mainly enhance the ability of restricting CM disturbances, and also brings in more flexibility of obtaining necessary filtering effect for drive systems at different power level, by adjusting relevant component values [13]. To be mentioned, the parameter identification and installation of CM transformer becomes much more convenient in low-power applications as all the coils can be uniform in structures and ratings.

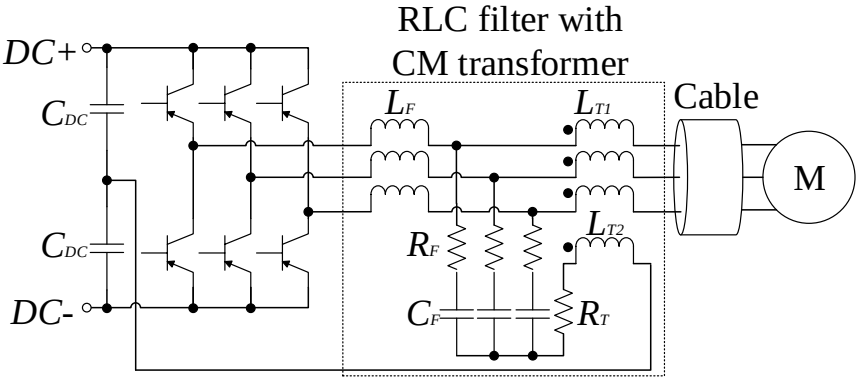


Figure 2.4: RLC filter with CM transformer

RLC at the motor terminals is also an option for the installation of filter topology in the practical application. This should be considered when only limited space is available at the inverter terminal. This brings new discussions about the best position for filter installation. Unfortunately, it is time-consuming and not cost-effective to compare the general performance of motor-terminal mounted case with the inverter-terminal one through the experiment. Additionally, the influence of filter topology on the voltage distribution in the motor stator winding and on the circulation of the CM currents has

not been widely studied in the literature. Thus the methodology of analyzing the filtering effect and influence on the motor of the filter topology is proposed [14]. With the help of the equivalent circuit that can represent the cable and motor accurately, RLC filter mounted at the inverter terminal was proved to be the best solution [2]. In the meantime, new thoughts of analyzing the filter performance also changes the way of designing and identifying parameters of the filter topology.

Based on the analysis of transfer function between inverter output and filter output in Laplace domain, du/dt values in phase/line and CM voltage can be minimized according to the practical condition. The advantage of this method is that it can identify the damping coefficient in the whole frequency range brought by the filter, the time delay of du/dt provided by the filter, as well as the power loss caused by the insertion of filter. Thus the concluded straightforward filter design procedure enables the du/dt values to stay below limits as wanted [14]. This article also demonstrates a new way of filter design and optimization through reliable mathematical analysis, and the theoretical way of analysis can also be extended to other types of drive system.

For some drive system with a low-power induction motor and a long cable, high du/dt PWM pulses can result in overvoltage spikes on the motor. This is due to the reason that the surge impedance of the low-power motor is usually greater than the characteristic impedance of a cable, thus the motor terminal voltage will be nearly twice the incident voltage if the cable is long enough. So specified passive filters are also required to suppress the overshoot voltage spikes in this case,.

A RL-Plus-C filter (Fig. 2.5) is proposed for its availability of largely suppressing the overvoltage. Besides, it also figures out the main drawback of high power dissipation confronted by the conventional passive filters like RLC filter and RC filter. Depend on the generalized model that can describe the interactions between the filter and the inverter-cable-motor system, the characteristics of an ideal RL-Plus-C filter can be derived. This model also enables the performance comparison between different filter topology theoretically [15].

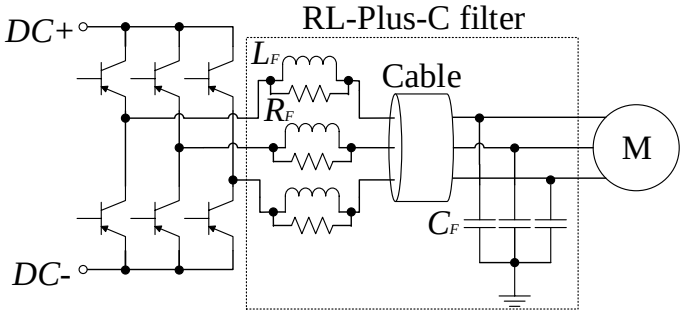


Figure 2.5: RL-Plus-C filter

However, as can be seen in Fig. 2.5, the star point of filter capacitors is grounded and this may result in less bearing life and worse cable insulation [16]. Thus a RLC$_{cm}$-

Plus-C filter is proposed as an optimization. This optimized filter topology is an optimal replacement to the conventional the RL-Plus-C filter when the CM current density is beyond $0.1A/mm^2$. Various filtering effect can also be obtained through adjusting the values of passive components.

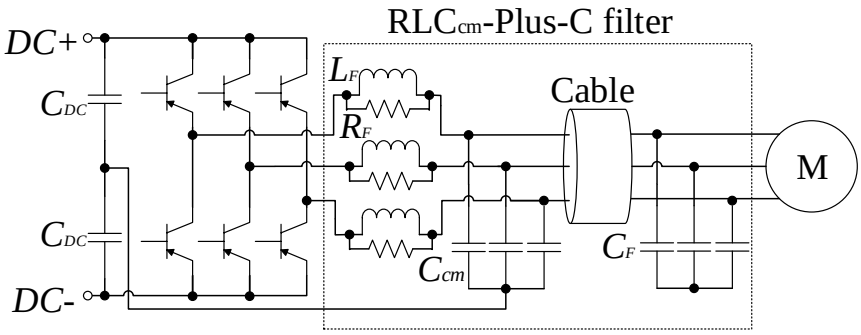


Figure 2.6: RLC$_{cm}$-Plus-C filter

2.1.2 Active Filter

Unlike passive filter that limits CM disturbance of a drive system through well set of passive components like resistor, inductor and capacitor. Active filter can cancel these CM disturbance directly with the help of inserting another power sources. These power sources can be either got from the dc-link, or brought in from the three-phase power cable.

A circuit for cancellation of CM voltage, called Active Common-Noise Canceler (ACC), was proposed more than 20 years ago. As shown in Fig. 2.7, the ACC is put between the inverter output terminals and the feeder wires. Specifically, the ACC consists of three parts: 1) a CM voltage detector with a plurality of capacitors linked to the converter output; 2) a push-pull type emitter follower circuit controlled by the detected CM voltage; 3) a CM transformer that will cancel the CM voltage by superimposing the output voltage from the emitter follower circuit [17]. The capacitors of the CM voltage detector should be with a small value for the protection of the semiconductor devices. Meanwhile, the emitter follower circuit has high input impedance to assure the high accuracy of the CM voltage detector. Moreover, the ACC can even remove any danger of an electric shock on the non-grounded motor frame.

Despite of the above listed advantages of ACC, it still has its own limitation. As shown in Fig. 2.7, each transistor of the ACC must endure the full dc-link voltage when the other transistor turns on, therefore this active filter topology is only suitable for low-voltage drive systems. So a new ACC powered by separate dc supplies and uses a CM transformer having a turns ratio of $a : a : a : 1$ ($a > 1$) is proposed [18] (Fig. 2.8). The design procedure involving the specification of capacitors, the separate power supplies, the complementary transistors and the turns ratio of the CM transformer, was also carefully

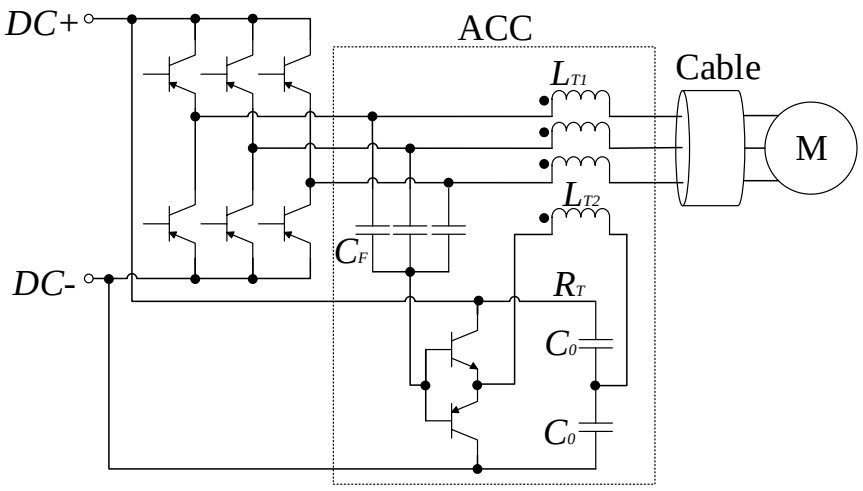


Figure 2.7: Active Common-Noise Canceler

concluded considering the voltage rating of the drive and the ratings of the availability of the complementary transistors.

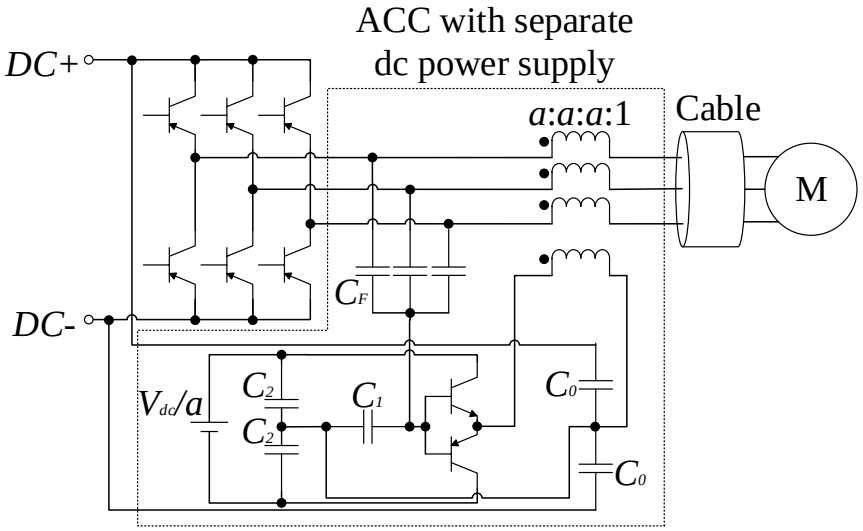


Figure 2.8: ACC with separate dc power supply

The optimized ACC received further development by applying dedicated dc power supply [19]. By doing so, new criteria for the correct choice of the CM voltage partition ratio and set-up of the active compensation device was addressed. It also leads to the more significant increase in reliability and effectiveness of drive systems.

To meet the demand of higher ratio of the power to size in the automotive field, a ACC that is dedicated to drive systems supplied by low-voltage dc bus and uses linear circuits [20] (Fig. 2.9), was proposed with more complicated but more compact structure. Specifically, based on the theoretical analysis, the open-loop transfer function had to be given, which results in the requirement of three filter stages: a low-pass filter stage to improve the filter dynamic response, a linear amplifier to achieve the highest bandwidth,

and a power amplifier to supply the primary winding of the CM transformer. The use of linear amplifiers enables the operation of the ACC through a feedback action. The performance of this kind of ACC reaches its best under the condition that the bandwidth of linear power amplifier is greater than that of the CM voltage expecting for compensation. But its performance can still be guaranteed for the greater CM voltage bandwidth if the proposed design criteria is strictly followed.

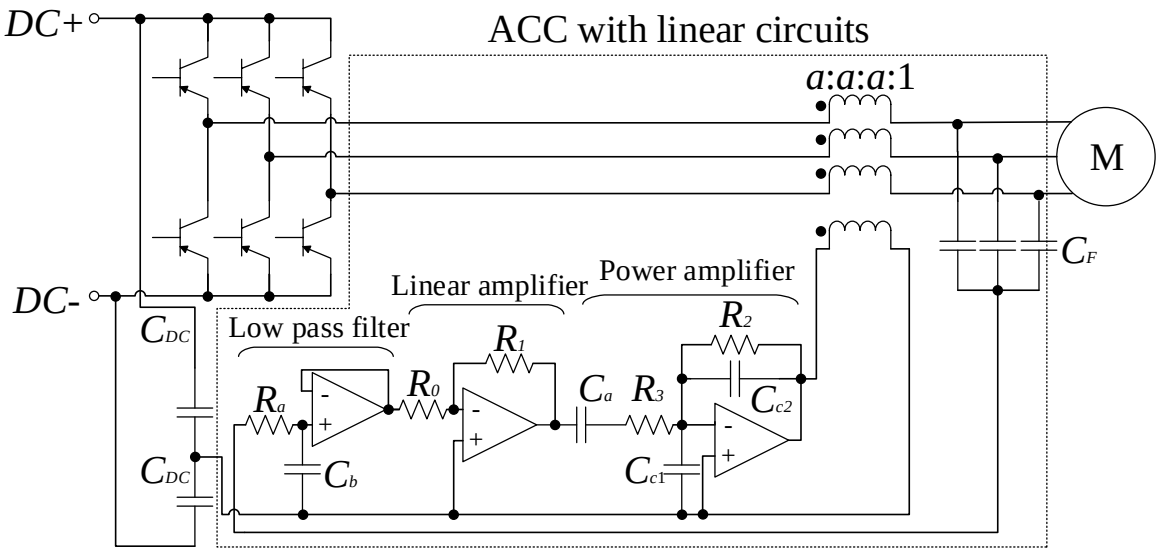


Figure 2.9: ACC with linear circuits

Within the feedback compensation system mentioned in [19, 20], the slope of the compensating voltage step is slightly different with the actual CM voltage step, which results from the limitation of the amplifier bandwidth and the delay of feedback signals. As a consequence, a residual disturbance at the motor terminals appears because of the insertion of the active filter. As the waveform of the residual disturbance looks similar to the CM current, this disturbance can be minimized by adding a supplementary signal proportional to the CM current to the delayed signal [21]. Thus a CM current estimator is required in addition to the active filter topology in Fig. 2.9, as shown in Fig. 2.10. With the assist of the resulted additional feedforward signal, the general performance of CM disturbance reduction can be further improved. Although the optimized ACC with linear circuits requires more and more passive and active components for an increasingly better filtering performance, and this seems to result in a bulky active filter topology. However, depending on the structured design procedure in [21], along with the experience in the application of filter topology assembling, the optimized ACC can still be a compact but efficient filtering system for the reduction of CM disturbance.

In summary, the ACC can be classified as open- and closed-loop. For open-loop ACC, as shown in Fig. 2.7 and 2.8, the input CM voltage is measured and subtracted afterwards. While for closed-loop ACC, as shown in Fig. 2.9, the output CM voltage is measured and fed back through a controller to nullify it.

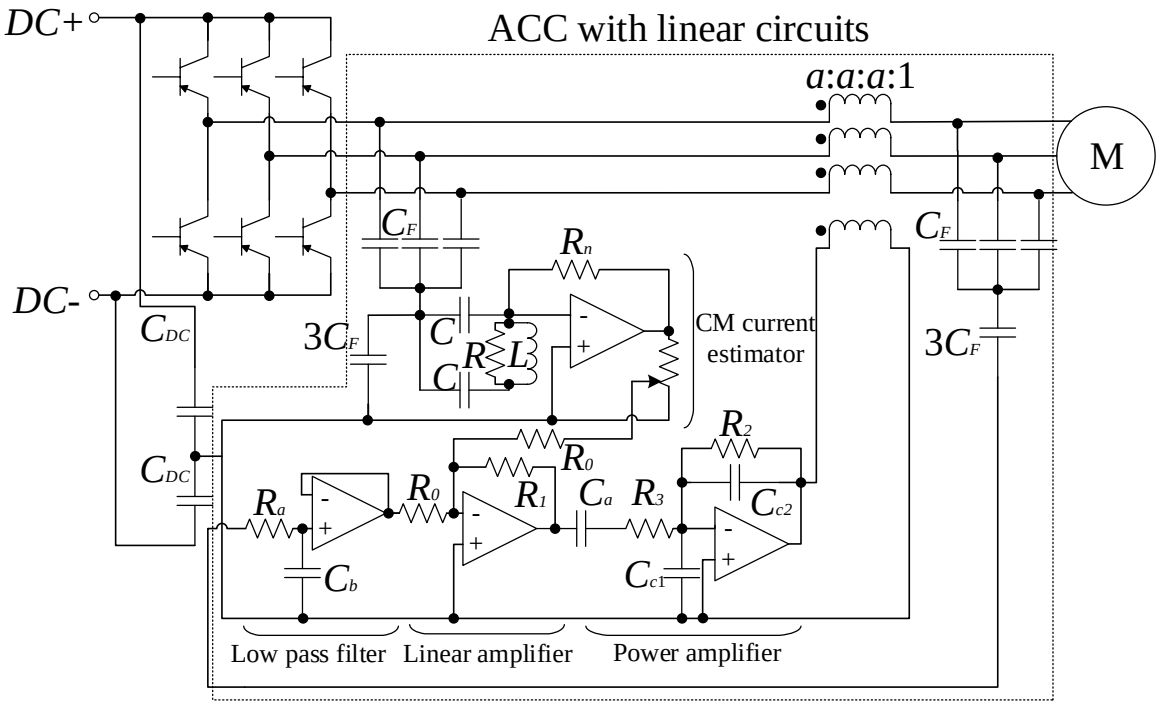


Figure 2.10: ACC with linear circuits including CM current estimator

2.2 PWM Optimization

Three-phase PWM converters is the most widely used power electronic converters for power conversion application such as AC motor drives, PWM rectifiers, grid-connected converters, and renewable energy converters. Space-vector PWM (SV-PWM) and Sine-Triangle PWM (S-PWM) are the most typical modulation methods [22].

A three-phase inverter converts a DC supply, via a series of switches, to three output legs which connects to a three-phase motor. The switches must be controlled so that at no time are both switches in the same leg turned on or else the DC supply would be shorted. This requirement may be met by the complementary operation of the switches within a leg. Given the equivalent circuit of a three-phase voltage-source inverter in Fig. 2.11, the switching function, $G_x = 1(x = U, V, W)$ represents that the corresponding phase is connected to the DC+, while $G_x = 0(x = U, V, W)$ means connection to the DC-.

Thus, for SV-PWM, it leads to eight possible switching vectors for the inverter, V0 through V7 with six active switching vectors (V1-V6) and two zero vectors (V0 and V7), as shown in Table. 2.1.

$$\begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} u_U \\ u_V \\ u_W \end{bmatrix} \tag{2.1}$$

As can be seen in Fig. 2.12(a), to implement space vector modulation, a reference signal U_{ref} is sampled with a frequency f_s (switching period $T_s = 1/f_s$). The reference signal

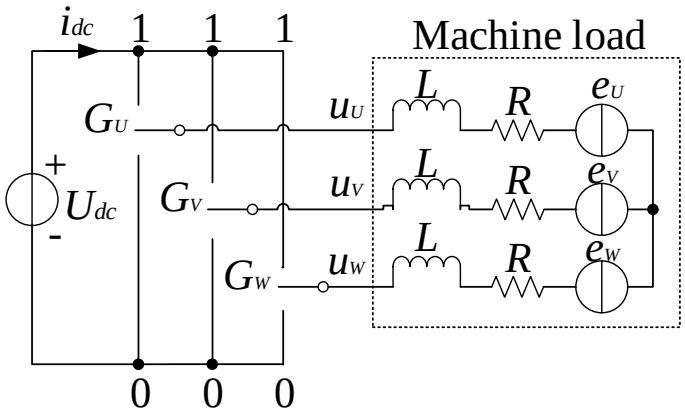


Figure 2.11: Equivalent circuit of the three-phase inverter.

Table 2.1: Switching vectors and phase-voltages of the three-phase voltage source inverter (VSI).

Vectors	G_U	G_V	G_W	u_U	u_V	u_W
V0	0	0	0	$-U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$
V1	1	0	0	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$
V2	1	1	0	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$
V3	0	1	0	$-U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$
V4	0	1	1	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$
V5	0	0	1	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$
V6	1	0	1	$U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$
V7	1	1	1	$U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$

may be generated from three separate phase references using the $\alpha\beta 0$ transformation (also known as Clark transformation), as shown in (2.1). For all eight switching combinations shown in Table. 2.1, their corresponding three phase voltages can be transformed into six active switching vectors (shown as V0-V7 in Fig. 2.12(a)) and two zero vectors using (2.1). The reference vector is then synthesized using a combination of the two adjacent active switching vectors and one or both of the zero vectors. Various strategies of selecting the order of the vectors and which zero vector(s) to use exist. Strategy selection will affect the harmonic content and the switching losses. To be mentioned, for this modulation algorithm, the zero vectors are usually selected in the PWM sequence just to minimize the switching losses. Consequently the CM voltage is not under control.

For S-PWM, a reference copy of the desired sinusoidal waveform, the modulating wave, is compared to a much higher frequency triangular waveform, called the carrier wave. The resulting drive signals cause multiple turn-on of the inverter switches in each half-cycle with variable pulse width to produce a quasi-sine wave of load voltage. The pulse width increases from a very narrow width at the start of each cycle to a maximum width in the middle of each cycle. Then the pulse width reduces again after maximum until its

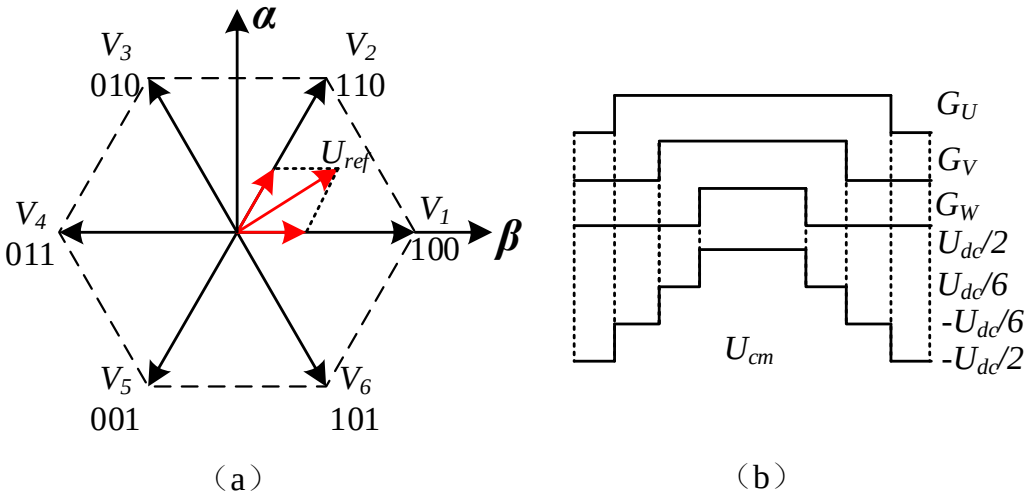


Figure 2.12: (a) Switching vectors V0-V7; (b) Triggering pulses and CM voltage.

minimum width at the end of the half-cycle period. Unlike SV-PWM, in which there are only two degrees of freedom u_α and u_β (the remaining u_0 is kept free to optimize the switching losses and maximize the voltage usage), S-PWM has three degrees of freedom, u_a, u_b, u_c, which can be transformed from/to u_α, u_β, u_0. Therefore, if the zero-sequence current/voltage also needs to be controlled during the operation of EDS, S-PWM other than SV-PWM should be used.

Two-level modulator studies have also shown that space vector modulation is similar to centered sine-triangle modulation, and can be realized through proper third harmonics or common-mode injection schemes [23, 24].

Normally, switching frequency of SV-PWM is usually fixed and all of its triggering pulses on each phase locates at the center of the whole period. This brings in great convenience of design and control, but will also result in the loss of an important freedom for system performance improvement and CM current reduction. For example, as shown in Fig. 2.12(b), symmetrical aligned triggering pulses on all three phases of a SV-PWM or S-PWM inverter will produce high peak value of the CM voltage. Thus advanced PWM techniques are expected to make use of these freedom to optimize the whole system performance.

2.2.1 Variable Switching Frequency PWM (VSF-PWM) Technology

Random PWM (R-PWM) updates the switching cycle randomly for the converter to distribute the spectrum in a wider range than the constant switching frequency PWM [25–27]. By doing this, the EMI noises of the converter system was reduced effectively. However, the randomness of the varied switching frequency is usually decided based on statistical effects other than calculation, which makes the losses and current ripple not controllable. Thus the PWM with controllable variable switching frequency is a better

choice.

To be mentioned, in practical cases, the phase current is the combination of an ideal sinusoidal wave and ripples. While the required current of the electrical machine is the mean value within a PWM period, the current ripple is the oscillation within the same period. As shown in Fig. 2.13, in the left is the measured phase current (blue) and its average (red), the current ripple can then be defined as the error between the phase current and its average value (in the right). As current ripple is an important parameter for design and control of three-phase PWM converters, and the change of switching frequency can alter the current ripple linearly, so increasingly more studies are required for the reliable prediction of the current ripple.

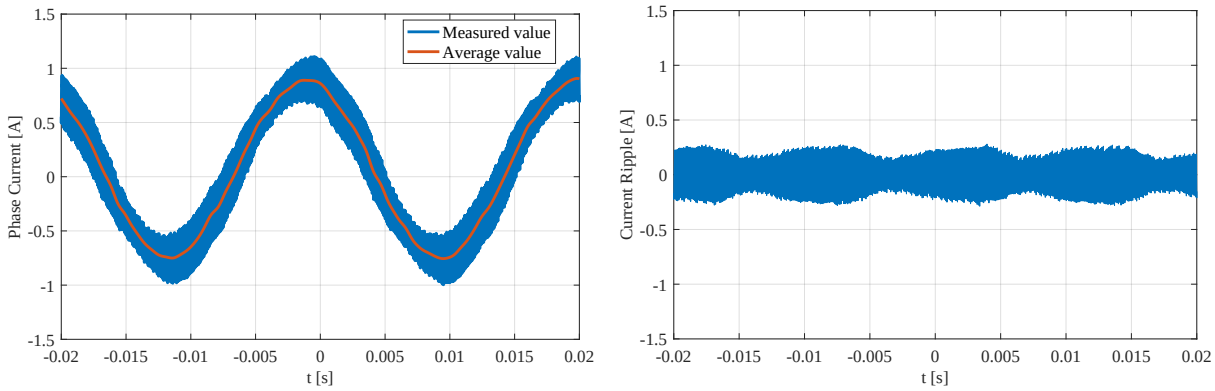


Figure 2.13: Phase current (left) and the corresponding current ripple(right).

Under the ideal condition, the current ripple in each switching cycle can be predicted by knowing the duty cycle, switching period, output inductance and dc voltage [28]. Then the current ripple can be controlled by shifting the switching frequency as required. This also leads to the availability of controlling switching losses, but these can only be realized in a single-phase inverter.

For the much more widely used three-phase converter, the expression of the ripple current is much more difficult to obtain. In each phase, the current ripple is influenced not only by its own switching action, but also the switching actions of other two phases. This means eight times of the expressions required for the similar prediction of a three-phase converter as compared with a single-phase one. To be mentioned, the vector acting time is required in addition to realize the current ripple prediction [29]. Specifically, the peak and RMS values of the current ripple had been chosen as the parameters to be predicted. The prediction process is shown in Fig. 2.14.

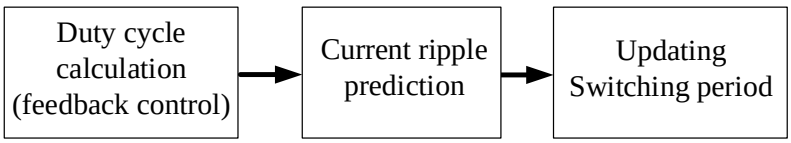


Figure 2.14: Switching period update process

With the help of current ripple estimation for the peak and RMS value, two types of VSF-PWM are proposed as VSF-PWM1 and VSF-PWM2, respectively. For VSF-PWM1, the ripple currents are made to under the specified limit in each switching period, which reduces the average switching frequency when compared with the constant switching frequency PWM. This also results in less switching losses and conducted EMI. For VSF-PWM2, the ripple currents are controlled to have the expected RMS value, which also leads to the reduction of conducted EMI, while the switching losses almost remains the same [29].

However, when the converter phase number keeps increasing, the method of using expression of ripple currents to predict the current ripple will become more and more complex, which creates great difficulty for the prediction. As a result, four-phase converter will need 16 expressions and five-phase converter needs even 32 expressions. Meanwhile, the calculation effort required for the real-time prediction of converters with more than three phases will be too much that the general system performance can be also influenced.

Thus a new current ripple prediction strategy was proposed based on the single-branch model [30]. All the voltage vectors can be contained in the model and the analysis is much simpler. The method also borrows the analysis for current ripple with different zones in each switching cycle. Specifically, each branch of an n-phase converter can be modeled with its single-phase equivalent circuit, which contains the converter terminal voltage, the ac load (average) voltage, and the common mode voltage. Then the voltage on the ac inductor can be derived from this single-phase equivalent circuit. Moreover, the current ripple in one switching cycle can be divided into $2n + 2$ linear zones in the n-phase converter.With the di/dt from the single-phase equivalent circuit and the active time for each zone, the ripple current can be predicted. With the proposed real-time current ripple prediction method, the current ripple in a multiphase converter can be readily controlled depending on the application needs.

As the current ripple is also directly related to the torque ripple of the electric machine and the bus voltage ripple of the PWM rectifier, VSF-PWM is also able to limit these two types of ripple for the improvement of the drive system performance. In [31], the VSF-PWM technique results in a lower peak-to-peak torque ripple than conventional SV-PWM at high speeds of an induction motor drive, while the magnitude of the dominant torque harmonic is significantly lower than that due to conventional SV-PWM at high speeds of the drive.

2.2.2 Phase-shift PWM (PS-PWM) Technology

As can be seen in Fig. 2.12, the utilization of alternating zero switching state V_0 and V_7 will result in a high peak-to peak value of CM voltage. So the PWM techniques shown in [32, 33] use only nonzero switching states for two-level inverter control. But their approaches also reduces the linear modulation range (narrower range of speed (torque)

control) and increases the current ripple, which cannot be accepted for many applications even considering their good performance of reducing CM voltage.

Another solution was given in [34], which demonstrates a PWM technique with synchronization of switching sequences of the front-end converter and the motor inverter. The inverter switching point is shifted in one control period and aligned to one of the switching points of the converter. This modification removes the limitation of narrower range of control, while maintains the low peak-to-peak value of CM voltage of the drive system. However, this PWM technique requires an inverter with an active front end, which also limits its application, e.g. not useful for battery supplied drives as in electric vehicles.

For a more widely used vector-controlled inverters with diode front ends, a PS-PWM called active zero-state PWM (AZS-PWM) was proposed with consideration of dead-time effect [35]. Normally, the remaining time that is not needed by the targeted switching vectors should be allocated to the zero vectors, as shown in Fig. 2.12. When zero vectors are not expected in the control loop, either this remaining time can be given to the two vectors that are adjacent to effective vectors and on the opposite direction (AZS-PWM1, in Fig. 2.15), or it can be assigned to vectors opposite to one of the two effective vectors (AZS-PWM2 and AZS-PWM3, in Fig. 2.16 and 2.17, respectively). Practically, AZS-PWM1-3 can be realized through shifting 180 degrees with respect to the switching period for the phase with the middle, longest and shortest triggering time, respectively. When the switching action is treated as ideal, three types of AZS-PWM have almost the same effects of reducing the CM voltage. However, this cannot happen actually, due to the existence of dead-time necessary for the safety of the inverter. Thus, considering the dead-time effect, the resulted CM voltage of AZS-PWM2 and AZS-PWM3 changes as shown in Fig. 2.18.

It can be seen in Fig. 2.18 that there exist unexpected voltage peaks and it should happen twice in each switching period. Thus this phenomenon will have great influence on the CM voltage reduction if the switching frequency is large enough. So it is concluded in [35] that AZS-PWM1 is the optimal CM voltage reduction PWM technique among the three. Meanwhile, applying AZS-PWM1 in a drive within the rated speed range will not deteriorate the system performance [36].

However, the pulse pattern of AZS-PWM1 leads to bipolar line-to-line voltage pulses. These pulses creates significant overvoltages at the motor terminals, especially for applications with long cable. Besides, by applying AZS-PWM, the PWM ripple of output current and dc bus current are higher than applying conventional PWM.

In [37], another PS-PWM named near-state PWM (NS-PWM) was proposed based on the modification of discontinuous PWM(D-PWM). Similarly, to avoid the use of zero vectors in D-PWM, NS-PWM uses a group of three nonzero vectors to match the reference volt-seconds (Fig. 2.19). Specifically, except for the two effective vectors, the third vector should be the one that is adjacent to the effective vectors (which one of the two adjacent vectors should be used depends on the specific algorithm that chooses the better one in

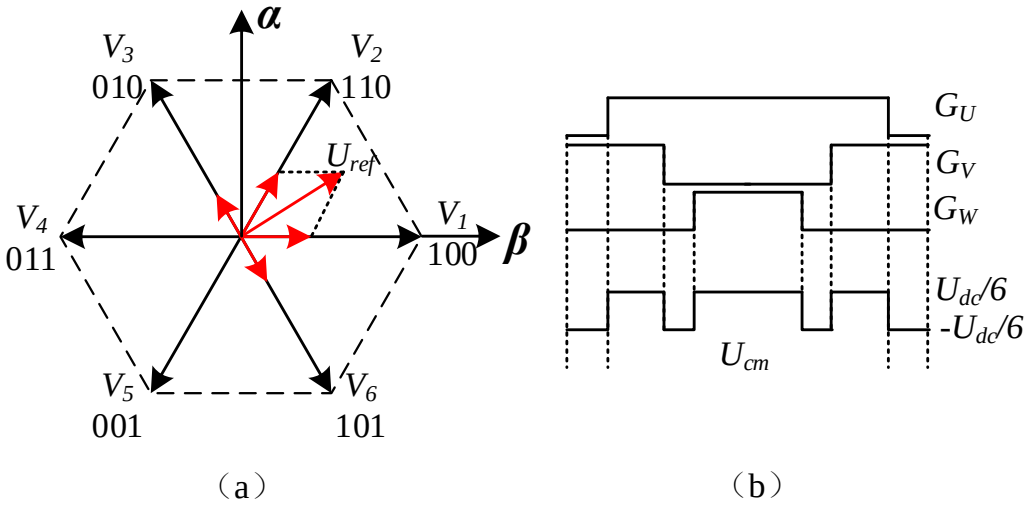


Figure 2.15: Shift the phase with the middle length of triggering time for 180^o (AZS-PWM1).

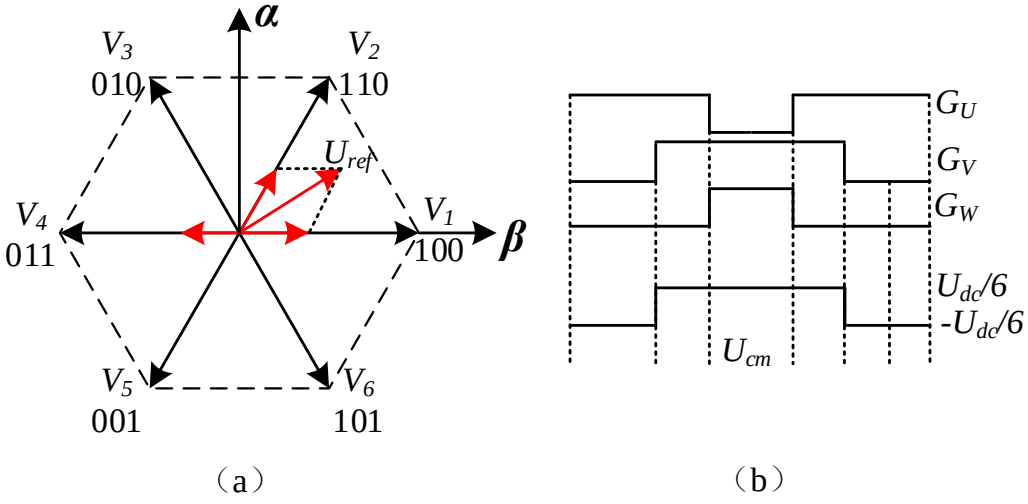


Figure 2.16: Shift the phase with the longest length of triggering time for 180^o (AZS-PWM2).

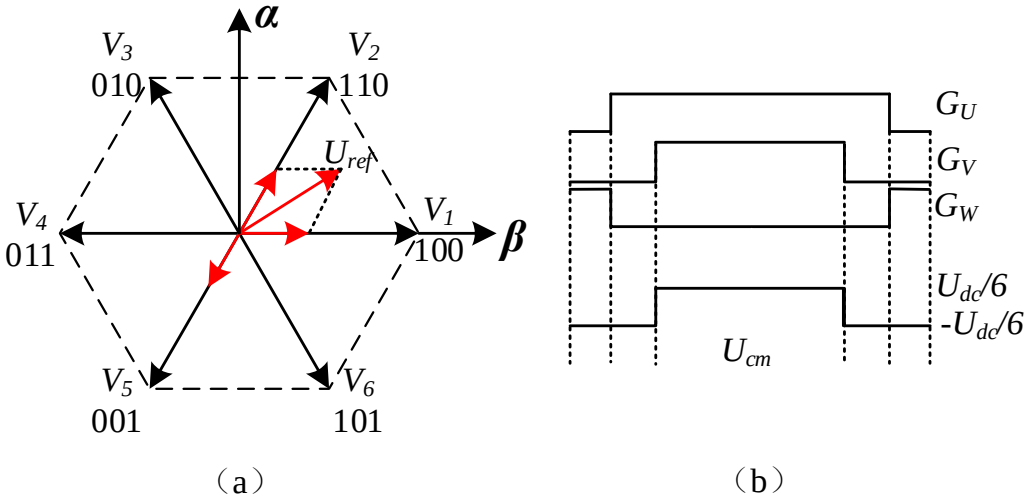


Figure 2.17: Shift the phase with the shortest length of triggering time for 180^o (AZS-PWM3).

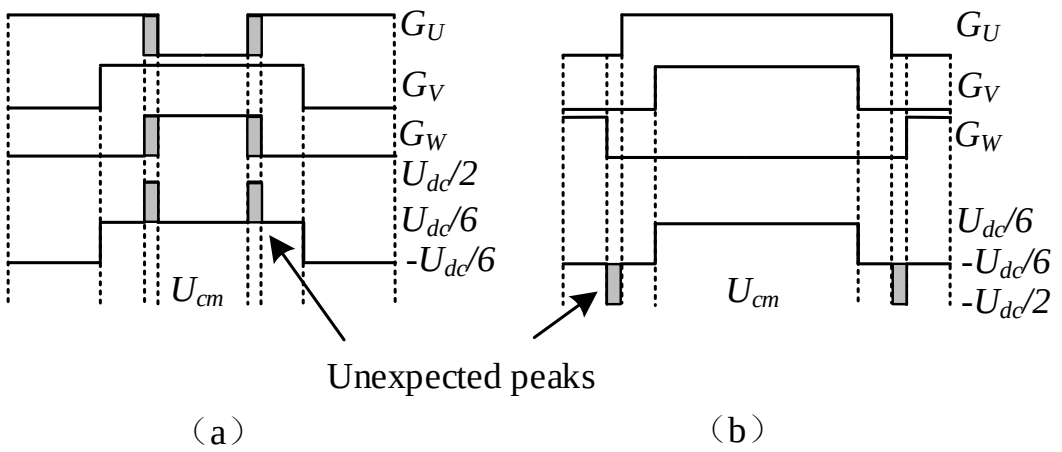


Figure 2.18: Influence of dead-time effect on: (a) AZS-PWM2; (b)AZS-PWM3.

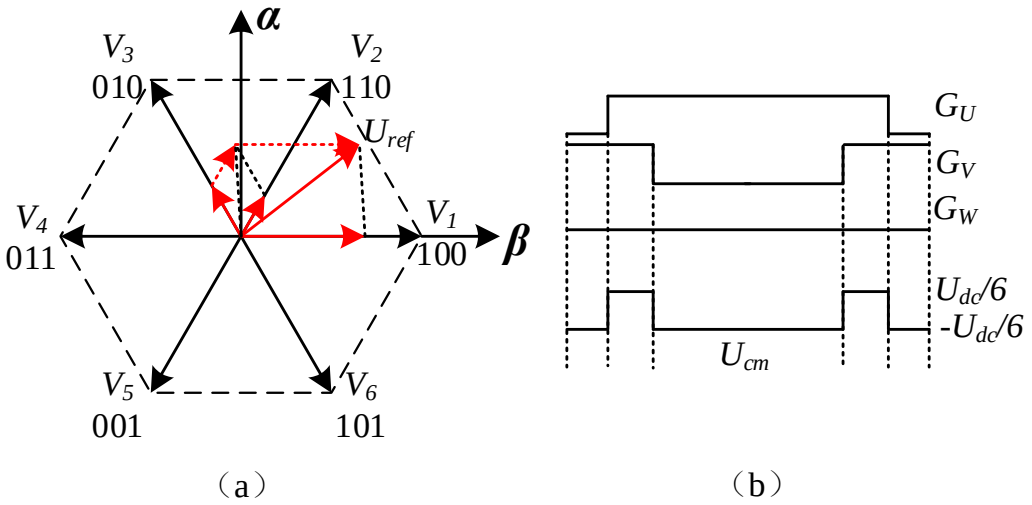


Figure 2.19: Near-state PWM technique.

each segment). Practically, NS-PWM is realized by shifting 180 degree for any one of the two phase with triggering action.

It is concluded in [37] that NS-PWM can reduce CM voltage substantially and CM current partially, and it maintains the advantage of less switching losses of D-PWM. Even though the line-to-line voltage pulse pattern of NS-PWM is partially bipolar, the voltage pulses are always sufficiently away from each other, thus excessive overvoltages will not appear at the motor terminals during switching. Furthermore, NS-PWM is found to have low PWM ripple when operating at a modulation index over 0.61, and this also demonstrates the best application field of it.

A general comparison of the performance characteristics of AZS-PWM1, NS-PWM, conventional D-PWM and SV-PWM is given in [38]. These performance characteristics include the dc-link current ripple, the ac output voltage and current ripple characteristic, and the voltage linearity characteristics. It is concluded that although AZS-PWM1

causes more serious PWM ripple than NS-PWM and SV-PWM at high modulation-index operation, but when the drive system is operated at the low modulation index region, the PWM ripple results from AZS-PWM1 reduces to the same level of NS-PWM and SV-PWM. Thus it is recommended to combine AZS-PWM1 and NS-PWM for a favorable low CM voltage operation in the whole range of modulation index.

To be mentioned, AZS-PWM1 has performance limitation as the zero-voltage time interval between the bipolar pulses periodically decreases within a fundamental cycle, to a very small value that the line-to-line voltage has rapid pulse reversals [39]. When this zero-voltage time interval becomes too small that it is comparable to the switching transient time, overvoltages may be produced at the motor terminals. To overcome this problem, each time when the reference voltage vector approaches the effective vectors, the duty cycle of the smaller vector should be increased by 2ε while that of the larger vector decreased by the same value, as shown in Fig. 2.20. Besides, for the balance of the vector volt-seconds, the two adjacent vectors also suffer the change of duty cycle by ε. The modification factor ε is dominated by the minimum zero-voltage interval duty cycle.

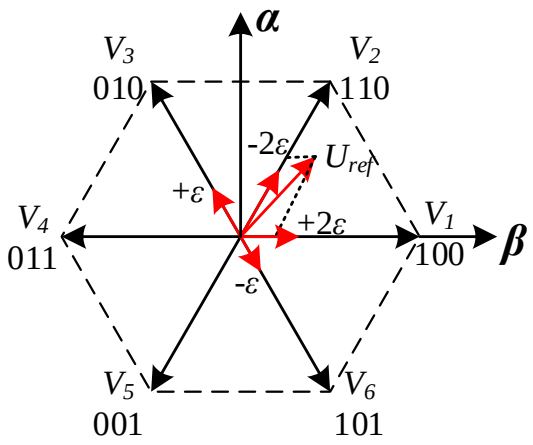


Figure 2.20: Modified AZS-PWM technique.

A combined PWM technique that utilizes the modified AZS-PWM at low modulation index and the NS-PWM at high modulation index seamlessly, is developed in [39]. Merging the benefits of both advanced PS-PWM, the combined PWM yields low CM voltage and current, acceptable PWM ripple at the input and output of the inverter, and has no overvoltage problems. When a small CM inductor is also included in the drive system with the combined PWM, the CM current can be further reduced significantly.

2.3 Four-wire Drive System

A three-phase-four-wire drive system is usually shown as 4wDC, 4wEL, or the combination of both. The 4wDC is the four-wire drive system that connects the motor neutral point of

PMSM to the mid of dc-link through capacitors, while in 4wEL, the motor neutral point is connected to the fourth leg. The advantage of 4wDC is that it requires no additional pair of IGBT and thus also results in less potential switching loss. For 4wEL, with the fourth leg, the mid of dc-link can be perfectly caught and available for compensation when the sudden imbalance occurs. Due to the existence of the fourth wire, functions like self-sensing control and fault-tolerant operation can be realized, and many more functions are also expected based on the further development of this four-wire topology.

2.3.1 Self-sensing Control

Self-sensing control strategy, also named as sensorless or encoderless, is the methods to identify the rotor position in electric machines by measuring only voltages and currents [40]. This control method is commonly applied in PMSM, and realized through determination of rotor position by the back electromotive force (EMF) or the position dependence of the inductances. However, methods based on the back EMF cannot work in standstill and even its accuracy of position identification becomes too low at low-speed. These limitations hinder its further application in the electric drive system. For the other method using the position dependence of the inductances, it works in the whole speed range involving stanstill as well. This makes it a favorable choice for the self-sensing control. Specifically, the position dependence of the inductance, later called magnetic saliency, is produced by saliencies in the rotor, magnetic anisotropy, or stator saturation due to the rotor flux.

Usually, injecting a signal in the nonzero-sequence components, such as $\alpha\beta$ or dq, is one way of detecting magnetic saliencies. It is proposed in [41] to use a rotating voltage vector as the inject signal. Specifically, through balanced high-frequency voltage injection, a high-frequency rotating field is added to the main field producing a modulation of the saturation level of the main flux. In saturated conditions, the variation of the saturation level creates a modulation of the third harmonic flux through the nonlinear relation between the main flux and the third harmonic flux. Consequently, the zero-sequence voltage also shows a high-frequency ripple that contains information on the relative position of the two rotating fields. Both of the zero-sequence voltage and its high-frequency ripple is used as the sensing variable, and this can be considered as an advantage as direct and inverse components are equal to zero on the zero-sequence axis.

In [42, 43], an alternating carrier is used as the inject signal for estimating the rotor position of a PMSM. The signal is injected in the spatial direction of the estimated rotor position axis, while the signal response in the quadrature axis is a function of the estimation error, which is used to correct the estimated angle. A particular demodulation technique is necessary to make the estimation immune against the delay of the PWM and the nonlinear distortions of the inverter. The position estimation scheme works accurately even without dead-time compensation. This is achieved by using a reference signal for decoding that has passed through the inverter and, thus, has undergone the same distortions as the

position error signal. Before the drive is started, the initial rotor position and the magnet polarity are detected. The spatial orientation of the magnet axis is identified using the carrier injection scheme. The polarity of the magnet is determined by injecting two short current pulses in alignment with the estimated magnet axis, but in opposed directions. The difference of the pulse amplitudes is used to identify the north pole axis. The proposed method exhibits high-sensitivity and good signal-to-noise ratio.

In some drives, the rotor position is also computed by measuring current ripples that are generated by supplying the PMSM periodically with high-frequency voltage test pulses [44].

When using methods proposed in [45], special care has to be taken to overcome the dead-time effect of the inverter, which causes current clamping and other side effects including those caused by the current control loop. An additional switching sequence has to be embedded and it will result in a torque and current ripple. To overcome these problems, a new flux-estimation algorithm that uses the phase current derivative to extract the flux-position information is presented [41]- [44]. In contrast to previously introduced methods, only fundamental-wave excitation using standard PWM or slightly modified PWM is required for this new algorithm. Furthermore, only the current response in the two active states of PWM is used. This makes it possible to use sensorless control for the whole speed range including overmodulation and removes the distortion and parasitic influence of the zero switching states during the estimation of the flux.

However, for all the above mentioned methods that inject a signal in the non-zero-sequence components, the signal processing for the position estimation is really complicated. Specifically, methods that inject the signal in $\alpha\beta$ or dq will interact with the current control loop [46]. Thus it can happen that the current controller counteracts the injected signal (may come in resonances), or current transients may perturb the position estimation. To avoid this, a low-pass filter is added in the current control feedback, or the controller is adjusted for a lower bandwidth. Both measures reduce the dynamic of the control. In comparison, methods that inject the signal in the zero sequence (connecting the neutral point) are decoupled from the current control, allowing higher control dynamics. Besides, as the filtering is often required to obtain the carrier response from the controlled current, this could result in a significant delay that degrades the dynamics of the self-sensing control [47].

To overcome these limitations, another way of producing saliencies is proposed in [6]. Instead of injecting the signal in the non-zero-sequence components, the signal is injected in the zero-sequence components and the response is evaluated through $\alpha\beta$ currents. For the excitation of the zero sequence and its action on the motor windings, the motor neutral point must be connected to the mid of dc-link to implement a three-phase four-wire topology (4wDC), as shown in Fig.2.21. A LC filter is inserted on the fourth wire to limit the zero-sequence current, and the current derivative can be computed from the measured current or acquired directly by a current derivative sensor shown in Fig. 2.21.

No modification of the standard PWM is required for the carrier injection. Due to the use of carrier injection in the zero sequence, no torque pulsation and additional audible noise are produced, and high dynamics of the position estimation can be expected. Moreover, the signal processing is simple and the estimation will not be perturbed by the dead-time effect.

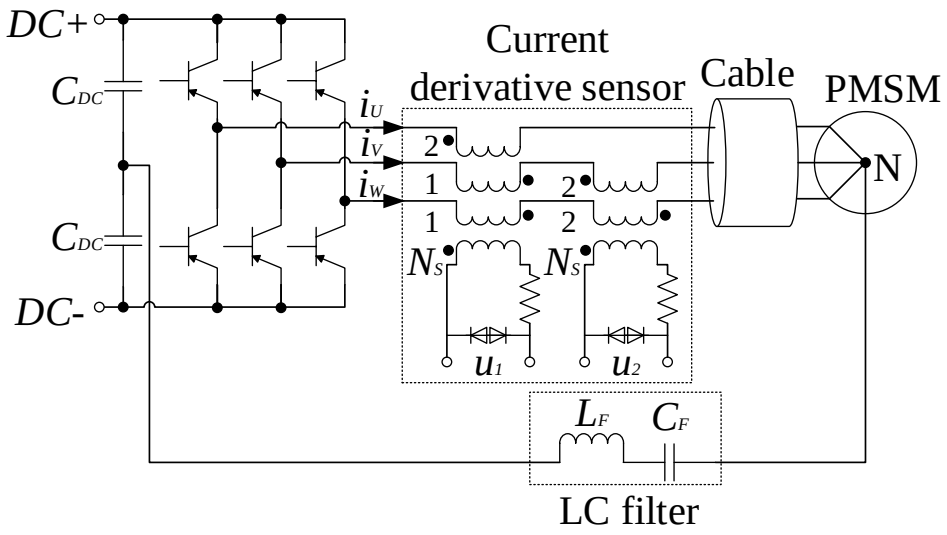


Figure 2.21: Three-phase four-wire topology for self-sensing control.

2.3.2 Fault-tolerant Operation

Fault-tolerant operation design for a adjustable speed ac electric drive system, as an important procedures that insure the reliable and continuous operation of the system, is always of great interest for all members of the drives community and marketplace. As a consequence, parallel redundancy is often applied for the drive systems. Modular parallel redundant systems, machine design modifications, intelligent control, as well as systems with phase numbers over three, have been proposed as means of realizing and improving fault tolerance.

An early attempt to add fault tolerant capacity to a standard three-phase inverter topology was presented in [48, 49], which proposes a switch-redundant topology as shown in Fig. 2.22. This topology includes four triode for alternating current (TRIAC) or back-to-back connected silicon controlled rectifiers (SCR) and three fast acting fuses.

In the case of an opened phase fault, only TRIAC TR_n is fired to connect the motor neutral point to the mid of dc-link, which maintains the system capacity to apply half of the dc-link voltage across each remaining phases.

When the system suffers a short-circuit switching device failure, the complementary transistor $S-ap$ will be automatically opened to avoid a short-through failure. Besides, the TRIAC TR_a turns on and the fuse opens and clears the shorted switch. Consequently,TR_a

is subsequently controlled to continuously on under the post-fault condition. This topology allows for the full rated torque production, but the system will enter the field weakening mode at about one-half speed. Thus the faulted system is able to producing power up to 1.5 times of the rated value.

In general, the switch-redundant topology is fault tolerant to a single shorted switch, a single opened switch, and an opened phase fault.

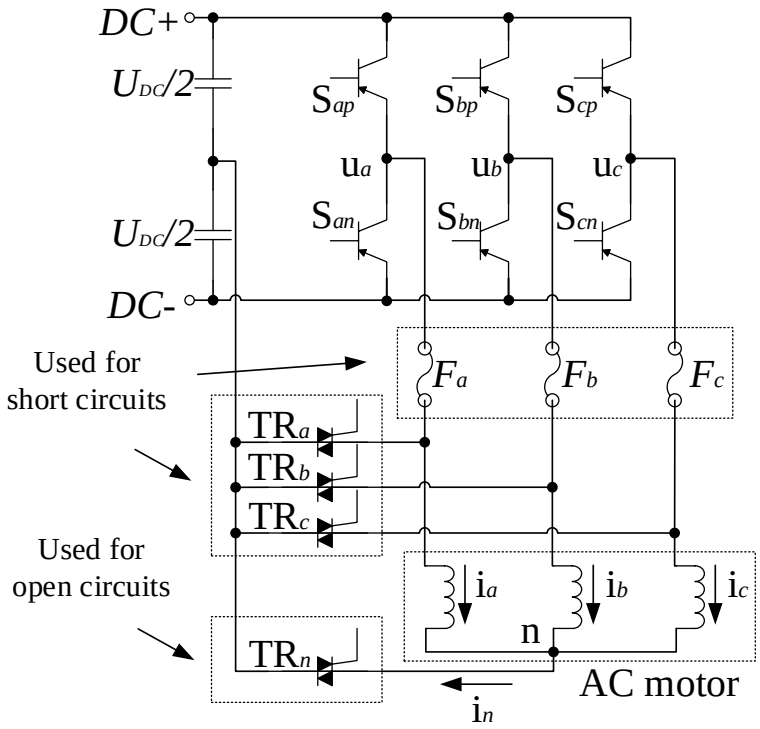


Figure 2.22: Switch-redundant topology.

Another fault tolerant topology that is unique in its capability of tolerating the phase-leg short-circuit, was proposed in [50]. As shown in Fig. 2.23, this topology involves a four-leg inverter with additional two fuses and two SCRs for each phase leg, and named as double switch-redundant topology. It is also fault tolerant to all the faults that can be overcame by the switch-redundant topology. It can be seen from Fig. 2.23 that the double switch-redundant topology is different for the motor neutral connection. By connecting the motor neutral to a fourth leg, the system is then free of the dc midpoint balancing problems, as well as the minimum capacitance sizing issues. Besides, the control method of shifting the voltage at the motor neutral point can be also applied to the three-phase system with an opened phase fault. To be mentioned, when a fault occurs in the neutral leg, it will be isolated and the remaining system will operate as a conventional three-phase inverter-fed drive system without fault tolerant capability.

Due to the existence of an additional inverter leg as shown in Fig. 2.23, it is also possible to replace the faulty phase leg directly with the spare inverter leg [50]. Thus the fault tolerant operation can be also realized in the four-wire topology as shown in Fig. 2.24.

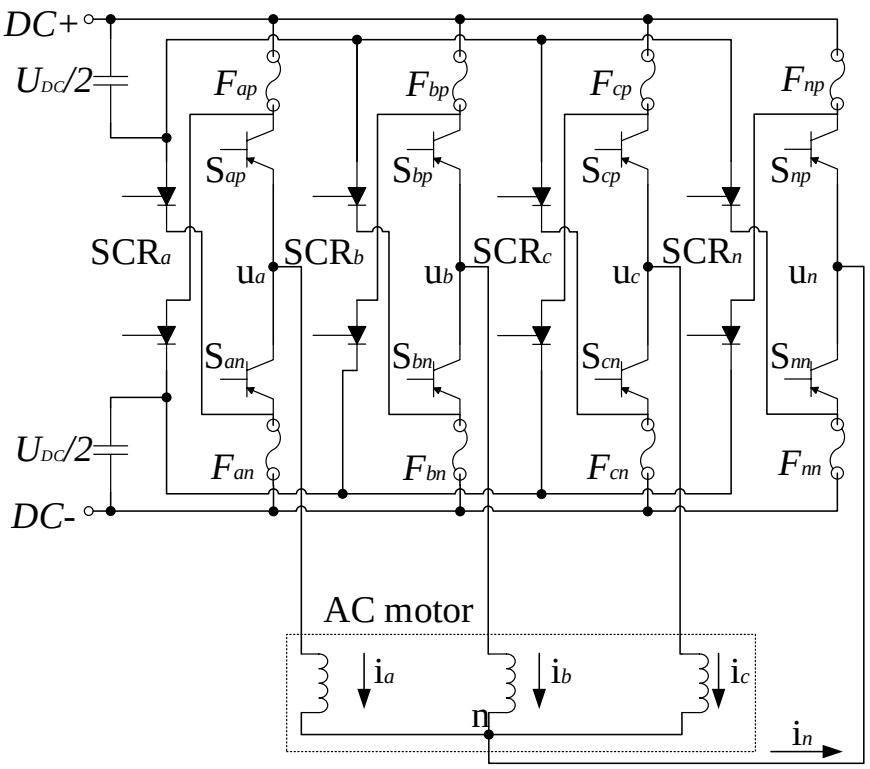


Figure 2.23: Double switch-redundant topology.

This topology incorporates the fault isolating SCRs and fuses only in the three active legs. The spare leg remains inactive during normal operation, when needed, the spare leg will be connected in place of the faulty leg and is therefore able to maintain rated output power during the post-fault operation. Besides, this topology is welcome in situations that the motor neutral point is not available. To be concerned, the presence of the fuses will result in additional inductance on the dc bus, the influence of which should be considered seriously during the system design. And fuse selection also needs to be careful for avoiding nuisance faults caused by fuse failure.

In [51], the four-leg inverter topology (Fig. 2.25) is demonstrated to improve the fault tolerance of drive systems. It utilizes the same control method as the phase-redundant topology. and also requires no access to the mid of dc-link. In [52], this topology is used for an opened switch fault resulting from gate drive unit failures. Practically, along with the method presented in [52], the four-leg inverter topology can identify the opened switch faults occurred in the upper or lower switches, but not the combination of them. However, this topology allows to work after any of following open fault: single top, single bottom or simultaneously top and bottom in the same phase, as illustrated in [7]. Besides, the topology allows to accommodate open fault in the neutral leg. If the neutral leg is open, a standard three-phase three-wire drive remains, which can be controlled as in usual drives.

The post-fault control action of the four-leg inverter topology consists of commanding a three-phase set of unipolar currents, with two phases always conducting a nonzero current.

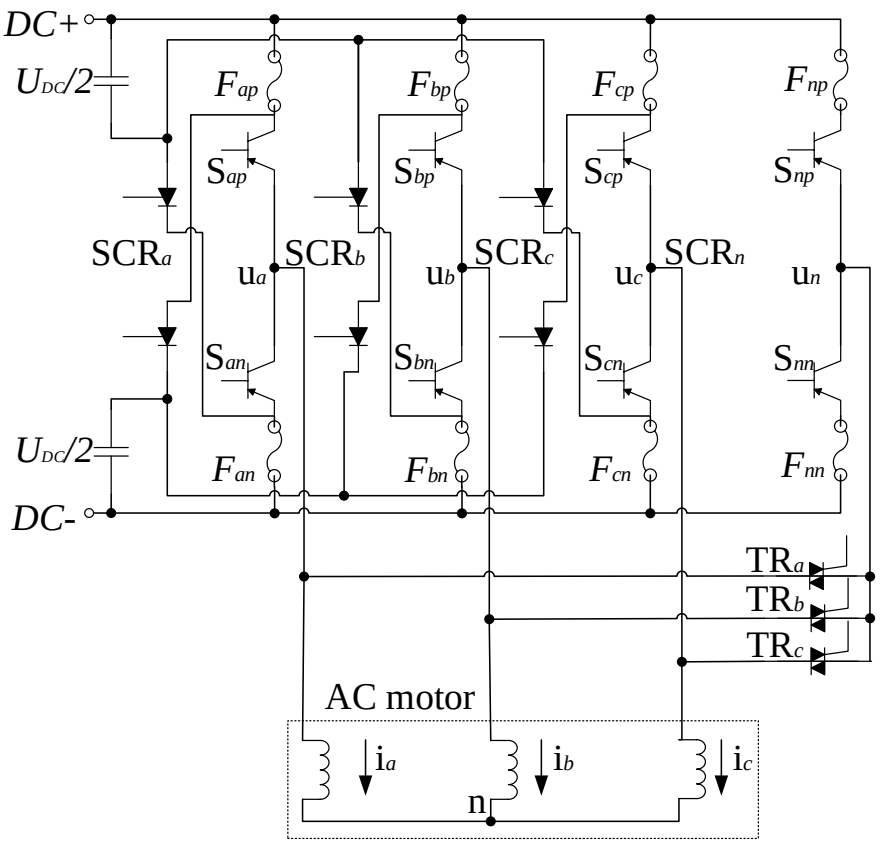


Figure 2.24: Phase-redundant topology.

This on one hand maintains the available voltage space of the converter, on the other hand reduces the current space.

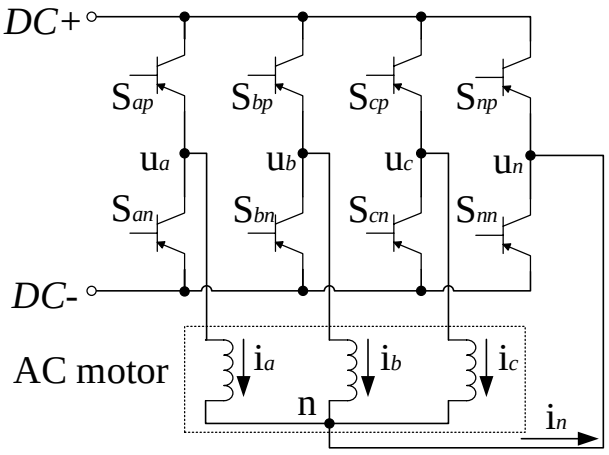


Figure 2.25: Four-leg inverter topology.

It is concluded in [7] that, except for the four-leg inverter topology, all the other topologies mentioned above have to reconfigure the power topology and/or the control strategy, and the power topology is more complex. This results in the transients and pulsed power, which are the root cause of the electrical stress on power electronic devices,

as well as the mechanical stress and fatigue in mechanical components. Thus two four-wire topologies with permanently connected fourth wire are used for a practically feasible control strategy that enables fault detection and tolerance. These two four-wire topologies, named 4wDC and 4wEL, respectively, are shown in Fig. 2.26. They avoid the reconfiguration of the power topology, and with the help of the presented control algorithm in [7], the transition from the normal to fault-tolerant operation is very smooth. To be mentioned, the disadvantage of bringing in 4wDC is that it produces higher current ripple with higher losses.

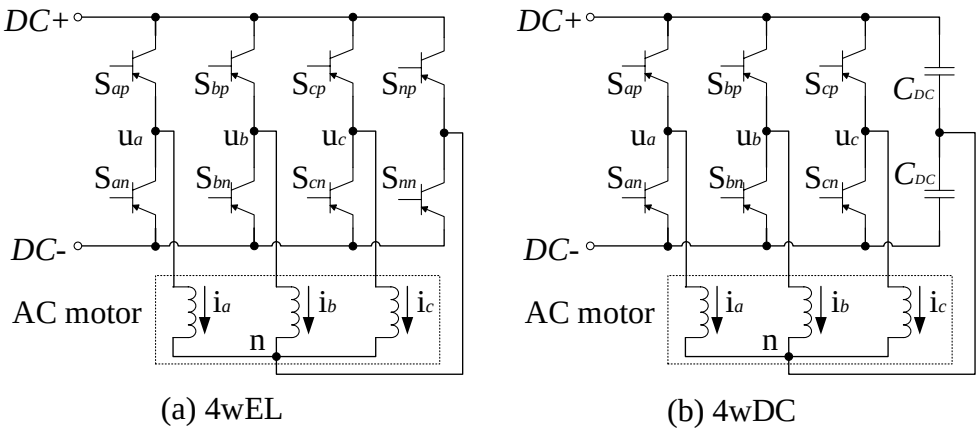


Figure 2.26: Three-phase four-wire drive topologies.

2.4 High-frequency Modelling of Electric Drive System

High-frequency modelling of the electric drive system is playing a significant role in predicting the conducted EMI resulted phenomenons with an acceptable accuracy. With the help of a model with sufficient accuracy, it is able to analyze the production and transmission of CM current theoretically and in numerical simulation as well.

However, it is always very difficult to identify the high-frequency parameters of ac motors. For the conventional modelling method that is based on the analysis of the physical characteristics of the drive system, it works fine in the low-frequency range as the relevant characteristics are not complicated. As the frequency increases, parasitic effects become as significant as the isolation thickness, layout of the windings and connection wires, etc., which leads to many resonances occurring in the motor impedance curve. This creates great difficulties for catching all physical characteristics that dominates the motor impedance. Thus additional tools are required in this high-frequency case.

Finite element (FE) method is used as one solution. Specifically, a high frequency phase variable model is built by developing and adding a high frequency branch to the low frequency phase variable model [53]. The high frequency branch enables the current penetration into the winding with frequency to be modeled while low frequency phase

variable model captures the dynamics of the low frequency. Parameters of the high frequency winding branch are determined from the FE solutions. This includes resistance and inductance of each individual turn of the whole winding as well as the capacitance between turns to ground and turn to turn. The technical details for parameter calculation, lumping of the distributed model and the formation of the physical phase variable model are also proposed and verified experimentally [54]. The model can be used for setting edge rates, selecting switching algorithms and predicting overvoltage at terminals.

Another solution is the experimental method. To identify the required model parameters, firstly, the phase-to ground and the phase-to-neutral motor impedance has to be measured in the form of frequency response by the Impedance Analyzer. Then, based on the least-squares data fitting method performed in complex domain, the parameters of an HF equivalent circuit can be identified [55]. This experimental method had been verified experimentally on different types of electric machine with a wide range of power level, which leads to the its availability of application not dependent on the ac motor types.

Based on the experimental method, the model of motor winding is decomposed into CM impedance (Z_{cm}, identified through phase-to-ground impedance) and DM impedance (Z_{dm}, identified through phase-to-neutral impedance). For the modelling of an intact motor winding, both CM and DM impedance are required in a unified equivalent circuit with the impedance conversion, as shown below:

$$Z_{DM} = \frac{12Z_{cm}Z_{dm} - 3Z_{dm}^2}{4Z_{cm} - 2Z_{dm}} \tag{2.2a}$$

$$Z_{CM} = \frac{12Z_{cm} - 3Z_{dm}}{2} \tag{2.2b}$$

And the obtained impedance network for each motor winding is shown in Fig. 2.27.

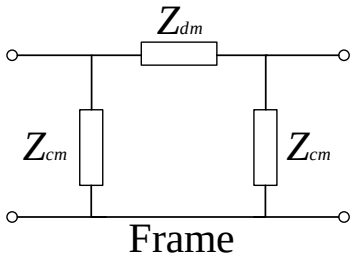


Figure 2.27: High-frequency model of the Motor winding.

For the modelling of power cables, it is well known that the use of distributed-parameter results in more accurate representation in the study of high-frequency transients than the lumped-parameter models [56]. But for the analysis of overvoltage phenomenon, the lumped-parameter representation of the transmission line with adequate segments is the optimal, especially for drive systems with very long cable. Thus a multiple segment lumped-parameter model is proposed in [57], for the accurate CM disturbance analysis of

power cable, as shown in Fig. 2.28. Specifically, the cable parameters are estimated through by checking the frequency response of the cable characteristic impedance experimentally. Both of short- and open-circuit impedance needs to be measure by a impedance analyzer. To be mentioned, in Fig. 2.28, the impedance of cable can be further classified as the cable CM impedance (Z_{Lcm}) and DM impedance (Z_{Ldm}), for the covenient analysis in the following sections.

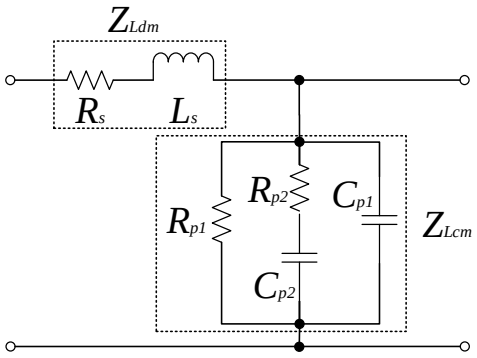


Figure 2.28: High-frequency per-unit length model of the power cable.

2.5 Summary

This chapter has presented the overview of CMCRT developed in the last decades and the state-of-art solutions in terms of filter design and PWM optimization. Meanwhile, the overview of advantages using three-phase four-wire drive system has also been illustrated in two main fields, self-sensing control and fault tolerant operation.

Until now, CMCRT based on filter design still suffers problems. For passive filters, the effective range of frequency for filtering is still limited due to the consideration of less bulky filter topology and insertion power losses. For active filter, its operational stability is still challenged, which hinters its application in commercial or industrial situations.

Advance PWM techniques have already been widely studied and proved to have great potential in further developing CMCRT. However, due to the fast development of power electronic devices and further application of electric drive system in aerospace, cruise and electric vehicle, the studies of the influence of the advanced PWM should be updated frequently. Besides, for a deeper study of advance PWM techniques, the combination of two or more of them for obtaining more and more advantages brought by each PWM algorithm has to be considered seriously.

Moreover, the three-phase four-wire topology has already shown its unique advantage in improving the general performance of the electric drive system. The further development of the four-wire topology based technology, like self-sensing control and fault tolerant operation, will also call for the research of CM disturbance in this topology.

Lastly, modeling methods that enable the accurate representation of the electric drive system (Motor and power cable only), have been reviewed. These models provide possibilities of both theoretical and simulation analysis of the conducted EMI problems in all kinds of EDSs.

3 Research Methodology

This chapter illustrates the research methodology used in the thesis. Firstly, the theoretical analysis of CM current flowing across the conventional three-phase electric drive system, as well as the three-phase four-wire drive system , will be given. It involves high-frequency lumped model of the power cable and electric machine, and the detailed deduction of analytical expression of CM current. In addition, experimental setup that includes two practical electric drive system will be described. Specifically, one of them is driven by a 2.2 kW PMSM, while the other is used as the prototype for driving an electric vehicle with a larger PMSM at 60 kW.

3.1 Theoretical Analysis

3.1.1 Transfer function approach for three-wire EDSs

The negative influences caused by the PWM switch-mode inverters on EDSs can be concluded as two main aspects:

- High values of phase/line voltage rise times at the motor terminals result in the failure of the motor winding isolation;
- High values of CM voltage rise times cause capacitive coupling effects in the motor, leading to motor bearing failures.

These two aspects well explain the production of CM current in the EDS. On one hand, the CM current originates from the large phase voltage rise during the transition of inverter branches, on the other hand, the resulted CM current reaches motor through the capacitive coupling due to large du/dt. Thus the equation of CM current for the three-phase EDS can be obtained:

$$I_{CM} = C_L \frac{dU_{tot}}{dt} + C_M \frac{dU_{nN}}{dt} + I_{other} \tag{3.1a}$$

$$U_{tot} = U_{UN} + U_{VN} + U_{WN} \tag{3.1b}$$

where C_L is the parasitic capacitance between power cable and ground, while C_M is that between motor and ground; U_{tot} is the sum of three phase voltages U_{UN}, U_{VN}, U_{WN}, also known as the cable input voltage; U_{nN} is the neutral voltage; I_{other} represents the CM current from other sources (incomparable with the two main sources). To be mentioned, the voltages refer to the points U, V, W, N and n as shown in the circuit of Fig. 3.1.

From (3.1) it can be known that the theoretical expression of neutral and phase voltage in relevant cases is required for the analysis of CM current. Fig. 3.1 shows the equivalent circuit of a conventional three-wire inverter-fed EDS. To be mentioned, considering that this study is focused on the application in EV, so the power cables are short and the DC-source (battery) is left floating for all EDSs. However, there exists considerable high capacitive couplings (stray capacitance C_{DC}) from battery and inverter to ground, which is also much higher than the capacitive couplings from electric machine to ground. The power cable and three-phase electric machine are represented by the high-frequency model as proposed in [55] and [57], respectively. Z_{Lcm}/Z_{Ldm} and Z_{Mcm}/Z_{Mdm} represents the CM/DM equivalent impedance of the cable and motor, respectively. For this conventional topology, the theoretical expression of neutral and cable input voltage in Laplace domain is known as:

$$U_{tot3w}(s) = U_{UN}(s) + U_{VN}(s) + U_{WN}(s) \tag{3.2}$$

$$U_{nN3w}(s) = \frac{U_{tot3w}(s)}{3} \tag{3.3}$$

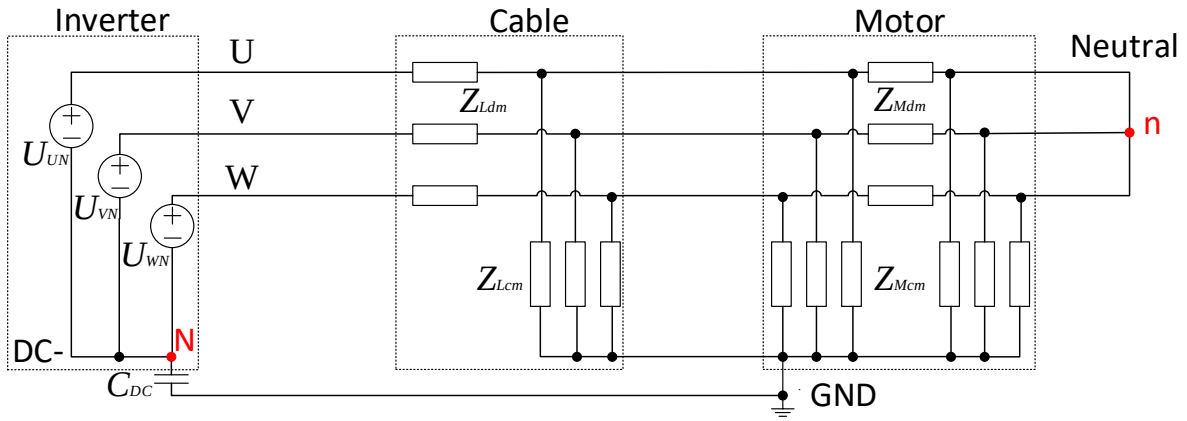


Figure 3.1: High-frequency equivalent circuit of the conventional three-wire inverter-fed EDS.

3.1.2 Transfer function approach for four-wire EDSs

As an extension of conventional three-wire EDSs, the equivalent circuit of four-wire inverter-fed EDSs 4wDC and 4wEL is shown in Fig. 3.2 and 3.3, respectively. To be mentioned, in Fig. 3.2, to make the neutral current flowing in 4wDC under the accepted level (usually 1 % of the rated current), a neutral capacitance C_{nN} has to be placed on the neutral line (the fourth wire), except for the fault tolerant topology, where it is connected directly.

For the analysis of neutral and cable input voltage of 4wDC and 4wEL, the intact topology shown in Fig. 3.2 and 3.3 has to be simplified firstly. It is widely known that

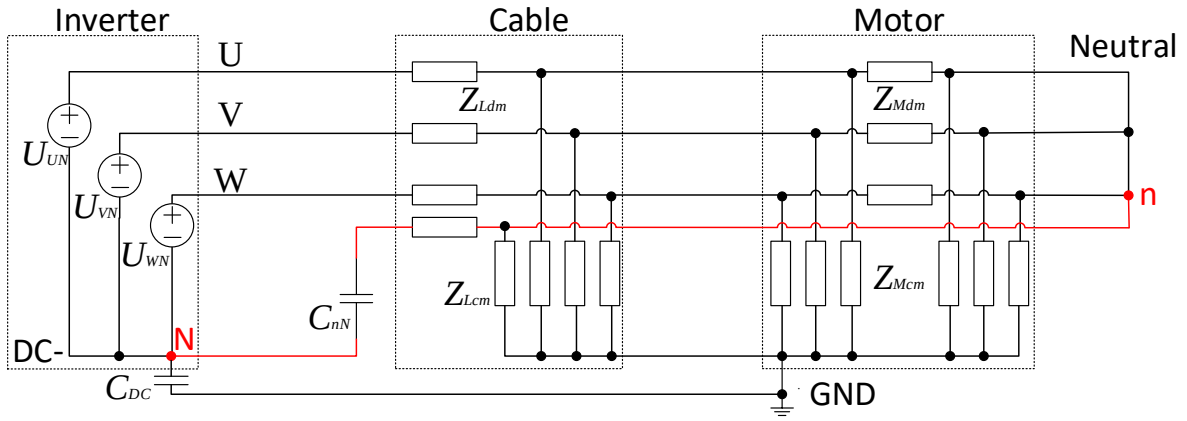


Figure 3.2: High-frequency equivalent circuit of 4wDC.

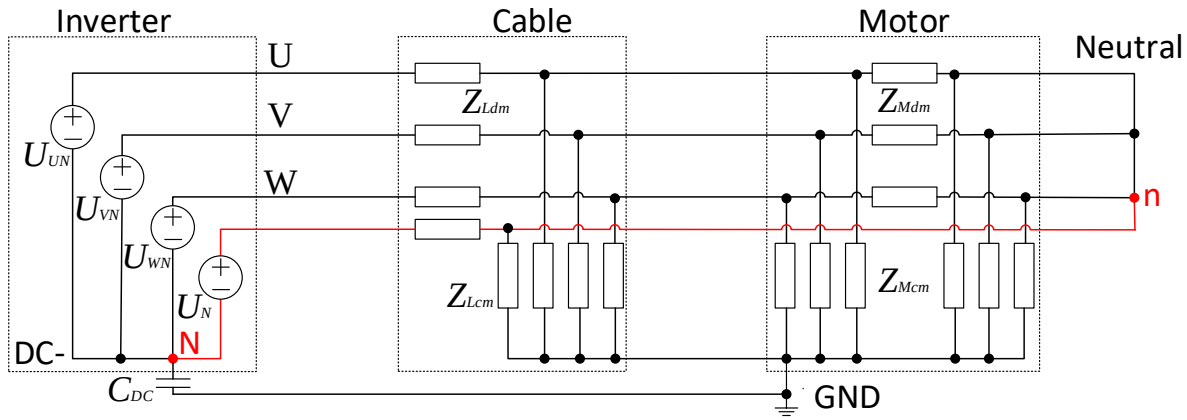


Figure 3.3: High-frequency equivalent circuit of 4wEL.

for power cables and motors, the CM impedance always has much larger magnitude than the DM impedance for the frequency range of interest. This enables the neglection of the effects of Z_{Lcm} and Z_{Mcm}, for a simplified topology of 4wDC and 4wEL as shown in Fig. 3.4.

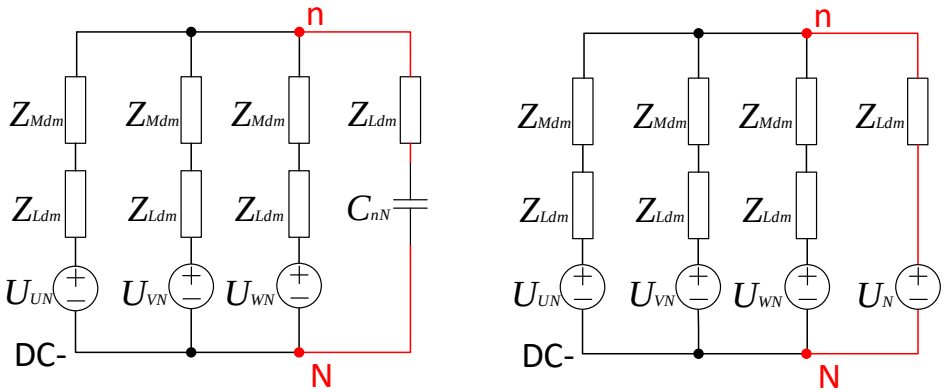


Figure 3.4: Simplified topology of: (a) 4wDC; (b) 4wEL.

According to the simplified topology, along with superposition theory, the corresponding theoretical expression of neutral and cable input voltage for 4wDC and 4wEL can be obtained as:

$$U_{tot4wDC}(s) = U_{UN}(s) + U_{VN}(s) + U_{WN}(s) \tag{3.4}$$

$$U_{tot4wEL}(s) = U_{UN}(s) + U_{VN}(s) + U_{WN}(s) + U_N(s) \tag{3.5}$$

$$U_{nN4wDC}(s) = \frac{3Z_{2DC}}{Z_{1DC} + 3Z_{2DC}} \frac{U_{tot4wDC}(s)}{3} \tag{3.6}$$

$$U_{nN4wEL}(s) = \frac{3Z_{2EL}}{Z_{1EL} + 3Z_{2EL}} \frac{U_{tot4wEL}(s)}{3} + \frac{Z_{1EL} - Z_{2EL}}{Z_{1EL} + 3Z_{2EL}} U_N(s) \tag{3.7}$$

$$Z_{1DC} = Z_{1EL} = Z_{Ldm}(s) + Z_{Mdm}(s) \tag{3.8}$$

$$Z_{2DC} = Z_{Ldm}(s) + \frac{1}{sC_{nN}} \tag{3.9}$$

$$Z_{2EL} = Z_{Ldm}(s) \tag{3.10}$$

where Z_{1DC} and Z_{1EL} represents the impedance between the inverter output and the neutral point of 4wDC and 4wEL, respectively, while Z_{2DC} and Z_{2EL} the impedance from the neutral point to the mid of dc-link; U_N is the voltage source on the neutral line caused by the fourth IGBT leg in 4wEL.

According to (3.4), (3.5), (3.6) and (3.7), it can be known that the neutral and cable voltage rise is dominated by two factors, one is the impedance at both side of neutral point, the other is the phase and neutral voltages originates from PWM switch actions. This leads to two possibilities of reducing CM current, inserting filter topologies to one or both side of the motor neutral point, and modifying the PWM algorithm. The more detailed discussion will be presented in following chapters.

3.2 Experimental setup

Based on the requirement of studying the characteristics of the CM current in a practical EDS, as well as the experimental validation and implementation of the theoretical research result, two test benches are used for this thesis. Specifically, one consists of a EDS driven by a 2.2 kW PMSM, while the other involves a EDS with a 60 kW PMSM (This is a prototype EDS used for the traction of an electric vehicle). A detailed description of these two EDSs will be given in this section.

3.2.1 EDS with 2.2 kW PMSM

This EDS consists of traction and load machine, inverters for both machines, and a self-developed controller board. Each part of the EDS will be described in details in the following.

Traction and load machines

The traction machine is a PMSM, G465-204, manufactured by MOOG, used as servo drive in tooling machines or other industrial automation systems. A special winding is applied for its outstanding performance and high power density. This PMSM enables direct connection from the drives to primary mains without additional system cost. The load machine is a 3.6 kW PMSM manufactured by ESR. The specific parameters of both machine are shown in Table. 3.1 and 3.2 , respectively. Besides, the picture of both machines in the test bench is shown in Fig. 3.5.

Table 3.1: Rated parameters of the traction machine.

P [kW]	U [V]	n [min^{-1}]	I [A]	T [Nm]
2.2	630	8000	5	5.8

Table 3.2: Rated parameters of the load machine.

P [kW]	U [V]	n [min^{-1}]	I [A]	T [Nm]
3.6	400	3000	10.6	13

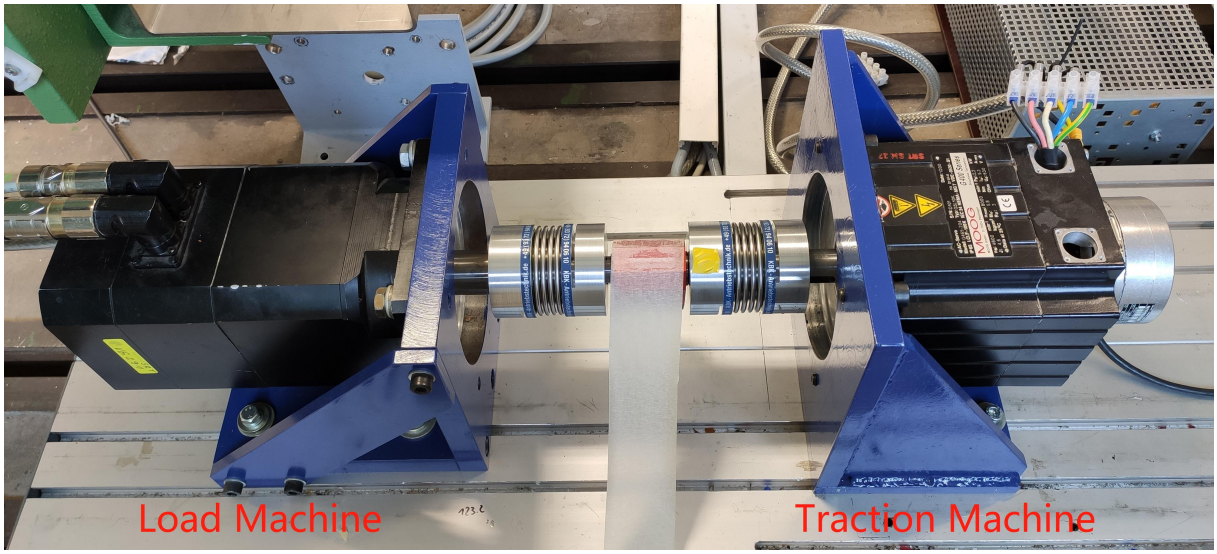


Figure 3.5: Traction (right) and Load machine (left) in the test bench.

Inverters

This test bench includes two same type of inverters for the drive of the traction machine. Both of them are manufactured by GUASCH, as shown in Fig. 3.6. They are used in two power topologies. When the triggering action requires maximal three IGBT bridges, only one of the two inverters will be used. But if more than three IGBT bridges are required,

like the control of the three-phase four-wire topology 4wEL, both of the two inverters should be used. During the "double-inverter" operation, both inverters share identical control and measuring signals, as well as the power supply.

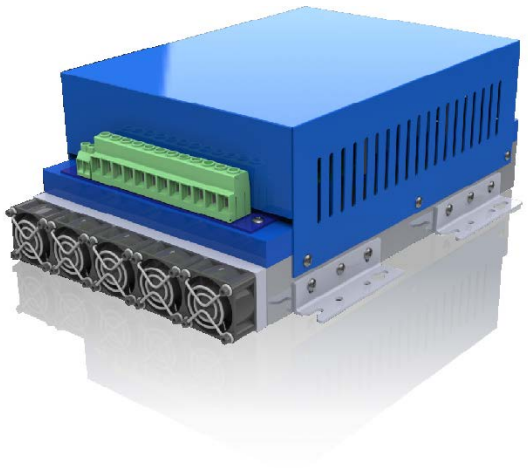


Figure 3.6: Inverter for the drive of Traction machine.

The inverter is included in the power stack MTL-CBI0060F12IXHF, which also contains a braking chopper, a heatsink, the optocoupled gate-drivers, output phase current sensors, DC-Link voltage sensors and module temperature. This MT series power stack is suitable to realize converters, choppers, half, full or three phase bridge inverters for motor control, welding, renewable energies, UPS, etc.

Controller board

The self-developed controller board is used for the adaptation of control and measuring signals of inverters to the microcontroller. On one hand, it sends out action signal to the IGBT bridges for the drive of the traction and load machine; On the other hand, it receives and processes all kinds of measuring signals from the inverters and machines for a better control of the whole EDS. The core part of the controller board is the microcontroller of Type TMS320F28069, namely DSP, manufacured by Texas Institute. The controller board and relevant development document are shown in Fig. 3.7. This board is designed to be capable of driving two three-phase inverters and even two electric machines in the meantime, and thus it contains two pairs of interfaces for receiving and sending signals of encoder, voltage and current sensor, etc.

3.2.2 EDS with 60 kW PMSM

Similar to the EDS with 2.2 kW PMSM, the EDS presented in this section also involves components like traction and load machine, inverters for the machines, as well as a self-developed controller board. Due to the higher power level of the machines, all the

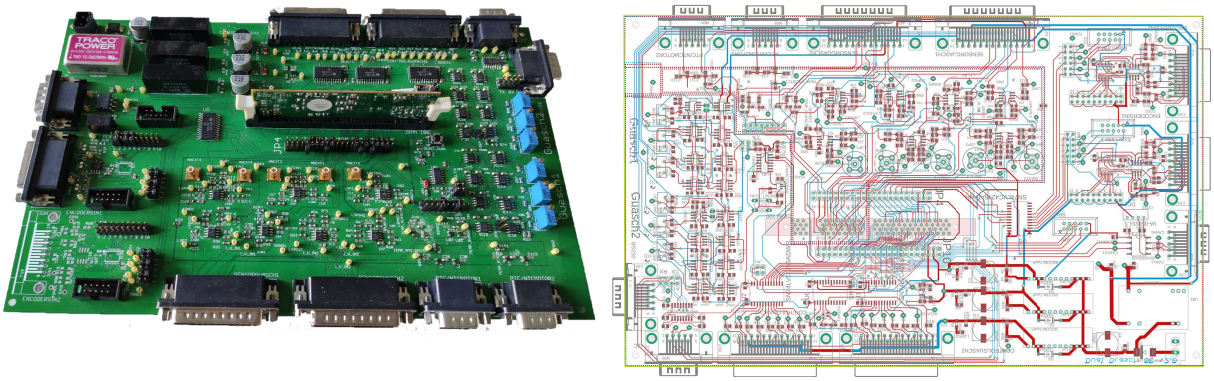


Figure 3.7: Seld-developed controller board and the development document in BRD form.

components are selected to stand higher voltage and current. Each part of the EDS will be described as follows.

Traction and load machines

The traction machine is a self-designed PMSM for the traction of an electric vehicle. This machine uses concentrated winding to obtain a larger power density, and lower the manufacturing cost in the meantime. With the optimization of some design parameter, this machine also enables self-sensing control with high accuracy. The load machine is a 75 kW induction machine manufactured by SIEMENS. The specific parameters of both machine are shown in Table. 3.3 and 3.4 , respectively. Besides, the picture of both machines in the test bench is shown in Fig. 3.8. To be mentioned, the traction machine in this experimental setup has a lower rated voltage due to the voltage limit of the used faster switching components (GaN) in other converters of the drive system.

Table 3.3: Rated parameters of the traction machine.

P [kW]	U [V]	n [min^{-1}]	I [A]	T [Nm]
60	380	2998	300	1000

Table 3.4: Rated parameters of the load machine).

P [kW]	U [V]	n [min^{-1}]	I [A]	T [Nm]
75	380	1500	143	1000

Inverters

This test bench includes two inverters, one for the drive of the traction machine, while the other for the load machine, as shown in Fig. 3.9. Both of them are manufactured by

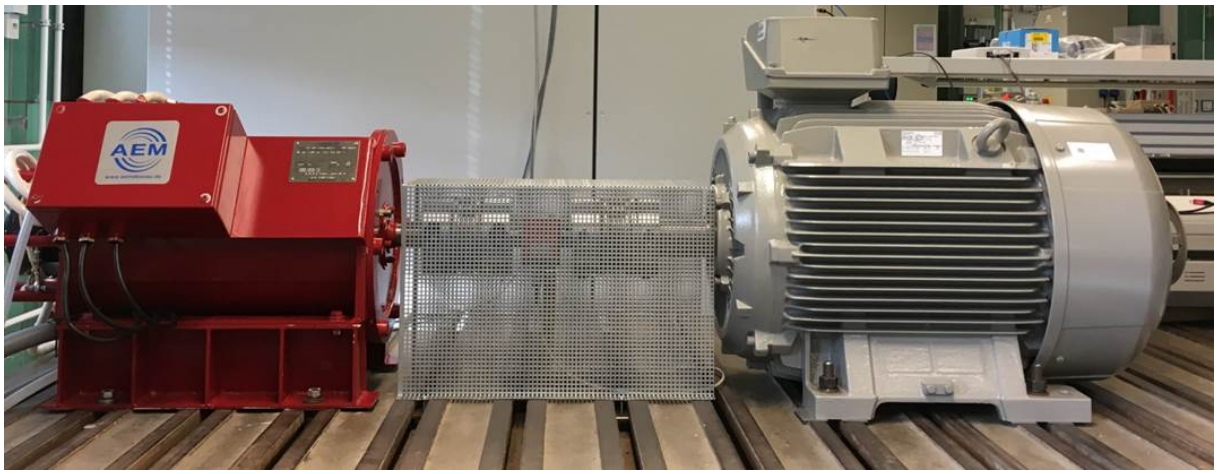


Figure 3.8: Traction (left) and Load machine (right) in the test bench.

SEMIKRON. During the operation, both inverters share identical control and measuring signals. Besides, they have own hardware safety circuits and can fulfill the operation requirement of both machines.

Figure 3.9: Inverter for the drive of traction and load machine.

SEMIKRON CUBE is chosen as the inverter used for both traction and load machine. It can work with the DC power supply up to 600 V and allow the flowing current til 300 A. It is able to supply continuous power of 65 kW at the switching frequency of 4 kHz. By supplying lower value of power, the switching frequency can reach its maximum, 16 kHz.

Both inverters are safely shielded and grounded in an electric cabinet as shown in Fig. 3.10.

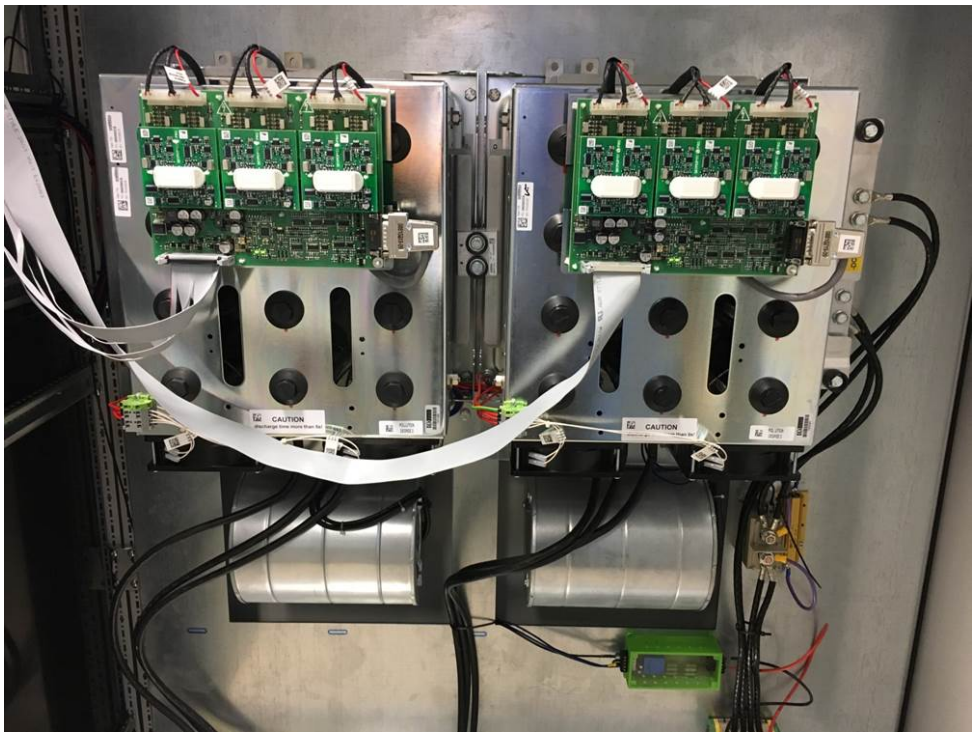


Figure 3.10: Inverters in the electric cabinet with necessary shield and ground.

Controller board

Similar to the controller board described in Section 3.2.1, another self-developed controller board is used for this experimental setup. The main difference of this board is that this setup only needs to drive one machine, thus there exists less port on it as compared with the former one. The controller board and relevant development document are shown in Fig. 3.11.

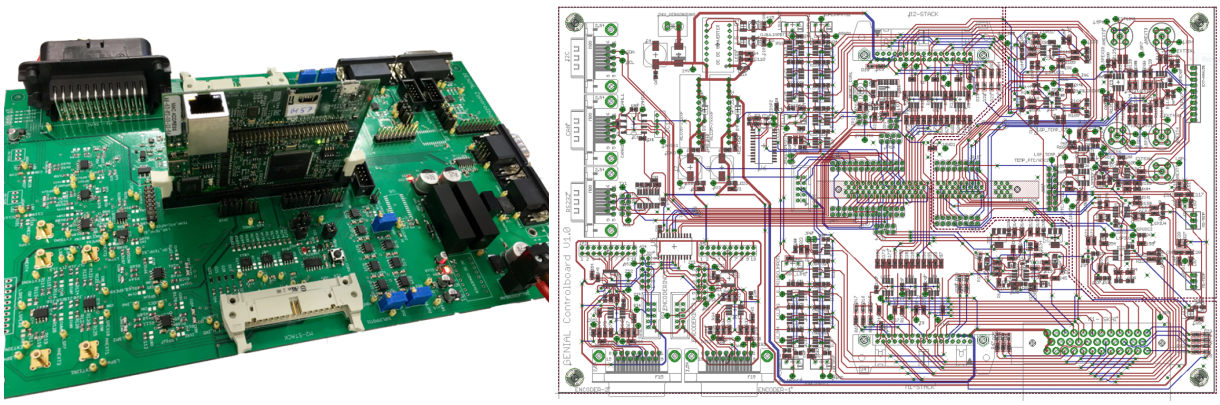


Figure 3.11: Seld-developed controller board and the development document in BRD form.

3.2.3 Software Architecture

As indicated earlier, the self-developed controller board with the microcontroller (DSP) has been used for a flexible and expandable control. Thus the main tasks of the DSP are PWM generation. SV-PWM is used as the original PWM technique applied in the EDSs of this thesis.

For the DSP manufactured by TI, Code Composer was the software running on the host PC used for programming and debugging. The DSP was running a field-oriented control (FOC) algorithm [58], where the reference values were supplied though the host PC. The latter was also used for logging variables from the control algorithm. For the present research, the relevant part of the FOC was the PWM implementation, which can be summarized as follows [59].

The switching period is generated by an up/down counter in the Time-Base Submodule, which can be configured through proper arrangement of relevant registers. At the end of each period an interrupt is generated, which triggers the control algorithm. The control algorithm has to return the new switching times before the beginning of the next period. The value in the up/down counter is compared with the switching times computed in the previous interrupt, in order to obtain the transition instant of the output. This is performed in the Counter-Compare Submodule. The action-qualifier module turns the gate signals on or off based on the comparison results. Afterwards, the Dead-Band Generator Submodule will add programmable delay to rising or falling edges, or both, to avoid the problematic situations that both IGBTs on the same bridge are at "on" state at the same time. When these procedures finish, the interrupt ends and the control signal starts to order the action of inverters.

The different PWM strategies are implemented by the computation of the switching times, period time, and action-qualifier configuration, which can be updated in the control algorithm at each interrupt. It has to be mentioned that, the programmed code should be simple and effective, otherwise, the interrupt may take too long time. This may result in the situation that the action signal already misses the expected sending time and cannot realize wanted actions before next switching period.

3.2.4 CM current measurement setup

For the CM current measurement, there exists a bit difference between the three- and four-wire drive topology. As can be seen in Fig. 3.12, for three-wire drives, the CM current equals to the sum of three phase currents, while for four-wire drives, the neutral current should also be included due to its connection between the neutral and the dc-bus. The used current sensor is the A6303 (manufactured by Tektronix), able to measure up to 15MHz, enough for the CM current measurement. The measured signal will firstly be amplified (AM 503 from Tektronix) and then presented and saved by the oscilloscope

(RTB2004 from ROHDE & SCHWARZ, bandwidth 200 MHz, sampling rate of 2.5 GSa/s).

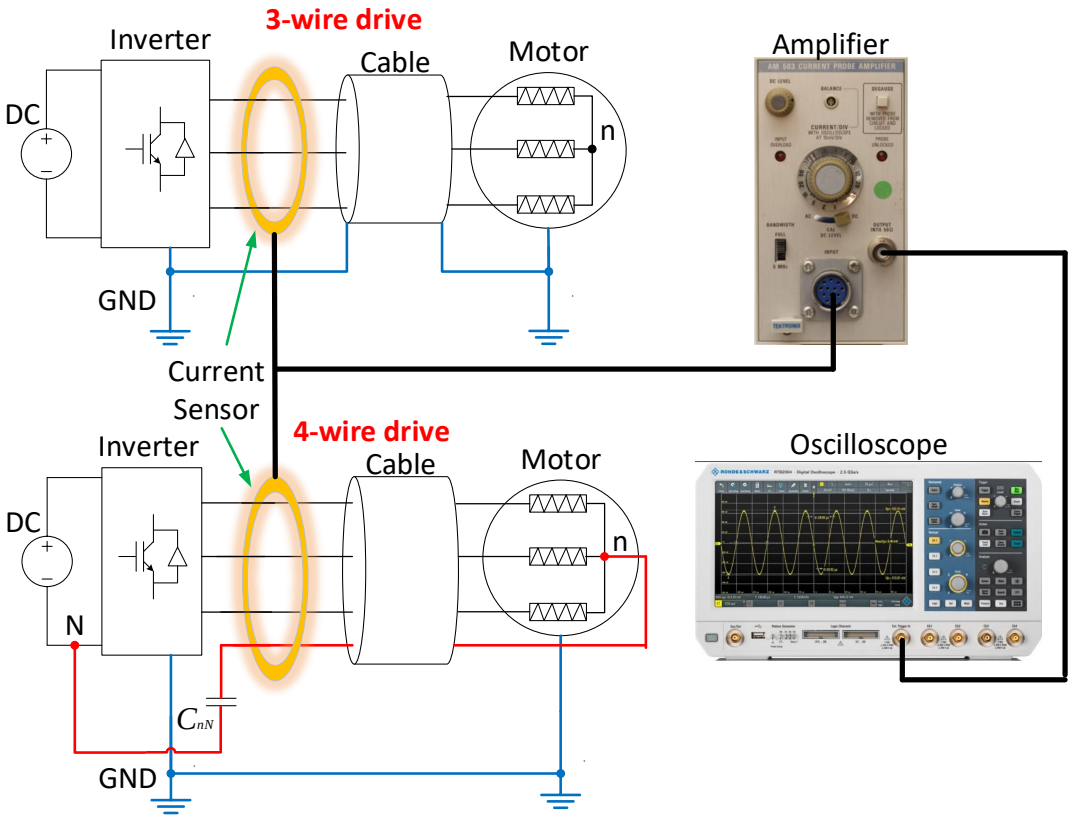


Figure 3.12: CM current measurement setup for three- and four-wire drive topologies.

3.3 Summary

This chapter has presented the research methodology applied in the dissertation, which would lead to a better understanding of the following chapters. The transfer function used for analyzing the source and coupling route of CM current in various EDSs were introduced firstly. Unlike conventional three-wire EDSs, for four-wire EDSs, the impedance between the inverter output and the neutral point and from the neutral point to the mid of dc-link can also directly influence the CM current. This characteristic showed the potential of three-phase four-wire EDSs in further reducing CM current. Furthermore, the experimental setups for the validation of the theoretical results in the subsequent chapters were illustrated specifically, along with the corresponding software architecture.

4 Optimization of PWM

In this chapter, two novel advanced PWM techniques are proposed to limit the CM disturbance in the EDS. In the first section, the fundamental theory for the realization of Hybrid PS-PWM (HPS-PWM) and Variable Switching Frequency (VSF-PWM) in a conventional three-phase EDS is described in detail. Then the application of these advanced PWM techniques in the four-wire topology 4wDC and 4wEL is presented in the second and third section, respectively. Specifically, the modifications required for the application of HPS-PWM and VSF-PWM in the four-wire EDS are explained, along with the system improvement due to the reduction of the CM disturbance. Besides, a new type of advanced PWM, which combine both HPS-PWM and VSF-PWM, is proposed and proved to be effective to further restrict the CM current in a wide range of frequency.

4.1 Theoretical analysis of advanced PWM technique

4.1.1 Fundamental theory of HPS-PWM

In [36], it has been indicated that shifting 180 degree of the phase with the longest (AZS-PWM1), shortest (AZS-PWM2) or mid (AZS-PWM3) length of the IGBT triggering time can reduce the peak of CM voltage from half to one-sixth of the DC voltage (seen in Fig. 2.15-2.17). And AZS-PWM3 is the optimal as the dead-time effects does not bring in unexpected CM voltage spikes as the other two types of AZS-PWM.

However, when applying AZS-PWM in the practical drive system, the reference vector fluctuates seriously when it approaches the sector boundary, resulting in that the phase-shift action cannot be completed smoothly when the reference vector moves from one sector to the next. Thus HPS-PWM is proposed for the first time, which can not only reduce the peak of CM voltage, but also maintain the operation stability of drive systems. Specifically, HPS-PWM performs as AZS-PWM3 in sector 1 and 4, while as AZS-PWM1 and AZS-PWM2 in sector 2, 3 and 5, 6, respectively (Fig. 4.1). For the realization of HPS-PWM in the practical application, only phase V requires to be shifted all the way around, which makes the phase shift action smoothly.

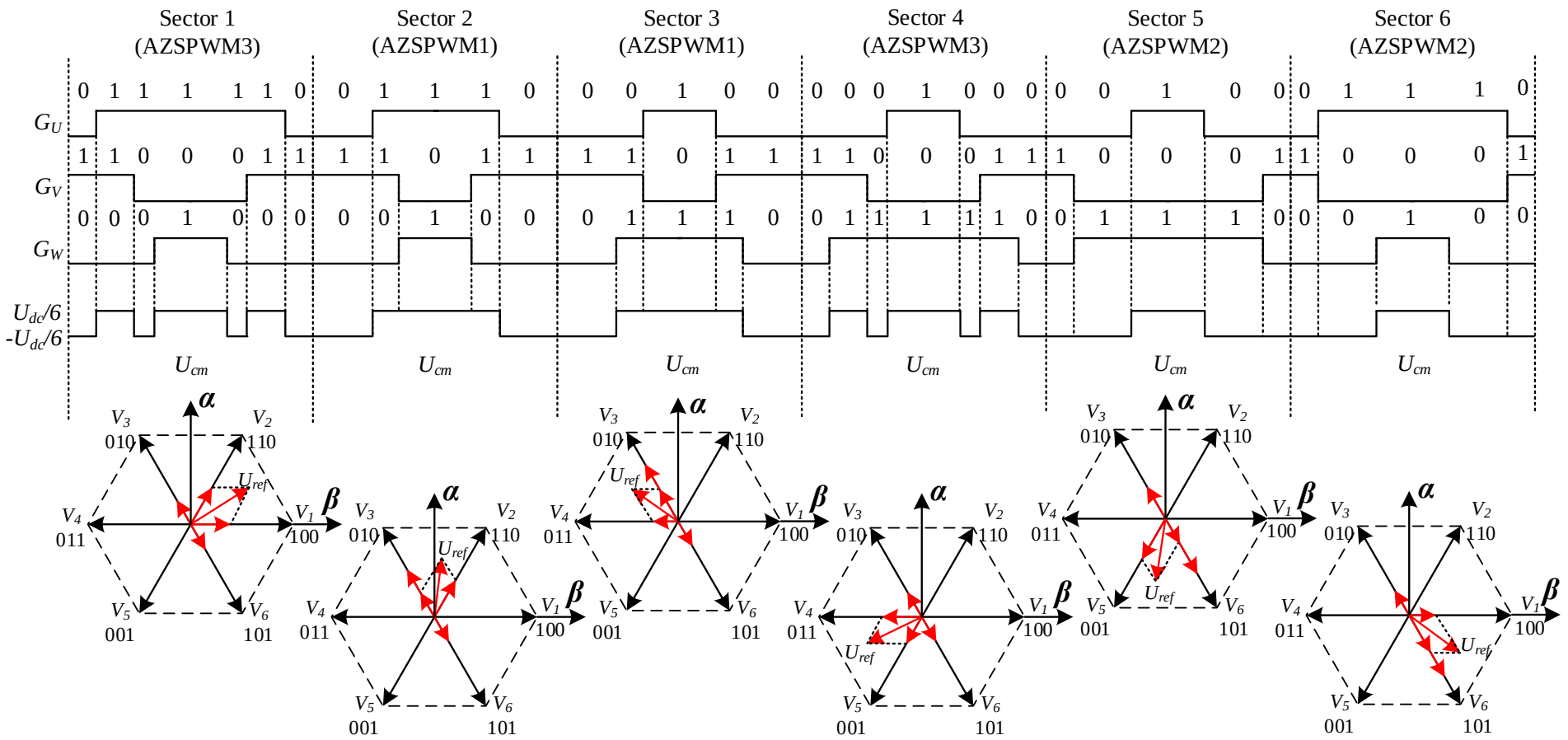


Figure 4.1: Proposed HPS-PWM with vector distribution in each sector.

It can be known from [36] that when HPS-PWM is applied, unexpected voltage errors will occur in sector 2, 3 and 5, 6 as it performs as same as AZS-PWM1 and AZS-PWM2, respectively. From the viewpoint of this thesis, it is a deserved compromise to the system stability. However, these unexpected voltage spikes can be largely mitigated through proper set of dead-time control strategy. As an example shown in Fig. 4.2, the unexpected voltage spikes reduce from $U_{dc}/2$ to $U_{dc}/6$ due to the optimization of the dead-band setting.

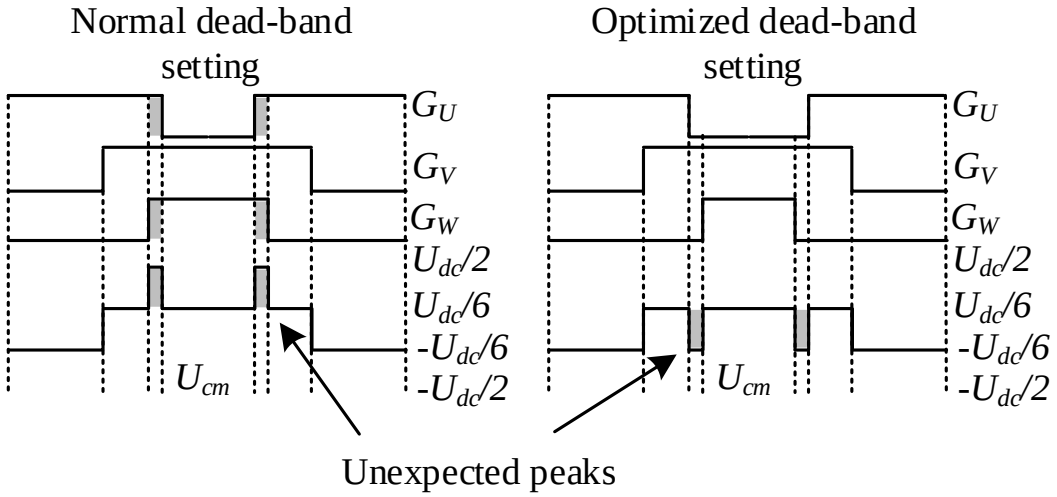


Figure 4.2: Dead-band optimization for the reduction of unexpected voltage error.

4.1.2 Fundamental theory of VSF-PWM

It is known from [30] that the first step of realizing the VSF-PWM in conventional three-wire EDSs is the prediction of current ripple. It is said that through the identification of the ripple current slope for each vector of a PWM, the peak value of the current ripple on each of the three phases can be obtained. Comparing the peak value of each phase and finding out the maximum, then the maximum is absolutely the peak of the current ripple in this switching period. In this section, the presentation of this prediction procedure will be more specific than in [30] for the analysis of the calculation effort of the microcontroller during the interrupt.

Based on the Thevenin equivalent circuit corresponds to each vector of SV-PWM (Fig. 4.3), the ripple current slope of phase U for each vector is presented in [30], as shown in Table. 4.1. To be mentioned, d_U, d_V, d_W are the duty cycles of the three phases ranging from 0 to 1, U_{dc} is the dc bus voltage, L represents the output inductance on each phase and k_U is the ripple current slope of phase U.

According to Table. 4.1, the current ripple on the phase U in one switching period can be obtained. Using Sector I as an example, the relevant current ripple curve can be seen in Fig. 4.4.

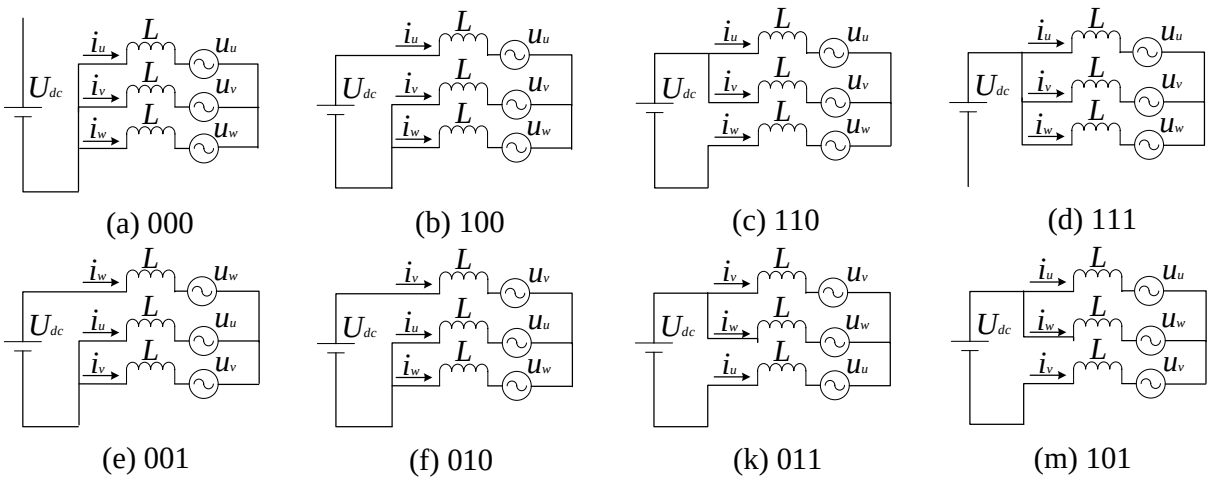


Figure 4.3: Equivalent circuit of switching combination of each vector.

Table 4.1: Eight switching vectors and the correspondent ripple current slope (Phase U).

Vector	Ripple Current Slope	Vector	Ripple Current Slope
000	$k_{U0} = \frac{U_{dc}}{3L}(d_V + d_W - 2d_U)$	011	$k_{U4} = \frac{U_{dc}}{3L}(d_V + d_W - 2d_U - 2)$
100	$k_{U1} = \frac{U_{dc}}{3L}(d_V + d_W - 2d_U + 2)$	001	$k_{U5} = \frac{U_{dc}}{3L}(d_V + d_W - 2d_U - 1)$
110	$k_{U2} = \frac{U_{dc}}{3L}(d_V + d_W - 2d_U + 1)$	101	$k_{U6} = \frac{U_{dc}}{3L}(d_V + d_W - 2d_U + 1)$
010	$k_{U3} = \frac{U_{dc}}{3L}(d_V + d_W - 2d_U - 1)$	111	$k_{U7} = \frac{U_{dc}}{3L}(d_V + d_W - 2d_U)$

According to Fig. 4.4, given the value of duty cycle for each switching cycle, the time span for each vector is known. Along with relevant ripple current slope in Table. 4.1, the peak values of the current ripple on phase U can be obtained as:

$$\begin{cases} x_U = k_{U0}\dfrac{t_0}{4} \\ y_U = k_{U0}\dfrac{t_0}{4} + k_{U1}\dfrac{t_1}{2} \\ x_U' = k_{U7}\dfrac{t_0}{4} \end{cases} \tag{4.1}$$

As $k_{U0} = k_{U7}$, the peak of current ripple on phase U in this switching period is $\max(|x_U|, |y_U|)$. Similarly, the ripple current slope of phase V and W can be obtained, as shown in Table. 4.2 and 4.3, respectively. In addition, the current ripple curves of these two phases are shown in Fig. 4.5 and 4.6.Based on this, the peak values of the current ripple on phase V and W in a switching period of Sector I are obtained:

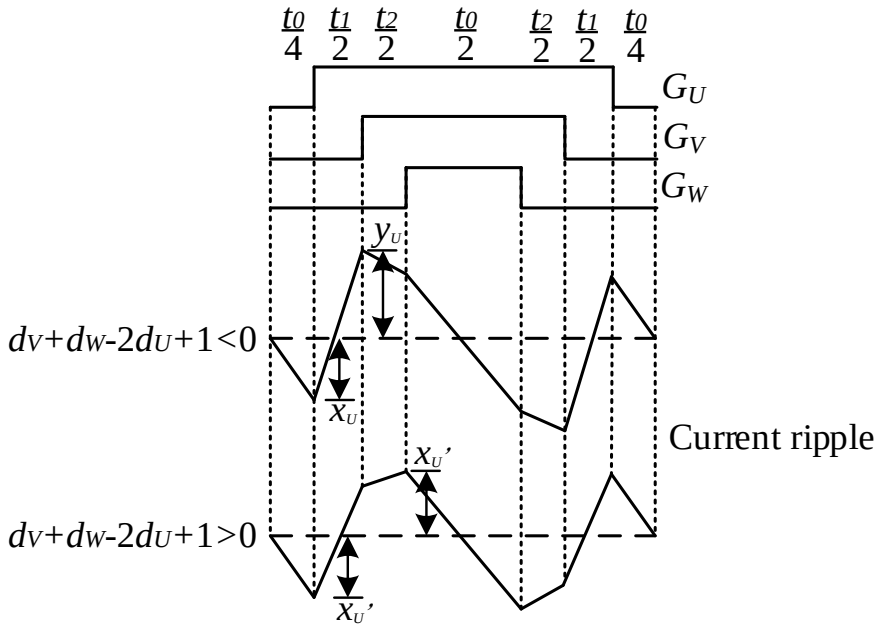


Figure 4.4: Current ripple in a switching period of Sector I (Phase U).

$$\begin{cases} x_V = k_{V7}\dfrac{t_0}{4} \\ y_V = k_{V0}\dfrac{t_0}{4} + k_{V1}\dfrac{t_1}{2} \\ x_V^{'} = k_{V0}\dfrac{t_0}{4} \\ y_V^{'} = k_{V0}\dfrac{t_0}{4} + k_{V1}\dfrac{t_1}{2} \end{cases} \tag{4.2}$$

$$\begin{cases} x_W = k_{W0}\dfrac{t_0}{4} \\ x_W^{'} = k_{W7}\dfrac{t_0}{4} \\ y_W^{'} = k_{W0}\dfrac{t_0}{4} + k_{W1}\dfrac{t_1}{2} \end{cases} \tag{4.3}$$

According to Table. 4.2 and 4.3, it is known that $k_{V0} = k_{V6}$, $k_{W0} = k_{W6}$, therefore the peak of current ripple on phase V and W in this switching period is $\max(|x_V|, |y_V|)$ and $\max(|x_W|, |y_W^{'}|)$, respectively. And so the peak of current ripple at each switching period of Sector I is $\max(|x_U|, |y_U|, |x_V|, |y_V|, |x_W|, |y_W^{'}|)$.

Assuming the original constant switching frequency is f_{sN}, at which the predicted ripple peak is defined as I_{rippl_ori}. When the switching frequency changes to f_s, the corresponding ripple peak is updated to I_{rippl_update}, then we can obtain the relationship between the updated and original ripple peak as:

$$I_{rippl\_update} = I_{rippl\_ori}\frac{f_{sN}}{f_s} \tag{4.4}$$

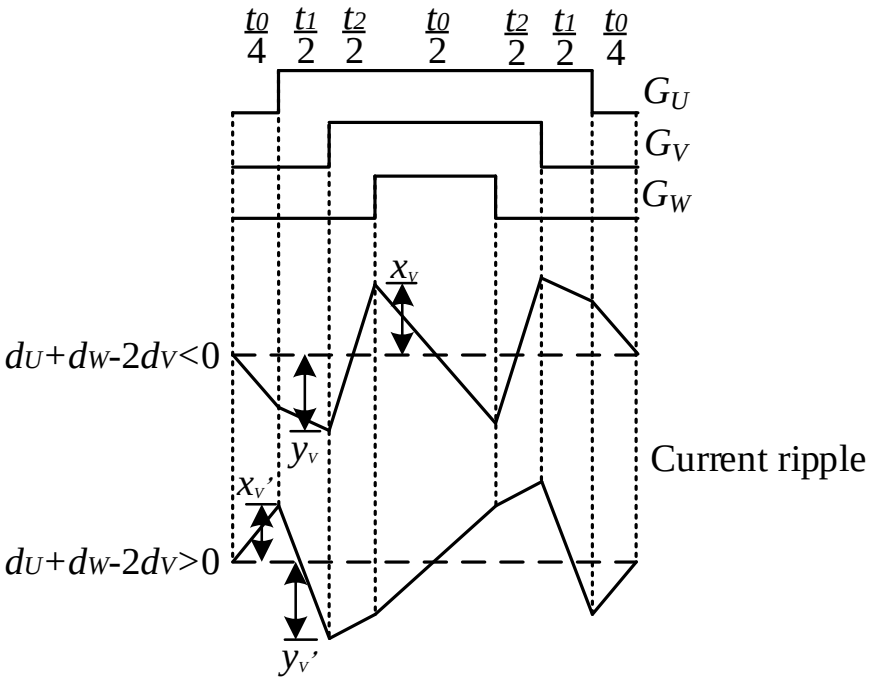


Figure 4.5: Current ripple in a switching period of Sector I (Phase V).

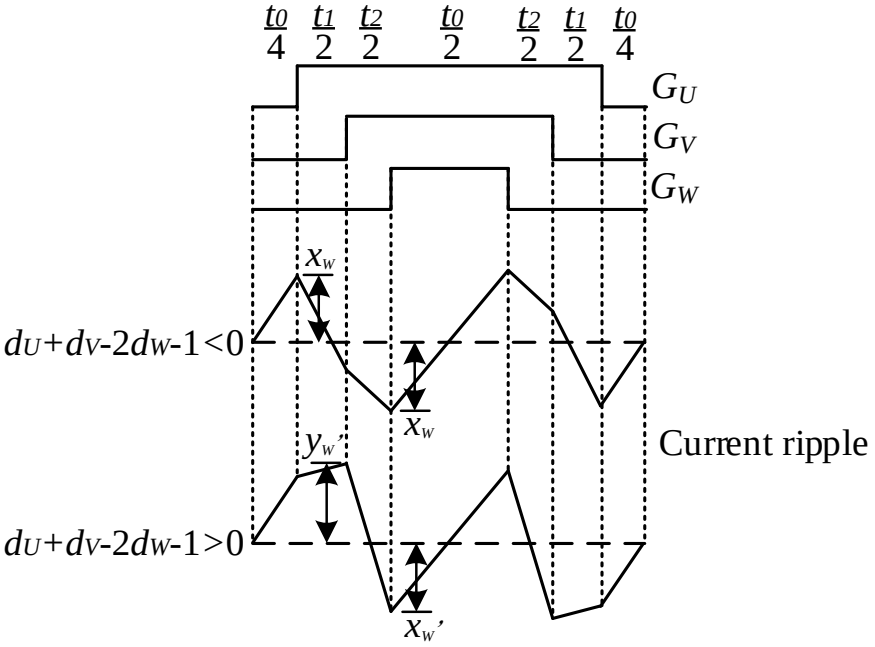


Figure 4.6: Current ripple in a switching period of Sector I (Phase W).

Table 4.2: Eight switching vectors and the correspondent ripple current slope (Phase V).

Vector	Ripple Current Slope	Vector	Ripple Current Slope
000	$k_{V0} = \frac{U_{dc}}{3L}(d_U + d_W - 2d_V)$	011	$k_{V4} = \frac{U_{dc}}{3L}(d_U + d_W - 2d_V + 1)$
100	$k_{V1} = \frac{U_{dc}}{3L}(d_U + d_W - 2d_V - 1)$	001	$k_{V5} = \frac{U_{dc}}{3L}(d_U + d_W - 2d_V - 1)$
110	$k_{V2} = \frac{U_{dc}}{3L}(d_U + d_W - 2d_V + 1)$	101	$k_{V6} = \frac{U_{dc}}{3L}(d_U + d_W - 2d_V - 2)$
010	$k_{V3} = \frac{U_{dc}}{3L}(d_U + d_W - 2d_V + 2)$	111	$k_{V7} = \frac{U_{dc}}{3L}(d_U + d_W - 2d_V)$

Table 4.3: Eight switching vectors and the correspondent ripple current slope (Phase W).

Vector	Ripple Current Slope	Vector	Ripple Current Slope
000	$k_{W0} = \frac{U_{dc}}{3L}(d_U + d_V - 2d_W)$	011	$k_{W4} = \frac{U_{dc}}{3L}(d_U + d_V - 2d_W + 1)$
100	$k_{W1} = \frac{U_{dc}}{3L}(d_U + d_V - 2d_W - 1)$	001	$k_{W5} = \frac{U_{dc}}{3L}(d_U + d_V - 2d_W + 2)$
110	$k_{W2} = \frac{U_{dc}}{3L}(d_U + d_V - 2d_W - 2)$	101	$k_{W6} = \frac{U_{dc}}{3L}(d_U + d_V - 2d_W + 1)$
010	$k_{W3} = \frac{U_{dc}}{3L}(d_U + d_V - 2d_W - 1)$	111	$k_{W7} = \frac{U_{dc}}{3L}(d_U + d_V - 2d_W)$

If the ripple peak of the EDS is required to be under a specific value (defined as $I_{rippl\_require}$), the switching frequency will be kept updating from the original constant frequency according to the expression below:

$$f_s = f_{sN}\frac{I_{rippl\_update}}{I_{rippl\_require}} \tag{4.5}$$

The VSF-PWM generation procedure can be summarized as shown in Fig. 4.7.

4.2 PWM optimization for 4wDC

For the four-wire topology 4wDC, as the electric machine is still powered by the three-phase inverter, and the fourth wire is connected to the mid of dc-link through a capacitor, so the triggering action of inverter is still based on the conventional SV-PWM. Thus to apply the advanced PWM technique for the four-wire topology, it just requires to replace the SV-PWM in the control algorithm with the corresponding PWM technique.

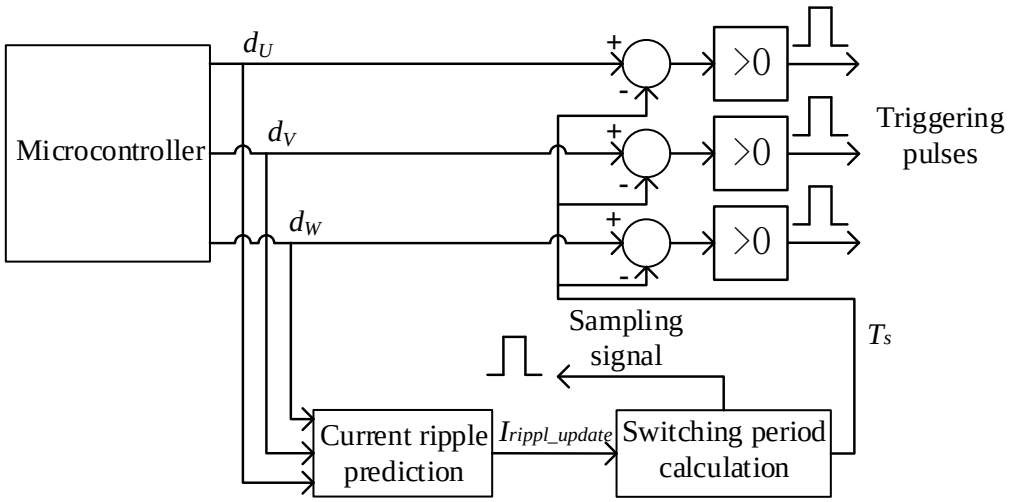


Figure 4.7: Control block diagram of VSF-PWM.

As an example for the application of the advanced PWM techniques, the EDS with a 2.2 kW PMSM is used as the experimental setup, with the neutral capacitance $C_{nN} = 0.027\ u$F. The switching frequency remains at 10 kHz for all measurements. A commercial current sensor (A6303 from Tektronix, further technical details of this equipment is given in the Appendix. A) is utilized for measuring the CM and neutral current. Both of load and no load condition are considered.

4.2.1 HPS-PWM applied in 4wDC

Using the CM current existing in a three-wire drive system, modulated by SV-PWM, as the reference, the CM current under standstill (the worst case, at which the upper or under three IGBTs turn on at the same time, resulting in maximal reachable voltage rise in every switching periods), constant-speed with and without load condition are considered. As a comparison, the CM current flowing across the 4wDC modulated by SV-PWM and HPS-PWM are also measured under the same working conditions, respectively. For a better comparison, the CM current reduction caused by changing the topology to four-wire is also shown. To be mentioned, this value will be positive when the CM current decreases and negative when it increases. All plots mentioned above are shown in the frequency domain, within the frequency range between 1 kHz and 1 MHz as the measured CM current out of this range is much less comparable.

From Fig. 4.8 to 4.10, it can be seen that when the electric machine is at standstill, the CM current flowing across 4wDC reduces significantly from 70 to 200 kHz, and over 400 kHz. While more reduction is obtained in the whole frequency range if HPS-PWM is applied (see in Fig. 4.10). The CM current reduction in 4wDC can be well explained by (3.6), in which the CM voltage is "filtered" by an impedance group resulted from the use of four-wire topology. To be mentioned, there always exists CM current increase for the application of 4wDC between 300 and 450 kHz, and this is caused by the resonance of

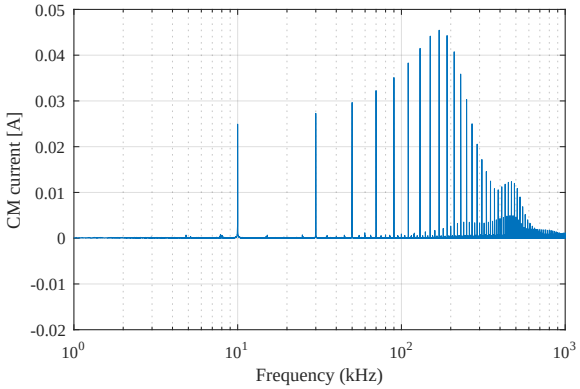


Figure 4.8: Standstill condition: CM current in the three-wire SV-PWM drive system (the reference case).

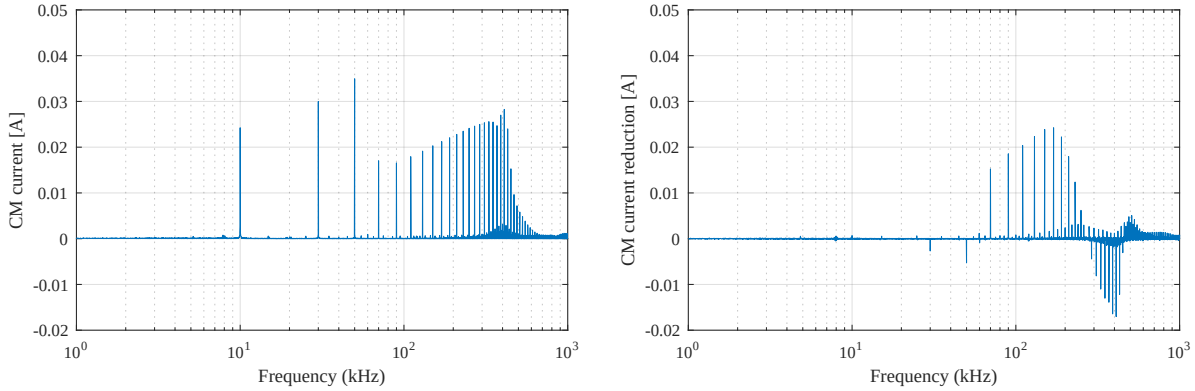


Figure 4.9: Standstill condition in the 4wDC modulated by SV-PWM: CM current (left) and its reduction compared with the reference (right).

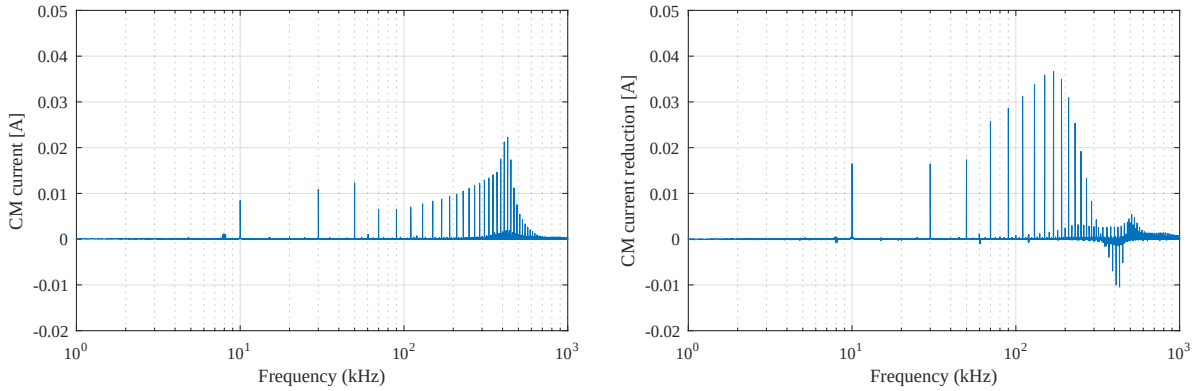


Figure 4.10: Standstill condition in the 4wDC modulated by HPS-PWM: CM current (left) and its reduction compared with the reference (right).

the impedance group. This drawback can be mitigated through modifying the frequency response of the impedance group, and one solution is the insertion of a neutral filter, which will be discussed in Chapter 5.

Fig. 4.11 to 4.13 show the CM current flowing across the EDS operating at a constant speed with no load. At this operation mode, the CM current decreases in the whole frequency range. Still, compared with the SV-PWM modulated 4wDC, the CM current decreases more in the whole frequency range due to the use of HPS-PWM. Considering the decreased value of CM current in the reference case, similar ratio of CM current is reduced by applying HPS-PWM (about 40 %).

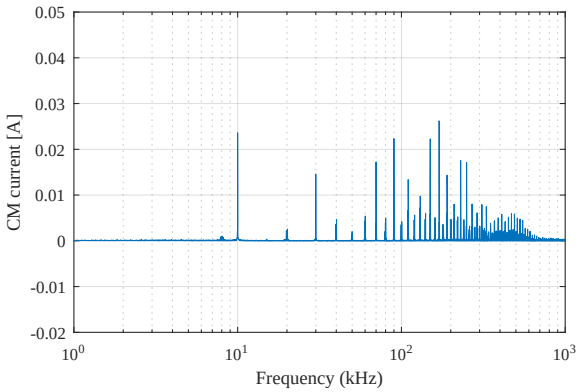


Figure 4.11: Constant-speed without load condition: CM current in the three-wire SV-PWM drive system (the reference case).

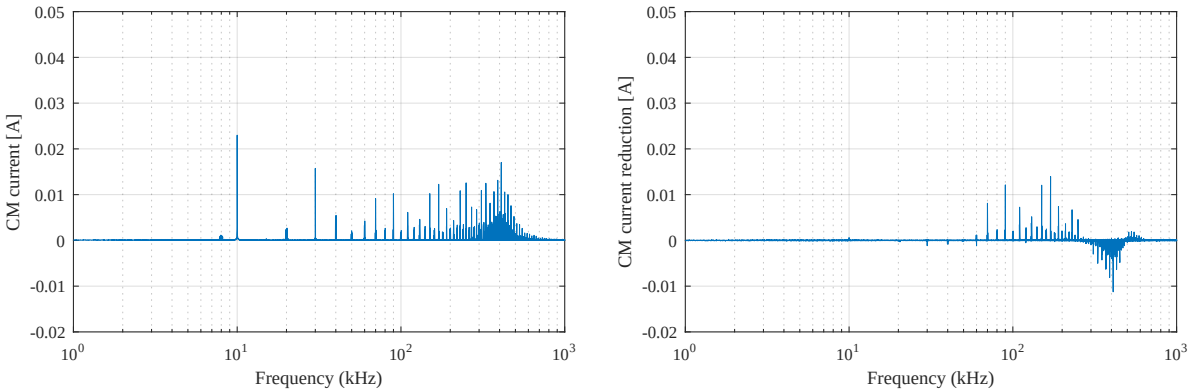


Figure 4.12: Constant-speed without load condition in the 4wDC modulated by SV-PWM: CM current (left) and its reduction compared with the reference (right).

When the load is added to the operating EDS at the same constant speed, as shown in Fig. 4.14 to 4.16,there exists no significant difference on the CM current in the whole frequency range. The CM current reduced by utilizing HPS-PWM is still much more significant than using conventional SV-PWM.

It has to be mentioned that, even though 4wDC resulted in less CM current in a wide range of frequency, it also brings in a new source of power loss, the neutral current, which has to be restricted for reducing the loss of supplied phase current. It is found in the measurement that modulating the EDS with HPS-PWM can also contribute to the

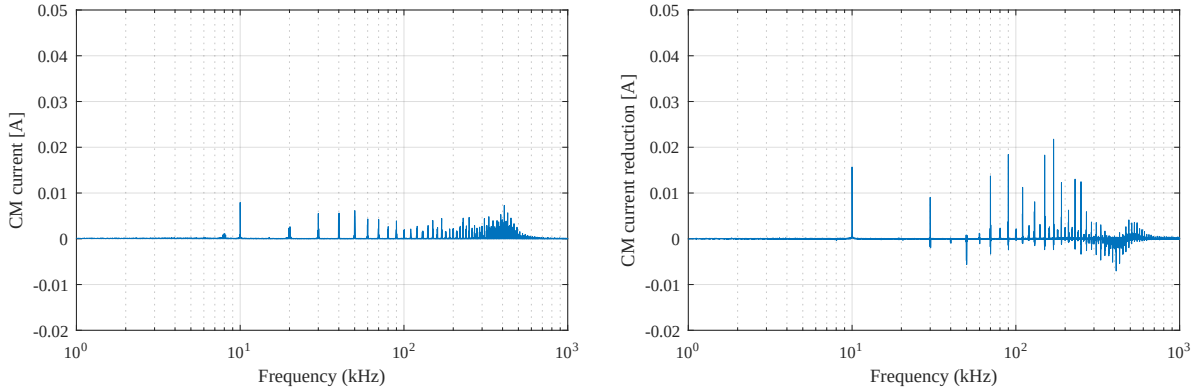


Figure 4.13: Constant-speed without load condition in the 4wDC modulated by HPS-PWM: CM current (left) and its reduction compared with the reference (right).

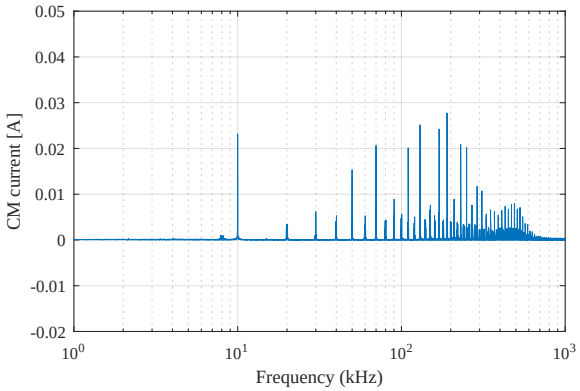


Figure 4.14: Constant-speed with load condition: CM current in the three-wire SV-PWM drive system (the reference case).

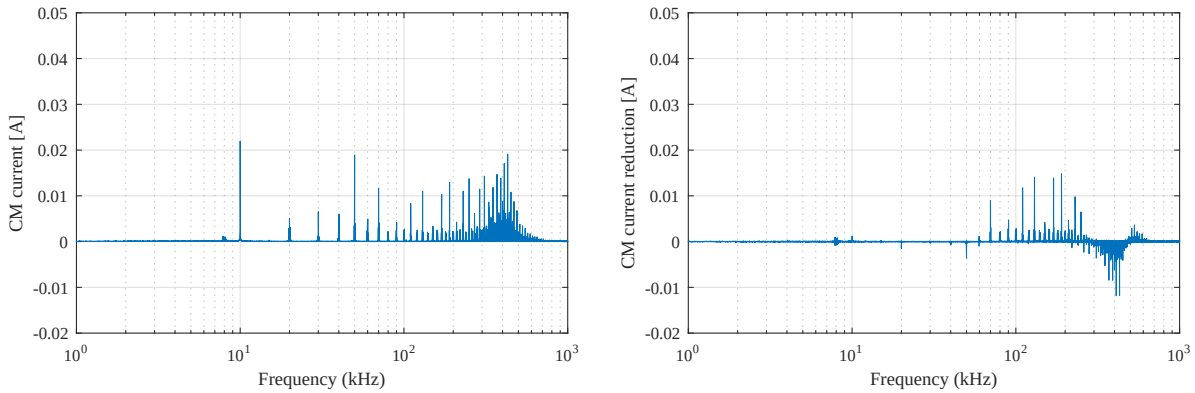


Figure 4.15: Constant-speed with load condition in the 4wDC modulated by SV-PWM: CM current (left) and its reduction compared with the reference (right).

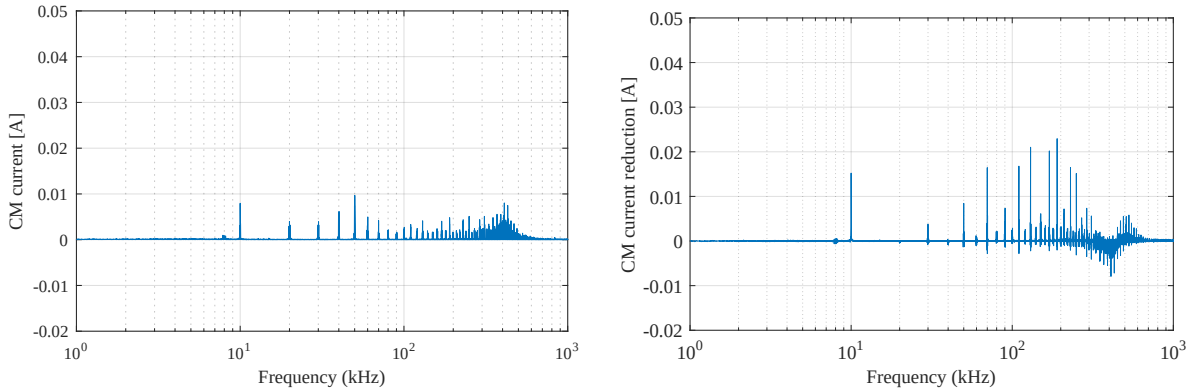


Figure 4.16: Constant-speed with load condition in the 4wDC modulated by HPS-PWM: CM current (left) and its reduction compared with the reference (right).

reduction of neutral current (from 0.332 A to 0.145 A, about 56.3 % decrease at standstill), and this can be explained by the expression of neutral current (represented by $I_{nN4wDC}(s)$) in 4wDC as:

$$I_{nN4wDC}(s) = \frac{U_{nN4wDC}(s)}{Z_{2DC}} = \frac{U_{tot4wDC}(s)}{Z_{1DC} + 3Z_{2DC}} \tag{4.6}$$

It can be seen that the decrease of CM voltage caused by HPS-PWM will result in the reduced neutral current as well.

In summary, the four-wire topology 4wDC alone can already reduce CM current in a wide frequency range. With the application of HPS-PWM for the modulation of EDS, much more CM current reduction can be obtained in the whole frequency range, and the power loss on the fourth wire can be largely reduced as well. This merit remains similar no matter the EDS is operated at standstill, constant speed with or without load.

4.2.2 VSF-PWM applied in 4wDC

VSF-PWM applied in addition to SV-PWM

According to 4.1.2, the application of VSF-PWM requires the prediction of the current ripple of the EDS at a constant switching frequency, and updates the switching frequency for every following switching period, to either reduce the switching loss maintaining the ripple peak or reduce the ripple peak with the same level of switching loss.

As the key of realizing VSF-PWM, the ripple peak prediction needs to calculate out the maximal value of the potential ripple peak on three phases, that is the maximum of $|x_U|, |y_U|, |x_V|, |y_V|, |x_W|, |y_W|$ as mentioned in 4.1.2. This maximum decision procedure for six components will result in an obvious increase of interrupt time interval for VSF-PWM as compared with conventional SV-PWM.

However, this procedure can be optimized according to the unique characteristic of each sector. Again, using Sector I as the reference, according to Fig. 4.4, it is apparently that

in this sector, the duty cycle of phase U is always the largest, and then comes the phase V, and lastly the phase W ($d_U > d_V > d_W$). Along with the characteristic of SV-PWM that the magnitude of the reference vector U_{ref} cannot exceed $\sqrt{3}U_{dc}/3$ for maintaining the positive value of t_0, it can be concluded that $|x_U|, |y_V|, |x_W|$ is always larger than $|y_U|, |x_V|, |y_W|$ within Sector I. This optimization is also valid in other five sectors and thus the realization of VSF-PWM in addition to SV-PWM requires the maximum calculation of at least three components. Based on this, the PWM program has been modified in the control algorithm for the realization of VSF-PWM in 4wDC.

As the obtained prediction equation of ripple peak was validated in a drive system using LRC circuit to approximate the machine in [30], the availability of the prediction equation for practical drive systems with a real electric machine has still not been studied. Through the measurement in the EDS with 2.2 kW PMSM (at the speed of 1000 rpm), the current ripple of a 4wDC and its predicted peak are shown in Fig. 4.17. Similar as the experimental setup with LRC circuit, there exists difference between the measurement and theoretical prediction, which can also be explained by the nonideal conditions such as the change of the output inductance L due to its characteristic of nonlinearity. Considering the acceptable level of deviation, the prediction equation of ripple peak is still reliable for 4wDC. Fig. 4.18 shows the CM current measured in EDS before and after applying VSF-PWM, along with the measured real time switching frequency.

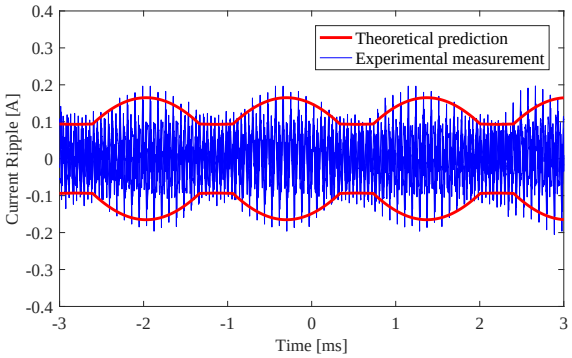
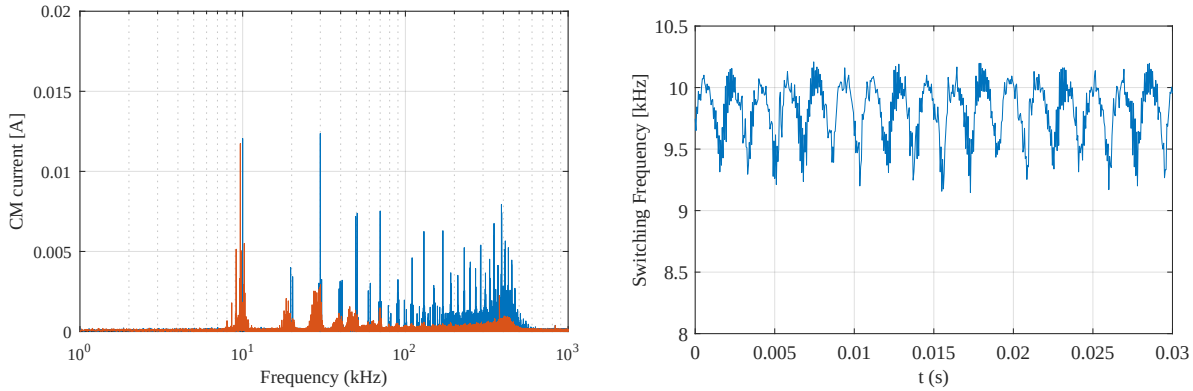


Figure 4.17: Comparison between theoretical predicted peak ripple and measurement results in 4wDC: SV-PWM.

It can be seen that similar as mentioned in [30], the peak of CM current is reduced and transferred to the adjacent frequencies. Besides, the equivalent switching frequency can be decreased while the ripple peak maintains the same. This also contribute to reduce the power losses.

VSF-PWM applied in addition to HPS-PWM

According to the former section, HPS-PWM has shown its advantage of lowering the CM current in the whole frequency range when applied in 4wDC. VSF-PWM also shows the benefit of reducing CM current peak and switching losses. In this section, the VSF-PWM



(a) (b)

Figure 4.18: (a) Comparison of CM current measured before and after applying VSF-PWM in SV-PWM modulated 4wDC; (b) Measured switching frequency applying VSF-PWM in SV-PWM modulated 4wDC.

is applied in addition to HPS-PWM for the first time, for the purpose of obtaining both of their advantages in the same EDS. The procedure of realizing this VSF-PWM+HPS-PWM technique will be explained specifically in the following.

As known before, the first step of realizing VSF-PWM is the prediction of current ripple. This procedure is different when applied in HPS-PWM as compared with SV-PWM, due to the different vectors required for the realization of the PWM technique. Using the Sector I as the example again, the current ripple of HPS-PWM in a switching period is shown in Fig. 4.19-4.21.

Similar to the VSF-PWM applied in a SV-PWM modulated EDS, when it is applied in addition to HPS-PWM, the ripple peak on phase U, V, W are shown in (4.7), (4.8) and (4.9), respectively:

$$\begin{cases} x_U = k_{U7}\dfrac{t_0}{4} \\ y_U = k_{U3}\dfrac{t_0}{4} + k_{U4}\dfrac{t_2}{2} \\ x_U^{'} = k_{U3}\dfrac{t_0}{4} \end{cases} \tag{4.7}$$

$$x_V = k_{V3}\frac{t_0}{4} + k_{V4}\frac{t_2}{2} \tag{4.8}$$

$$\begin{cases} x_W = k_{W7}\dfrac{t_0}{4} \\ x_W^{'} = k_{W3}\dfrac{t_0}{4} \\ y_W^{'} = k_{W3}\dfrac{t_0}{4} + k_{W4}\dfrac{t_2}{2} \end{cases} \tag{4.9}$$

Although it seems that the ripple peak of the EDS in a switching period requires

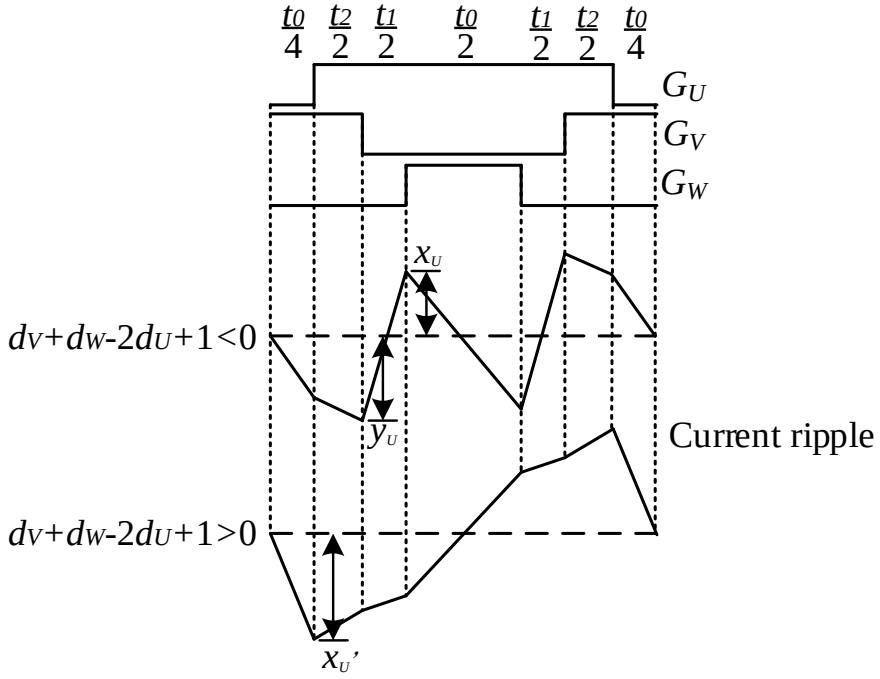


Figure 4.19: Current ripple in a switching period of Sector I (Phase U).

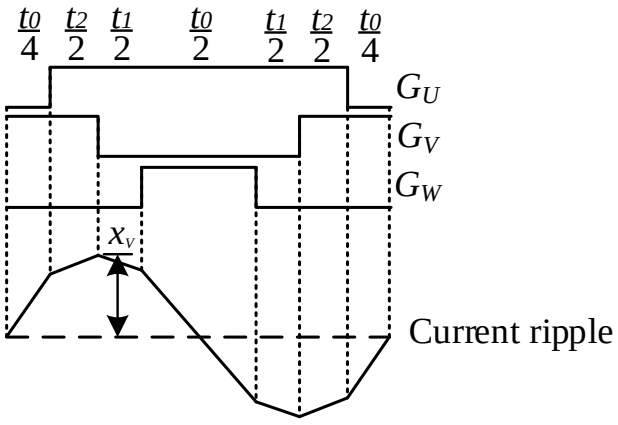


Figure 4.20: Current ripple in a switching period of Sector I (Phase V).

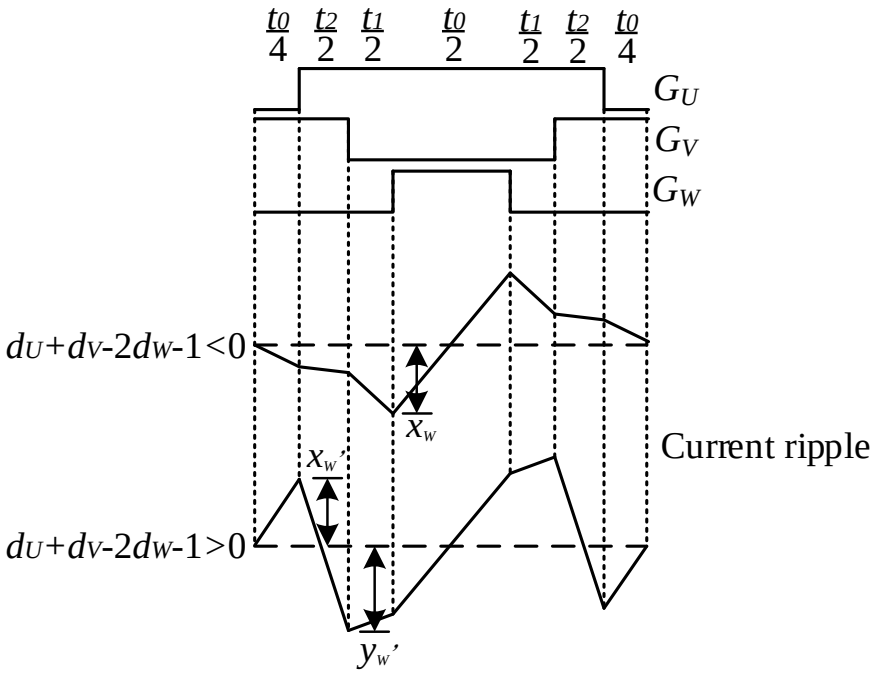


Figure 4.21: Current ripple in a switching period of Sector I (Phase W).

maximum calculation of seven components, actually, when the unique characteristic of Sector I is considered ($d_U > d_V > d_W$), it is easy to see that $|x_V|$ is always the maximum within this sector. This feature also exists in other five sectors, thus it is concluded that the acquisition of ripple peak of the EDS does not need any maximum calculation, which means much less required calculation effort of microcontroller.

Using the same experimental platform in section 4.2.1, the measured current ripple of a HPS-PWM modulated 4wDC and its predicted peak are shown in Fig. 4.22. It is obviously that the theoretical prediction fits the measurement well except for the existing difference due to the nonideal condition of the drive system. Moreover, the comparison of the real time switching frequency between VSF +SV-PWM and VSF+HPS-PWM modulated EDS is shown in Fig. 4.23. All the measurements are carried out at the motor speed of 1000 rpm with 10 kHz as the original fixed switching frequency. It can be seen that using VSF+HPS-PWM modulation strategy can result in a lower equivalent switching frequency (about 9 kHz) than using VSF+SV-PWM modulation strategy (about 9.8 kHz), with the similar value of ripple peak.

Moreover, the measured CM current before and after applying VSF-PWM in addition to the HPS-PWM modulated 4wDC is shown in Fig. 4.24. It is obviously that the CM current at the integral multiple of the original fixed switching frequency (10 kHz) decreases and moves to other adjacent frequencies. This effect becomes stronger at higher frequencies and will not increase the RMS value of CM current.

In summary, the application of VSF-PWM technique in 4wDC can reduce the peak of CM current appearing at the multiple of the original constant switching frequency

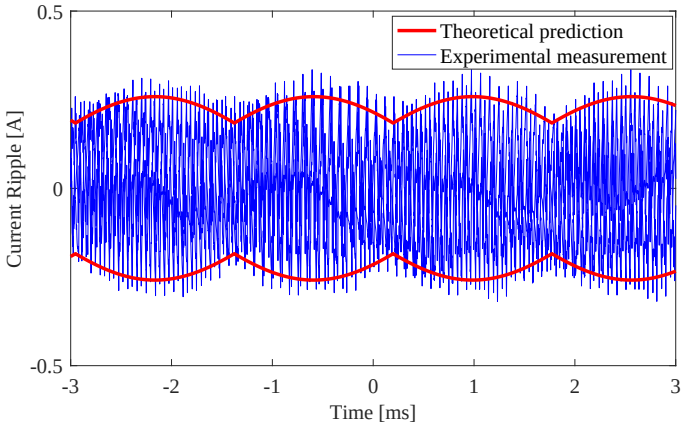


Figure 4.22: Comparison between theoretical predicted peak ripple and measurement results in 4wDC: HPS-PWM.

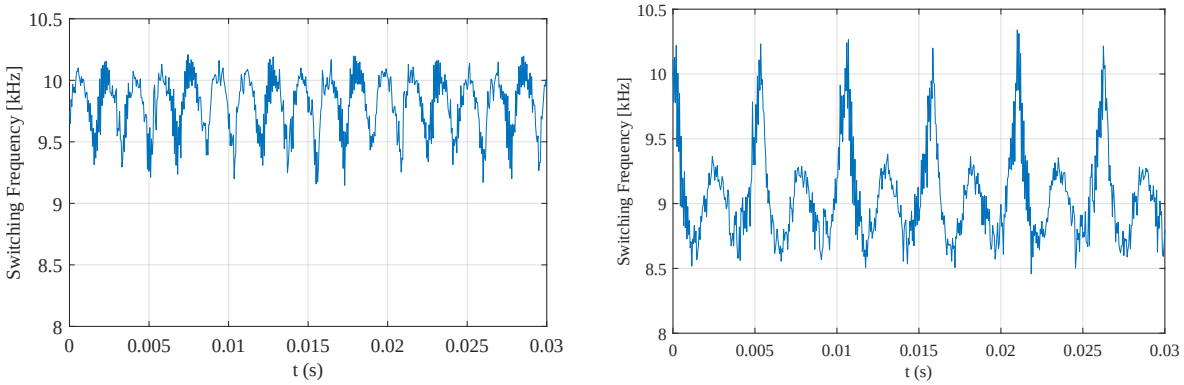


Figure 4.23: Measured switching frequency applying VFS-PWM in SV-PWM (left) and HPS-PWM (right) modulated EDS.

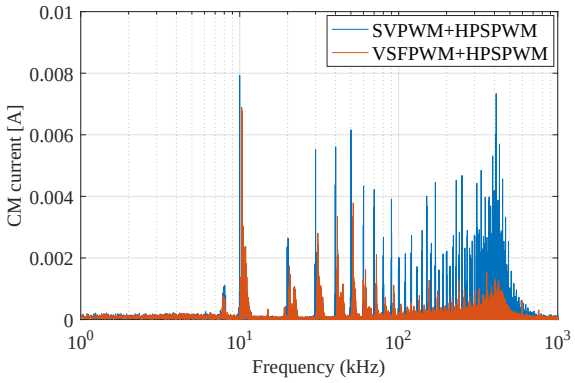


Figure 4.24: Comparison of CM current measured before and after applying VSF-PWM in HPS-PWM modulated 4wDC.

and remove them to other adjacent frequencies. Furthermore, applying VSF-PWM in a HPS-PWM modulated EDS can on one hand maintain the benefit of much less CM current in the whole frequency due to the use of HPS-PWM technique, on the other hand, it also further reduces the peak of the CM current. Besides, the calculation effort required for the ripple peak prediction is much less than that in a SV-PWM modulated EDS, resulting in a much less interrupt interval as well. Lastly, the switching losses were also reduced while maintaining the same ripple peak when applying VSF-PWM together with HPS-PWM in 4wDC.

4.3 PWM optimization for 4wEL

For the four-wire topology 4wEL, it seems that the electric machine is powered by a four-phase inverter as the neutral point is connected to the fourth IGBT bridge. However, for the application of fault-tolerant operation of EDS, the fourth IGBT bridge will always be triggered with a centralized half-period drive signal (duty cycle maintains constant at 0.5), so the fourth IGBT bridge actually contributes nothing to the output power except in fault conditions.

Besides, the drive of 4wEL requires the control of zero sequence components, so the triggering action of inverter is based on the conventional S-PWM. To apply the advanced PWM technique for 4wEL, the S-PWM was just replaced in the control algorithm with the corresponding proposed PWM technique.

The EDS with a 2.2 kW PMSM (described in Section 3.2.1) is used again as the experimental setup for the application of advanced PWM technique. The switching frequency is set to 10kHz for all measurements. The commercial current sensor A6303 from Tektronix (Appendix. A) is utilized for measuring the CM and neutral current under both load and no-load conditions.

4.3.1 HPS-PWM applied in 4wEL

Before discussing the application of HPS-PWM in 4wEL, it is necessary to clarify the difference between SV-PWM (used in 4wDC) and S-PWM (used for 4wEL). It has been mentioned in section 2.2 that S-PWM is similar to SV-PWM when the centered triangular carrier wave is applied. For the fundamental cycle generated by the SV-PWM, with any fixed modulation ratio, it can be divided into six sectors equally, and the duty cycle of three phases has a fixed relationship between each other. Given the duty cycle of SV-PWM in a fundamental cycle with the fixed modulation ratio 0.5, as shown in Fig. 4.25, the relationship between d_U, d_V, d_W in each sector is listed in Table. 4.4

For S-PWM, the duty cycle in a transition cycle with the same modulation ratio 0.5 is shown in Fig. 4.26 Although it looks not the same as that of SV-PWM, but the relationship between duty cycle of each phase turns to be the same as in Table. 4.4. Thus the analysis

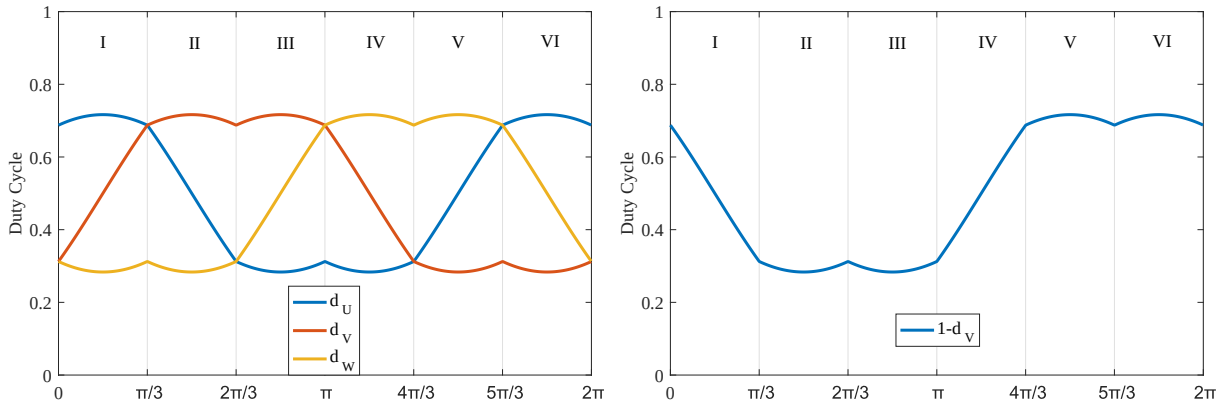


Figure 4.25: Duty cycle of SV-PWM in one transition cycle.

of the influence of applying advanced PWM technique to 4wEL can be carried out in the same way as for 4wDC.

Table 4.4: Relationship between d_U, d_V and d_W in each sector (SV-PWM).

Sector	Relationship between $d_U, d_V and d_W$
I	$d_U > d_V > d_W$
II	$d_V > d_U > d_W$
III	$d_V > d_W > d_U$
IV	$d_W > d_V > d_U$
V	$d_W > d_U > d_V$
VI	$d_U > d_W > d_V$

It is known in section. 4.1.1 that the application of HPS-PWM in SV-PWM will result in unexpected voltage spikes in Sector II, III, V and VI. This is actually caused by another characteristic of the duty cycles of SV-PWM. Due to the need of shifting phase V for 180° of the switching period, the "off" time of phase V is determined by $(1 - d_V)T_s$. Given the plot of $1 - d_V$ in a transition cycle, as shown in the right of Fig. 4.25, it can be easily seen that there exists relationships $d_W = 1 - d_V$ and $d_U = 1 - d_V$ in sector II, V and III, VI, respectively. Therefore, the unexpected voltage errors will always occur during the dead time when the "off" time of phase V equals to the "on" time of any of the other two phases.

However, when we see the plot of $1 - d_V$ of S-PWM (shown in the right of Fig. 4.26), it can be known that the application of HPS-PWM will not result in unexpected voltage errors. This is because that $1 - d_V$ will only equal to the duty cycle of other phases at one time point in each sector. Thus the resulted errors can be neglected considering the extremely low frequency that this condition is met.

Another point that has to be paid attention for the application of HPS-PWM in 4wEL is the existence of the fourth IGBT bridge connecting to the neutral point. From (3.7) it can be known that the voltage source on the neutral wire also contributes to the CM and

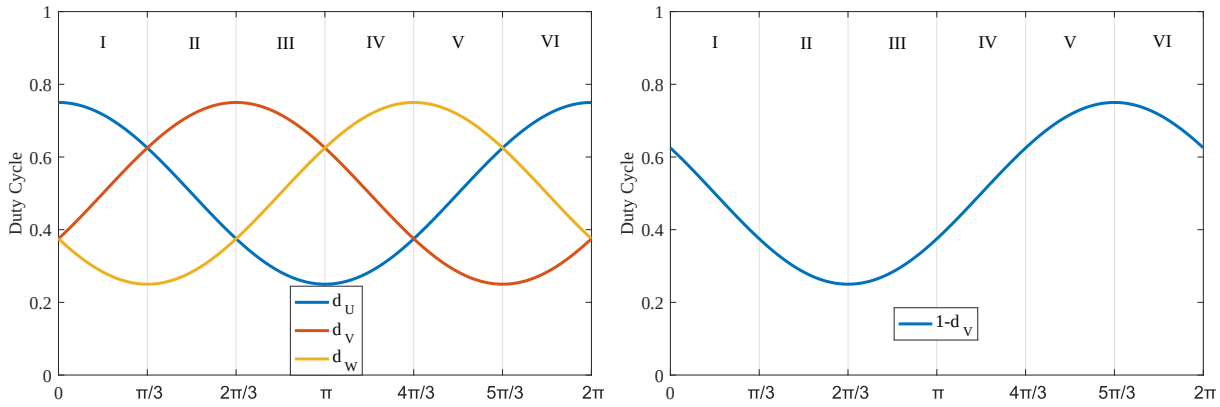


Figure 4.26: Duty cycle of S-PWM in one transition cycle.

neutral voltage together with three phase voltages. Thus for the analysis of the influence of HPS-PWM on CM current reduction, the voltage on the neutral phase also needs to be considered seriously.

Knowing that the duty cycle of the "neutral phase" maintains at 0.5 all the way around, so for the centered PWM, the "on" time of the "neutral phase" can be centered or equally distributed to both sides (centered "off" time).

Using the unfiltered three-wire EDS as the reference again, and both conditions of standstill and constant speed are considered as done in 4wDC. As a comparison, the CM current flowing across the 4wEL modulated by S-PWM are measured under the same working conditions. For the analysis of HPS-PWM in 4wEL, the case with centered "on" (HPS-PWMN+) and "off" (HPS-PWMN-) time of the "neutral phase" are involved. For a better comparison, not only the measured CM current but also the corresponding CM current reduction are plotted, as shown in Fig. 4.27-4.32. The measured CM current of the reference case has already been given in section 4.2.1 (Standstill and constant-speed condition in Fig. 4.8 and 4.11, respectively). To be mentioned, as discussed in section 4.2.1, adding load to the operating EDS at a constant speed will nearly not influence the flowing CM current, thus in this section, the loaded constant-speed condition will not be discussed any more.

In Fig. 4.27, it can be seen that changing the original three-wire topology to 4wEL alone can already largely reduce the CM current in almost the whole frequency range. There only exists slight increase of CM current between 200 and 300 kHz. When HPS-PWMN+ is applied in 4wEL, as shown in Fig. 4.28, the CM current can be further reduced, which results in CM current reduction happening in the whole frequency range. Furthermore, in Fig. 4.29, HPS-PWMN- shows even better performance of CM current reduction than HPS-PWMN+ in the frequency range below 400 kHz, in which the measured CM current can almost be neglected. Although the CM current turns to be a bit more than applying S-PWM and HPS-PWMN+ when the frequency is over 400 kHz, it still maintains at a quite low level and results in the fact that CM current is reduced in the whole frequency

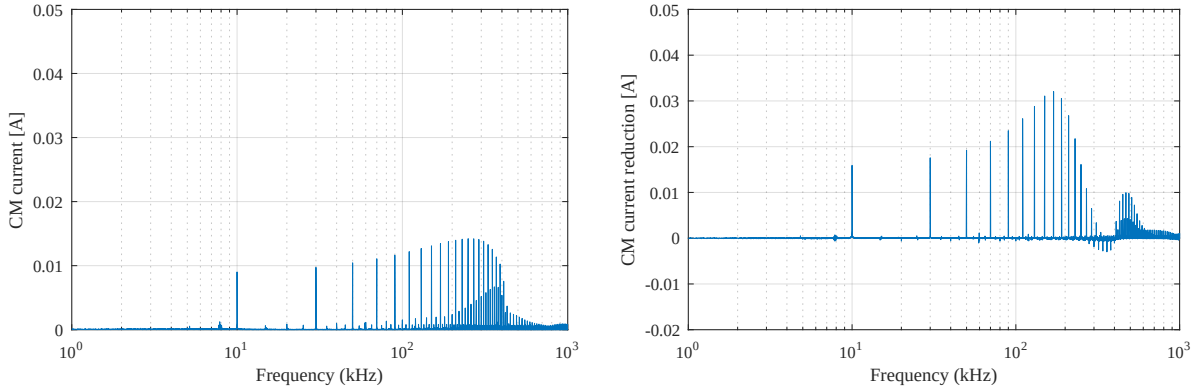


Figure 4.27: Standstill condition in the 4wEL modulated by S-PWM: CM current (left) and its reduction compared with the reference (right).

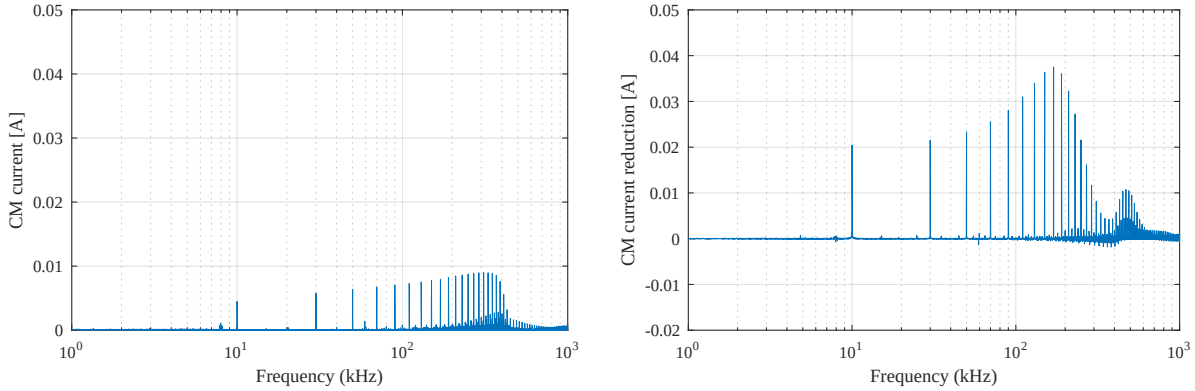


Figure 4.28: Standstill condition in the 4wEL modulated by HPS-PWMN+: CM current (left) and its reduction compared with the reference (right).

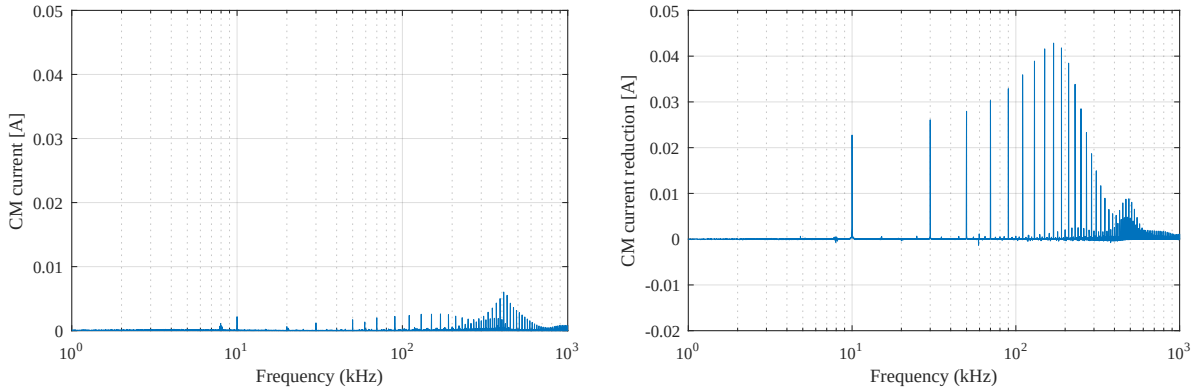


Figure 4.29: Standstill condition in the 4wEL modulated by HPS-PWMN-: CM current (left) and its reduction compared with the reference (right).

range.

The CM current flowing in the operating 4wEL EDS at the same constant speed as in the measurements for 4wDC is shown in Fig. 4.30-4.32. It can be seen that applying HPS-PWM results in less CM current than applying S-PWM under about 120 kHz. In the meantime, more CM current appears in HPS-PWM modulated 4wEL at frequencies over 120 kHz. When HPS-PWMN+ and HPS-PWMN- modulated 4wEL are compared, it is seen that more CM current exists in the 4wEL modulated by HPS-PWMN+ under 300 kHz and HPS-PWMN- over 300 kHz, respectively. However, all these differences of CM current flowing in S-PWM, HPS-PWMN+ and HPS-PWMN- modulated 4wEL actually results in tiny deviation of CM current reduction in the whole frequency range.

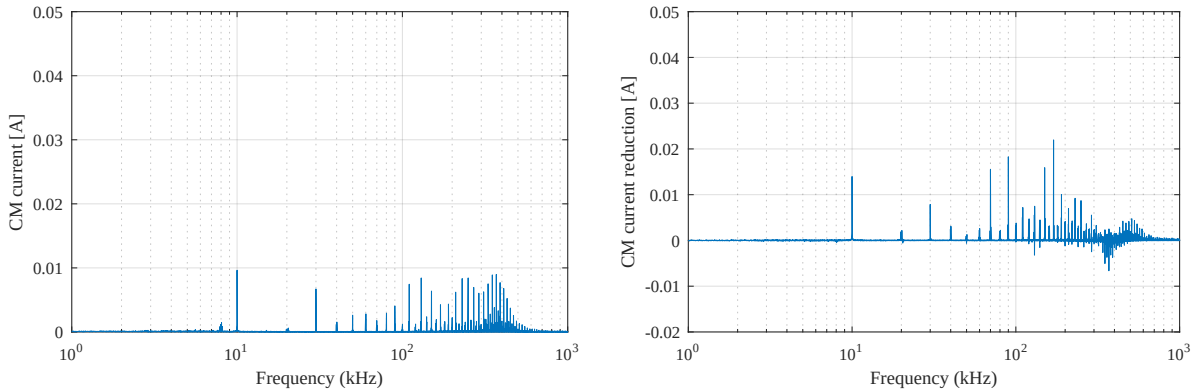


Figure 4.30: Constant-speed condition in the 4wEL modulated by S-PWM: CM current (left) and its reduction compared with the reference (right).

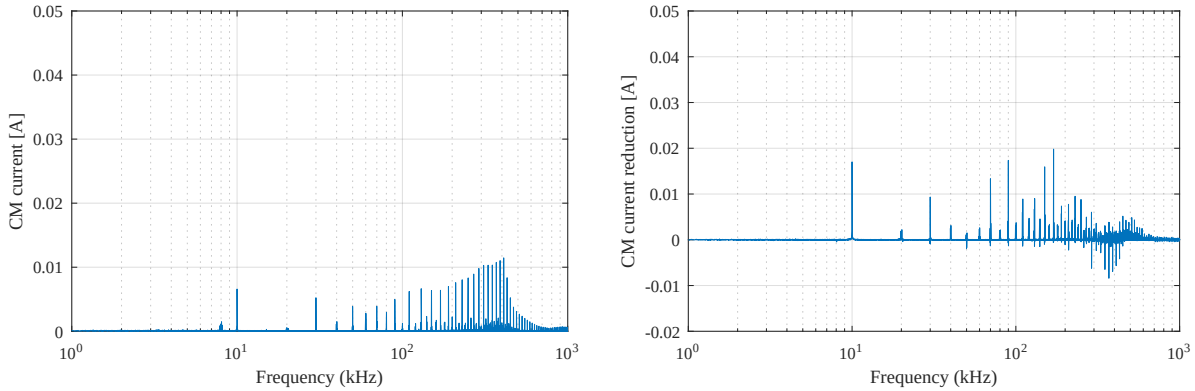


Figure 4.31: Constant-speed condition in the 4wEL modulated by HPS-PWMN+: CM current (left) and its reduction compared with the reference (right).

In summary, the four-wire topology 4wEL alone can already result in much less CM current in a quite wide range of frequency. Applying HPS-PWM can further reduce CM current in the whole freqeuncy range when the EDS is at standstill, this effect is stronger for HPS-PWMN- than for HPS-PWMN+. Although similar influence of HPS-PWM on CM current can be observed when the EDS is operating at a constant speed, but this

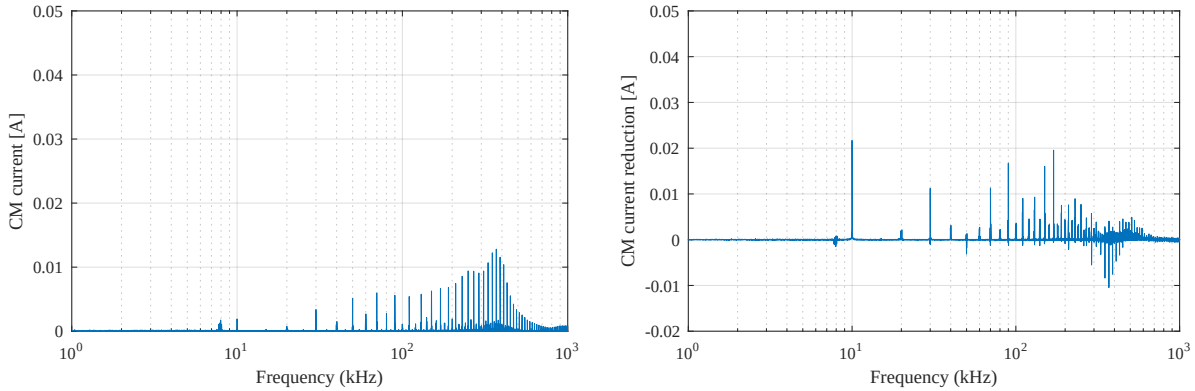


Figure 4.32: Constant-speed condition in the 4wEL modulated by HPS-PWMN-: CM current (left) and its reduction compared with the reference (right).

influence is too weak that its contribution to the CM current reduction can be neglected. This leads to the fact that applying HPS-PWM in 4wEL cannot obviously improve the performance of CM current reduction when the EDS is rotating.

4.3.2 VSF-PWM applied in 4wEL

VSF-PWM applied in addition to S-PWM

Again, the first step of realizing VSF-PWM is the prediction of current ripple. As discussed in the former sections that centered S-PWM can be equivalent to SV-PWM, thus the method of predicting current ripple according to the equivalent circuit for each vector is still available for S-PWM.

However, for the four-wire topology 4wEL, unlike 4wDC, except for the voltage sources on three phases, the voltage source on the "neutral phase" also needs to be considered. Given the equivalent circuit for each vector of 4wEL, as shown in Fig. 4.33. Similarly, based on the corresponding equivalent circuit, defining d_n as the duty cycle of the "neutral phase" switching from 0 to 1, the ripple current slope of phase U, V and W can be presented as shown in Table. 4.5, 4.6 and 4.7, respectively.

Considering the relationship between d_U, d_V and d_W, as same as SV-PWM, the fundamental cycle of S-PWM can also be divided into six sectors equally. However, as d_n also needs to be considered along with d_U, d_V and d_W for the four-wire topology 4wEL, each of the original six sectors should be further divided into two sub-sectors equally, as shown in Fig. 4.34.

According to Table. 4.5, the current ripple on the three phases in one switching period can be obtained. Using Sector 1-1 as an example, the relevant current ripple curve can be plotted as shown in Fig. 4.35. Thus the peak of the current ripple on three phases can be obtained as:

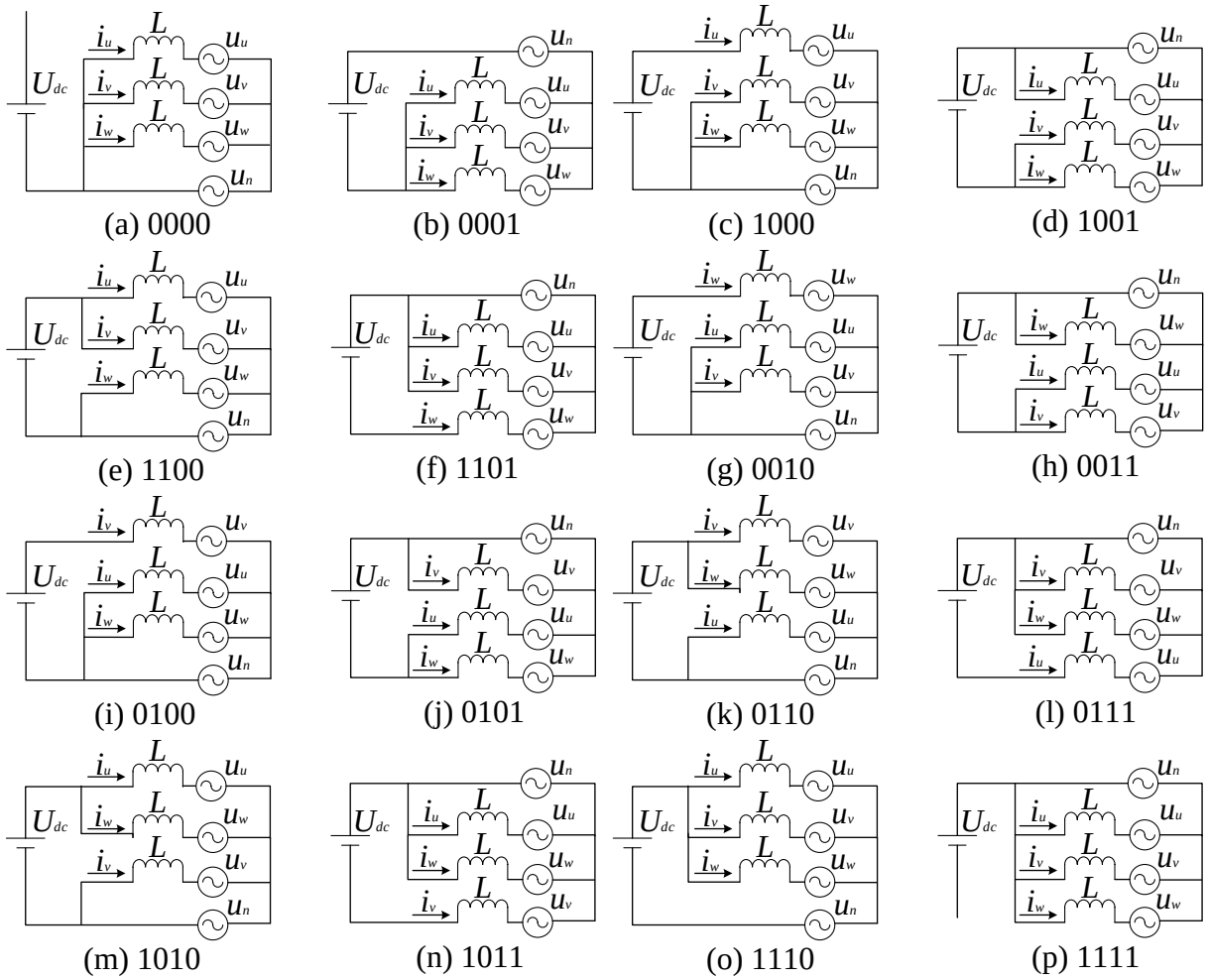


Figure 4.33: Equivalent circuit of switching combination of each vector.

$$\begin{cases} x_U = k_{U00}\dfrac{1-d_U}{2}T_s \\ y_U = k_{U00}\dfrac{1-d_U}{2}T_s + k_{U10}\dfrac{d_U-d_n}{2}T_s \end{cases} \tag{4.10}$$

$$\begin{cases} x_V = k_{V00}\dfrac{1-d_U}{2}T_s + k_{V10}\dfrac{d_U-d_n}{2}T_s \\ y_V = k_{V71}\dfrac{1-d_W}{2}T_s + k_{V21}\dfrac{d_V-d_W}{2}T_s \end{cases} \tag{4.11}$$

$$\begin{cases} x_W = k_{W00}\dfrac{1-d_U}{2}T_s + k_{W10}\dfrac{d_U-d_n}{2}T_s \\ y_W = k_{W71}\dfrac{d_W}{2}T_s \end{cases} \tag{4.12}$$

Considering the relationship between d_U, d_V and d_W in Sector 1-1, it can be easily known that $|x_U|$ is the maximum among all peak values of current ripple in three phases. Similarly, through further deduction, the peak of current ripple in all three phases in a switching period of other sectors can be obtained as well (shown in Table. 4.8). Furthermore, as

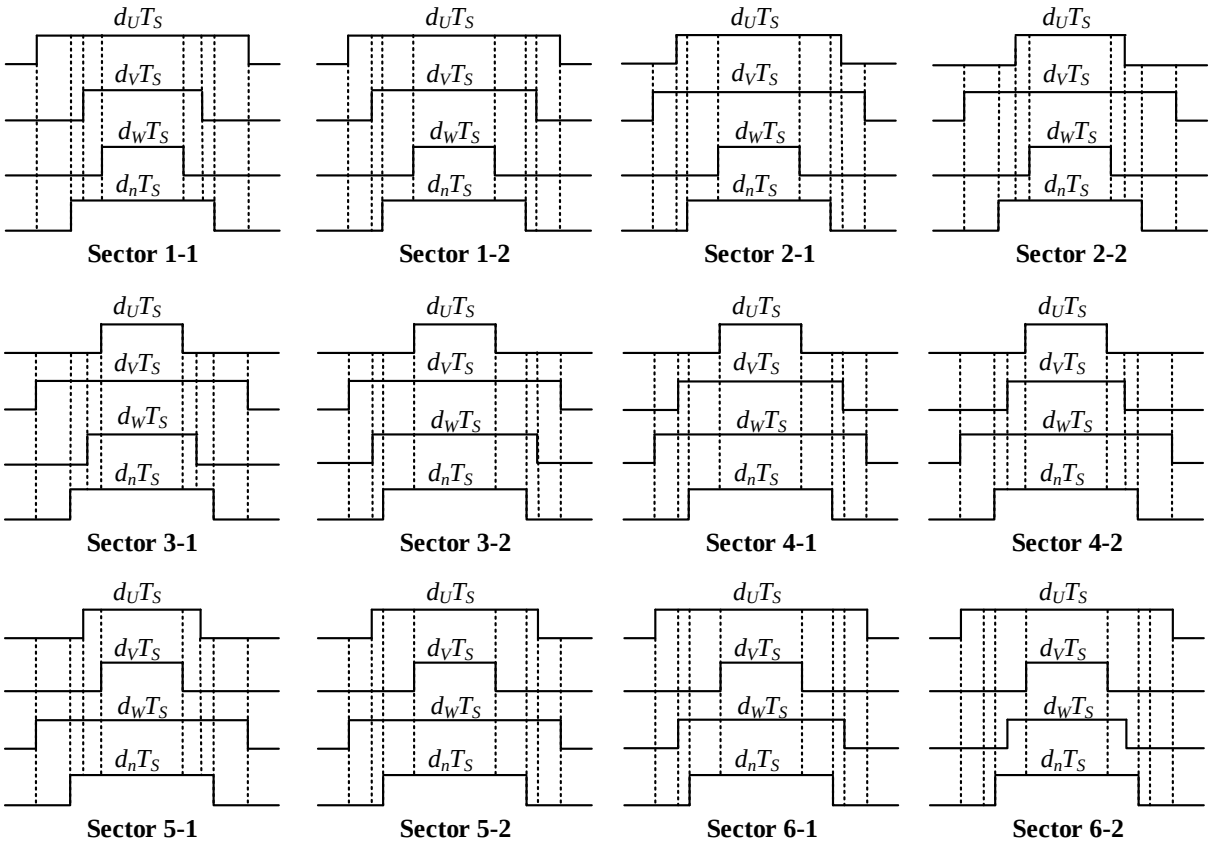


Figure 4.34: Sectors of the transition cycle of 4wEL.

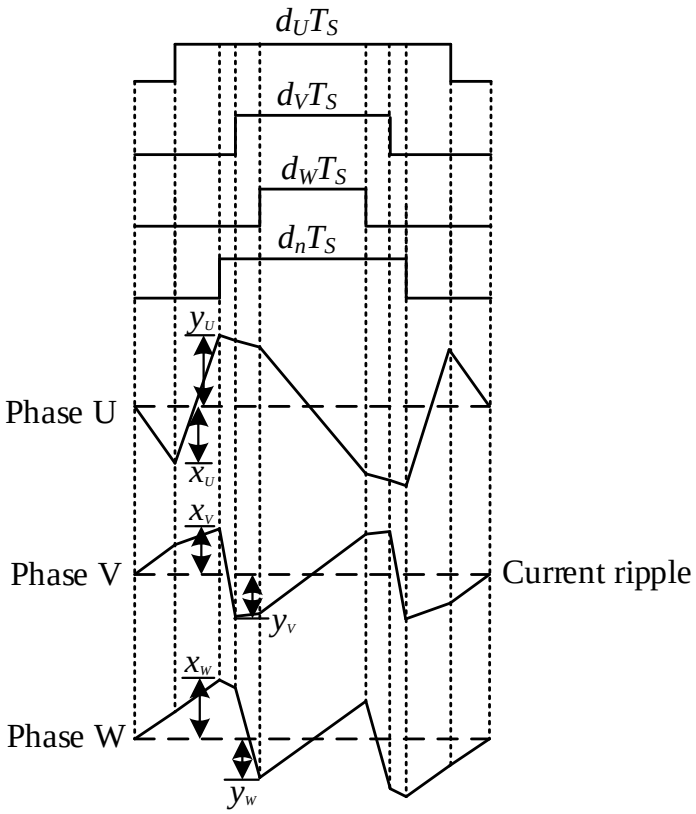


Figure 4.35: Current ripple in a switching period of Sector 1-1.

Table 4.5: Switching vectors and the correspondent ripple current slope (Phase U).

Vector	Ripple Current Slope	Vector	Ripple Current Slope
0000	$k_{U00} = \frac{U_{dc}}{L}(d_n - d_U)$	0001	$k_{U01} = \frac{U_{dc}}{L}(d_n - d_U - 1)$
1000	$k_{U10} = \frac{U_{dc}}{L}(d_n - d_U + 1)$	1001	$k_{U11} = \frac{U_{dc}}{L}(d_n - d_U)$
1100	$k_{U20} = \frac{U_{dc}}{L}(d_n - d_U + 1)$	1101	$k_{U21} = \frac{U_{dc}}{L}(d_n - d_U)$
0010	$k_{U30} = \frac{U_{dc}}{L}(d_n - d_U)$	0011	$k_{U31} = \frac{U_{dc}}{L}(d_n - d_U - 1)$
0100	$k_{U40} = \frac{U_{dc}}{L}(d_n - d_U)$	0101	$k_{U41} = \frac{U_{dc}}{L}(d_n - d_U - 1)$
0110	$k_{U50} = \frac{U_{dc}}{L}(d_n - d_U)$	0111	$k_{U51} = \frac{U_{dc}}{L}(d_n - d_U - 1)$
1010	$k_{U60} = \frac{U_{dc}}{L}(d_n - d_U + 1)$	1011	$k_{U61} = \frac{U_{dc}}{L}(d_n - d_U)$
1110	$k_{U70} = \frac{U_{dc}}{L}(d_n - d_U + 1)$	1111	$k_{U71} = \frac{U_{dc}}{L}(d_n - d_U)$

the duty cycle of "neutral phase", d_n, remains at 0.5 for the application of 4wEL in this study, thus the peak of current ripple in all sectors can be represented by six expressions only, as shown in Table. 4.9. This is of great meaning as the calculation effort required for the micro-controller to realize the VSF-PWM in 4wEL is much less than in traditional three-wire EDSs.

Similar to 4wDC, the simplified VSF-PWM program in addition to S-PWM for 4wEL, has been applied in the control algorithm. The measured current ripple of a S-PWM modulated 4wEL and its predicted peak are shown in Fig. 4.36. It is obviously that the theoretical prediction fits the measurement well except for the existing difference due to the nonideal condition of the drive system. Fig. 4.37 shows the measured CM current in 4wEL before and after applying VSF-PWM (at the motor speed of 1000 rpm), along with the measured real-time switching frequency.

In Fig. 4.37, it can be seen that due to the use of VSF-PWM, the CM current at the integral multiple of the original fixed switching frequency (10 kHz) reduces and is transferred to other adjacent frequencies. This effect results in no influence on the RMS value of CM current. Besides, the utilization of VSF +S-PWM modulation strategy lowers the equivalent switching frequency (9.1 kHz) while maintaining the ripple peak.

Table 4.6: Switching vectors and the correspondent ripple current slope (Phase V).

Vector	Ripple Current Slope	Vector	Ripple Current Slope
0000	$k_{V00} = \frac{U_{dc}}{L}(d_n - d_V)$	0001	$k_{V01} = \frac{U_{dc}}{L}(d_n - d_V - 1)$
1000	$k_{V10} = \frac{U_{dc}}{L}(d_n - d_V)$	1001	$k_{V11} = \frac{U_{dc}}{L}(d_n - d_V - 1)$
1100	$k_{V20} = \frac{U_{dc}}{L}(d_n - d_V + 1)$	1101	$k_{V21} = \frac{U_{dc}}{L}(d_n - d_V)$
0010	$k_{V30} = \frac{U_{dc}}{L}(d_n - d_V)$	0011	$k_{V31} = \frac{U_{dc}}{L}(d_n - d_V - 1)$
0100	$k_{V40} = \frac{U_{dc}}{L}(d_n - d_V + 1)$	0101	$k_{V41} = \frac{U_{dc}}{L}(d_n - d_V)$
0110	$k_{V50} = \frac{U_{dc}}{L}(d_n - d_V + 1)$	0111	$k_{V51} = \frac{U_{dc}}{L}(d_n - d_V)$
1010	$k_{V60} = \frac{U_{dc}}{L}(d_n - d_V)$	1011	$k_{V61} = \frac{U_{dc}}{L}(d_n - d_V - 1)$
1110	$k_{V70} = \frac{U_{dc}}{L}(d_n - d_V + 1)$	1111	$k_{V71} = \frac{U_{dc}}{L}(d_n - d_V)$

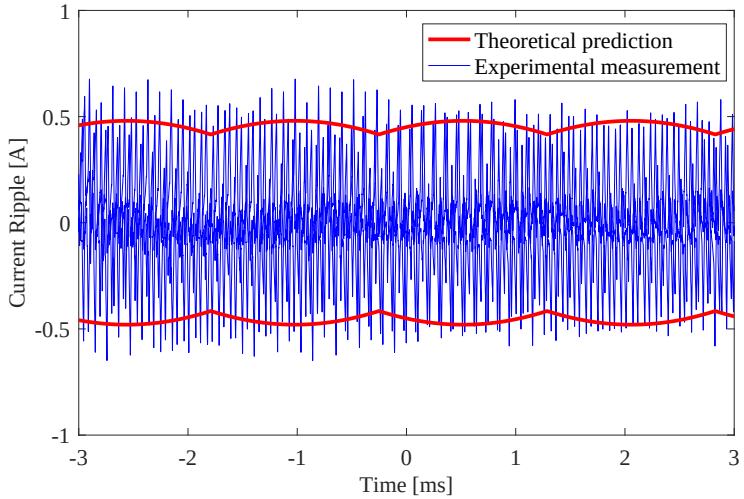


Figure 4.36: Comparison between theoretical predicted peak ripple and measurement results in 4wEL: S-PWM.

Table 4.7: Switching vectors and the correspondent ripple current slope (Phase W).

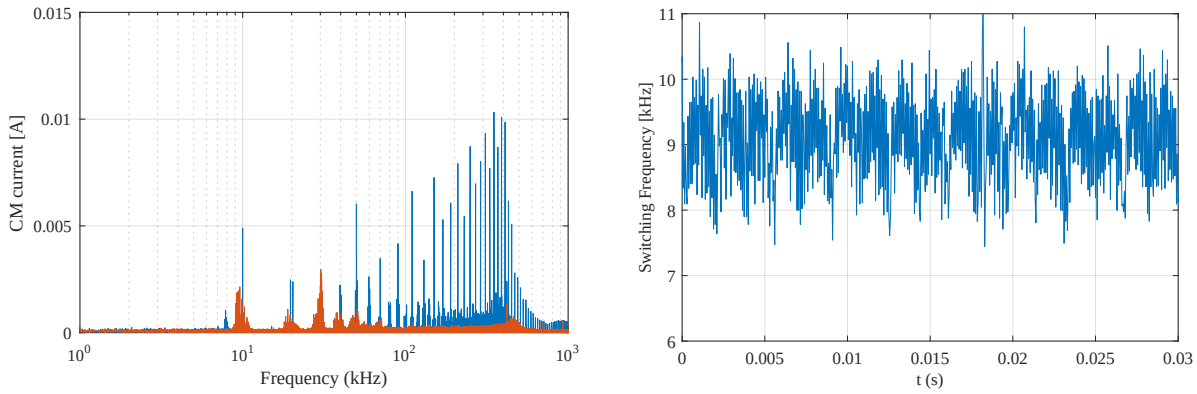
Vector	Ripple Current Slope	Vector	Ripple Current Slope
0000	$k_{W00} = \frac{U_{dc}}{L}\,(d_n - d_W)$	0001	$k_{W01} = \frac{U_{dc}}{L}\,(d_n - d_W - 1)$
1000	$k_{W10} = \frac{U_{dc}}{L}\,(d_n - d_W)$	1001	$k_{W11} = \frac{U_{dc}}{L}\,(d_n - d_W - 1)$
1100	$k_{W20} = \frac{U_{dc}}{L}\,(d_n - d_W)$	1101	$k_{W21} = \frac{U_{dc}}{L}\,(d_n - d_W - 1)$
0010	$k_{W30} = \frac{U_{dc}}{L}\,(d_n - d_W)$	0011	$k_{W31} = \frac{U_{dc}}{L}\,(d_n - d_W - 1)$
0100	$k_{W40} = \frac{U_{dc}}{L}\,(d_n - d_W)$	0101	$k_{W41} = \frac{U_{dc}}{L}\,(d_n - d_W - 1)$
0110	$k_{W50} = \frac{U_{dc}}{L}\,(d_n - d_W + 1)$	0111	$k_{W51} = \frac{U_{dc}}{L}\,(d_n - d_W)$
1010	$k_{W60} = \frac{U_{dc}}{L}\,(d_n - d_W + 1)$	1011	$k_{W61} = \frac{U_{dc}}{L}\,(d_n - d_W)$
1110	$k_{W70} = \frac{U_{dc}}{L}\,(d_n - d_W + 1)$	1111	$k_{W71} = \frac{U_{dc}}{L}\,(d_n - d_W)$

Table 4.8: Sectors and the correspondent peak of current ripple.

Sector	Peak of Current Ripple	Sector	Peak of Current Ripple
1-1	$\frac{U_{dc}T_s}{L}\,(d_U - d_n)\,\frac{d_n}{2}$	1-2	$\frac{U_{dc}T_s}{L}\,(d_n - d_W)\,\frac{1-d_n}{2}$
2-1	$\frac{U_{dc}T_s}{L}\,(d_n - d_W)\,\frac{1-d_n}{2}$	2-2	$\frac{U_{dc}T_s}{L}\,(d_V - d_n)\,\frac{d_n}{2}$
3-1	$\frac{U_{dc}T_s}{L}\,(d_V - d_n)\,\frac{d_n}{2}$	3-2	$\frac{U_{dc}T_s}{L}\,(d_n - d_U)\,\frac{1-d_n}{2}$
4-1	$\frac{U_{dc}T_s}{L}\,(d_n - d_U)\,\frac{1-d_n}{2}$	4-2	$\frac{U_{dc}T_s}{L}\,(d_W - d_n)\,\frac{d_n}{2}$
5-1	$\frac{U_{dc}T_s}{L}\,(d_W - d_n)\,\frac{d_n}{2}$	5-2	$\frac{U_{dc}T_s}{L}\,(d_n - d_V)\,\frac{1-d_n}{2}$
6-1	$\frac{U_{dc}T_s}{L}\,(d_n - d_V)\,\frac{1-d_n}{2}$	6-2	$\frac{U_{dc}T_s}{L}\,(d_U - d_n)\,\frac{d_n}{2}$

Table 4.9: Sectors and the corresponding peak of current ripple after simplification (S-PWM).

Sector	Peak of Current Ripple
1-1, 6-2	$\frac{U_{dc}T_s}{4L}\ (d_U - d_n)$
3-2, 4-1	$\frac{U_{dc}T_s}{4L}\ (d_n - d_U)$
2-2, 3-1	$\frac{U_{dc}T_s}{4L}\ (d_V - d_n)$
5-2, 6-1	$\frac{U_{dc}T_s}{4L}\ (d_n - d_V)$
4-2, 5-1	$\frac{U_{dc}T_s}{4L}\ (d_W - d_n)$
1-2, 2-1	$\frac{U_{dc}T_s}{4L}\ (d_n - d_W)$



(a) (b)

Figure 4.37: (a) Comparison of CM current measured before and after applying VSF-PWM in S-PWM modulated 4wEL; (b) Measured switching frequency applying VSF-PWM in S-PWM modulated 4wEL.

VSF-PWM applied in addition to HPS-PWM

According to the former section, HPS-PWM has been proved to be able to largely reduce the CM current in the whole frequency range when applied in 4wEL at standstill. But this effect becomes much weaker when the electric machine is operating at a constant speed. As VSF-PWM shows its availability of reducing CM current peak as well as switching losses, in this section, the VSF-PWM is applied in addition to the two types of HPS-PWM in 4wEL, for the first time, to bring further improvement in reducing CM current at constant-speed condition. The specific procedure of realizing VSF+HPS-PWM technique will be explained firstly.

It is known that predicting the current ripple is always the first step of realizing VSF-PWM. As the use of HPS-PWM changes the vectors and their action time in each sector comparing with S-PWM, thus the current ripple of HPS-PWM in a switching period also varies, as shown in Fig. 4.38 and 4.39 (Sector 1-1 as the example again). Additionally, the peak of the current ripple on three phases can be obtained for HPS-PWMN+ as:

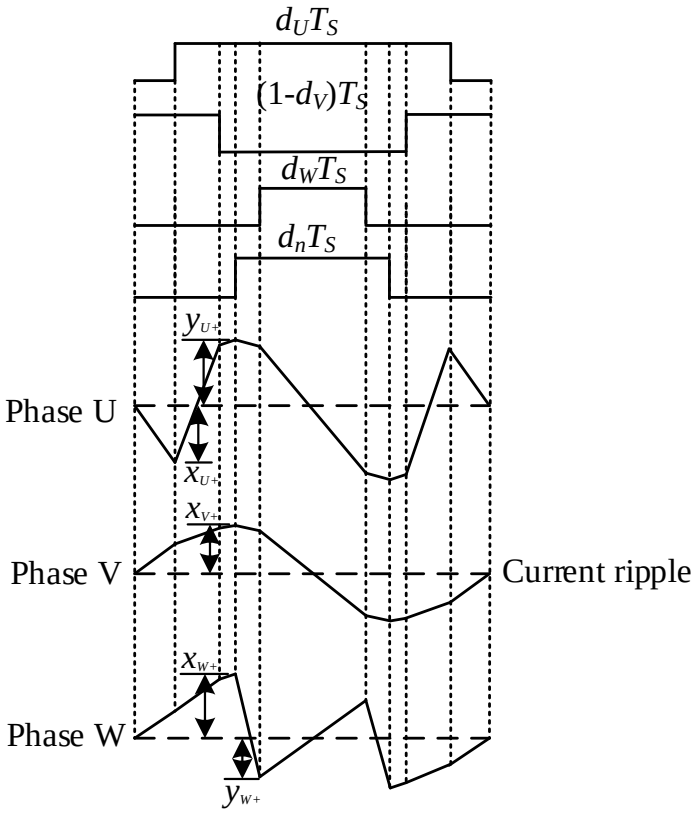


Figure 4.38: Current ripple in a switching period of Sector 1-1 (HPS-PWMN+).

$$\begin{cases} x_{U+} = k_{U40}\dfrac{1-d_U}{2}T_s \\ y_{U+} = k_{U61}\dfrac{d_W}{2}T_s + k_{U11}\dfrac{d_n-d_W}{2}T_s \end{cases} \tag{4.13}$$

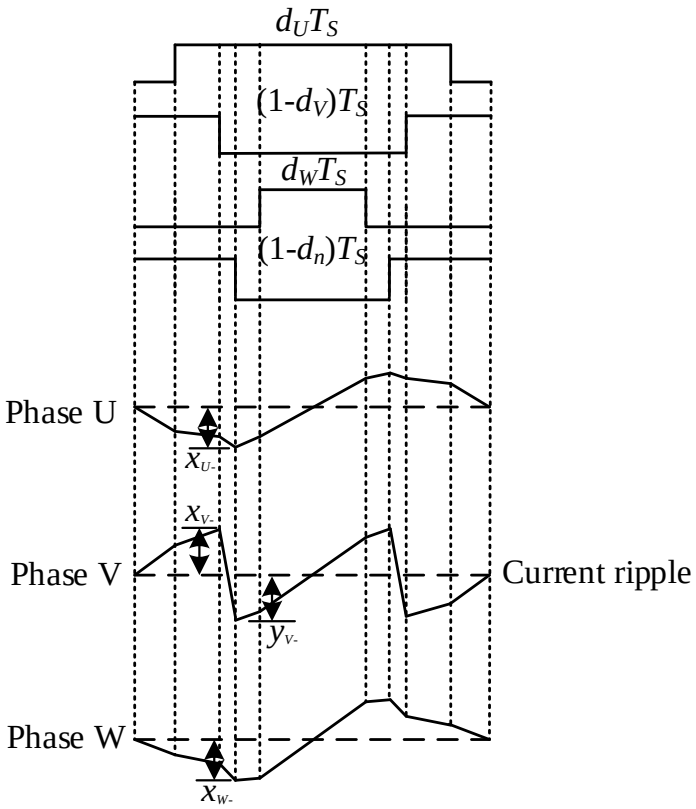


Figure 4.39: Current ripple in a switching period of Sector 1-1 (HPS-PWMN-).

$$x_{V+} = k_{V61}\frac{d_W}{2}T_s + k_{V11}\frac{d_n - d_W}{2}T_s \tag{4.14}$$

$$\begin{cases} x_{W+} = k_{W61}\dfrac{d_W}{2}T_s \\ y_{W+} = k_{W61}\dfrac{d_W}{2}T_s + k_{W11}\dfrac{d_n - d_W}{2}T_s \end{cases} \tag{4.15}$$

and for HPS-PWMN- as:

$$x_{U-} = k_{U60}\frac{d_W}{2}T_s + k_{V10}\frac{d_n - d_W}{2}T_s \tag{4.16}$$

$$\begin{cases} x_{V-} = k_{V60}\dfrac{d_W}{2}T_s + k_{V10}\dfrac{d_n - d_W}{2}T_s \\ y_{V-} = k_{V41}\dfrac{d_W}{2}T_s + k_{V21}\dfrac{d_n - d_W}{2}T_s \end{cases} \tag{4.17}$$

$$x_{W-} = k_{W60}\frac{d_W}{2}T_s + k_{V10}\frac{d_n - d_W}{2}T_s \tag{4.18}$$

Again, considering the fact that d_n remains at 0.5, thus the ripple peak in all sectors of HPS-PWMN+ and HPS-PWMN- can be listed in Table. 4.10 and 4.11, respectively. It is obviously that the calculation effort of microcontroller required for realizing VSF-PWM in HPS-PWM modulated 4wEL becomes further less. This is due to the less expressions of representing the ripple peak in all sectors (reducing from six to two for HPS-PWMN+

and four for HPS-PWMN-, respectively).

Table 4.10: Sectors and the corresponding peak of current ripple after simplification (HPS-PWMN+).

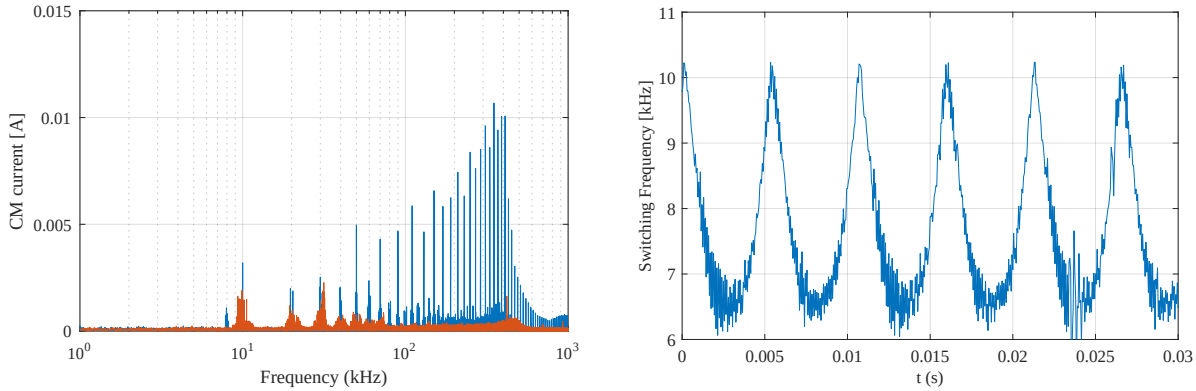
Sector	Peak of Current Ripple
1-1, 4-2, 5-1, 5-2, 6-1, 6-2	$\frac{U_{dc}T_s}{4L}\ (d_V - d_n + 1)$
1-2, 2-1, 2-2, 3-1, 3-2, 4-1	$\frac{U_{dc}T_s}{4L}\ (d_n - d_V + 1)$

Table 4.11: Sectors and the corresponding peak of current ripple after simplification (HPS-PWMN-).

Sector	Peak of Current Ripple
1-1, 6-1, 6-2	$\frac{U_{dc}T_s}{4L}\ (d_n - d_U + 1)$
1-2, 2-1, 2-2	$\frac{U_{dc}T_s}{4L}\ (d_W - d_n + 1)$
3-1, 3-2, 4-1	$\frac{U_{dc}T_s}{4L}\ (d_U - d_n + 1)$
4-2, 5-1, 5-2	$\frac{U_{dc}T_s}{4L}\ (d_n - d_W + 1)$

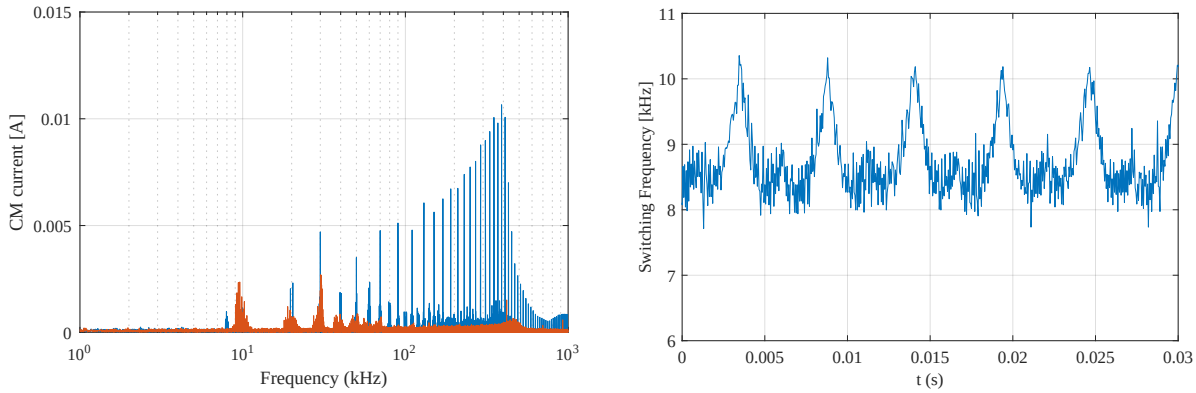
Based on the given expressions of ripple peak as shown in Table. 4.10 and 4.11, the corresponding VSF-PWM program has been applied in the control algorithm. Fig. 4.40 and 4.41 show the measured CM current in 4wEL before and after applying VSF-PWM in addition to HPS-PWMN+ and HPS-PWMN- (at the motor speed of 1000 rpm), respectively. The corresponding measured real-time switching frequencies are shown as well.

It can be seen that for both types of HPS-PWM, due to the use of VSF-PWM, the CM current at the integral multiple of the original fixed switching frequency (10 kHz) reduces and is transferred to other adjacent frequencies. This effect results in no influence on the RMS value of CM current. Besides, the utilization of VSF+HPS-PWM modulation strategy lowers the equivalent switching frequency (7.8 kHz for HPS-PWMN+ and 8.8 kHz for HPS-PWMN-, at the motor speed of 1000 rpm) while maintaining the ripple peak.



(a) (b)

Figure 4.40: (a) Comparison of CM current measured before and after applying VSF-PWM in HPS-PWMN+ modulated 4wEL; (b) Measured switching frequency applying VSF-PWM in HPS-PWMN+ modulated 4wEL.



(a) (b)

Figure 4.41: (a) Comparison of CM current measured before and after applying VSF-PWM in HPS-PWMN- modulated 4wEL; (b) Measured switching frequency applying VSF-PWM in HPS-PWMN- modulated 4wEL.

4.4 Summary

This chapter has discussed the application of advanced PWM technique in four-wire EDSs. Using traditional SV-PWM in 4wDC already results in a significant reduction of CM current, while the utilization of HPS-PWM in 4wDC can result in even further reduction. This influence maintains strong at both standstill and constant-speed condition of the electric machine. Meanwhile, the use of HPS-PWM in 4wEL also reduces more CM current than the S-PWM modulated EDS at standstill, but the resulted CM current reduction is similar at constant-speed condition except for low frequencies.

Through the analysis of the difference between three- and four-wire topology, some modification has been done to the original expressions of predicting the current ripple. Based on the updated ripple prediction expressions, VSF-PWM has been applied in both 4wDC and 4wEL and the peak of CM current all reduces and transfers to adjacent frequencies. This phenomenon becomes stronger in the high frequency range. Besides, the combination of VSF+HPS-PWM has been found to be with much less calculation effort of micro-controller and switching losses than the combination of VSF+SV-PWM (4wDC) or S-PWM (4wEL). Specifically, for 4wDC, VSF+SV-PWM reduces 2 % of the switching loss, while VSF+HPS-PWM reduces the loss for 10 %. For 4wEL, VSF+S-PWM is already with 9 % less switching loss, however, this value can reach 12 % for VSF+HPS-PWMN- and even 22 % for VSF+HPS-PWMN+.

All the above conclusions have been validated in the practical EDS with 2.2 kW PMSM.

5 Design of Filter Topology

This chapter presents the transfer function approach method of analyzing the filtering effects resulting from the insertion of filter topologies to four-wire EDS, 4wDC and 4wEL. Firstly, the filtering effect of a conventional CM filter used for three-wire EDS (CMMF in [14]) is analyzed theoretically, also in four-wire EDS. Then, the potential filtering effect of other types of filter topology are also analyzed and compared with CMMF. Lastly, optimized filter topologies are proposed, along with its well-structured step-by-step design procedure. Based on the design procedure, an optimized filter topology is designed and built for both types of four-wire drive system, and also validated in both experimental setups. The relevant CM current measurement is carried out.

5.1 Analysis of transfer function resulted from different filters

5.1.1 Analysis of transfer function in 4wDC

As discussed in [3], the influence of phase voltage rise on CM current is much lower than that of neutral voltage rise, thus the following analysis will be only on the neutral voltage. Firstly, a three-wire EDS along with its high frequency (HF) model are given as shown in Fig. A.1, while a CMMF is the optional filter topology for the filtered case. To be mentioned, considering that this study is focused on the application in EV, so the power cables are short and the DC-source (battery) is left floating for all EDSs in this study. However, there exists considerable high capacitive couplings (stray capacitance C_{DC}) from battery and inverter to ground, which is also much higher than the capacitive couplings from electric machine to ground. According to the analysis in Section 3.1.1, along with the transfer function given in [14], for CMMF filtered three-wire EDS, the theoretical expression of neutral voltage in Laplace domain can be obtained:

$$U_{tot3w}(s) = K_{3wF}(s)(U_{UN}(s) + U_{VN}(s) + U_{WN}(s)) \tag{5.1}$$

$$U_{nN3w}(s) = \frac{U_{tot3w}(s)}{3} \tag{5.2}$$

$$K_{3wF}(s) = \frac{1 + sR_FC_F}{s^2L_FC_F + sR_FC_F + 1} \tag{5.3}$$

where $K(s)$ represents the transfer function between the cable input or neutral voltage and the original phase voltage in Laplace domain; R_F, C_F and L_F are the selected components

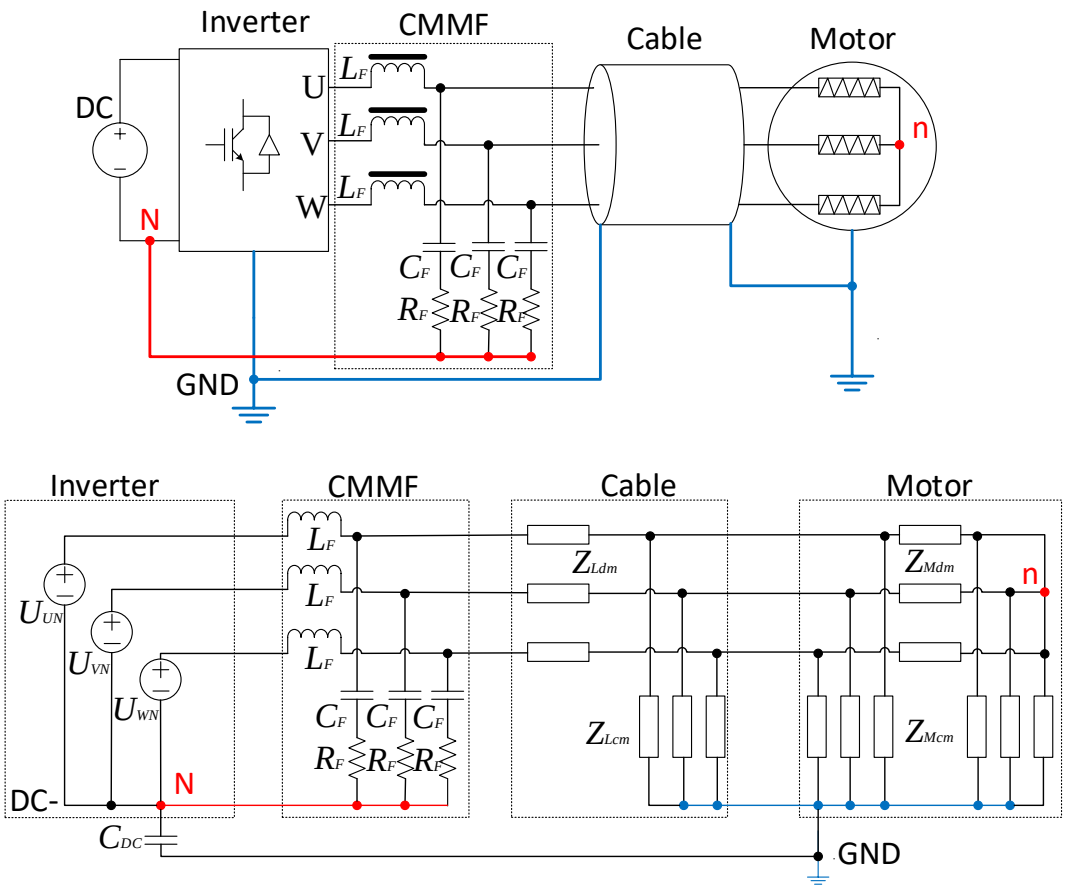


Figure 5.1: Three-wire EDS (top) and corresponding HF equivalent circuit (bottom) with CMMF as the filter topology.

for CMMF.

It can be seen that, the insertion of CMMF results in the change of the transfer function from (3.2) to (5.3), and thus it is possible to lower the CM current in a specified frequency range through well selection of R_F, C_F and L_F. To be mentioned, this CMMF has been proved to be very effective in reducing CM current in three-wire EDS [14]. However, its filtering effect has not been researched before and remains unclear in any four-wire EDSs.

Inserting the same CMMF in a 4wDC, the high-frequency equivalent circuit will change from Fig. 3.2 to Fig. 5.2, as shown below. Thus the theoretical expression of cable input and neutral voltage for the CMMF filtered 4wDC can be obtained:

$$U_{tot4wDC\_F}(s) = K_{4wDC\_F}(s)(U_{UN}(s) + U_{VN}(s) + U_{WN}(s)) \tag{5.4}$$

$$U_{nN4wDC\_F}(s) = K_{nN4wDC\_F}(s)\frac{U_{UN}(s) + U_{VN}(s) + U_{WN}(s)}{3} \tag{5.5}$$

$$K_{4wDC\_F}(s) = \frac{Z_{1DC} + 3Z_{2DC}}{Z_{1DC} + sL_F K_{3wF}(s) + 3Z_{2DC}} K_{3wF}(s) \tag{5.6}$$

$$K_{nN4wDC\_F}(s) = \frac{3Z_{2DC}}{Z_{1DC} + sL_F K_{3wF}(s) + 3Z_{2DC}} K_{3wF}(s) \tag{5.7}$$

where the definition of Z_{1DC} and Z_{2DC} are given in 3.8 and 3.9, respectively.

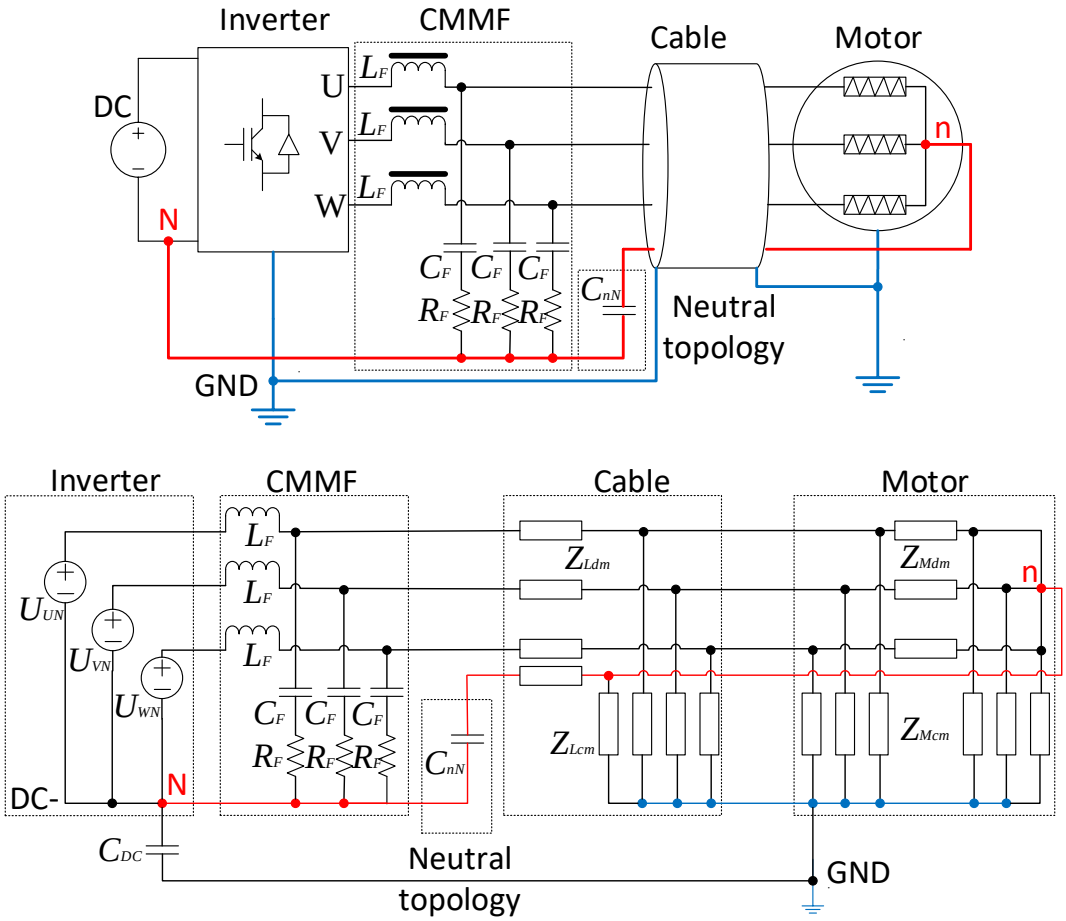


Figure 5.2: Four-wire EDS 4wDC (top) and corresponding HF equivalent circuit (bottom) with CMMF as the filter topology.

It has to be considered, that the CMMF block of Fig. 5.2 uses individual inductances for each phase. This is necessary to limit the current peaks in the inverter that results from the voltage edges and the parallel capacitors if no or only a CM inductor is used. The disadvantage is that the magnetic flux of the inductance will depend on the phase current and will require bulky cores.

Due to the unwanted bulky size of CMMF, another filtered case is also considered in 4wDC, in which only a CM choke with value L_{FCC} is placed between the inverter and power cable without parallel capacitors, as shown in Fig. 5.3. The advantage is that the core flux will only depend on the CM current and being consequently much smaller. In

this case, the relevant theoretical expressions yield:

$$U_{tot4wDC\_FCC}(s) = K_{4wDC\_FCC}(s)(U_{UN}(s) + U_{VN}(s) + U_{WN}(s)) \tag{5.8}$$

$$U_{nN4wDC\_FCC}(s) = K_{nN4wDC\_FCC}(s)\frac{U_{UN}(s) + U_{VN}(s) + U_{WN}(s)}{3} \tag{5.9}$$

$$K_{4wDC\_FCC}(s) = \frac{Z_{1DC} + 3Z_{2DC}}{Z_{1DC} + sL_{FCC} + 3Z_{2DC}} \tag{5.10}$$

$$K_{nN4wDC\_FCC}(s) = \frac{3Z_{2DC}}{Z_{1DC} + sL_{FCC} + 3Z_{2DC}} \tag{5.11}$$

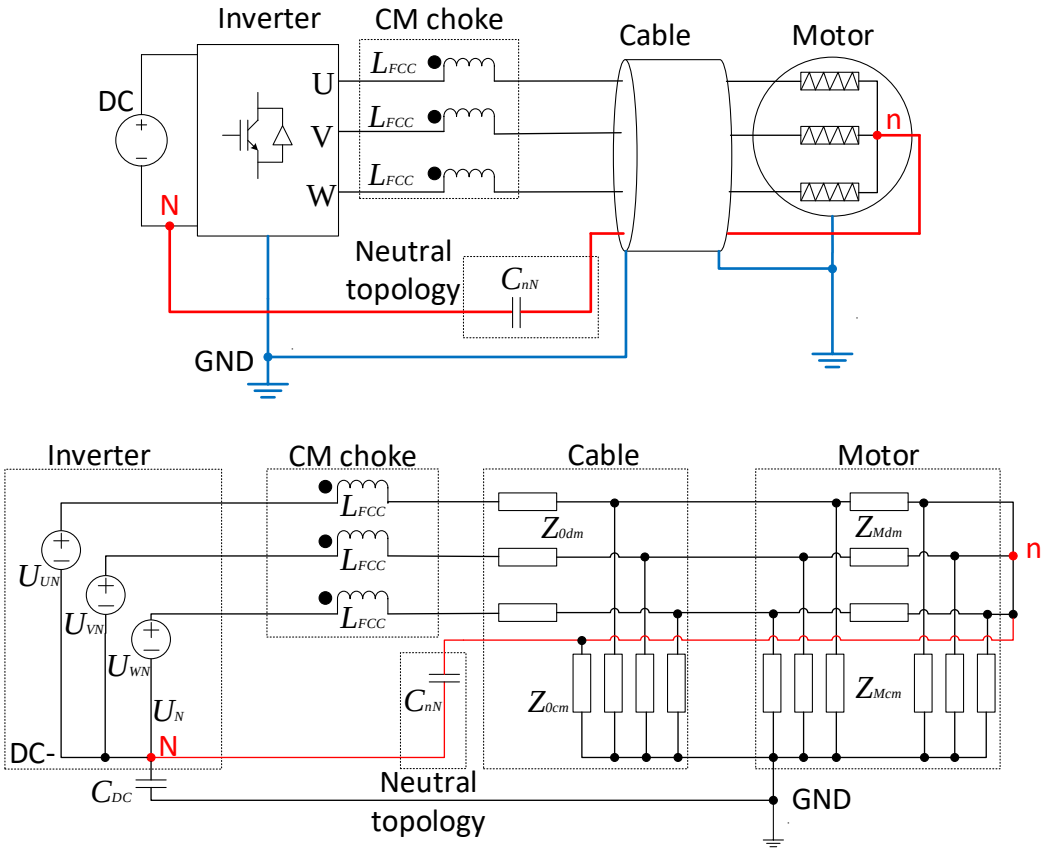


Figure 5.3: Four-wire EDS 4wDC (top) and corresponding HF equivalent circuit (bottom) with a CM choke as the filter topology.

5.1.2 Analysis of transfer function in 4wEL

Similar to the four-wire topology 4wDC, when the CMMF is inserted in a 4wEL, the high-frequency equivalent circuit will change from Fig. 3.3 to the one as shown in Fig. 5.4. Thus the theoretical expression of the cable input and neutral voltage for the CMMF filtered 4wEL can be obtained:

$$U_{tot4wEL\_F}(s) = K_{4wEL\_Fcm}(s)U_{cm}(s) + K_{4wEL\_Fn}(s)U_N(s) \tag{5.12}$$

$$U_{nN4wEL\_F}(s) = K_{nN4wEL\_Fcm}(s)\frac{U_{cm}(s)}{3} + K_{nN4wEL\_Fn}(s)U_N(s) \tag{5.13}$$

$$K_{4wEL\_Fcm}(s) = \frac{Z_{1EL} + 3Z_{2EL}}{Z_{1EL} + sL_F K_{3wF}(s) + 3Z_{2EL}} K_{3wF}(s) \tag{5.14}$$

$$K_{4wEL\_Fn}(s) = \frac{3sL_F - Z_{1EL} - 3Z_{2EL}}{Z_{1EL} + sL_F K_{3wF}(s) + 3Z_{2EL}} K_{3wF}(s) \tag{5.15}$$

$$K_{nN4wEL\_Fcm}(s) = \frac{3Z_{2EL}}{Z_{1EL} + sL_F K_{3wF}(s) + 3Z_{2EL}} K_{3wF}(s) \tag{5.16}$$

$$K_{nN4wEL\_Fn}(s) = \frac{Z_{1EL} + sL_F K_{3wF}(s) - Z_{2EL}K_{3wF}(s)}{Z_{1EL} + sL_F K_{3wF}(s) + 3Z_{2EL}} \tag{5.17}$$

$$U_{cm}(s) = U_{UN}(s) + U_{VN}(s) + U_{WN}(s) + U_N(s) \tag{5.18}$$

where the definition of Z_{1EL} and Z_{2EL} are given in 3.8 and 3.10, respectively.

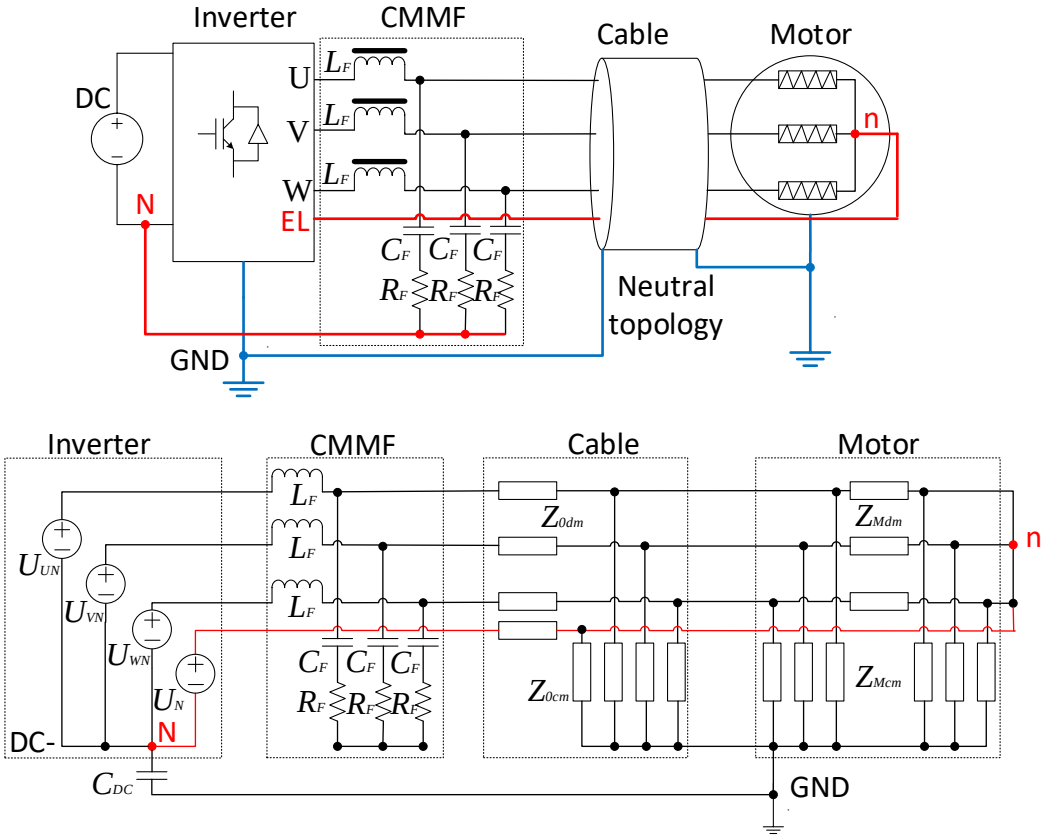


Figure 5.4: Four-wire EDS 4wEL (top) and corresponding HF equivalent circuit (bottom) with CMMF as the filter topology.

Again, the choke filtered case is considered in 4wEL as a compromise for limiting the size of filter topology, as shown in Fig. 5.5, along with its corresponding theoretical expressions:

$$U_{tot4wEL\_FCC}(s) = K_{4wEL\_FCCcm}(s)\, U_{cm}(s) + K_{4wEL\_FCCn}(s)\, U_N(s) \tag{5.19}$$

$$U_{nN4wEL\_FCC}(s) = K_{nN4wDC\_FCCcm}(s)\,\frac{U_{cm}(s)}{3} + K_{nN4wEL\_FCCn}(s)\,U_N(s) \tag{5.20}$$

$$K_{4wEL\_FCCcm}(s) = \frac{Z_{1EL} + 3Z_{2EL}}{Z_{1EL} + sL_{FCC} + 3Z_{2EL}} \tag{5.21}$$

$$K_{4wEL\_FCCn}(s) = \frac{3sL_{FCC} - Z_{1EL} - 3Z_{2EL}}{Z_{1EL} + sL_{FCC} + 3Z_{2EL}} \tag{5.22}$$

$$K_{nN4wEL\_FCCcm}(s) = \frac{3Z_{2EL}}{Z_{1EL} + sL_{FCC} + 3Z_{2EL}} \tag{5.23}$$

$$K_{nN4wEL\_FCCn}(s) = \frac{Z_{1EL} + sL_{FCC} - Z_{2EL}}{Z_{1EL} + sL_{FCC} + 3Z_{2EL}} \tag{5.24}$$

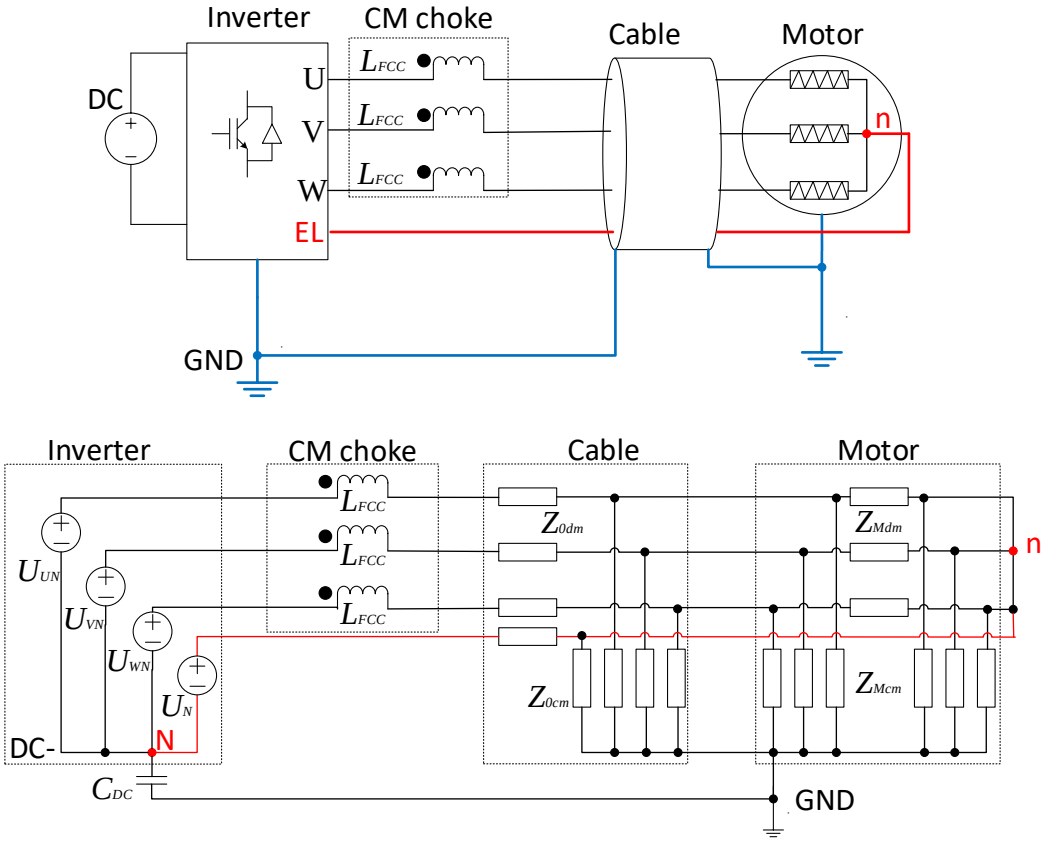


Figure 5.5: Four-wire EDS 4wEL (top) and corresponding HF equivalent circuit (bottom) with a CM choke as the filter topology.

5.2 Filter design for 4wDC

To compare the filtering effect between different types of filter and EDS topology, the experimental setup with 60 kW PMSM is used as the example for analysis.

However, for two three-wire EDSs with different type of electric machine (one with surface-mounted magnet and the other with interior-mounted magnet, for instance), the

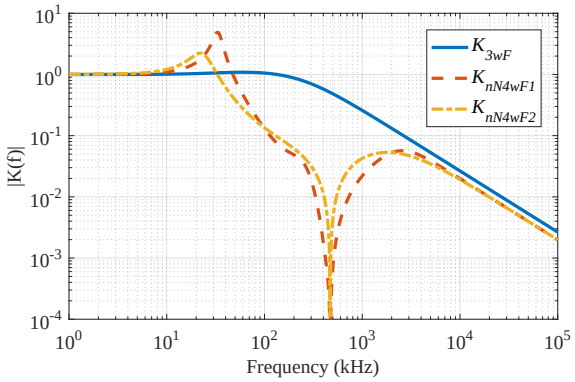


Figure 5.6: Frequency response of transfer function for CMMF filtered EDS.

power parameter could be designed to be similar, while the motor impedance could be absolutely different. In this case, according to the design procedure of CMMF summarized and validated in [14], same design parameters will be obtained for both EDSs and the filtering effect should be similar. However, when it is applied in the 4wDC modified from the original three-wire EDS, the filtering effect will be totally different considering the influence of motor impedance (same cable is used for both EDSs). As an example, two EDSs used for the drive of an EV are introduced here. Due to the drive demand of the EV, electric machines of both EDSs are designed with the power of 60 kW, rated voltage and current of 380 V and 300 A, respectively. Nevertheless, the motor impedance is different in the whole frequency range due to the difference of their magnetic mounting, size, etc. According to [14], the CMMF is designed with the parameters $L_F = 58\ \mu$F, $R_F = 100\ \Omega, C_F = 47\ n$F for both EDSs.

From [3], as the influence of phase voltage rise on CM current is much lower than that of neutral voltage rise, the poor CM current reduction on the phase voltage of choke-filtered four-wire topology can hardly affect the intact CM current reduction. Thus the analysis in the following will be on the transfer function for neutral voltage only.

Knowing the parameters of CMMF, according to (3.6), (5.3) and (5.7), the frequency response of the transfer function between the neutral voltage and the inverter output voltage is shown in Fig. 5.6 (K_{nN4wF1} and K_{nN4wF2} corresponds to surface- and interior-mounted PMSM, respectively). Here, specially the difference in the resonance peak, regarding amplitude and frequency, should be observed. This peak has to be kept as far as possible from the switching frequency and its harmonic components. It can be seen that due to the difference of the motor impedance, the designed CMMF in both type of 4wDC does not work as effective as each other. Thus for 4wDC, the design procedure of filter topology should be reconsidered.

The transfer function for unfiltered 4wDC can be obtained from (3.6) as (5.25). Given its frequency response as shown in Fig. 5.7. Then it is known that the limited effective frequency range in which the CM current is reduced, is due to the two resonances of its

transfer function in the LF and HF range, respectively. To be mentioned, even when the filtering frequency range is limited, it has its maximal filtering action there where the emission is the highest (see spectrum of the unfiltered 3-wire topology in Fig. 5.13).

$$K_{nN4wDC}(s) = \frac{3Z_{2DC}}{Z_{1DC} + 3Z_{2DC}} \tag{5.25}$$

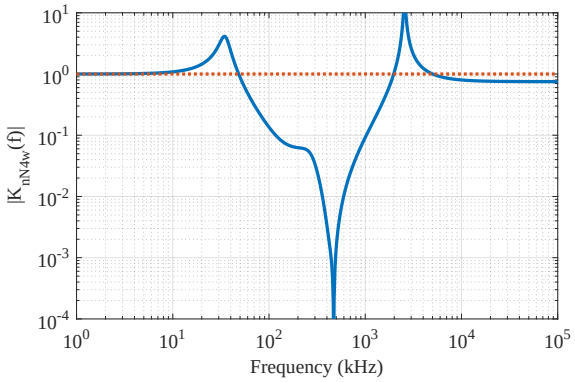


Figure 5.7: Frequency response of transfer function for unfiltered 4wDC.

In the LF range, according to (5.25), as Z_{Mdm} can be represented by ωL_M, which is much larger than Z_{Ldm}, thus the resonance within this frequency range occurs when ωL_M is close to $1/(\omega C_{nN})$.

As the frequency increases, the imaginary part of the cable impedance keeps increasing and getting increasingly closer to $1/(\omega C_{nN})$. This trend will make the numerator decrease and finally reach nearly zero, which result in the appearance of the minimum of the magnitude of the transfer function between the two resonance.

In the HF range, Z_{Ldm} already becomes comparable to Z_{Mdm}, along with the much smaller value of $1/(\omega C_{nN})$ than in the LF range, then the magnitude of the transfer function reaches the second resonance. This happens under the condition:

$$|4Z_{Ldm}(j\omega) + Z_{Mdm}(j\omega)| \approx 0 \tag{5.26}$$

These three extreme values of $|K_{nN4wDC}|$ dominates the characteristics of the CM current reduction performance of 4wDC. More specific analysis is given in the following sections.

5.2.1 Influence of the neutral capacitance and phase inductance on unfiltered 4wDC

According to the former analysis, the neutral capacitance C_{nN} is directly related to the resonance of the transfer function in the LF range, as well as the minimal magnitude of K_{nN4wDC}. Thus the change of C_{nN} will result in the shift of the above mentioned resonance and the minimum of K_{nN4wDC}, while having nearly no influence on the resonance in the

HF range. This phenomenon is plotted based on the motor characteristics of a practical EDS, as shown in Fig. 5.8.

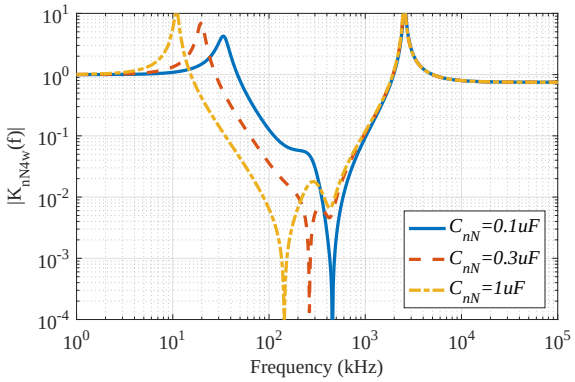


Figure 5.8: Frequency response of K_{nN4wDC} for different value of C_{nN}.

It seems that the shift of low-frequency resonance may improve the CM current reduction performance in the LF range, as the CM current in 4wDC is always seriously reduced after the resonance. However, this requires the increase of C_{nN}. Given the expression of neutral current:

$$I_{nN}(s) = \frac{U_{nN}(s)}{Z_{nN}(s)} \tag{5.27}$$

where Z_{nN} is the neutral impedance. For the case considered in this section, Z_{nN} equals to $1/(s\,C_{nN})$, which means the increase of C_{nN} will also result in larger neutral current (higher loss on the neutral line as well). Therefore, changing the value of C_{nN} alone is not a suitable option for restricting the CM current.

Inserting a CM choke on the power cable at the inverter output (around the three phases), an inductance L_{FCC} will be added between the inverter output and cable input, resulting in the transfer function (5.11). As $s\,L_{FCC}$ keeps enlarging with increasingly higher frequency, it seems that both unwanted resonance of $|K_{nN4wDC}|$ can be attenuated effectively by inserting L_{FCC} that is large enough. However, considering the practical condition, the value of L_{FCC} usually cannot be set to extremely large. Besides, due to the existence of the fourth wire in 4wDC, the sum of three phase current becomes much larger than in three-wire EDS, thus adding the turns on CM choke for higher inductance will easily result in its saturation. Therefore, considering the available value of L_{FCC}, only high-frequency resonance can be seriously attenuated. Again, as an example, the practical EDS in the last section is analyzed with various value of L_{FCC}, as shown in Fig. 5.9.

It can be seen that the HF resonance disappears due to the insertion of a CM choke, and the EDS becomes more competitive in reducing CM current when L_{FCC} increases. This is reasonable as Z_{Ldm} becomes much larger than Z_{Mdm} and tends to be inductive in the HF range, which results in a constant $|K_{nN4wDC\_FCC}|$ there. In the meantime, the insertion of L_{FCC} largely increases the minimum of the denominator when (5.26) is satisfied and dominates the constant $|K_{nN4wDC\_FCC}|$ in the HF range.

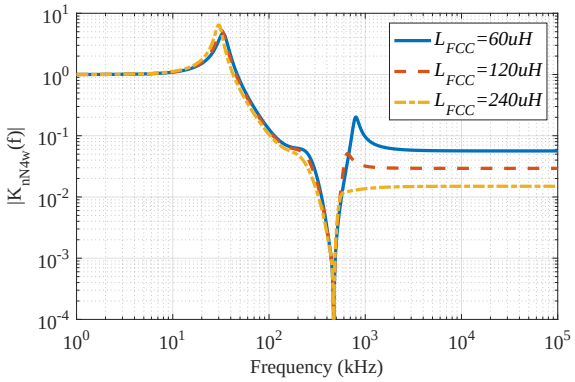


Figure 5.9: Frequency response of K_{nN4wDC_FCC} for different value of the CM choke L_{FCC}.

5.2.2 Filter design: CMMF + Neutral Topology (CMMFNT)

As can be seen in Fig. 5.6, along with the analysis in the former section, CMMF is able to attenuate the HF resonance of $|K_{nN4wDC}|$, and maintain the similar ability of reducing CM current as $|K_{3wF}|$ in the HF range. The only left problem of this filter topology is that it cannot restrict the negative influence of the LF resonance.

Based on the fact that the neutral impedance can seriously influence the LF resonance and changing C_{nN} alone cannot satisfy the demand of reducing CM current, an optimized neutral topology is proposed as shown in Fig. 5.10. The choose of components for the optimized neutral topology follows four relevant criterions, which will be discussed in this section.

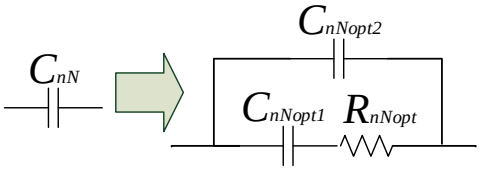


Figure 5.10: Optimized neutral topology.

Neutral current criterion

As known from Fig. 5.10, the neutral impedance of the original topology is:

$$Z_{nN}(s) = \frac{1}{s\,C_{nN}} \tag{5.28}$$

and the impedance of the optimized one is:

$$Z_{nNopt}(s) = \frac{1 + s\,C_{nNopt1}\,R_{nNopt}}{s\,C_{nNopt2}\,(1 + s\,C_{nNopt1}\,R_{nNopt} + \dfrac{C_{nNopt1}}{C_{nNopt2}})} \tag{5.29}$$

According to (5.27), to be sure that the optimized neutral topology will not increase the neutral current, $Z_{nNopt}(s)$ has to be larger than $Z_{nN}(s)$ in most parts of frequency range. Knowing that in the LF range, for a better comparison with $Z_{nN}(s)$, $Z_{nNopt}(s)$ can be treated approximately as

$$Z_{nNoptL}(s) = \frac{1}{s\,C_{nN}\,(\frac{C_{nNopt1}+C_{nNopt2}}{C_{nN}})} \tag{5.30}$$

After a short transition, $Z_{nNopt}(s)$ reaches another stable level in the HF range as

$$Z_{nNoptH}(s) = \frac{1}{s\,C_{nN}\,(\frac{C_{nNopt2}}{C_{nN}})} \tag{5.31}$$

Thus it is obviously that, firstly, C_{nNopt2} and C_{nN} should maintain the relationship

$$C_{nNopt2} < C_{nN} \tag{5.32}$$

From (5.25) and (5.7) it is known that if Z_{nNopt} becomes too small, the four-wire topology will perform like a three-wire one as the neutral line can be treated as "open". Thus it is necessary to maintain Z_{nNopt} as close to Z_{nN} as possible at both HFs and LFs. In the LF range, in addition to the condition (5.32), it is also necessary to fulfill

$$C_{nNopt1} + C_{nNopt2} < C_{nN} \tag{5.33}$$

However, if the sum of C_{nNopt1} and C_{nNopt2} becomes smaller than C_{nN}, according to (5.30), the LF resonant frequency (approximates $1/\sqrt{L_M\,(C_{nNopt1}+C_{nNopt2})}$) will increase, which shifts the CM current peak to higher frequencies and make the filtering start from higher frequencies as well. This is not acceptable as it may largely reduce the effective frequency range of the filter topology. Thus it is better to maintain the sum of C_{nNopt1} and C_{nNopt2} close to C_{nN}, and reduce the value of C_{nNopt2} for less neutral current in general, as shown in (5.34)

$$C_{nNopt1} + C_{nNopt2} \approx C_{nN} \tag{5.34}$$

In summary, to obtain an acceptable level of neutral loss, along with a wider range of effective filtering frequency, C_{nNopt1} needs to be set as close to C_{nN} as possible. Besides, from (5.34) it is also obviously that C_{nNopt2} should always be much smaller than C_{nNopt1}.

Efficiency criterion

According to the analysis of the neutral current criterion, Z_{nNopt} can be treated as $1/(s\,C_{nNopt1})$ in the LF range and $1/(s\,C_{nNopt2})$ at HFs. So according to (5.7), the resonant frequency (f_{res}) must be between the frequency range where ωL_M equals to $3/(\omega\,C_{nNopt1})$

and $3/(\omega\, C_{nNopt2})$, that is

$$\frac{\sqrt{3}}{2\pi\sqrt{L_M\, C_{nNopt1}}} < f_{res} < \frac{\sqrt{3}}{2\pi\sqrt{L_M\, C_{nNopt2}}} \tag{5.35}$$

Referring to Fig. 5.8 and 5.9, filter will not be effective immediately after the resonance. Thus to make sure that filtering starts from the frequency f_{start}, it requires to be set as

$$f_{start} > \frac{\sqrt{3}}{2\pi\sqrt{L_M\, C_{nNopt2}}} \tag{5.36}$$

which leads to

$$C_{nNopt2} > \frac{3}{4\pi^2\, f_{start}^2\, L_M} \tag{5.37}$$

Besides, considering the expected power loss P_{RnN} caused by the neutral topology, along with the fact that the voltage time constant $R_{nNopt}C_{nNopt1}$ is always much smaller than the modulation period, according to [14], C_{nNopt1} should satisfy the condition:

$$C_{nNopt1} > \frac{2\, P_{RnN}}{U_{dc}^2\, f_m\, (1 - e^{-6})} \tag{5.38}$$

where f_m is the modulation frequency, U_{dc} is the dc-bus voltage.

LF resonance criterion

Similar to the analysis in Section II, at the LF resonance, $\omega_{res}\, L_M \approx -3\ \mathrm{Im}(Z_{nNopt}(j\,\omega_{res}))$ for the optimized neutral topology, thus the expression of $|K_{nN4wF}(j\,\omega)|$ turns to:

$$|K_{nN4wFopt}(j\,\omega_{res})| = 3\sqrt{\frac{(Re(Z_{nNopt}(j\,\omega_{res}))^2 + (Im(Z_{nNopt}(j\,\omega_{res}))^2}{(Re(Z_{Mdm}(j\,\omega_{res}) + 3Re(Z_{nNopt}(j\,\omega_{res})))^2}} \tag{5.39}$$

As $|K_{nN4wF}(j\,\omega)|$ equals to 1 before the resonance (see Fig. 5.8), the overshoot of the resonance can be represented by α as:

$$\alpha = |K_{nN4wFopt}(j\,\omega_{res})| - 1 \tag{5.40}$$

Similar to $\mathrm{Im}(Z_{Mdm})$, $\mathrm{Re}(Z_{Mdm})$ around the resonance in the LF range can also be simplified based on the lumped-parameter model of the machine. Therefore, when the expected overshoot of the resonance α is specified where the denominator of (5.39) approaches its minimum at the resonance, under the condition that C_{nNopt1} and C_{nNopt2} have already been given, R_{nNopt} and the resonant frequency f_{res} can be obtained by solving

the equation set:

$$\begin{cases} \omega_{res}\, L_M = -3Im(Z_{nNopt}(j\,\omega_{res})) \\ \alpha = |K_{nN4wFopt}(j\,\omega_{res})| - 1 \end{cases} \tag{5.41}$$

HF resonance criterion

As the existence of inductance between the cable input and inverter output can attenuate the HF resonance of $|K_{nN4wDC}|$ effectively, thus the insertion of CMMF should have even better performance in the HF range, as shown in Fig. 5.6.

According to (5.3), in the HF range, $|K_{3wF}(j\,\omega)|$ can be represented as $R_F/(\omega\, L_F)$. Meanwhile, the imaginary part of cable and motor impedance becomes dominant at HFs, so $|K_{nN4wF}(j\,\omega)|$ is approximated as:

$|K_{nN4wF}(j\,\omega)|$

$$\approx |\frac{3Im(Z_{Ldm}(j\,\omega))}{4Im(Z_{Ldm}(j\,\omega)) + Im(Z_{Mdm}(j\,\omega)) + R_F}|\,\frac{R_F}{\omega\, L_F} \tag{5.42}$$

At HFs, as $\mathrm{Im}(Z_{Ldm}(j\,\omega))$ and $\mathrm{Im}(Z_{Mdm}(j\,\omega))$ tends to be inductive (can be approximated as $\omega\, L_{Ldm}$) and capacitive, respectively, $|K_{nN4wF}(j\,\omega)|$ reaches its maximum

$$\beta = \max(|K_{nN4wF}(j\,\omega)|) = \frac{3L_{Ldm}}{L_F} \tag{5.43}$$

when $4Im(Z_{Ldm}(j\,\omega))$ is close to $-Im(Z_{Mdm}(j\,\omega))$, and then approximates $0.75\,|K_{nN3w}(j\,\omega)|$ in the following. Practically, β represents the maximal percentage of the CM current remaining in the HF range.

Design procedure

Based on the relevant criterion above, the design procedure of CMMFNT for 4wDC is summarized into two parts, one for the optimized neutral topology, while the other for the CMMF. Firstly, the design procedure for the neutral topology of CMMFNT can be concluded as:

1. Based on the expected starting frequency of the filtering f_{start}, determine the C_{nNopt2} according to (5.37), and make it as small as possible in the meantime;

2. Based on the expected power loss of the neutral topology P_{RnN}, determine the value of C_{nNopt1} according to (5.38), besides, considering the value of C_{nN} due to the allowed neutral current, C_{nNopt1} can be determined within the region:

$$C_{nNopt1} < \min(\frac{2\,P_{RnN}}{U_{dc}^2\, f_m\,(1-e^{-6})}, C_{nN} - C_{nNopt2}) \tag{5.44}$$

3. Based on the expected overshoot of resonance α, determine the value of R_{nNopt} through (5.41).

Meanwhile, considering the original design procedure of CMMF for three-wire EDS in [14], along with the new features of 4wDC, the design of CMMF for CMMFNT follows the steps as shown below.

1. Based on the expected value of β (indicated in (5.43)), the inductance L_F can be determined through solving the equations below;

$$\begin{cases} 4\,Im(Z_{Ldm}(j\,\omega)) = -Im(Z_{Mdm}(j\,\omega)) \\ \beta = \dfrac{3\,L_{Ldm}}{L_F} \end{cases} \tag{5.45}$$

2. Based on the expected value of du/dt, as well as the confirmed L_F, determine the value of R_F through

$$R_F < \frac{6 \times 10^6 L_F(\dfrac{du}{dt})}{0.63\,U_{dc}} \tag{5.46}$$

3. Based on the maximal allowed filter-caused power loss P_{Rmax}, determine the value of C_F through

$$C_F < \frac{2\,(P_{Rmax} - P_{RnN})}{U_{dc}^2\,f_m\,(1 - e^{-6})} \tag{5.47}$$

5.2.3 Filter design: CM Choke + Neutral Topology (CMCNT)

Although CMMFNT has the potential to largely reduce the CM current in the whole frequency range, however, the use of conventional CMMF still results in the bulky size of the filter topology. This seriously restricts the application of CMMFNT in EDSs that limited space is left for installing filters. As can be seen in Fig. 5.9, a CM choke with the inductance L_{FCC} placed between the inverter and power cable without parallel capacitors is already capable of attenuating the HF resonance and reducing CM current in the mean time. Thus, another filter topology for four-wire EDSs that consists of CM choke and neutral topology is proposed and named as CMCNT, as shown in Fig. 5.3. The advantage is that the core flux will only depend on the CM current and being consequently much smaller.

Same as CMMFNT, the neutral topology is also required for restricting the LF resonance in CMCNT, thus the selection of components for the neutral topology should follow the same criterion (Neutral current, Efficiency and LF resonance criterion). For the selection of CM choke, the different HF resonance criterion should be followed.

HF resonance criterion

As shown in Fig. 5.9, when a CM choke is inserted, the CM current can be largely reduced, but unlike the CMMFNT that can further enhance the reduction level as the frequency increases, the CM current reaches a resonance and then becomes constant in the HF range.

According to (5.7), when the sum of $4Im(Z_{Ldm}(j\,\omega))$ and $\omega\,L_{FCC}$ is close to $-Im(Z_{Mdm}(j\,\omega))$, $|K_{nN4wFC}(j\,\omega)|$ will reach a peak

$$|K_{nN4wFC}(j\,\omega)| \approx |\frac{3\,Im(Z_{Ldm}(j\,\omega))}{Re(Z_{Mdm}(j\,\omega))}| \tag{5.48}$$

As the cable impedance tends to be inductive ($\omega\,L_{Ldm}$) in the HF range, considering that L_{FCC} is much larger than L_{Ldm}, after the resonance, $|K_{nN4wFC}(j\,\omega)|$ will reach a constant value

$$|K_{nN4wFC}(j\,\omega)| \approx \frac{3\,L_{Ldm}}{4\,L_{Ldm} + L_{FCC}} \tag{5.49}$$

As can be seen in (5.48) and (5.49), the change of L_{FCC} and motor impedance results in the fact that, the maximal value of $|K_{nN4wFC}(j\,\omega)|$ can either occur at the resonance or be the ultimate constant (seen in Fig. 5.9 at about 800 kHz).

Design procedure of CMCNT

According to the analysis above, for the design procedure of the neutral topology, it is exactly the same for both CMCNT and CMMFNT as shown in Section 5.2.2. Besides, the inductance of the CM choke, L_{FCC}, needs to be determined.

Again, base on the expected value of β, the inductance L_{FCC} can be obtained by solving the equation set below:

$$\begin{cases} 4\,Im(Z_{Ldm}(j\,\omega)) + \omega\,L_{FCC} = -Im(Z_{Mdm}(j\,\omega)) \\ \beta = |\dfrac{3Im(Z_{Ldm}(j\,\omega))}{Re(Z_{Mdm}(j\,\omega))}| \end{cases} \tag{5.50}$$

Based on the analysis of section A, the value of L_{FCC} has to be further verified by the expression below:

$$\beta > \frac{3\,L_{Ldm}}{4\,L_{Ldm} + L_{FCC}} \tag{5.51}$$

If the relationship above is satisfied, the inductance L_{FCC} is confirmed. Otherwise, L_{FCC} should be revised and determined based on (5.49), as shown below:

$$L_{FCC} = \frac{3\,L_{Ldm}}{\beta} - 4\,L_{Ldm} \tag{5.52}$$

5.3 Filter design for 4wEL

Unlike the 4wDC topology, for the filter-design analysis of the 4wEL, the experimental setup with 2.2 kW PMSM is used as the example due to its availability of adding the fourth IGBT leg to form the 4wEL. According to [14], the parameters for the CMMF is obtained as $L_{FCC} = L_F = 35\ \mu$F, $R_F = 100\ \Omega$, $C_F = 22\ n$F. It is known from (5.12) and (5.19) that the neutral voltage is influenced by two transfer functions (one for CM voltage and the other for the voltage source on the neutral line), thus both of them should be analyzed extensively. The frequency response of the transfer functions are shown in Fig. 5.11.

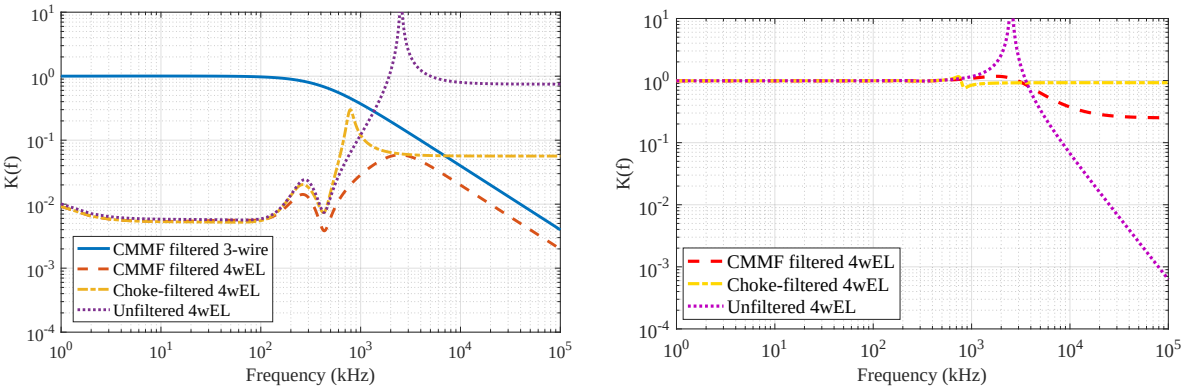


Figure 5.11: Frequency response of transfer function for CM voltage (left) and voltage source on the neutral line (right).

In the left subfigure of Fig. 5.11, for the unfiltered four-wire topology 4wEL, the resulted transfer function for CM voltage causes much more CM current reduction (decrease about 99.5 % of the CM current) than the filtered three-wire topology in the frequency range under 1 MHz. However, the CM current becomes increasingly larger from 1.5 MHz and reaches the maximum due to the resonance at around 2.6 MHz. Finally, the transfer function of the unfiltered 4wEL tends to neither increase nor decrease the CM current in the HF range. The insertion of CMMF or CM choke in the unfiltered 4wEL can largely decrease the CM current existing in the HF range. Specifically, the significant CM current reduction in the LF range can be maintained for the two filtered cases, while the difference starts from 200 kHz. Although the reduction caused by the CM choke turns to be less than that caused by CMMF in the three-wire topology from 7 MHz, however, as the CM current becomes very small from 300kHz upwards, the total filtering is still very effective. Unlike the CMMF filtered 4wEL that can keep enhancing its reduction ability on increasingly higher frequencies, the choke-filtered one reaches a limit from 2 MHz and remains at the level of 1/50 of the neutral voltage rise.

Known from the transfer function for the neutral voltage source (in the right subfigure of Fig. 5.11), the unfiltered 4wEL can seriously reduce the potential CM current caused by the voltage rise during the transition happening on the "neutral" bridge in the very

high-frequency range. However, this is reachable at the price of suffering a huge CM current increase at frequencies around the existed resonance. The use of CMMF can largely attenuate the resonance and maintain the CM current reduction at the level of 25 %, while the CM choke can only remove the negative influence of the resonance.

Therefore, due to the fact that the level of CM current reduction resulted from the choke-filtered 4wEL is already significant for the very small value of CM current from 1 MHz, along with the space and weight that can be saved by the use of CM choke as compared with the corresponding CMMF, the 4wEL filtered by a CM choke is a very reasonable compromise.

Given the frequency response of K_{nN4wEL_FCCcm} in (5.23) with various value of CM choke inductance, as shown in Fig. 5.12, L_{FCC} is found to dominate the CM current reduction in the high-frequency range. Specifically, increasing L_{FCC} can cause more CM current reduction from 500 kHz. Thus the filtering effect of CM choke is very strong and can even be further enhanced by simply increasing the inductance. In summary, the choke-filtered 4wEL can also largely reduce the CM current in a wide range of frequency and requires much less installing space than the traditional CMMF in the EDS.

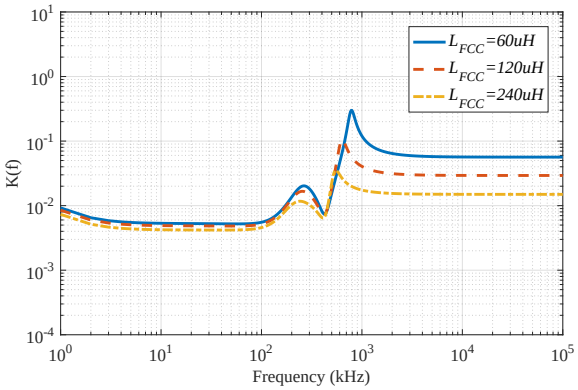


Figure 5.12: Frequency response of K_{nN4wEL_FCCcm} for different values of CM choke inductance.

Unlike the choke filtered 4wDC, the CM choke inductance L_{FCC} is the only parameter that requires to be selected in the choke filtered 4wEL, the selection procedure should follow the HF resonance criterion.

HF resonance criterion

According to (5.23), when the sum of $4Im(Z_{Ldm}(j\omega))$ and ωL_{FCC} is close to $-Im(Z_{Mdm}(j\omega))$, $|K_{nN4wF}(j\omega)|$ will reach a peak

$$|K_{nN4wFC}(j\omega)| \approx |\frac{3Im(Z_{Ldm}(j\omega))}{Re(Z_{Mdm}(j\omega))}| \tag{5.53}$$

As the cable impedance tends to be inductive (represented by ωL_{Ldm}) in the HF range,

considering that L_{FCC} is much larger than L_{Ldm}, after the resonance, $|K_{nN4wFC}(j\omega)|$ will reach the constant

$$|K_{nN4wFC}(j\omega)| \approx \frac{3L_{Ldm}}{4L_{Ldm} + L_{FCC}} \tag{5.54}$$

As can be seen in (5.53) and (5.54), the change of L_{FCC} and motor impedance results in the fact that, the maximal value of $|K_{nN4wFC}(j\omega)|$ can either occur at the resonance or be the ultimate constant.

Design procedure

Again, based on the wanted maximal percentage of the CM current (with respect to the unfiltered three-wire EDS) remaining in the HF range, β, the inductance L_{FCC} can be obtained by solving the equation set below:

$$\begin{cases} 4Im(Z_{Ldm}(j\omega)) + \omega L_{FCC} = -Im(Z_{Mdm}(j\omega)) \\ \beta = |\dfrac{3Im(Z_{Ldm}(j\omega))}{Re(Z_{Mdm}(j\omega))}| \end{cases} \tag{5.55}$$

According to the HF resonance criterion, the value of L_{FCC} has to be further verified by the expression below:

$$\beta > \frac{3L_{Ldm}}{4L_{Ldm} + L_{FCC}} \tag{5.56}$$

If the relationship above is satisfied, the inductance L_{FCC} is confirmed. Otherwise, L_{FCC} should be revised and determined based on (5.49), as shown below:

$$L_{FCC} = \frac{3L_{Ldm}}{\beta} - 4L_{Ldm} \tag{5.57}$$

5.4 Experimental validation

It has to be mentioned that in this section, all measurements are carried out when the experimental EDSs were operated at standstill, where the highest level of CM current flows across the drive system (the worst case).

5.4.1 CMMFNT and CMCNT filtered 4wDC

To validate the capability of the proposed filter design procedure, a series of measurement of CM current across a practical EDS were carried out. The EDS with 60 kW PMSM is used as the experimental setup (Section. 3.2.2). The filter was designed for a maximal current of 100 A, which is less than the motor rated current. The current sensor A6303 from Tektronix (Appendix. A) is used to measure the CM current.

SV-PWM is used and the switching frequency remains at 5 kHz for all the measurements. Using the unfiltered three-wire topology as the reference case, and the measured CM current of this case is plotted in Fig. 5.13 in both time and frequency domain. It can be seen that, the CM current accumulates at the integral multiple of the switching frequency and becomes much smaller from 3 MHz. Meanwhile, there exists two frequency range that contains extremely high value of CM current, one is under 300 kHz and the other between 1.5 and 3 MHz.

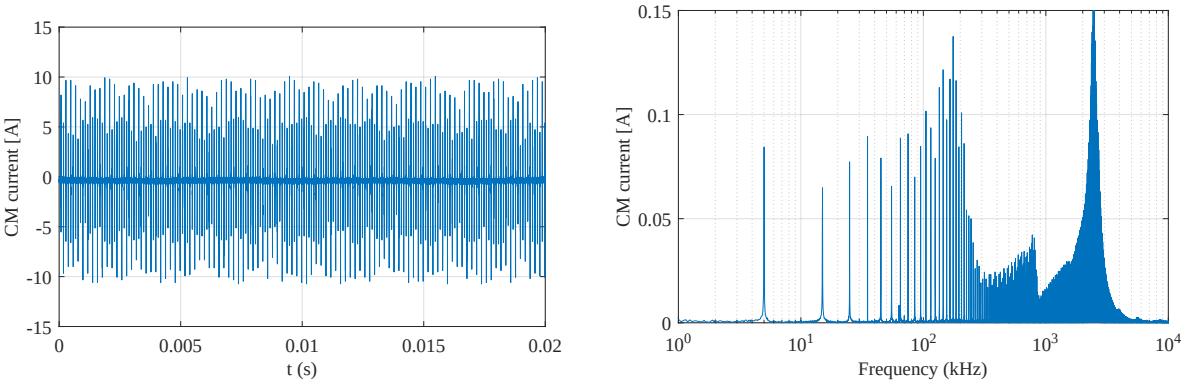


Figure 5.13: Measured CM current in time (left) and frequency domain (right) in the unfiltered three-wire EDS as the reference case.

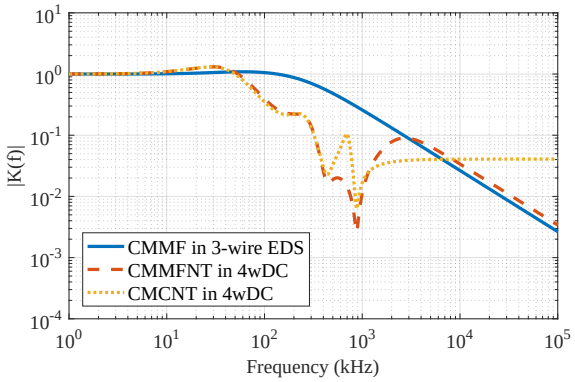


Figure 5.14: Frequency response of transfer function.

Based on the design procedure of CMMFNT and CMCNT, both filter topologies use the same optimized neutral topology with the parameters: $C_{nNopt1} = 0.027\ \mu$F, $C_{nNopt2} = 0.094\ \mu$F, $R_{nNopt} = 100\ \Omega$. To be mentioned, the neutral topology was designed to reduce the overshoot of LF resonance to 20 % ($\alpha = 0.2$) and the neutral current was restricted to 2 A (about 1 % of the rated phase current). Additionally, for CMMFNT, it is designed that 90 % CM current at HFs needs to be eliminated ($\beta = 0.1$), resulting in the parameters of the CMMF as $L_F = 35\ \mu$H, $R_F = 100\ \Omega, C_F = 0.022\ \mu$F. Meanwhile, L_{FCC} was set to be 85μH for CMCNT. Therefore, the frequency response of the relevant transfer functions can be shown in Fig. 5.14. As a comparison, the transfer function of the CMMF filtered three-wire EDS was involved as well. The parameters of the used CMMF

is selected as $L'_F = 60\ \mu$H, $R'_F = 100\ \Omega, C'_F = 0.047\ \mu$F. It is obviously that the optimized design procedure allows CMMFNT to use smaller inductance for a even better filtering effect, and the resulted power loss also turns smaller. In practical, a ring-shape ferrite HF60T80X20X50 from TDK is used as the CM choke L_{FCC}, while L_F and L'_F are given by soft magnetic powder composites (Pot-type cores VA00097 from HKR).

From Fig. 5.14, with the optimized neutral topology, and CMMF or CM choke at the inverter output, both LF and HF resonance of 4wDC are seriously attenuated. Specifically, compared with the three-wire EDS filtered by conventional CMMF, 4wDC with CMMFNT performs better between 50 kHz and 2 MHz, while 4wDC with CMCNT is more effective in reducing CM current til 6 MHz. Although the filtering effect of CMCNT remains constant from 6 MHz, but on one hand, the filtering effect is practically strong enough (eliminating 96 % of the CM current), and on the other hand, the existed CM current in this ultra HF range is actually very tiny already. Besides, CMMFNT is more effective than CMCNT between 400 kHz and 1 MHz and less effective between 1 and 7 MHz. However, this is not the general case as it may vary when the design parameter of the HF resonance criterion of CMCNT changes.

The measured CM current in the CMMF filtered three-wire EDS, CMMFNT and CMCNT filtered 4wDC are shown in Fig. 5.15-5.17, along with their corresponding CM current reduction compared with the reference case (this value should be positive if CM current decreases, or negative when CM current increases). To be mentioned, the CM current reduction is only shown under 1 MHz, as the high values of CM current out of this frequency range is almost eliminated for all filtered cases.

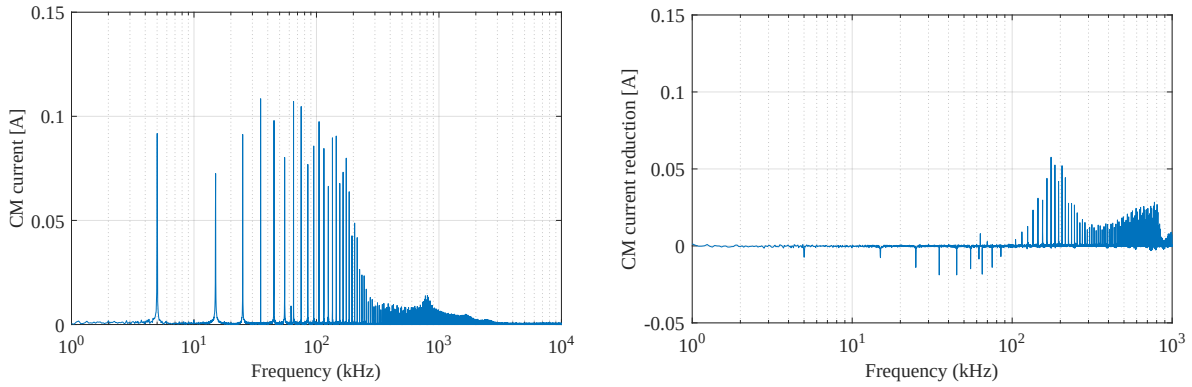


Figure 5.15: CMMF filtered three-wire EDS: measured CM current (left) and corresponding CM current reduction (right).

From the experimental measurement, the CMMF becomes effective from 100 kHz for the three-wire EDS as designed, but the CM current increases slightly under 100 kHz. For CMMFNT and CMCNT, the negative effect of LF and HF resonance on the CM current reduction disappears, resulting in the reduction of CM current in the whole frequency range as shown in Fig. 5.16 and 5.17. Specifically, the filtering effect of CMMFNT is similar

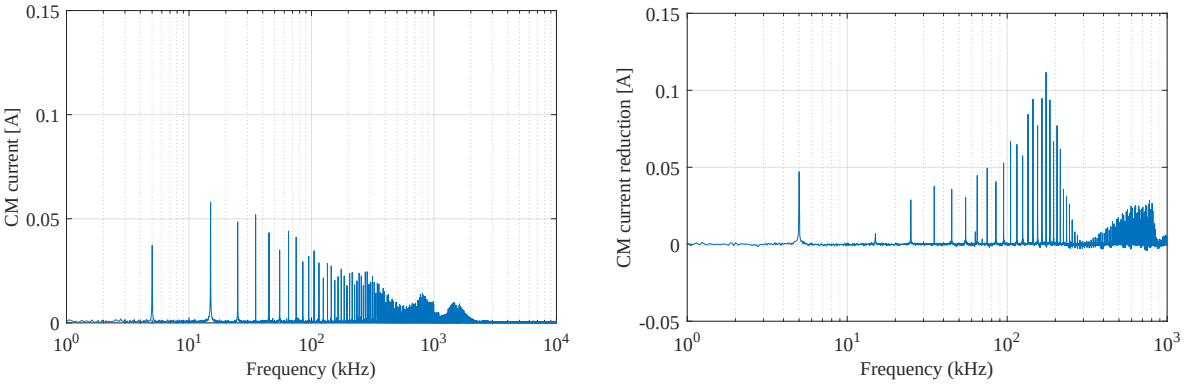


Figure 5.16: CMMFNT filtered 4wDC: measured CM current (left) and corresponding CM current reduction (right).

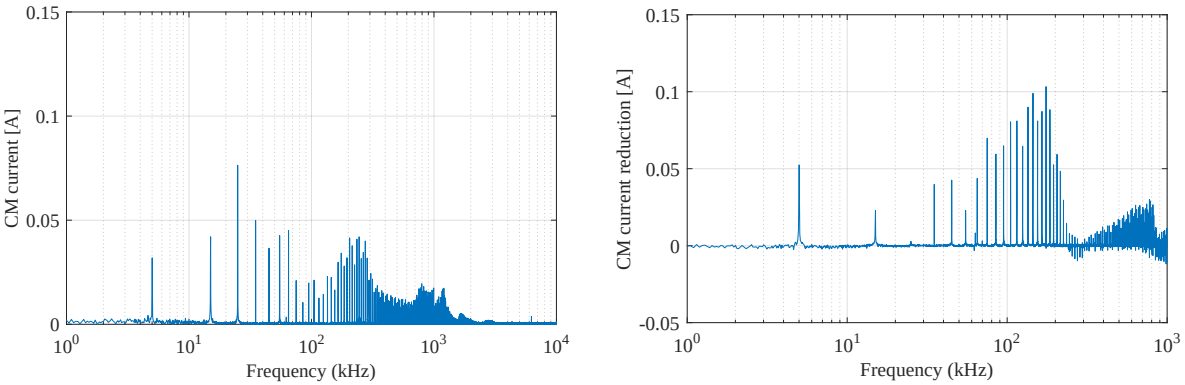


Figure 5.17: CMCNT filtered 4wDC: measured CM current (left) and corresponding CM current reduction (right).

to CMCNT before 300 kHz, and becomes better afterwards. This fits the theoretical analysis well. Meanwhile, considering the RMS value of the measured CM current in the full frequency range, it decreases from 1.05 A to 0.58 A due to the insertion of CMMF in the three-wire EDS. For the 4wDC, this value even reduces to 0.27 A and 0.28 A when CMMFNT and CMCNT is applied, respectively.

Considering the power loss due to the insertion of the filter topology, the power was measured for all cases at standstill, as it is the worst case. The high-precision high-bandwidth power meter LMG670 from ZES Zimmer was used for the measurement. Firstly, it is measured between the inverter and the motor in the unfiltered three-wire EDS (the reference case), including all three phases with respect to ground. Thereafter the power of the filtered EDSs were measured between the inverter and the filter, including the three phases, neutral and for the CMMF also the DC-bus, all with respect to ground. The experimental results are shown in Table. 5.1. It can be seen that the CMMFNT results in a loss around two thirds of the power loss in the CMMF filtered three-wire EDS, while the CMCNT causes even much less power loss (about 13 % of that in the filtered three-wire EDS). Therefore, the power loss caused by the filter in the four-wire EDS is much less

than in the three-wire EDS.

Table 5.1: Power loss of the filter topologies.

Drive topology	Power loss (W)
CMMF filtered three-wire EDS	150.34
CMMFNT filtered 4wDC	100.24
CMCNT filtered 4wDC	19.85

5.4.2 Choke-filtered 4wEL

Similar to the validation procedure of the choke-filtered 4wDC, the validation for the choke-filtered 4wEL were carried out in a practical EDS as well. To be mentioned, the EDS with 2.2 kW PMSM (Section. 3.2.1) is selected as the experimental setup due to its availability of adding the fourth IGBT bridge to form the 4wEL. The current sensor A6303 from Tektronix is used again for measuring the CM current.

Based on the characteristics of the selected experimental setup, along with the filter design procedure, a ring-shape ferrite from TDK is used to form the CM choke with $L_{FCC} \approx 240\,\mu$H. To be mentioned, the resulted power loss can be neglected as compared with that in the CMMF designed for the same practical EDS (about 20 W). Again, the unfiltered three-wire topology is set as the reference, and the measured CM current of this case is shown in Fig. 5.18, in both time and frequency domain. The frequency response of the transfer function for CM voltage in the choke-filtered 4wEL, K_{nN4wEL_FCCcm}, compared with the unfiltered 4wEL, is shown in the right of Fig. 5.19. The HF resonance of the transfer function for unfiltered 4wEL can be largely attenuated by inserting the CM choke, this can be reached at the cost of slightly less CM current reduction in the LF range (from 500 kHz to 1 MHz for the selected experimental setup). To be mentioned, S-PWM is used and the switching frequency is set to 10 kHz for all the measurements in this section. It can be easily seen that the CM current mainly appears at the integral multiple of the switching frequency and turns to be much smaller from around 400 kHz.

Meanwhile, the measured CM current in the unfiltered and choke-filtered 4wEL are shown in Fig. 5.20 and 5.21, along with the corresponding CM current reduction.

In Fig. 5.20, it is known that using 4wEL alone can already largely reduce the CM current in almost the whole frequency range of interest, except for a tiny increase of CM current between 300 and 400 kHz. This fits the theoretical analysis of the transfer function as shown in Fig. 5.18.

From Fig. 5.21 it is obvious that the use of CM choke in 4wEL can further improve the performance of CM current reduction in a wide range of frequency. Specifically, under 300 kHz, the level of CM current reduction increases about 18 %, and the negative performance in the unfiltered 4wEL (the rise of CM current between 300 and 400 kHz)

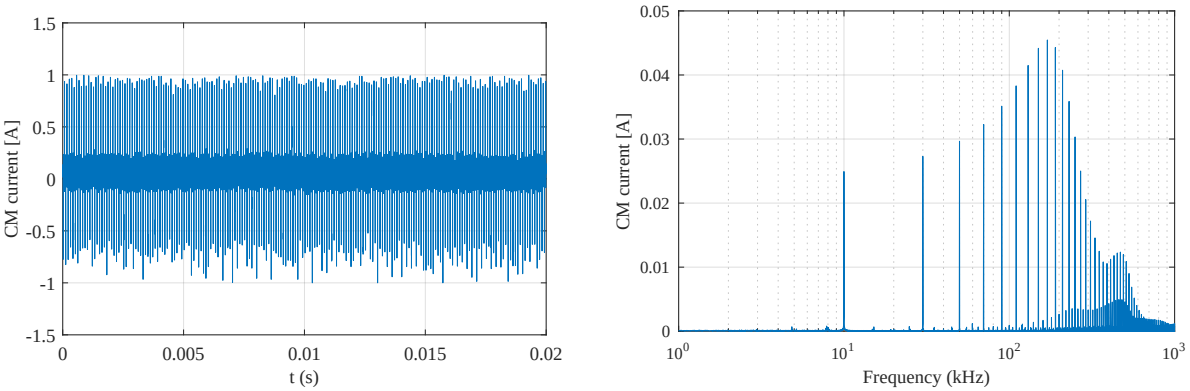


Figure 5.18: Measured CM current in time (left) and frequency domain (right) in the unfiltered three-wire EDS as the reference case.

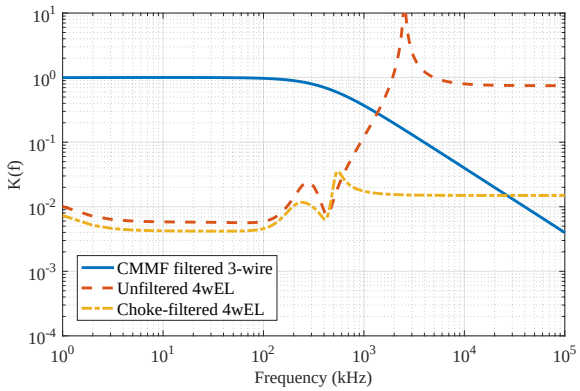


Figure 5.19: Frequency response of transfer functions

does not exist in the choke-filtered 4wEL any more, which enables the reduction of CM current in the whole frequency range. Thus it can be summarized that the choke-filtered 4wEL is an effective optimization for the unfiltered 4wEL, which not only reduces more CM current than the unfiltered situation, but also results in almost no additional power loss to the EDS.

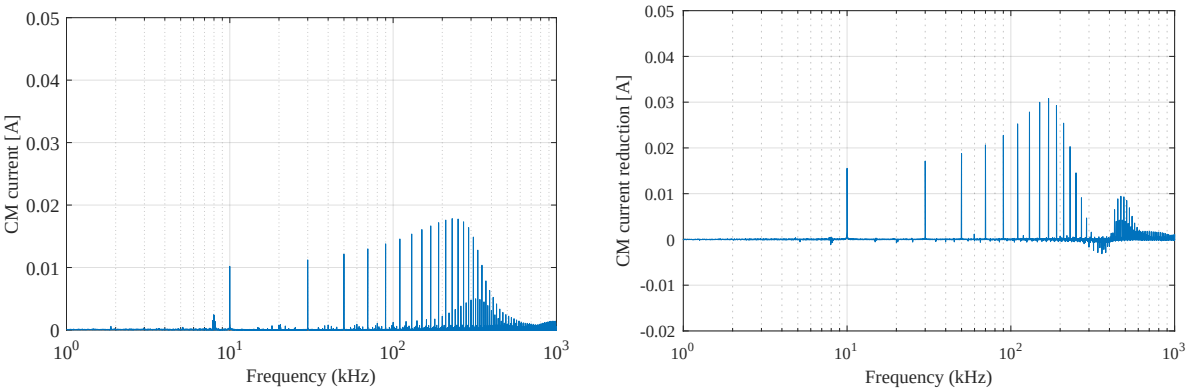


Figure 5.20: Unfiltered 4wEL: measured CM current (left) and corresponding CM current reduction (right).

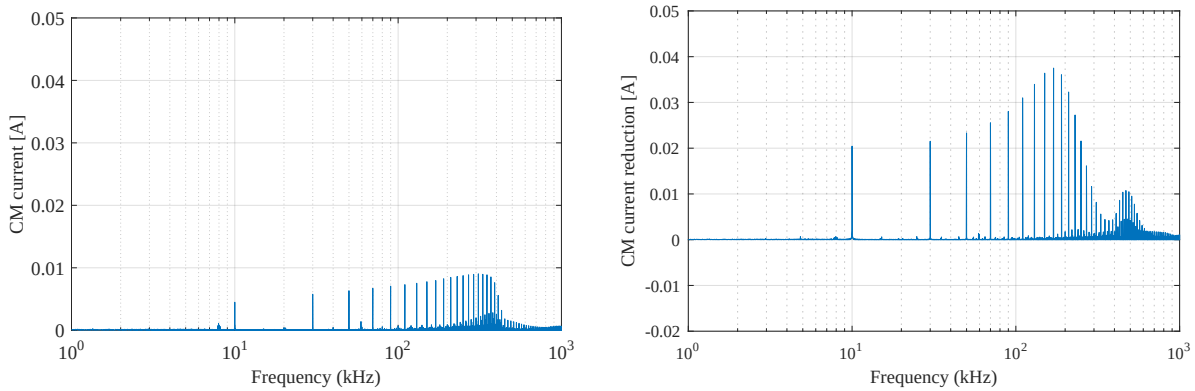


Figure 5.21: Choke-filtered 4wEL: measured CM current (left) and corresponding CM current reduction (right).

5.5 Summary

This chapter has discussed the filter-design procedure of four-wire EDSs. Through the analysis of the relevant transfer function, the level of reduced CM current that can be reached by different filter and EDS topologies has been evaluated. Specifically, for both types of four-wire topology, 4wDC and 4wEL, the transfer function between neutral and CM voltage dominates the CM current reduction. Considering the size and weight, along with the additional power loss brought by the insertion of filter topology, for both 4wDC and 4wEL, the CM choke is selected as an effective solution for the CM current reduction. For the elimination of CM current increase at low frequencies due to the existence of a low-frequency resonance in transfer functions of 4wDC, additional optimization of neutral topology has been designed. This neutral optimization leads to less power loss on the neutral wire. The intact filter topology designed for 4wDC and 4wEL also results in a much less power loss than the conventional CMMF. The effectiveness of the choke-filtered four-wire topology has been validated in the proper experimental setup. The method of analysis through transfer function approach has also been verified and expects to further contribute to the optimization of filter-design for four-wire EDSs.

6 Application of Filter Design and PWM Optimization in the EDS of an Electric Vehicle

In former chapters, the effectiveness of filter-design and PWM optimization in reducing CM current in four-wire EDSs has been discussed and validated experimentally. Based on this, in this chapter, these two CMCRTs will be applied together in the experimental setup with 60 kW PMSM (shown in Section. 3.2.2). To be mentioned, this experimental setup is also designed as one of the prototype EDS used for the drive of an electric vehicle. Firstly, the original three-wire topology of the experimental setup will be modified to a four-wire one. Because the prototype is designed for the conventional control of a three-phase PMSM with concentrated winding, it was not possible to build the four-wire topology 4wEL that requires an additional IGBT bridge. Thus in this chapter only 4wDC will be considered. Then the optimized filter topology as well as the advanced PWM technique (HPS-PWM and VSF-PWM) will be applied together in 4wDC. Finally, the comparison of the CM current reduction when applying these two kinds of CMCRT together or separately will be shown and discussed.

6.1 CM current reduction at standstill

As known that the CM current reaches its maximum when the electric machine is at standstill, this is due to the fact that all three phases are switched on or off simultaneously at this mode, which uses only zero sequence vectors in the whole fundamental cycle. Therefore, the effectiveness of CMCRT at standtill should be considered seriously. In former chapters, it has been confirmed that both CMCRT of filter-design and PWM-optimization can largely contribute to the CM current reduction in the whole frequency range, this positive influence becomes even stronger when the relevant CMCRTs are applied in the four-wire EDSs (both 4wDC and 4wEL). Thus, considering the fact that it is easy to apply both CMCRTs together, the performance of CM reduction when both optimized filter topology (CM choke and optimized neutral topology) and advanced PWM technique (HPS-PWM and VSF-PWM) are applied, will be obtained experimentally and discussed seriously.

As mentioned before, the prototype EDS designed for the drive of an electric vehicle (experimental setup with 60 kW PMSM in Section. 3.2.2) will be used for applying both CMCRTs. the parameters of the optimized filter topology as $C_{nNopt1} = 0.027\,\mu\text{F}$, $C_{nNopt2} = 0.094\,\mu\text{F}$, $R_{nNopt} = 100\,\Omega$ and $L_{FCC} \approx 60\,\mu\text{H}$, can be known from Section. 5.4.1.

As only zero sequence vectors exist at standstill, VSF-PWM will not be active. SVPWN was used with the switching frequency at 10 kHz.

Firstly, the CM current is measured when the conventional unfiltered three-wire topology is applied, as shown in Fig. 6.1. Same as former chapters, this measured CM current from 1 kHz to 10 MHz will be used as the reference for other cases applying CMCRTs. As compared with Fig. 5.13, the increase of switching frequency from 5 to 10 kHz moves the CM current to multiple integrals of 10 kHz, and the magnitude of CM current also increases a lot in the whole frequency range due to more switching actions happen in the same time period. Besides, the CM current becomes much smaller above 3 MHz.

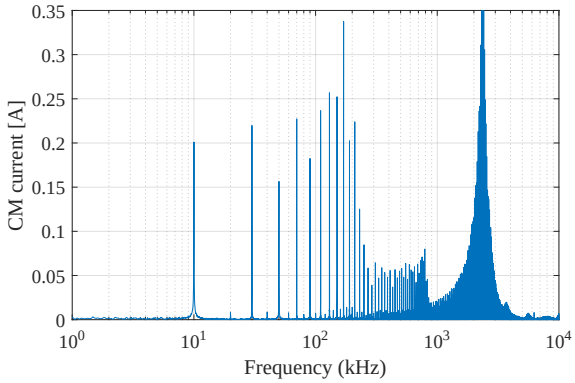
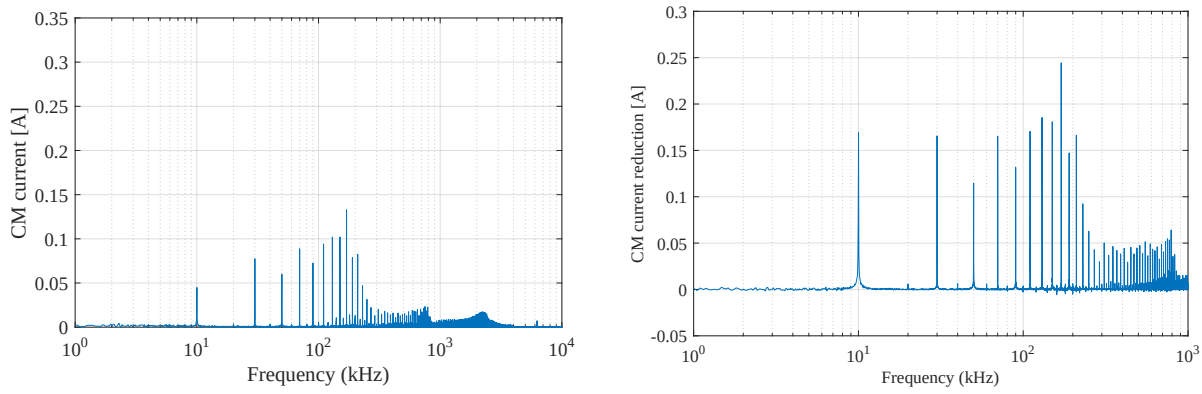


Figure 6.1: Measured CM current in the unfiltered three-wire EDS as the reference case.

Similarly, the CM current reduction is shown between 1 kHz and 1 MHz for a better comparison between cases applying CMCRTs, as the CM current out of this frequency range will be almost eliminated when any of CMCRTs were applied. As the first comparison to see the influence of HPS-PWM on the CM current reduction, the CM current is measured in the unfiltered three-wire topology modulated by HPS-PWM, as shown in Fig. 6.2(a). The corresponding CM current reduction compared with the reference case is also given. It can be seen that the CM current reduces a lot in the whole frequency range due to the application of HPS-PWM, indicating its availability of largely reducing CM current in the unfiltered three-wire EDS as well.

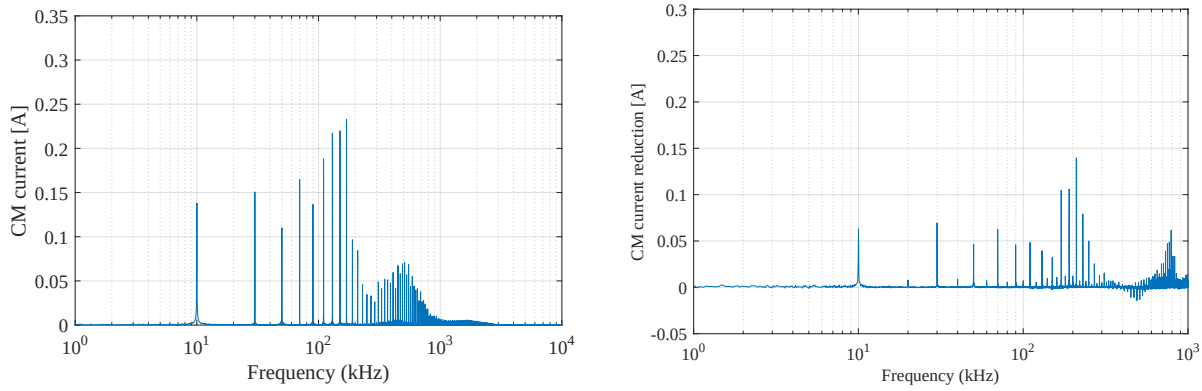
Additionally, for a second comparison, the topology is modified to 4wDC by connecting the neutral point of machine to the negative terminal of DC bus. Due to the high switching frequency (10 kHz), both positive and negative terminals of DC bus can be treated as equivalent to the mid of DC bus. Meanwhile, the CM choke (with inductance of about 60 μH) is placed on the power cables, and also the optimized neutral topology is applied. Again, the CM current is measured in this optimized choke-filtered 4wDC, along with the corresponding reduction of CM current, as shown in Fig. 6.3. To see the CM current caused by the filter topology alone, SV-PWM is applied in this case. It can be seen that through well design of filter topology, along with the application of four-wire topology, the CM current can also be effectively reduced in almost the whole frequency range. When it



(a) (b)

Figure 6.2: Unfiltered three-wire EDS modulated by HS-PWM: (a) Measured CM current; (b) Corresponding CM current reduction.

comes to the level of reduction, the CMCRT of filter-design seems not to be that effective as the use of HPS-PWM at standstill. However, this should be further studied in the future by fully considering the available area and acceptable cost for the build of filter topologies.

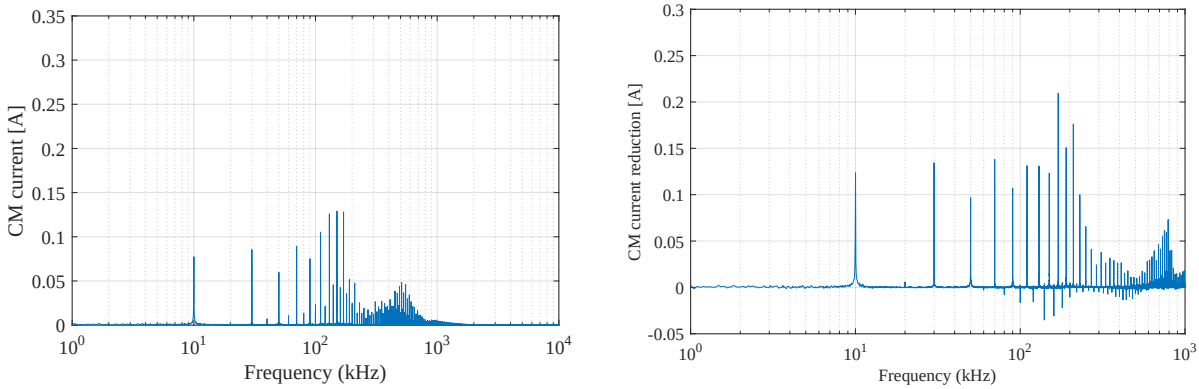


(a) (b)

Figure 6.3: Choke-filtered 4wDC modulated by SV-PWM: (a) Measured CM current; (b) Corresponding CM current reduction.

As the last comparison, the optimized choke-filtered 4wDC is modulated by HPS-PWM, the relevant experimental results are shown in Fig. 6.4. It can be seen that the application of both CMCRTs in the meantime can also result in the large decrease of CM current. When compared with SV-PWM modulated 4wDC, the CM current reduction turns to be much larger in the whole frequency range except for several negative values between 100 and 200 kHz. Meanwhile, there seems to be no significant difference between the measured CM current in the HPS-PWM modulated three-wire and four-wire EDS, which means the application of optimized filter topology as well as the HPS-PWM does not result in the addition of both effects. Specifically, between 180 and 300 kHz, the CM current reduced by

both CMCRTs is larger than that by each of them separately. This indicates that it is still possible to further reduce CM current by applying both filter topology and HPS-PWM together.



(a) (b)

Figure 6.4: Choke-filtered 4wDC modulated by HPS-PWM: (a) Measured CM current; (b) Corresponding CM current reduction.

In summary, although it is simple to apply both methods, namely the filter-design and PWM-optimization in the same four-wire EDS, but the influence of this attempt on the resulting CM current reduction is not simply an answer if the effects of both are added up. The exploration of interaction between the filter topology and the applied PWM technique is a necessary step for a better use of both CMCRTs.

6.2 CM current reduction at constant-speed

In the last section, the CM current reduction resulting from both CMCRTs has been studied considering the motor is at standstill. This really makes the sense as it is the operation mode that the worst case of CM current happens in the EDS. But most frequently, EDSs operates at the speed mode, either variable or constant. Due to the reality that even if the electric machine operates at variable speed, at any specific moment, the machine can be treated as operating at a constant speed, thus the performance of CM current reduction of CMCRTs when the EDS is operating at a constant-speed needs to be studied in detail.

The only difference between the experimental condition at constant-speed and standstill is given by making the 60 kW PMSM operating at the speed of 500 rpm. Besides, as the machine starts rotating, vectors other than zero sequence vector appear in each switching cycle, thus VSF-PWM can be effective under this operation mode.

Similarly, the CM current measured in the conventional unfiltered three-wire EDS is used as the reference, as shown in Fig. 6.5. Compared with the case that the electric machine is at standstill, CM current becomes less in the whole frequency range as expected

and the high level of CM current above 1 MHz also disappears at the constant-speed mode.

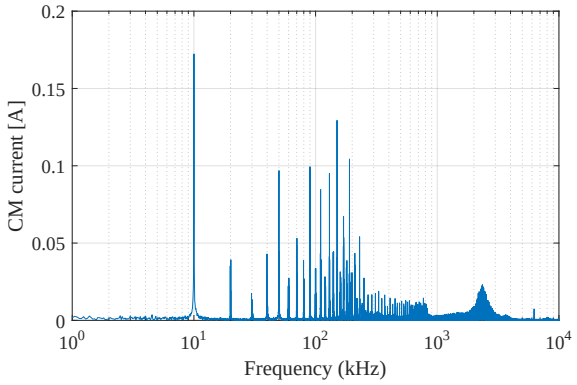
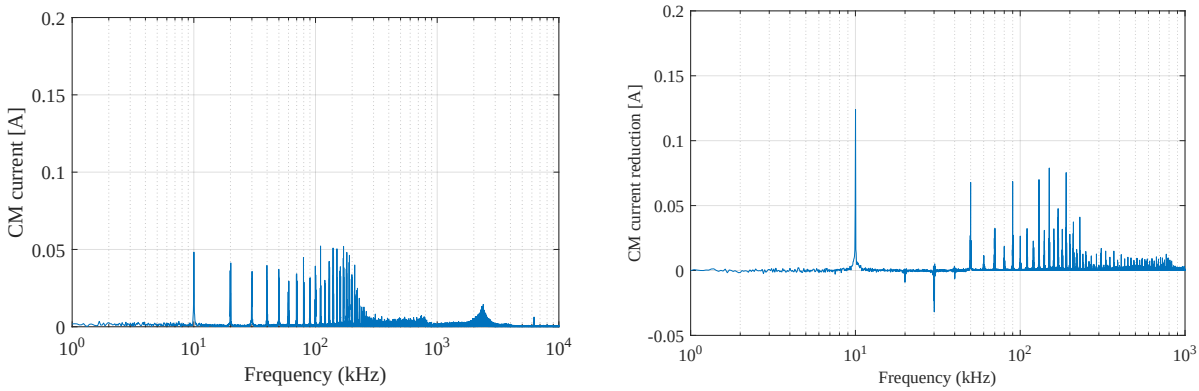


Figure 6.5: Measured CM current in the unfiltered three-wire EDS as the reference case.

Again, the HPS-PWM modulated unfiltered three-wire topology is used as the first comparison, with the measured CM current and the corresponding reduction shown in Fig. 6.6. As can be seen, except for the frequencies between 20 and 40 kHz, the CM current decreases in the whole frequency range. As it is expected, the HPS-PWM is not as effective as for the standstill mode in reducing CM current in the whole frequency range. This is mainly due to the fact that the application of single phase-shift turns to be the most effective when only zero sequence vectors exist in the switching cycle. As the machine starts to rotate, other effective vectors appear and replace part of the zero sequence vectors. This phenomenon will become increasingly more visible as the speed keeps increasing.

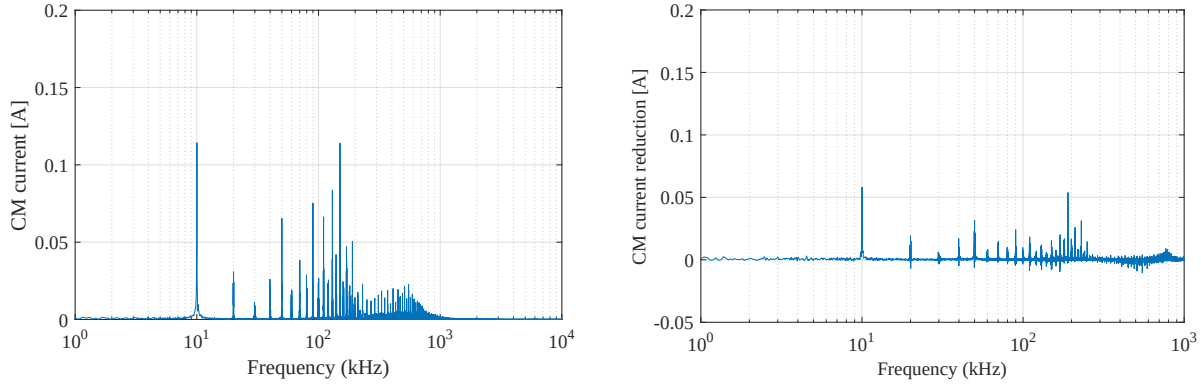


(a) (b)

Figure 6.6: Unfiltered three-wire EDS modulated by HS-PWM: (a) Measured CM current; (b) Corresponding CM current reduction.

Given the measured CM current and the corresponding reduction of it in Fig. 6.7. The insertion of filter topology into the four-wire topology 4wDC results in less CM current in most frequencies as expected. Similar to the standstill mode, the level of the CM current

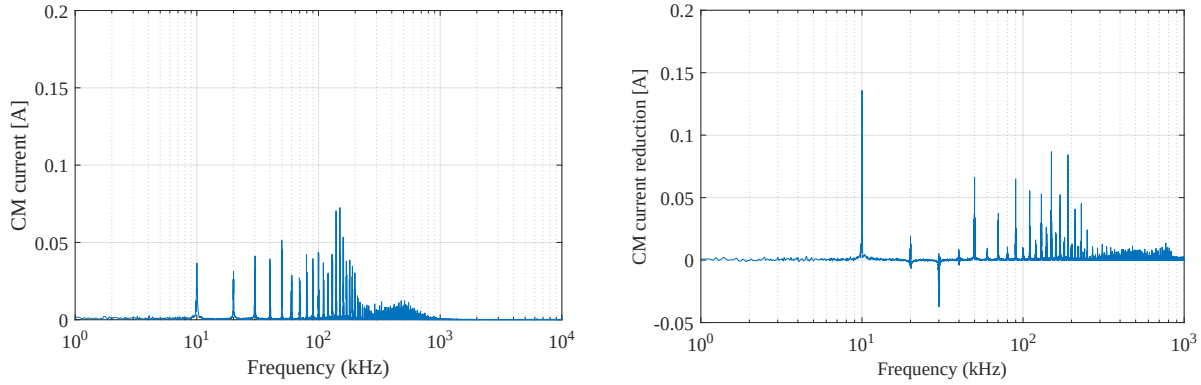
reduction caused by the optimized filter topology is incomparable to that brought by the utilization of HPS-PWM. Besides, the filter topology also becomes obviously less effective in reducing the CM current.



(a) (b)

Figure 6.7: Choke-filtered 4wDC modulated by SV-PWM: (a) Measured CM current; (b) Corresponding CM current reduction.

Lastly, the HPS-PWM modulated 4wDC with CM choke and optimized neutral topology is discussed for its effectiveness of reducing CM current. In Fig. 6.8(a), the measured CM current of this case has been given. It is similar to the case of standstill that the insertion of filter topology in addition to the application of HPS-PWM does not make obvious difference to the level of CM current reduction. In the meantime, the slight increase of CM current in the unfiltered three-wire EDS between 20 and 40 kHz is not improved by the use of filter and four-wire topology. But, again, at some frequencies (eg. 10 kHz, from 100 to 200 kHz), further reduction of CM current has been realized through applying both CMCRTs.



(a) (b)

Figure 6.8: Choke-filtered 4wDC modulated by HPS-PWM: (a) Measured CM current; (b) Corresponding CM current reduction.

However, although the CM current cannot be further reduced significantly, the applica-

tion of VSF-PWM still has the potential to largely decrease the peaks of measured CM current. Given the comparison of CM current measured before and after applying VSF-PWM in 4wDC (with optimized filter and neutral topology, modulated by HPS-PWM), as shown in Fig. 6.9. It can be seen that VSF-PWM is still very effective in reducing the existing CM current at multiple integral of switching frequency, as well as transferring it to adjacent frequencies. The insertion of filter topology does not influence this effect as well. Therefore, unlike the interaction between the filter topology and HPS-PWM that can bring either positive or negative to the reduction of CM current, the application of VSF-PWM seems to be much more independent so that its availability of controlling CM current remains strong all the way around.

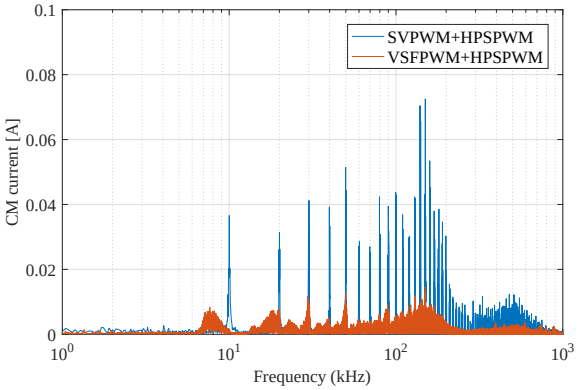


Figure 6.9: Comparison of CM current measured before and after applying VSF-PWM in HPS-PWM modulated 4wDC.

In summary, similar as the cases at standstill, there must exist interaction between the two CMCRTs, which integrates their ability of reducing CM current at some frequencies, while weakens this ability of one or both CMCRTs at some other frequencies. Although the performance of CM current reduction of both CMCRTs becomes less effective when the machine operates at a constant speed, the interaction between the filter topology and HPS-PWM still influences the CM current reduction in the whole frequency range. Meanwhile, when VSF-PWM is applied, its effect of reducing and moving the peak of CM current still remains strong.

6.3 Summary

Considering the positive influence of both filter-design and PWM-optimization in reducing CM current, along with the convenience of applying them together in the same EDS, the application of these two CMCRTs in a prototype EDS designing for the drive of an electric vehicle has been discussed in this chapter. Two most frequently used operation mode, standstill and constant-speed, have been involved in the discussion, respectively.

When the electric machine is at standstill, the application of HPS-PWM and the

insertion of filter topology can both significantly reduce CM current in the whole frequency range. The CM current reduction caused by HPS-PWM is higher than that resulting from filtering procedure in consideration of the limitation of intalling an additional topology to the conventional drive system. Considering the CM current reduction by applying both filter topology and HPS-PWM in 4wDC, there exists interactions between each of two CMCRTs. These interactions have considerable influence on the CM current reduction resulting from CMCRTs. Specifically, in the whole frequency, CM current can be further reduced by applying both CMCRTs at some frequency points, while can even increase at some other frequencies.

For the constant-speed mode, filter-design and PWM-optimization can also effectively reduce CM current. The level of reduction becomes lower at this operation mode for both CMCRTs. Similar to the standstill mode, HPS-PWM is more effective than filter-insertion in reducing CM current. There exists interactions between both CMCRTs when they are applied in 4wDC. These interactions can also influence the value of CM current differently at various frequencies within the whole frequency range. However, the application of VSF-PWM does not interact with HPS-PWM, changed drive topology as well as the inserted filter circuit, which results in its significant ability of reducing and transferring the CM current peaks.

7 Conclusions and Future Work

7.1 Conclusions

As introduced in the first chapter, the ever increasing utilization of three-phase EDSs in the field of electrified transportation leads to numerous studies of improving their operation performance. However, many of these improvements also result in the increase of CM current that can bring negative influence to the performance of EDSs, or even cause physical damage to them. Thus numerous research has been carried out for lowering the CM current while resulting tiny or even no negative influence to the performance of EDSs. Most of these researches can be involved into the two main directions, filter-design and PWM-optimization. Meanwhile, optimization of conventional three-phase three-wire topology has also been widely researched for either bringing useful new functions or lowering the size, the loss and the building cost of EDSs. One of the most significant optimization of the drive topology is modifying the traditional topology to a four-wire topology through connecting the neutral of electric machine to the mid of dc bus (4wDC) or the output of the fourth leg of inverter (4wEL). Former studies has shown that this four-wire topology can well support the realization of sensorless control as well as fault-tolerant operation of EDSs.

In Chapter 2, an overview of former studies of filter-design and PWM-optimization has been given firstly. For the design of the filter topology, there are mainly two types, passive and active filter. Specifically, the build of passive filters requires only passive components like resistor, capacitor and inductor. Thus this kind of filters are very cost effective and easy to install, while the size of filter topologies may become too bulky for a better filtering effect. Taking advantages of active components, active filters can be designed to be much more effective in producing filtering effect in any wanted frequency ranges. However, this also leads to a much higher cost of building an effective active filters. When it comes to the optimization of PWM techniques, this way of reducing CM current has an obvious benefit of requiring no additional electronic components to be added in the drive topology. But the optimization of conventional PWM algorithm eg. SV-PWM and S-PWM has been found to have the possibility of damaging the operation stability of EDSs or requiring much more calculation effort of the micro-controller. Thus it is a basic requirement for attempts of modifying PWM algorithm to enhance the EMC performance of EDSs while maintaining or even improving their original operation performance. Lastly, the development of four-wire EDSs in recent years has been illustrated in detail. Due

to the countless endeavor for the ever improving strategy of realizing useful functions like sensorless control and fault-tolerant operation (also requires fast, accurate detection and prediction of all kinds of fault that happens frequently in EDSs), four-wire EDSs has shown their unique advantage comparing with conventional EDSs in some applications. Thus all these overviews emphasize the necessity and importance of evaluating the level of flowing CM current in four-wire EDSs, as well as developing proper CMCRTs for them.

The research methodology of analyzing the origin and coupling route of CM current in a EDS has been introduced in Chapter 3. Firstly, the transfer function approach is chosen as the theoretical foundation for the analysis of the flowing CM current in different drive systems. It is found that the voltage rise of neutral and phase voltage is the main reason for the existing CM current. Through the comparison of the transfer function between inverter output and neutral/phase voltage of conventional three-phase and four-wire EDSs (both 4wDC and 4wEL), several conclusions can be obtained. One is that the insertion of CMMF to three-phase EDSs changes the transfer function from unity to a damping equation that behaves as a low-pass filter. Another obtained conclusion is that four-wire EDSs alone already has a damping behaviour in its transfer function, this shows the advantage of four-wire EDSs with always less CM current as compared with corresponding three-wire EDSs. Thus the way of using transfer function for analyzing CM current is of great importance. For the experimental verification of the theoretical analysis, two experimental setups, with 2.2 kW and 60 kW PMSM as traction machine, respectively, have been presented. Both of them are well-structured practical EDSs that consists of load and traction machine, inverters and self-designed controller board. Because both of them are self-built, it is very convenient to do modifications on them, which fits perfectly the requirement of applying all kinds of CMCRT for obtaining their performance of CM current reduction. The experimental setup with 60 kW PMSM is also one of the prototype EDS designed for the drive of an electric vehicle. Although the other experimental setup is with much less driving power, but it is even more flexible for modification that it is the only setup that can form the 4wEL (requires an additional IGBT leg) in this study. Meanwhile, the relevant parts of the soft and hardware architecture has also been briefly introduced.

For the reduction of CM current in four-wire EDSs, the way of PWM optimization has been discussed in the fourth chapter. Phase-shift and real-time switching frequency variation, which have been researched only in three-wire EDSs until now, are the selected strategy for the PWM-optimization. Considering the summarized advantages and disadvantages of three phase-shift PWM technique that shifts the phase with longest, shortest or mid triggering time, the HPS-PWM is proposed for the first time in this study. The use of HPS-PWM in 4wDC can result in further reduction of CM current in the whole frequency range than the use of traditional SV-PWM in this four-wire topology. At both standstill and constant-speed condition of the electric machine, the level of CM current

reduction maintains strong. Meanwhile, the use of HPS-PWM in 4wEL also reduces more CM current than the S-PWM modulated EDS at standstill, but the resulted CM current reduction under constant-speed condition is similar except for low frequencies. For the application of VSF-PWM, the current ripple has to be predicted precisely in advance. Through the analysis of the difference between three- and four-wire topology, some modification has been done to the original expressions of predicting the current ripple. Based on the updated ripple prediction expressions, VSF-PWM has been applied in both 4wDC and 4wEL and the peak of CM current all reduces and transfers to adjacent frequencies. This phenomenon becomes stronger in the high frequency range. Besides, the combination of VSF+HPS-PWM has been found to require much less calculation effort of micro-controller. This is due to the less expressions required for the current-ripple prediction in each sector of the fundamental cycle. For 4wDC modulated by SV-PWM, the total amount of prediction expressions is eighteen. It could be shown, that this value decreases sharply to six for HPS-PWM modulated 4wDC. The S-PWM modulated 4wEL also requires only six expressions for the prediction, but when the EDS is modulated by HPS-PWM, this value can be further reduced (two and four expressions for HPS-PWMN+ and HPS-PWMN-, respectively). In addition, switching loss caused by the combination of VSF+HPS-PWM also turns to be less than the combination of VSF+SV-PWM (4wDC) or +S-PWM (4wEL). Specifically, for 4wDC, VSF+SV-PWM reduces 2 % of the switching loss, while VSF+HPS-PWM reduces the loss for 10 %. For 4wEL, VSF+S-PWM is already with 9 % less of switching loss, however, this value can reach 12 % for VSF+HPS-PWMN- and even 22 % for VSF+HPS-PWMN+.

Another CMCRT, design of filter topology, has been discussed in Chapter 5 for the CM current reduction in four-wire EDSs. The limitation of the well known CMMF in three-wire EDSs appears when the effective filtering is expected in lower frequencies. Normally, moving the boundary of filtering effect to a little bit lower frequency needs significantly bulkier filter topology, which will not be possible for most commercial EDSs. Through the analysis of the relevant transfer function, the level of CM current reduction that can be reached by different filters and EDS topologies has been evaluated. Specifically, for both type of four-wire topologies, 4wDC and 4wEL, the transfer function between neutral and CM voltage dominates the CM current reduction. Because of the much stronger coupling route of neutral voltage, it is treated as the main source of CM current in four-wire EDSs. Although the four-wire drive topology alone already has a damping behaviour in transfer function, but its filtering effect becomes worse in the high frequency range so that results in even more CM current there, thus the insertion of filter topologies still makes sense. Considering the size and weight, along with the additional power loss brought by the insertion of filter topology, for both 4wDC and 4wEL, the CM choke is selected as an effective solution for the CM current reduction. However, the increase of CM current due to the existence of low-frequency resonance in 4wDC cannot be removed

by the filter topology installing on power cables. Therefore, an optimized neutral topology has been proposed, which eliminates the unwanted resonance in the low-frequency range while brings no influence to the filtering effect of the inserted CM choke. The effectiveness of the choke-filtered four-wire topology has also been validated in the experimental setup. The method of analysis through transfer function approach is also verified and expects to further contribute to the optimization of filter design for four-wire EDSs.

Lastly, in Chapter 6, the CM current reduction caused by the application of both filter topologies and optimized PWM techniques has been evaluated in the EDS designed for an electric vehicle. Due to the limitations of this target EDS, only the 4wDC topology is considered. Standstill and constant-speed modes of operation were tested on the electric machine. For a reasonable comparison, not only the measured CM current and its corresponding CM current reduction in the 4wDC with both CMCRTs were obtained, but also the experimental results in the choke-filtered 4wDC and the three-wire topology with HPS-PWM. There exists interaction between the filter topology and the application of HPS-PWM. Due to this interaction, CM current can be further reduced at some frequency points by applying both CMCRTs, while can even increase at some other frequencies. When it comes to the constant-speed mode, the level of CM current reduction becomes lower for both CMCRTs, considering the less existing CM current at this operation mode. Similar to the standstill mode, an interaction exists when both CMCRTs are applied in 4wDC and influences the value of CM current differently in various frequencies. However, the application of VSF-PWM does not interact with HPS-PWM, changed drive topology and the inserted filter circuit, which results in its maintaining significant ability of reducing and transferring the CM current peaks. This also means applying VSF-PWM along with all other CMCRTs is always an advisable option.

7.2 Future Work

Based on the obtained results of this dissertation, some future work for the extension of the study is recommended as below:

1. Further optimization of both CMCRTs in 4wEL

   The fourth leg in 4wEL has shown its potential of influencing the reduction of CM current in the whole frequency range. The influence of modifying the neutral topology of 4wEL remains unclear. Thus inserting a properly designed filter to the neutral wire could be one direction of future work. The difficulty may be the requirement of not affecting the performance of fault-tolerant operation of the EDS. Besides, for the optimization of PWM techniques, adjusting the duty cycle of the "neutral phase" could be another good attempt. It can be expected that the duty cycle should keep updating to reach the best performance of CM current reduction.

2. Discussion of interaction between both CMCRTs in 4wEL

   Due to the limitation of the experimental setup, the CM current reduction that could be reached by applying both CMCRTs in a high-power 4wEL remains unknown. Whether the existing interaction between both CMCRTs in 4wDC also makes sense in 4wEL will be of great meaning. As a compromise, it will be a reasonable first step to carry out this experiment in the experimental setup in Section. 3.2.1. The possible difficulty could be that it is hard to recognize the influence of the interaction due to the much less CM current flowing in the low-power 4wEL.

3. Research of the interaction between CMCRTs

   As known from the experiment done in 4wDC, there exists unknown interaction between both CMCRTs. this interaction can be either helpful or harmful to the reduction of CM current. Thus further effort could be made to explore the specific cause of this interaction, as well as the detailed influence on the CM current. This future attempt is meaningful as it may provide hints of a reasonable combination of the effective filter-design and PWM-optimization CMCRT.

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A Current Sensor A6303 from Tektronix

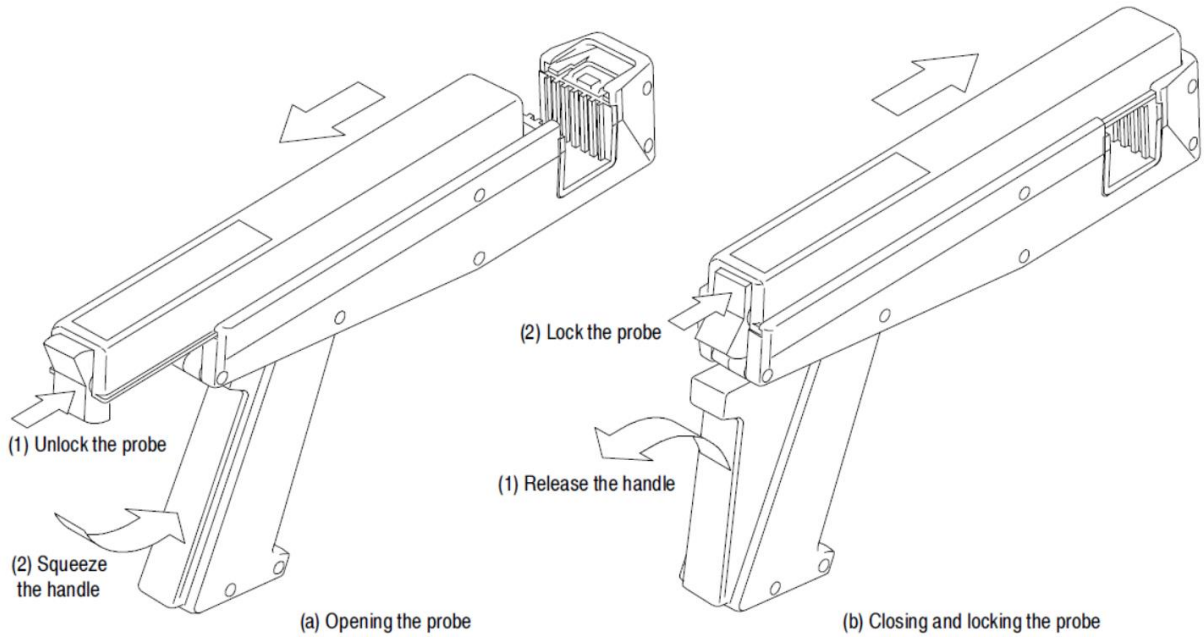

Figure A.1: Operating the probe slide.

Table A.1: Electrical Characteristics.

Bandwidth (-3 dB)	DC to 15 MHz
Rise Time (10 % to 90 %)	$\leq$ 23 ns
Frequency Derating	12 A at 10 MHz
Maximum Bare Wire Working Voltage	600 V_{RMS}, CAT II 300 V_{RMS}, CAT III
Maximum Continuous Current	100 A (DC + peak AC)
Maximum Pulsed Current	500 A
Amp. Second Product	1×10^{-2} $A.s$(10000 $A.\mu s$)
Insertion Impedance	0.02 Ω at 1 MHz 0.15 Ω at 1 MHz

Table A.2: Mechanical Characteristics.

Probe Dimensions	Length: 26.8 cm (10.6 inches) Width: 4.05 cm (1.6 inches) Height: 15.6 cm (6.13 inches)
Cable Length	2 m (6.6 feet)

Table A.3: Mechanical Characteristics.

Operating Temperature	0^o C to 50^o C
Storage Temperature	-40^o C to 75^o C
Humidity: Nonoperating Operating	 30^o C to 60^o C at 90 to 95 % RH 30^o C to 50^o C at 90 to 95 % RH
Altitude: Operating	 2000 m (6416 ft)
Transportation	Qualifies under National Safe Transit Procedure 1 A, category II, 36 in. drop
Mechanical Shock	500 g. Half sine. Three shocks on three of the probe for 1 ms duration. Total of 9 shocks.
Vibration	0.025 in. pk-pk displacement. 10 - 50 Hz in 1 min. cycles. Hold 9 min. at any major resonance, or if none, at 55 Hz. Total time, 54 min.
Random Vibration: Operating	 0.31 g_{RMS}, 5 to 500 Hz, 10 minutes on each axis. Tektronix Std. 062-2858-00, Rev. B, Class 3.

Declaration of Honor

„I hereby declare that I produced this thesis without prohibited external assistance and that none other than the listed references and tools have been used. I did not make use of any commercial consultant concerning graduation. A third party did not receive any nonmonetary perquisites neither directly nor indirectly for activities which are connected with the contents of the presented thesis.

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Magdeburg, 26.10.2020

List of Publications

Journal articles

[1] Z. Zhao, M. Leone, "On the Radiated Susceptibility of a Two-Wire Transmission Line under Near and Far-field Conditions", *IEEE Trans. Electromagn. Compat*, vol. 60, pp. 1348 - 1356, 2018.

[2] Z. Zhao, R. Leidhold, "Investigation of Current-Ripple for Three-Phase Four-Wire Inverter-Fed Motors", accepted by *Energy Reports*, vol. 6, pp. 330 - 337, 2021.

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