Fabrication and Investigation of Three-dimensional Ferroelectric Capacitors for the Application of FeRAM

Dissertation

zur Erlangung des akademischen Grades

Doktoringenieur

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Zusammenfassung

Das Ziel der Arbeit in der vorgelegten Dissertation ist, mehrere notwendige Technologien für ferroelektrische Kondensatoren, die Schlüsselkomponente der FeRAMs zu entwickeln und die Eigenschaften von damit hergestellten ferroelektrischen Kondensatoren zu untersuchen. Zunächst wird in Kapitel 1 der Zustand der gegenwärtigen Halbleiterspeicherbauelemente zusammengefasst und die potenzialen Kandidaten für die Zukunft werden vorgestellt. Eine Einführung von ferroelektrischen Materialien und eine Überblick des aktuellen Status der FeRAMs werden in Kapitel 2 gegeben. Die folgenden Kapiteln sind fokussiert auf: Kapitel 3, Untersuchungen der ferroelektrischen PZT-Dünnschichtabscheidung mit neuen Präkursoren. Kapitel 4, Untersuchungen des reaktiven Ionenätzens des Iridium-Elektrodenmaterials. Kapitel 5, Untersuchungen der Abscheidung von Iridium als Elektroden in drei-dimensionalen Strukturen. Kapitel 6, Realisierung und Charakterisierung von drei-dimensionalen ferroelektrischen Kondensatoren.

In dieser Arbeit konnten die unten aufgeführten Zielstellungen erreicht werden:

(1) Ein MOCVD-PZT-Dünnschichtabscheidungs-Prozess auf Ir Substraten mit neuartigen Zr und Ti Präkursoren wurde entwickelt. Die PZT-Filme, die bei 450/500/550°C abgeschieden wurden, sind ferroelektrisch und die Filme, die bei 500/550°C abgeschieden wurden, zeigen gute remanente Polarisationen.

(2) Reaktives Ionenätzen von Iridium mit einer Al-Maske und CF_4/O_2/Ar Gasmischungen wurde entwickelt. Höhere Ätzraten wurden bei erhöhten Substrattemperaturen erreicht. Eine hohe Selektivität zwischen Iridium und der Al-Ätzmaske wurde erhalten.

(3) Ein Abscheidungsverfahren für Ir-Dünnschichten auf 3D-Strukturen wurde unter Verwendung von plasmaunterstützter MOCVD entwickelt. Bei ausreichender Qualität der Ir-Schichten für die Anwendung als Elektroden von 3D-Kondensatorstrukturen wurden annehmbare Kantenbedeckung und Oberflächenmorphologie erreicht.

(4) Ir/PZT/Ir ferroelektrische Kondensator-Stapel auf 3D-Strukturen wurden realisiert. Die 3D-Kondensatoren zeigen gute ferroelektrische Eigenschaften, die mit 2D-Kondensatoren vergleichbar sind, haben aber höhere Leckströme als 2D-Kondensatoren und neigen bei Zykel-Testen stärker zu Ausfällen.

Nach Zusammenfassung der Ergebnisse dieser Arbeit können einige Schlussfolgerungen für die künftige Arbeit gegeben werden:

Obwohl die bei 450°C abgeschiedenen PZT-Filme ferroelektrisch sind, sind ihre remanenten Polarisationen zu niedrig. Weitere Verbesserungen ihrer Qualität sind erforderlich. Eine weitere Reduzierung der Abscheidungstemperatur erhöht die Kompatibilität zu herkömmlichen CMOS-Prozessen. Um mit anderen Speicherbauelementen zu konkurrieren, ist auch eine Reduzierung der Schichtdicke von PZT unter 50nm in 3D-Kondensatoren erforderlich. Ungleichmäßige Pb Gehalte, inhomogene Mikrostrukturen und teilweise kristallisierte Phasen in PZT-Filmen können für die ferroelektrischen Eigenschaften schädlich sein. Dies sind wichtige Fragen, die vor einer Massenproduktion noch gelöst werden müssen.

Ein reaktives Ionenätzverfahren für Ir wurde in dieser Studie entwickelt. Weitere Untersuchungen mit Ir/PZT/Ir-Stapel sind notwendig, um die Kompatibilität mit PZT-Filmen zu gewährleisten. Es erscheint auch lohnenswert, Al_2O_3-Dünnfilme als Hartmaske für das Ir Ätzen mit CF_4/O_2 Gasmischungen zu untersuchen.

Obwohl die in dieser Arbeit entwickelte Abscheidungstechnik von Ir Dünnschichten für 3D-ferroelektrische Kondensatoren anwendbar ist, sind weitere Verbesserungen der Kantenbedeckung erforderlich. Die Abscheidung von Ir durch ALD kann eine Alternative zu MOCVD sein, um eine bessere Kantenbedeckung zu erreichen.

Die Gründe für die in dieser Arbeit beobachteten relativ hohen Leckströme der 3D-ferroelektrischen Kondensatoren müssen weiter untersucht werden. Außerdem, sollten komplexere Elektroden mit leitfähigen Oxiden wie $SrRuO_3$ und $LaNiO_3$, in den 3D-Kondensator-Stapel integriert werden, um die langzeitstabilität der Speicherstrukturen zu erhöhen.

Abstract

The aim of this work in the thesis is to develop several necessary technologies for ferroelectric capacitors, the key component of FeRAMs, and to investigate the properties of ferroelectric capacitors manufactured in this work. At first, the status of present semiconductor memory devices is summarized and the potential candidates for the future are introduced in Chapter 1. An introduction of ferroelectric materials and a review of the status of FeRAMs are given in Chapter 2. In the following chapters the effort is focused on the following topics, Chapter 3: Investigation of PZT ferroelectric thin film deposition with novel precursors, Chapter 4: Investigation of reactive ion etching for the iridium electrode material, Chapter 5: Investigation of the deposition of iridium as electrodes in three-dimensional structures, Chapter 6: Realization and characterization of three-dimensional ferroelectric capacitors.

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1 Introduction of Semiconductor Memory Devices

1.1 Storage Media for Modern Life

Integrated-Circuit (IC) technology has changed the life of human beings very much since the 70's in the last century. Nowadays cell phones, computers, multimedia products and many other devices and equipments, which base on IC technology, have played an important role in our daily life.

In order to achieve the functions of these equipments and devices, storage components are usually indispensable in the whole system. There are many types of storage components. Hard disk, CD and DVD, which work according to magnetic or optical characteristics of materials, have usually lower cost but larger equipment dimensions. DRAM, SRAM and Flash which base on IC technology, have higher storage density, and, therefore, have smaller dimensions but higher cost.

Different types of storage components can satisfy criteria of different applications. In the example of computer, hard disk has substituted floppy disk since decades of years to be the main system storage device in computer because it has much larger capacity, faster read/write speed and better reliability than floppy disk. The operating system, software programs and user data are usually saved in hard disks.

Hard disk cannot fulfill the demand of all kinds of memory function because its speed (access time and data transport rate) is much slower relative to system operation speed. In order to enhance the performance of computer, DRAM and SRAM are also necessary in addition to hard disk. They can operate in higher speed than hard disk and are used as buffer between hard disk and CPU (central processing unit) or between many other components in a computer. DRAM and SRAM are so-called volatile memories. The data in DRAM/SRAM will be lost after the power is turned off. If it's necessary to keep the data in DRAM/SRAM,

they must be transferred to nonvolatile storage device, for example hard disk, before power-off.

It is very usual to transfer data between computers. A removable storage medium is necessary for such a demand. A hard disk is very sensitive to shock and vibration, so it's not suitable to be used as removable storage medium. A floppy disk, as mentioned above, has only small capacity, low read/write speed and bad reliability, is already out of date. DVD, CD and Flash memory devices are state-of-the-art as removable storage mediums. Besides, DVD and CD have replaced video tape and audio tape to be the main storage mediums of movies and music.

In recent years, portable devices, such as cell phone, mp3 player, digital camera, PDA, etc., are more and more popular. These products demand high capacity of memories with high storage density, low power consumption and nonvolatile property as criteria.

Flash memory chips are so far the primary candidate as storage medium for these portable devices. Flash memory is nonvolatile memory, so continuous power consumption is not necessary for data conservation. However, there are other disadvantages. First, a Flash memory can only be rewritten for about 10^5 to 10^6 times. There will be a reliability problem in some applications. Second, writing data takes much longer time than for other semiconductor type memories. In addition, the cost of a Flash memory is much higher than for other storage mediums such as hard disk, DVD and CD.

Scientists and engineers are always looking for a universal memory device. It must be nonvolatile and must have low power consumption, high speed, good reliability, high storage density and low cost. Many candidates have been researched and developed to fulfill these criteria. Among them, FeRAM (Ferroelectric Random Access Memory), MRAM (Magnetic Random Access Memory), PCRAM (Phase Change Random Access Memory) are more popular and have more potential to be the universal memory device.

This thesis is focused on FeRAM. The effort is concentrated on the ferroelectric thin film deposition and the realization of a 3-dimensional ferroelectric capacitor, which is the key structure in a FeRAM.

1.2 Current Status of Semiconductor Memory Devices

Nowadays the most commonly used semiconductor memory devices are SRAM, DRAM and Flash. They play different roles in different applications.

1.2.1 SRAM

An SRAM (Static Random Access Memory) cell consists of 6 transistors – two CMOS inverters stand back-to back with two additional transistors for input/output control (**Figure 1.1**). Two CMOS inverters (transistors P1/N1 and P2/N2) form a latch to keep complement logic levels 0 and 1 in each inverter. The two additional control transistors (N3, N4) are turned off except during read and write operations.

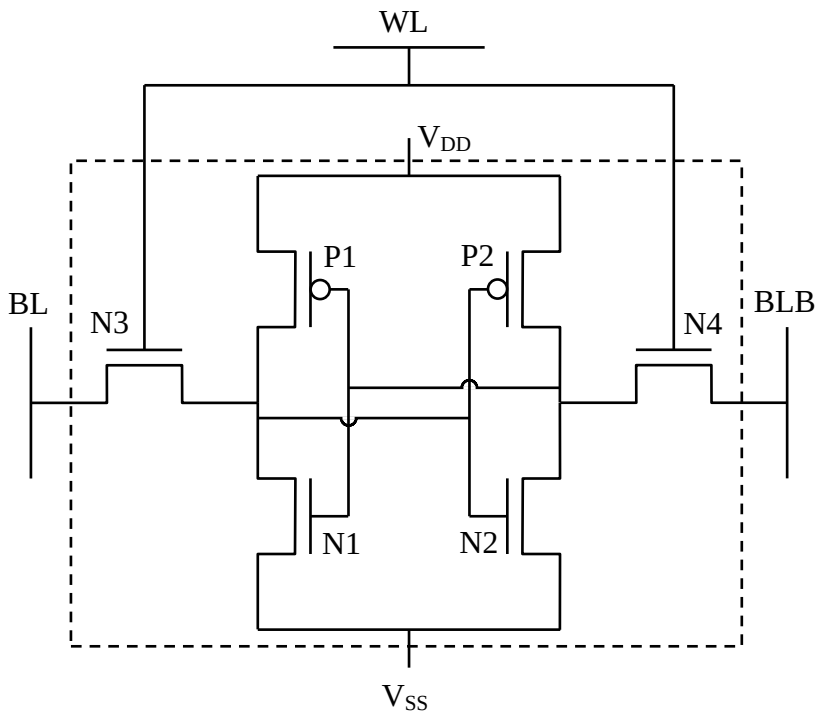


Figure 1.1 SRAM memory cell.

In write operation, BL (bit line) and BLB (bit line bar, conjugated bit line) are kept in complement logic level 0 and 1, N3 and N4 are turned on through WL (word line). The logic state in latch will be overwritten by BL and BLB. In read operation, BL and BLB are precharged. After turning on N3 and N4, the data in latch will cause charge redistribution in BL and BLB. A sensing amplifier, which is connected to both BL and BLB detects the voltage difference between BL and BLB after charge redistribution and reads out the data in cell.

Such a SRAM memory cell in **Figure 1.1** uses six transistors, which occupy a quite large chip area. It's so-called 6T-SRAM. There is an alternative 4T-SRAM, in which two PMOS transistors P1 and P2 are replaced by two poly-Si resistors. Poly-Si resistors can be made over MOS transistors therefore the cell area can be reduced but at the expense of higher power consumption.

A permanent power V_{DD} is necessary to keep the data in latch. The data will be lost without power supply, so SRAM is a volatile memory device. It seems that SRAM has the highest operation speed than other semiconductor memory types. This is the reason why it can survive in the market in spite of its large cell area.

Further information about SRAM is available in reference. [1.1]–[1.4]

1.2.2 DRAM

A DRAM (Dynamic Random Access Memory) memory cell has an NMOS transistor as a switch and a capacitor for data storage (**Figure 1.2**). The electrical charge stored in capacitor represents the logic level of this cell.

The write operation is very simple. Switch transistor N1 is turned on by WL, capacitor C1 is charged or discharged by the voltage between BL and PL to write data 0 or 1. In read operation, BL is precharged and then N1 is turned on. There is charge redistribution between capacitor C1 and BL. A sensing amplifier, which is connected with BL, can detect the voltage change of BL to read out the data in cell. It should be noticed that, after read operation the

data stored in capacitor is disturbed because of charge redistribution. Such a read operation is a destructive read operation. It's necessary to rewrite the data back into the capacitor.

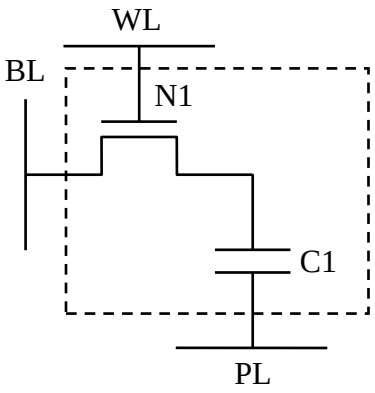


Figure 1.2 DRAM memory cell.

An ideal DRAM cell should always keep the charge in the capacitor. In reality there is a leakage current through the dielectric of the capacitor or through the p-n junction of the source node of the NMOS transistor at capacitor side. The charge in the capacitor will be lost after a certain time. A "refresh" procedure is necessary, which reads all the cells in the whole memory and rewrites their data back. The common refresh period is every 64ms. Of course, the data will be lost after turning off the power. DRAM is a volatile memory, too.

Further information about DRAM is available in reference. [1.1]–[1.4]

1.2.3 Flash Memory

A Flash memory cell consists of only one transistor, but the transistor is not a normal transistor. A Flash transistor has an extra floating gate between the normal gate and the substrate (see **Figure 1.3**).

The floating gate can be charged and discharged during “program” and “erase” operations. A charged floating gate increases the threshold voltage (V_t) of this transistor so that this transistor cannot be turned on with the same WL voltage, which is used to turn on transistors with discharged floating gate. Different V_t’s caused by charged/discharged floating gate represent logic levels 0 and 1.

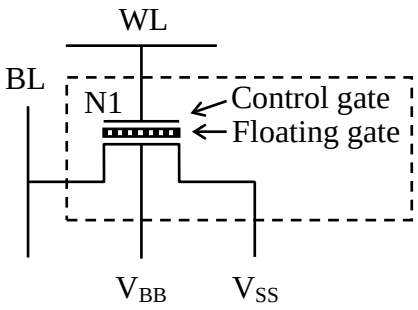


Figure 1.3 Flash memory cell.

In read operation, BL is precharged and a voltage is added to control the gate through WL. If the floating gate is discharged, the transistor is turned on. BL is discharged through the transistor. If the floating gate is charged, the transistor cannot be turned on. BL will not be discharged. The charged/discharged BL causes difference on sensing amplifier and the logic level in the cell can be detected. To write data into a Flash cell is a little more complicated than in a SRAM and a DRAM. There are dielectric films above and under the floating gate and these dielectric films are insulators. Only with a very high voltage a tunnel current can occur and flows through the dielectric film to charge/discharge the floating gate. The write operation is divided into “program” and “erase” operations. In program operation, electrons tunnel from the substrate into the floating gate with very high WL voltage or both high WL and BL voltages. The floating gate is charged and V_t becomes higher. This cell is programmed to 0. In erase operation, either V_{SS} or V_{BB} voltage is kept very high. The electron charge in the floating gate can tunnel through the dielectric film into the substrate. V_t becomes lower and this cell is erased to 1.

Because a tunnel current is usually very small, such a program/erase operation takes very long time compared with write operation in SRAM and DRAM. In addition, the

dielectric film degrades with program/erase cycles. The state-of-the-art Flash product has the endurance of around 10^6 program/erase cycles. This is much less than over 10^{15} read/write cycles of SRAM and DRAM.

In spite of the disadvantages mentioned above, Flash has a superiority that SRAM and DRAM don't have. The charged electron can stay in the floating gate even when the power is turned off. The data in memory cell can be kept without power. A Flash memory is a nonvolatile memory. This is the reason why Flash dominates the memory component market of portable equipment such as cell phones and mp3 players.

Further information about Flash is available. [1.2][1.3][1.5]

1.3 Emerging Memory Technologies

Several technologies are under development to carry out the next generation semiconductor memory devices. Several criteria must be fulfilled, such as nonvolatile capability, low power consumption, high storage density, high speed, good reliability and low cost. The most promising candidates are Ferroelectric Random Access Memory (FeRAM, also FRAM), Magnetic Random Access Memory (MRAM) and Phase Change Random Access Memory (PCRAM).

1.3.1 FeRAM

The function of Ferroelectric Random Access Memory (FeRAM) bases on a capacitor with a ferroelectric thin film as dielectric layer. [1.6]–[1.8] Ferroelectric materials can be polarized by external electric fields. After the external electric field is removed, a portion of polarization remains in ferroelectric materials, which is called remanent polarization and shown as $+P_r$ and $-P_r$ in **Figure 1.4**.

In a ferroelectric capacitor, the external voltage, which is associated with an external electric field mentioned above, can be in positive or negative direction. That means the

polarization of a ferroelectric film is bidirectional. After reset the external voltage to zero, the remanent polarization induces complementary charges in the capacitor electrodes. Remanent polarization and induced complementary charges interact with each other and form a stable state that the remanent polarization can be kept for a long time. This characteristic can be used to define 0 and 1 states for memory application.

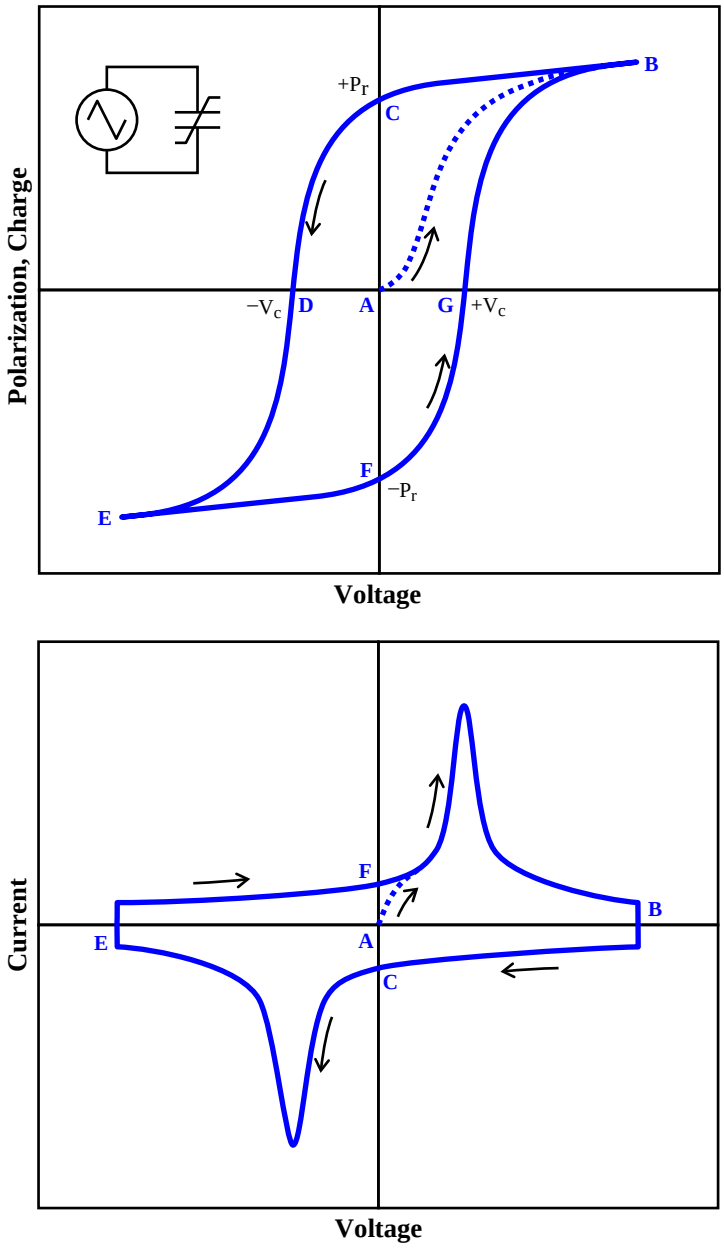


Figure 1.4 Ferroelectric capacitor polarized by an external voltage.

The structure of a FeRAM memory cell is similar to a DRAM memory cell. In the simplest way, it consists of an NMOS transistor as a switch and a ferroelectric capacitor for data storage (**Figure 1.5**).

The read/write operation of FeRAM is similar to that of DRAM. The only difference is that in DRAM the 0 and 1 states are decided by stored charge but in FeRAM they depend on polarization direction of the ferroelectric capacitor. During write operation, the switch transistor N1 is turned on by WL, a positive or negative voltage bias is added on capacitor C_F by setting the voltage between BL and PL to change the polarization direction for writing data 0 or 1. After writing, the voltage bias between BL and PL is set to zero again and the switch transistor is turned off. The ferroelectric capacitor is kept at positive/negative remanent polarization with complementary charges in the electrodes. In read operation, BL is precharged and then N1 is turned on. There is a charge redistribution between capacitor C_F and BL. The polarization direction of C_F can affect the charge redistribution and cause different final voltage on BL according to different polarization direction. A sensing amplifier which is connected with BL can detect the voltage change of BL to read out the data in cell. During read operation, the polarization of the ferroelectric capacitor is disturbed. A rewrite operation is necessary.

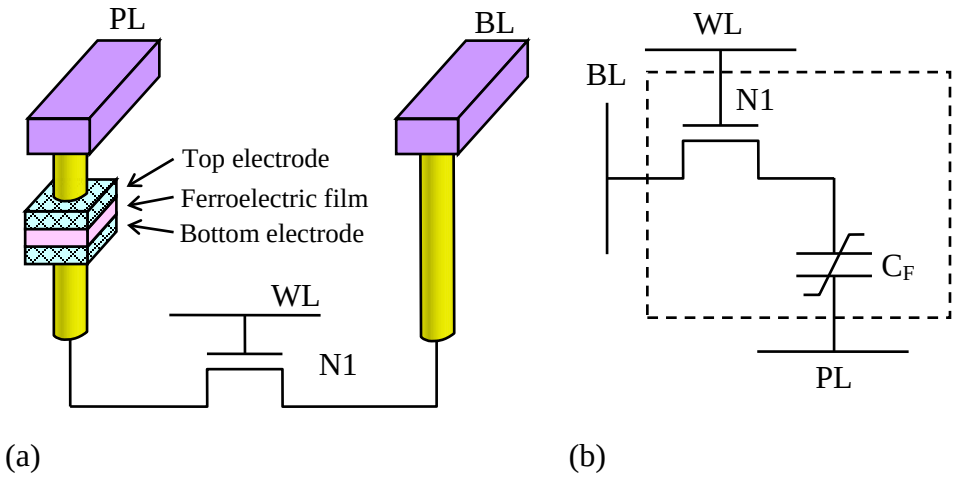


Figure 1.5 FeRAM memory cell, (a) Architecture, (b) Circuit diagram.

Because the structure and operation of a FeRAM are very similar to those of a DRAM, it's not difficult to implement mature DRAM technology on development of FeRAM. This is an advantage that the learning curve of developing FeRAM can be reduced. FeRAM has superiority than other emerging memory technologies.

1.3.2 MRAM

A variety of Magnetic Random Access Memory (MRAM) technologies have been explored over a period of many decades. [1.7][1.9][1.10] The state-of-the-art MRAM cell has a magnetic tunnel junction (MTJ) as memory cell. A simplified MTJ structure is shown in **Figure 1.6**. A ferromagnetic layer is deposited on an antiferromagnetic layer. The interaction between ferromagnetic layer and antiferromagnetic layer causes an offset on the magnetic hysteresis curve of the ferromagnetic layer. It becomes a "pinned" ferromagnetic layer. An insulating layer is sandwiched between this pinned ferromagnetic layer and another free ferromagnetic layer. This insulating layer is very thin, so that a tunnel current can flow through under voltage bias. This layer works as a tunnel barrier.

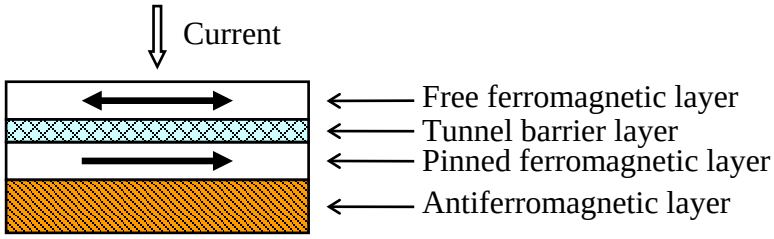


Figure 1.6 MTJ structure

The relation between magnetization directions of the two ferromagnetic layers can affect tunnel resistance of the MTJ. When both layers are parallel magnetized, the resistance is lower. When both layers are anti-parallel magnetized, resistance becomes higher. The change of the tunnel resistance caused by the relative magnetization direction is called tunnel

magnetoresistance (TMR). **Figure 1.7** shows the hysteresis curve of tunnel magnetoresistance vs. external magnetic field.

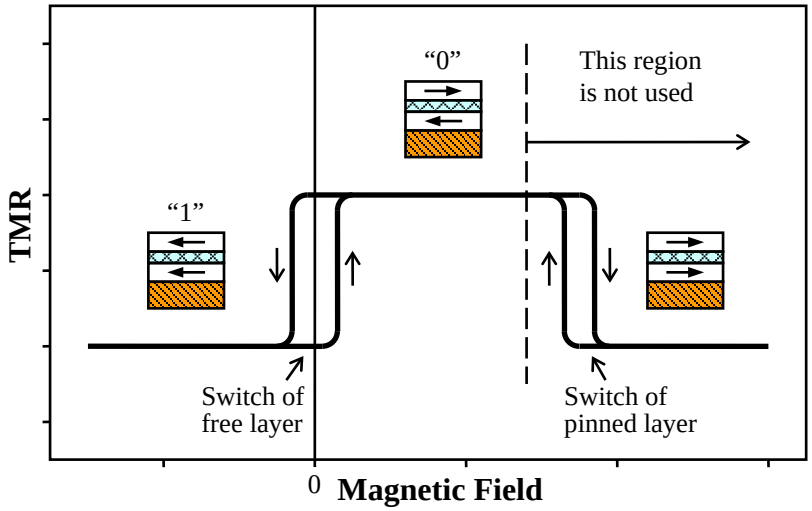


Figure 1.7 Tunnel magnetoresistance vs. magnetic field

The architecture of a MRAM cell is shown in **Figure 1.8(a)**. A bit line (BL) goes over MTJ and is in contact with the MTJ. A write word line (write WL), which is perpendicular to the bit line, goes direct under the MTJ with a separation spacing. The pinned layer of the MTJ is magnetized along write word line direction in manufacture procedure and will not be changed during operation. When current flows through BL and write WL, magnetic field arises around BL and write WL. This magnetic field can change the magnetization of the free layer.

In write operation, the switch transistor N1 is turned off by read WL and there is a current flowing through BL and write WL. With assistance of the magnetic field of write WL, the free layer can be magnetized by BL either parallel ("1" state) or anti-parallel ("0" state) to the magnetized direction of the pinned layer.

In read operation, the switch transistor N1 is turned on. A small voltage on BL causes a current flowing through MTJ and N1. A sensing amplifier connected with BL can sense the current at different TMR caused by different magnetization states of the MTJ.

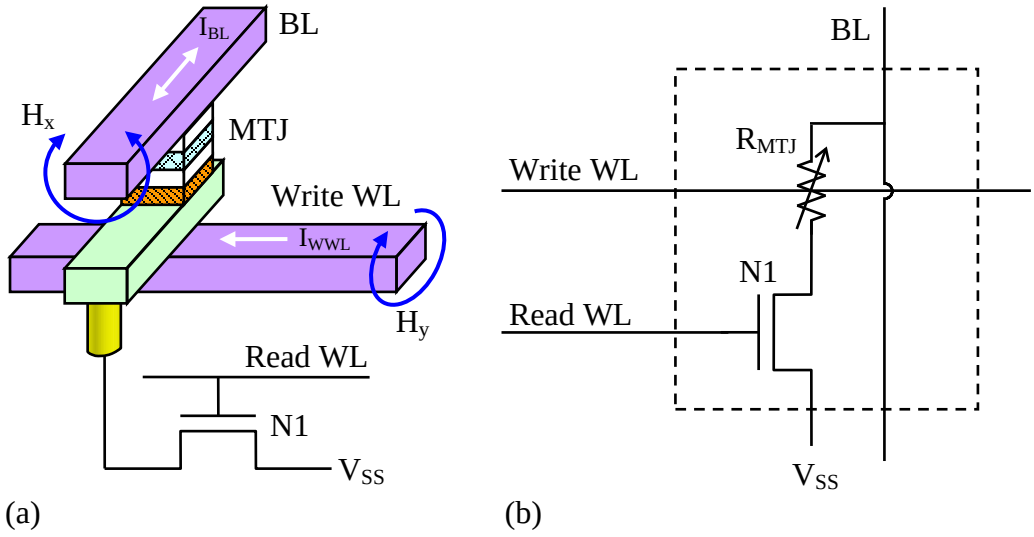


Figure 1.8 MRAM memory cell, (a) Architecture, (b) Circuit diagram.

In recent years, a new generation of MRAM has been developed with switching the magnetization of the free layer by using a high current direct through the MTJ rather than using the external magnetic field caused by BL and write WL. The write WL is not necessary any more. Therefore the cell structure can be simplified and easily scaled down. The new generation is called Spin-Torque-Transfer MRAM (or Spin-Transfer-Torque MRAM, STT-MRAM).

The MTJ of STT-MRAM is similar to a traditional field-switch MRAM. When electrons flow from the pinned layer to the free layer, the electrons will become spin-polarized according to the magnetization of the pinned layer. If the tunnel layer is thin enough, this electron current will keep spin-polarized when it flows into the free layer. If the current density is high enough (about 10^7–10^8 A/cm^2), the interaction between spin-polarized electrons and free layer can cause magnetization switching of the free layer to align parallel to the magnetization of the pinned layer. In the reversed process when electrons flow from the free layer to the pinned layer, the magnetization of the pinned layer will not be influenced. But some electrons are reflected by the pinned layer with antiparallel direction and flow back to the free layer. The interaction between reflected electrons and the free layer causes magnetization switching of the free layer to align antiparallel to the pinned layer. [1.11][1.12]

With this property of interaction between pinned layer, free layer and spin-polarized electron current, the magnetization of the free layer can be switched either parallel or antiparallel to the pinned layer by a current flowing directly through the MTJ. The characteristic curve of TMR versus current is also hysteretic.

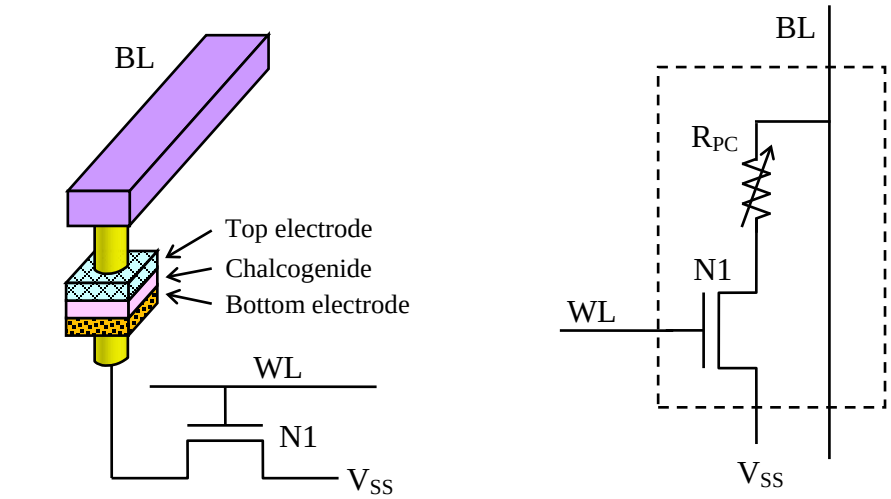
In write operation of a STT-MRAM, depending on whether "1" or "0" should be written, a high current pulse flows through the MTJ either in positive or negative direction to switch the magnetization of the free layer to be parallel or antiparallel to the pinned layer. In read operation, a small current should be used to sense the MTJ status in order not to disturb the magnetization of the free layer. [1.13][1.14]

1.3.3 PCRAM

In the late 1960s it was found that chalcogenide glass exhibited a reversible change in resistivity upon a change between polycrystalline and amorphous phases. Chalcogenides are alloys that contain an element in the Oxygen/Sulfur family of the Periodic Table, for example, GeSbTe (GST). This kind of materials is called phase change materials. Phase change materials have been already used in rewriteable CDs and DVDs because different laser heating procedures can induce transition between polycrystalline and amorphous phases of these materials and cause different surface roughness and optical reflection rate. Phase Change Random Access Memory (PCRAM) makes use of resistive difference between polycrystalline and amorphous phases of phase change materials.

The concept of phase change memory manufactured with IC technology is carried out by proper heating and cooling of the material, which is made as a variable resistor in series with a transistor in a memory cell. The architecture of a PCRAM cell is shown in **Figure 1.9**. The I-V characteristic of such a phase-change resistor is shown in **Figure 1.10**. An amorphous phase change material has a resistance a few orders higher than that in the polycrystalline phase. The I-V characteristic of the amorphous phase is initially ohmic with high resistance. But when the voltage increases over a threshold V_{th}, the current rises swiftly with a voltage snap-back and the resistance becomes lower and lower until it becomes the same as the resistance of the polycrystalline phase. The beginning of resistance change is a

pure electronic phenomenon, but with increasing current the phase transition from amorphous into crystalline will happen since Joule heating is high enough to cause crystallization. With further increasing of current the material will finally melt.



(a) (b)

Figure 1.9 PCRAM memory cell, (a) Architecture, (b) Circuit diagram.

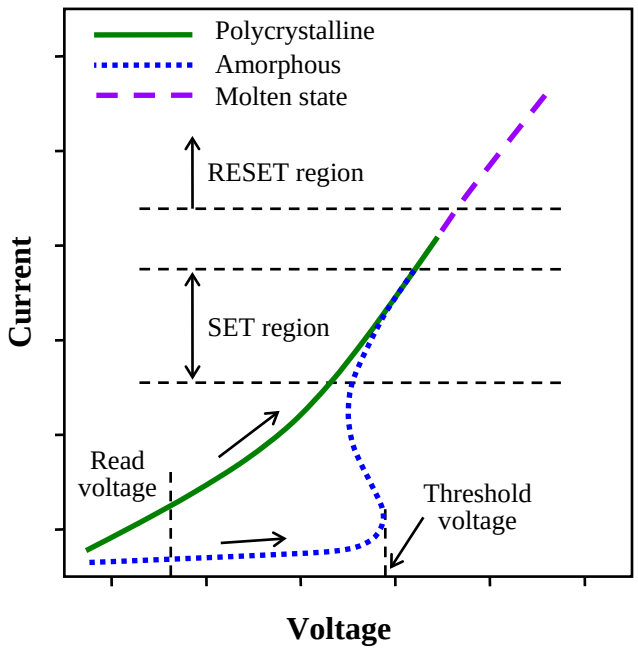


Figure 1.10 Current-Voltage characteristics of a phase-change element.

The memory device is programmed by the application of a current pulse of appropriate magnitude and duration shown in **Figure 1.11**. A short pulse of a high current is used to melt the material, which is then allowed to cool quickly enough to "freeze in" the amorphous state with high resistance. It's the so-called RESET operation. The SET operation is the reverse process, in which a longer pulse with lower current is used to heat the material to a temperature below the melting point, but at which crystallization could occur rapidly.

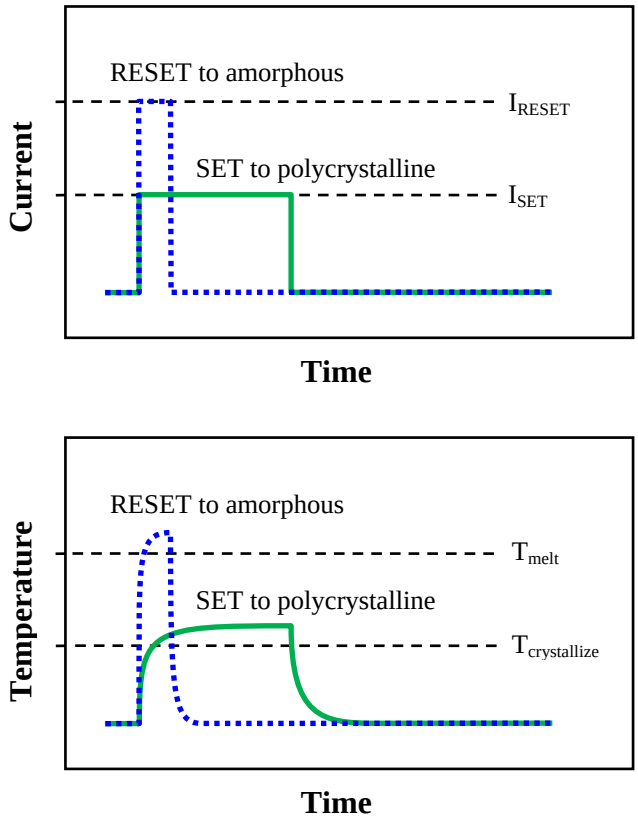


Figure 1.11 Operating principle of phase-change memory.

A voltage which is much lower than the programming voltage is used to read the memory cell in order not to disturb the data in the cell.

In the RESET operation, the resistance of the polycrystalline phase is usually very small, so a rather high current is necessary to switch the material from the polycrystalline to

the amorphous phase. Scaling down can help to reduce the electric energy and, therefore, the current load necessary for the phase changes. The interaction between neighbored PCRAM cells may become an undesired problem.

Further information about PCRAM is available. [1.15]–[1.17]

1.4 Reviews and Perspectives

The structure of the FeRAM is similar to the DRAM except that the FeRAM is nonvolatile; so it doesn't need refresh. The merits of FeRAM are that FeRAM technology could be developed with small modification of DRAM circuit and process, and the read/write current of the cell capacitor is much smaller in comparison with PCRAM and MRAM. There are still some barriers to make FeRAM really competitive to DRAM, Flash, MRAM and PCRAM. The thickness of the ferroelectric film in a FeRAM capacitor is still kept around 50–100nm and is difficult to reduce. The area density of the remanent polarization of a ferroelectric film is not large enough. Therefore, it is difficult to scale down the capacitor size. The read/write endurance is usually only up to 10^{13} cycles [1.18] and is not high enough for usual application such as main memory in computers with 10 years life time. So a FeRAM is limited to some certain applications such as RF ID card [1.19] or nonvolatile cache. In 2009 Toshiba demonstrated a 128Mbit FeRAM which is compatible to DDR2 DRAM. [1.18] This FeRAM used 0.13μm design rules, had a $0.28\times0.30=0.084\mu m^2$ ferroelectric capacitor in each memory cell. In 2014, commercialized FeRAM chips up to 4Mbit have been available since many years on the product lists of several companies such as Cypress, TI, Fujitsu and Lapis. The FeRAM of Cypress has an endurance of 10^{14} read/write cycles. Microcontrollers with embedded FeRAM up to 64KByte are available from TI and are guaranteed with a minimum endurance of 10^{15} cycles.

The first commercially available MRAM device is Freescale's 4Mbit, 1-transistor, 1-MTJ MRAM in 2006, which is manufactured with 0.18μm design rules. [1.20] In 2009 NEC announced a 32Mbit, 2-transistors, 1-MTJ MRAM with 90nm design rules. [1.21] Both of them use conventional field-switch technology. A conventional field-switch MRAM has an unlimited write endurance and fast read/write time but needs very high write current (over

1mA/bit [1.21]) and the necessary write current increases with scaling down. The additional write word line or 2-transistor scheme also makes cell structure complicated and difficult to scale down. In the year of 2014 MRAMs are provided up to 64Mbit by several manufacturers such as Everspin, Aeroflex, Honeywell and Crocus.

New generation STT-MRAMs have a simpler structure than field-switch MRAMs. The switching of data depends on current density flowing through the MTJ and it can be reduced by scaling down. The necessary write current is still at a high level between 50 to 300μA. [1.22][1.23] According to publications, the write endurance is proved to be over 10^{12} cycles. [1.24] But the high density current during writing may be a concern to damage the MTJ and to cause endurance issues. Furthermore, the thermal stability of the free layer could also cause the problem of retention with continuing scaling down. In 2010 Toshiba announced a 64Mb STT-MRAM with 65nm design rules, which has a write current around 49μA. [1.22] Until 2014 STT-MRAM is still not yet in mass production.

The RESET operation of a PCRAM needs a pulse with a high current around 100–900μA in order to melt the phase change material. [1.25] The SET operation needs a lower current but a longer pulse time of a few hundreds nanoseconds to heat the phase change material to a temperature high enough for the transition to the polycrystalline phase but keeps the temperature low enough to prevent it to melt. These characteristics are weak points of the PCRAM. A high current pulse means not only high power consumption during operation but also a concern about reliability of the electrode/heater material itself and of the interface between phase change and electrode/heater materials. The superiority of the PCRAM is that the phase change material can be integrated into a contact/via hole. Therefor a PCRAM has a smaller cell size and a higher memory capacity than a MRAM and a FeRAM. In 2010 Hynix demonstrated a 1Gbit PCRAM with 84 nm design rules. Its SET current is about 80μA with 300ns pulse time and its RESET current is between 140–200μA with 30ns pulse time. The write endurance is about 10^8 cycles. [1.26] At the end of 2012, Samsung presented their 20nm, 8Gb PCRAM at ISSCC. [1.27] Earlier in July of 2012, Micron announced the mass production of their 45nm, 1Gb PCRAM for mobile devices. [1.28] But after a year this product became not available any more.

Many factors, such as non-volatility, low power consumption, high speed, good reliability, high storage density and low cost, must be taken into account in order to evaluate

semiconductor memory devices. **Table 1.1** shows the comparison between SRAM, DRAM, Flash, FeRAM, MRAM and PCRAM.

Table 1.1 Comparison of semiconductor memory devices.

	SRAM	DRAM	Flash	FeRAM	MRAM	STT-MRAM	PCRAM
Maturity	Mass Prod.	Mass Prod.	Mass Prod.	Mass Prod.	Mass Prod.	Test Chip	Test Chip
Nonvolatile	No	No	Yes	Yes	Yes	Yes	Yes
Destructive read	No	Yes	No	Yes	No	No	No
R/W Endurance	$>10^{15}/>10^{15}$	$>10^{15}$	$>10^{15}/10^{6}$	10^{13}	$>10^{15}/>10^{15}$	$>10^{15}/>10^{12}$	$>10^{15}/10^{12}$
Cell Size	Large	Small	Small	Medium	Medium	Medium	Small
Write Time	Very Fast <10ns/bit	Fast ~10ns/bit	Slow ~1us/bit	Fast <100ns/bit	Fast <100ns/bit	Fast <100ns/bit	Medium ~200ns/bit
Write Energy	Low	Low	High	Low	High	High	High

There are many publications about the universal memory. [1.25][1.29]–[1.31] Many candidates including those mentioned above are discussed but the final winner is still unknown until now.

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2 Ferroelectric Materials

2.1 Ferroelectricity

The “ferro” part in the name of ferroelectricity doesn’t mean the presence of iron in the ferroelectric materials. Rather it arises from some properties analogous to ferromagnetism, for example, the spontaneous electric polarization vs. spontaneous magnetization, the hysteresis loop of ferroelectric materials vs. ferromagnetic materials, the domain structure, etc.

In order to introduce ferroelectricity, it’s worth to introduce pyroelectricity and piezoelectricity, too. Pyroelectricity is a characteristic of some crystals which show spontaneous electrical polarization when they are heated or cooled. As a result of temperature change, positive and negative charges are induced on the opposite sides of the crystals. The electric polarization exists only below a certain temperature called Curie temperature. When a pyroelectric material is heated above Curie temperature, it is paraelectric. That means, it can be electric polarized under an applied external electric field, but after removing the external field, the polarization returns to zero again. After cooling down the crystal below Curie temperature, a spontaneous polarization in the crystal occurs even if there is no external electric field. The value of the spontaneous polarization depends on the temperature and it suddenly falls to zero on heating the crystal above the Curie temperature. It’s called the pyroelectric effect. Usually, applying an external electric field cannot change the spontaneous polarization of pyroelectric materials. If the magnitude and direction of the spontaneous polarization can be reversed by an external electric field, then such crystals are said to show ferroelectric behavior. Hence ferroelectric materials are a subgroup of pyroelectric materials.

Piezoelectricity is a property of some materials which can be polarized by applying mechanical stress, resulting in a charge density on their surface. This phenomenon is known as direct piezoelectric effect. There is also a reversed effect, converse piezoelectric effect, which describes the strain that is developed in a piezoelectric material due to the applied

electric field. All the pyroelectric materials, including ferroelectric materials are a subgroup of piezoelectric materials.

2.2 Ferroelectric Domains and Hysteresis Loop

Ferroelectric crystals possess regions in which spontaneous polarization is uniformly oriented. These regions are called ferroelectric domains. The boundary between two domains is called domain wall. The width of ferroelectric domain walls is in the order of a few nanometers. It should be noted not to mistake domain wall for grain boundary in polycrystalline materials. Ferroelectric domain walls separate domains with different directions of polarization.

The polarization orientation in ferroelectric crystals is not arbitrary but depends on the crystal structure. For example, in ferroelectric tetragonal $BaTiO_3$, the possible orientations are any of the six ‹001› directions in its paraelectric cubic unit cell. There is a small elongation along polarization direction with a little contraction perpendicular to it and the cubic cell becomes tetragonal. This gives two kinds of relation between the orientations of neighboring domains: (1) If the orientations of neighboring domains are antiparallel (180°), their domain wall is called 180° domain wall. (2) If the orientations of neighboring domains are perpendicular (90°), their domain wall is called 90° domain wall, which exists in ferroelectric tetragonal $BaTiO_3$. In ferroelectric rhombohedral $BaTiO_3$, the possible polarization orientations are any of the eight ‹111› directions in its paraelectric cubic unit cell. Hence there can be 180°, 109° and 71° domain walls.

The directions, along which the polarization will develop, depend on the electrical and mechanical boundary conditions imposed on the material. Ferroelectric domains form in order to minimize the total energy in whole system including domain wall energy and the dipole-dipole interaction energy which are internal, and the electrostatic energy from compensating charges and the elastic interaction energy from boundary constraints which are external. [2.1] In addition, vacancies, dislocations and dopants can also influence domain formation.

A very important characteristic of ferroelectric materials is their hysteresis loop of polarization vs. external electric field which is shown in **Figure 2.1**. The domain structures under different external electric fields are also shown in insets. If we assume that all the domains orient randomly at initial state without external electric field, then the net polarization is zero and the crystal state is at point A (origin). As the external electric field increases, the domains start to align in the direction of the electric field. When the electric field increases to point B, all of the domains are switched to the nearest possible orientation toward the electric field, the polarization is saturated. Further increasing the electric field doesn't switch any domain more and the crystal behaves like a normal dielectric. An extrapolated line intersects the polarization axis at P_s, which is called saturation polarization.

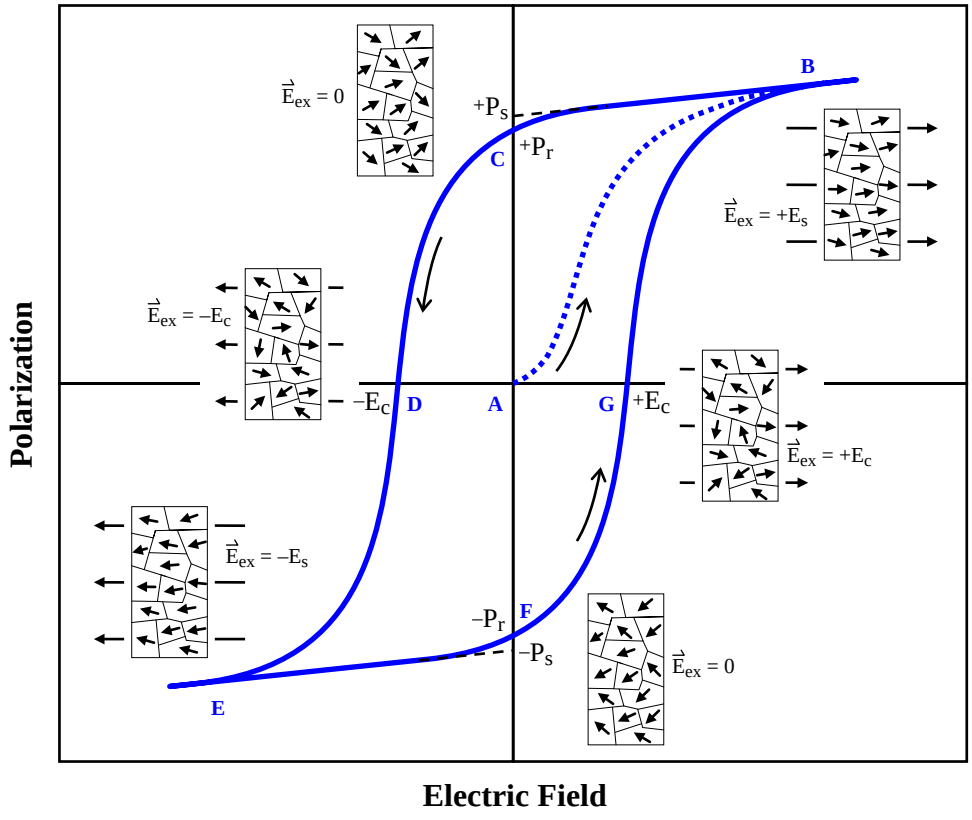


Figure 2.1 Hysteresis Loop of Ferroelectric materials.

The polarization decreases but doesn't fall to zero when the electric field decreases to zero at point C. Some of the domains still remain aligned toward the positive direction. The crystal shows a remanent polarization $+P_r$ even if the external electric field is removed. With further decreasing the electric field to point D some domains begin to be switched to negative direction and the net polarization falls to zero. The electric field required to reduce polarization to zero is defined as coercive field $-E_c$. If the electric field decreases more to point E, all domains are switched to the negative direction and the polarization saturates at negative direction. With the electric field returning to zero at point F, a remanent polarization $-P_r$ still exists which is similar to the situation in the positive direction. Further increasing of the electric field to $+E_c$ at point G makes polarization to zero again.

The insets shown in **Figure 2.1** are only a simplified illustration of domain reorientation. It is not easy to study detailed mechanism of domain switching by direct observation of ferroelectric domains, especially dynamically in real time. Nevertheless, domain behavior and switching dynamics is always an attractive topic for scientists. [2.2]–[2.6] This topic is very complex and it seems there is no universal mechanism which would be valid for polarization reversal in all ferroelectrics.

A polarization switching is called homogeneous polarization switching if the entire ferroelectric material switches to opposite direction simultaneously at a certain threshold electric field which is called intrinsic coercive field E_{ci}. However, based on Landau's mean-field theory, [2.7] the estimated E_{ci} values should be on the order of a few MV/cm for most known ferroelectric materials. These values are much higher than the experimental results of coercive field E_c, which are typically around 100kV/cm. That means, homogeneous polarization switching is probably not the general case in usual polarization switching. In many researches it is believed that the usual polarization switching is inhomogeneous and is initiated by nucleation of domains, which have the polarization along the switching field, and is followed by growth of these domains through domain wall motion. [2.8]–[2.10] The complete process of inhomogeneous polarization switching is illustrated in **Figure 2.2**. The initial state is assumed as a polarized single domain. Nucleation occurs under application of an external electric field. It is thought that nucleation occurs inhomogeneously at particular sites where material defects exist, which can reduce the energy barrier for nucleation. And such defects are thought to occur frequently at electrode/ferroelectric material interfaces of ferroelectric capacitors. In the next step, the nucleated domains grow parallelly to the external electric field

in a needle-like geometry from one electrode/ferroelectric material interface through the ferroelectric material to the interface at the other side. This step is called forward growth. After forward growth, domains spread also sideways, known as lateral growth. During lateral growth, coalescence of domains happens and finally the whole ferroelectric material is switched to a single domain and the switching is complete.

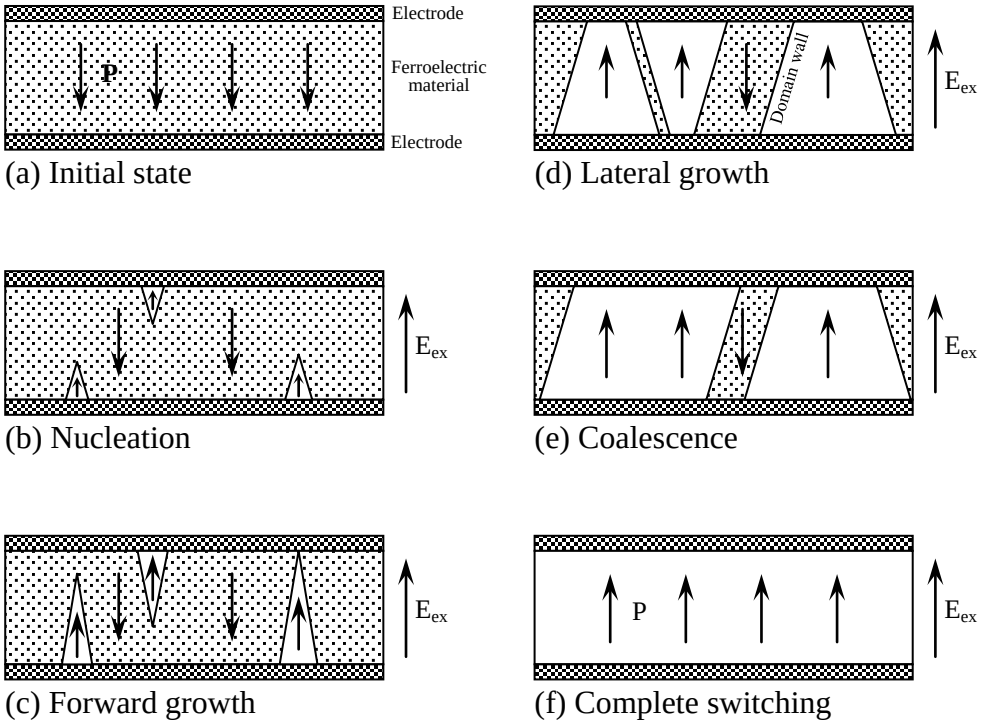


Figure 2.2 Inhomogeneous polarization (P) switching process induced by an external electric field (E_{ex}) in a ferroelectric thin film capacitor.

2.3 Perovskite Oxides

There are many kinds of materials with ferroelectric properties, for example, perovskite oxides, bismuth oxide layer structured compounds, tungsten bronze type compounds, organic polymers, etc. Perovskite oxides are the most studied family of ferroelectric materials.

The name “perovskite” comes from the mineral perovskite $CaTiO_3$ because of the similar structure. Perovskite oxides are a very large family with the structure ABO_3, where A and B represent a cation element, respectively. The valence of A cations may be from +1 to +3 and of B cations from +3 to +6. The physical properties of the entire family are extremely diverse. Some of them are ferroelectric. Some others of them are superconductive or ion conductive. The ideal perovskite structure has a simple cubic lattice and a basis of 5 atoms. As shown in **Figure 2.3(a)**, if A atom is taken at the corner of the cube, B atom will locate at the center and there is an oxygen atom at the center of each face. Alternatively in **Figure 2.3(b)**, if the B atom is taken at the corner, the A atom is at the center and the O atoms are located at the midpoint of each edge. Each A atom is surrounded by twelve equidistant O atoms and each B atom by six O atoms. B atom and its six oxygen first neighbors form an octahedron, in which B atom locates at the center and O atoms at six corners. As shown in **Figure 2.3(c)**, the lattice can be regarded as octahedra connected at their corners to a 3-dimensional simple cubic structure with their interspaces occupied by A atoms.

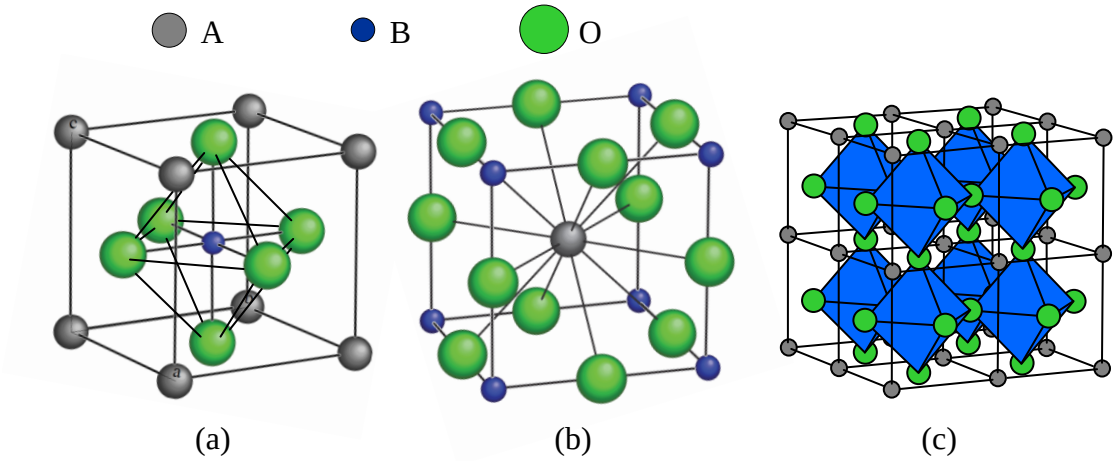


Figure 2.3 The unit cell of ideal ABO_3 cubic perovskite.

It’s very usual that many perovskite structures can be regarded as a distortion of ideal perovskite cubic structure. In 1926 Goldschmidt provided an empirical criterion for the stability of an ideal perovskite structure, based on the rules he had previously derived for

ionic binary compounds. [2.11]–[2.13] His model is based on the concept of ionic radius and the following rules:

(i) a cation will be surrounded by as many anions as can touch it, but not more;

(ii) all the anions must touch the cations and the anion–cation distance is obtained as the sum of their ionic radii.

The perovskite structure is determined by the size of the oxygen octahedra containing the B atoms, while the A atoms must fit the holes between the octahedra. Following the rules of Goldschmidt, this condition provides a relation between ionic radii for ideal cubic perovskite structure:

$$r_A + r_O = \sqrt{2}(r_B + r_O) \tag{2.1}$$

where r_A, r_B, r_O are the ionic radii of A atom, B atom and oxygen atom, respectively. In general case, this will not always be satisfied. The deviation can be described through a tolerance factor t defined as follows:

$$t = \frac{r_A + r_O}{\sqrt{2}(r_B + r_O)} \tag{2.2}$$

Goldschmidt has shown that the perovskite structure is formed when the condition expressed by **Equation (2.1)** is satisfied ($t \approx 1$).

For a critical value t=1, the cubic paraelectric phase is stable. This unique case can be found in $SrTiO_3$, which has an ideal cubic perovskite structure at room temperature and doesn't show ferroelectricity down to the absolute 0 K.

When t > 1, the structure is imposed by the A–O distance and the B atom is too small for the oxygen octahedron. The cations and anions move off the high-symmetry positions and the positive and negative charge center are no longer coincident, so that the structure will develop a small polar distortion, leading to the occurrence of displacive-type ferroelectricity in the crystal such as in $BaTiO_3$.

Conversely, when t < 1, the A atom is too small in comparison to the hole between the oxygen octahedra. The A atom cannot effectively bond with all 12 neighboring O atoms, so coupled tilts and rotations of oxygen octahedral framework can occur. These perovskite oxides are in general not ferroelectrics because different tilts and rotations of BO_6 octahedra still preserve the inversion symmetry. Some exceptions may be found in the bismuth oxide layer structured ferroelectrics, which will be discussed later. If t is only slightly less than one, rotations and tilting of the oxygen octahedra will be favored (as in $SrTiO_3$ and $CaTiO_3$); for even smaller t the compound will favor a strongly distorted structure with only 6 neighbors for the A atom as in $LiNbO_3$. If the value of t is very different from unity, then the perovskite-type structures will be unfavorable relative to another of the known ABO_3 structure types.

2.4 Barium Titanate $BaTiO_3$

A very good typical example for ferroelectric perovskite is barium titanate, $BaTiO_3$. Barium titanate is the first identified perovskite oxide which is ferroelectric. The formal valences are +2 for Ba and +4 for Ti, exactly balancing the negative total valence of the oxygens. At high temperature, it has a paraelectric cubic perovskite structure. At 403 K, it transforms from a cubic phase to a ferroelectric tetragonal phase, as shown in **Figure 2.4(a)**. This phase remains stable until 273 K, where there is a second transformation to a ferroelectric phase of orthorhombic symmetry. The last transition occurs at 183 K. The low-temperature ferroelectric phase is rhombohedral. In the successive ferroelectric phases, the polar axis is aligned respectively along the ‹001›, ‹101› and ‹111› directions corresponding to the direction of the atomic displacements with respect to their position in the cubic reference structure. Each transition is accompanied by small atomic displacements, dominated by displacement of the Ti ion relative to the oxygen octahedron network, and a macroscopic strain. [2.11] From a crystal chemical view, the volume inside the TiO_6 octahedron for the central Ti^{4+} ion is larger than the actual size of the Ti^{4+} ion. As a result, the series of phase transformations takes place to reduce the Ti cavity size. Certainly, the radii of the involved ions impact the tendency for forming ferroelectric phases; thus both $PbTiO_3$ and $BaTiO_3$ have ferroelectric phases, while $CaTiO_3$ and $SrTiO_3$ do not. [2.14]

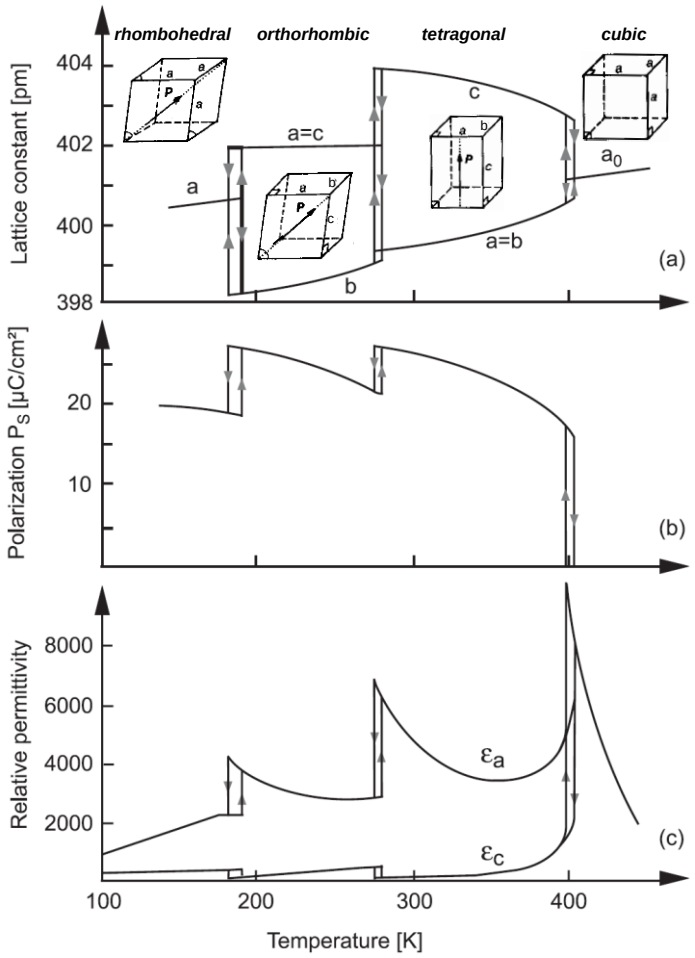


Figure 2.4 Properties of $BaTiO_3$, (a) Lattice constants,
(b) Spontaneous polarization,
(c) Relative permittivity.

In the paraelectric cubic phase of $BaTiO_3$, the energy of the Ti^{4+} ion in terms of its position along the c axis takes the form of a single well with the minimum at the cubic center (**Figure 2.5(a)**). So the Ti^{4+} ion stays at the cubic center without spontaneous polarization. But in the ferroelectric tetragonal phase of $BaTiO_3$ the energy takes the form of two wells along the c axis (**Figure 2.5(b)**). The Ti^{4+} ion must stay at one of the wells away from the center and that means a spontaneous polarization. An applied electric field in the opposite direction to the polarization may enable a Ti^{4+} ion to pass over the energy barrier between the two wells and so reverse the direction of the polarity at that point.

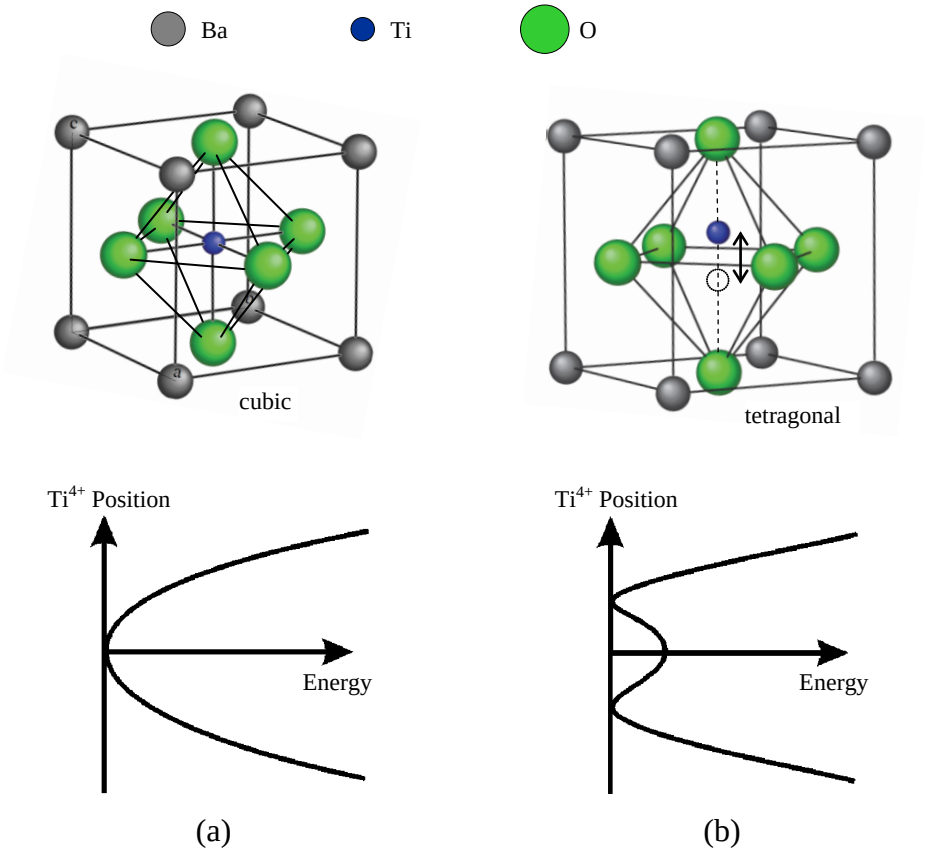


Figure 2.5 Comparison of cubic and tetragonal $BaTiO_3$ perovskite.

A similar mechanism is available for changes of polarity through 90° but in this case there is an accompanying dimensional change because the polar c axis is longer than the non-polar a axis (**Figure 2.4(a)**). Switching through 90° can also be induced through the ferroelastic effect by applying a compressive stress along the polar axis without an accompanying electric field. But mechanical stress does not induce 180° switching. [2.15]

It should be noticed that although in **Figure 2.5(b)** a two-well form of the energy of the Ti^{4+} is shown, that doesn't mean only Ti^{4+} cations move during polarization reversal. Actually all the cations and anions have different displacements caused by polarization reversal. [2.15]–[2.18] **Figure 2.6** is an illustration of the ionic displacement in the $BaTiO_3$ tetragonal unit cell at room temperature. In addition to Ti^{4+} cations, Ba^{2+} cations have also a

displacement relative to the O^{2-} anions and even some of the O^{2-} anions have a displacement relative to other O^{2-} anions.

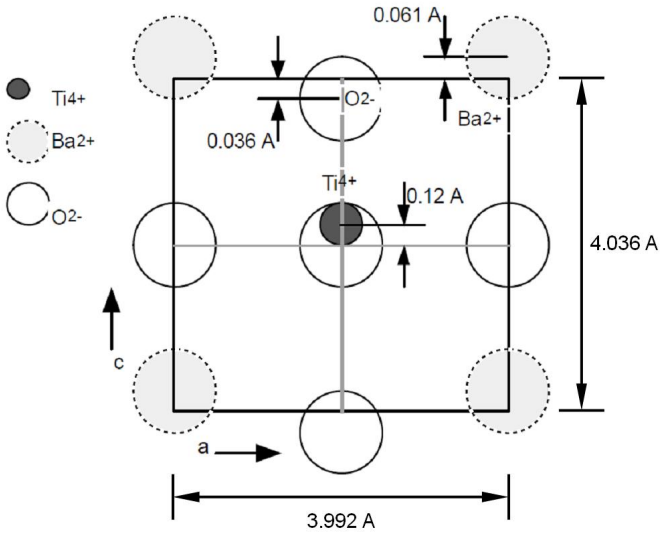


Figure 2.6 Ionic displacements in $BaTiO_3$. [2.16]

2.5 Lead Titanate (PT) and Lead Zirconate Titanate (PZT)

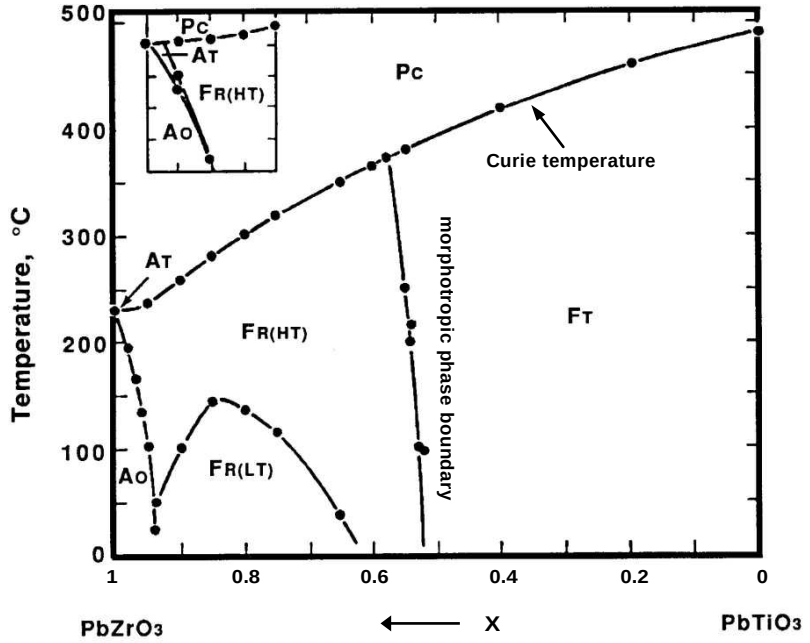
Lead Titanate ($PbTiO_3$, PT) is ferroelectric, has a structure similar to $BaTiO_3$ with a higher Curie temperature (490°C). $PbTiO_3$ is difficult to fabricate in bulk form because it undergoes a large volume change during temperature change beyond Curie temperature. The transition between the cubic phase (c/a=1.00) and the tetragonal phase (c/a=1.065) leads to large strain. Hence, a piece of $PbTiO_3$ ceramic can crack into fragments during fabrication. Therefore, PT materials are prepared usually with modification by proper dopants.

Although $PbTiO_3$ is similar to $BaTiO_3$, there are many important differences between the two materials. The tetragonal lattice distortion in $PbTiO_3$ is much larger than in $BaTiO_3$. The lattice constants of $PbTiO_3$ at room temperature are a = 3.900Å and c = 4.153 Å. [2.19] This gives a value of c/a = 1.065 while it is only 1.01 in $BaTiO_3$. Another difference is that

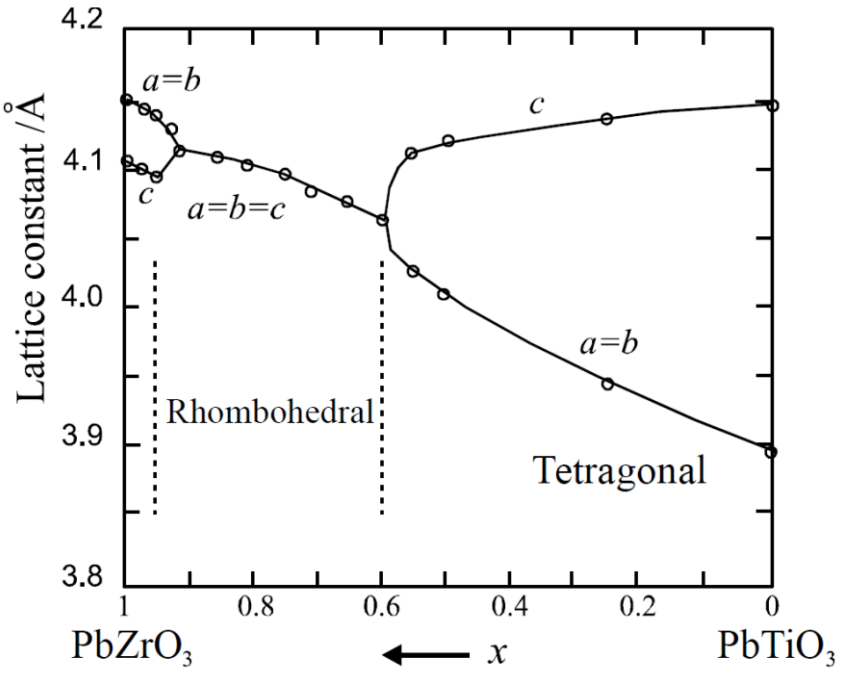
$BaTiO_3$ has a sequence of ferroelectric phases (tetragonal-orthorhombic-rhombohedral), while only the tetragonal ferroelectric phase seems to be present in $PbTiO_3$.

Perovskite oxides can easily form solid solutions. Ba/Sr in $Ba_xSr_{1-x}TiO_3$ or Zr/Ti in $PbZr_xTi_{1-x}O_3$ ($0<x<1$) are very common examples. Such a change in cations can lead to a shift of the transition temperature as well as the appearance/disappearance of the phase, etc. Lead zirconate titanate ($PbZr_xTi_{1-x}O_3$, PZT) is a binary solid solution of $PbZrO_3$ (PZ) and $PbTiO_3$ (PT) which are soluble in any mixing ratios. Isovalent Ti^{4+} and Zr^{4+} occupy B sites of perovskite randomly. $PbZrO_3$ is antiferroelectric and has an orthorhombic perovskite structure. In antiferroelectric materials, for every polarized dipole there is always a coupled antiparallel dipole in the neighborhood. Therefore, the macroscopic net polarization is zero. With a small amount substitution of Zr by Ti in $PbZrO_3$, the resulting $PbZr_xTi_{1-x}O_3$ becomes ferroelectric with a rhombohedral structure. **Figure 2.7(a)** shows the phase diagram of PZT with different Zr/Ti compositions. There is a nearly vertical boundary at the middle of the phase diagram with a Zr/Ti composition about 52/48 at room temperature. This boundary is called morphotropic phase boundary (MPB). On the Zr-rich side of the MPB, PZT is rhombohedral and on the Ti-rich side PZT is tetragonal. Near this boundary, rhombohedral and tetragonal phases can coexist. The lattice constant is also dependent on the Zr/Ti ratio, which is shown in **Figure 2.7(b)**.

The polarization of PZT with a composition at the morphotropic phase boundary becomes easier because there can be 14 possible orientations (six ‹001› directions of the tetragonal phase and eight ‹111› directions of the rhombohedral phase). Many physical properties show anomalous behavior near the MPB. For example, dielectric and piezoelectric constants have peak values here. But for the remanent polarization, some studies show peaks, some not. [2.22]–[2.24] The ferroelectric rhombohedral phase is divided into two regions: the low temperature region and the high temperature region. In the high temperature region, there are cation displacements along [111]. In addition, the oxygen octahedron tilt is found in the low temperature region. [2.25][2.26] In recent studies, an additional narrow region of the monoclinic phase near the MPB in the temperature range of 20–300K is found. [2.27][2.28]



(a)



(b)

Figure 2.7 (a) Phase diagram of $PbZr_xTi_{1-x}O_3$, "F" = ferroelectric, "A" = anti-ferroelectric, "P" = paraelectric, "O" = orthorhombic, "R" = rhombohedral, "T" = tetragonal, "C" = cubic [2.20]
(b) Lattice constant of PZT at room temperature. [2.21]

2.6 Bismuth Layer Structured Ferroelectric Materials

The bismuth layer structured ferroelectric (BLSF) materials were discovered in a comprehensive study of bismuth compounds by Bengt Aurivillius in 1949. [2.29] The ferroelectric nature of these materials was discovered about a decade later. [2.30][2.31] This family of compounds (also named the Aurivillius phases) has the general formula $(Bi_2O_2)^{2+}(A_{n-1}B_nO_{3n+1})^{2-}$. Their structure can be regarded as a regular stacking of rocksalt $(Bi_2O_2)^{2+}$ slabs with n perovskite oxygen octahedra. "n" is sometimes called "Aurivillius parameter". Here A can be mono-, di- or trivalent ions or a mixture of them (Na^+, Sr^{2+}, Pb^{2+}, Bi^{3+}, etc.), B can be Ti^{4+}, Ta^{5+}, Nb^{5+}, etc. Examples include Bi_2WO_6 (n = 1), $SrBi_2Ta_2O_9$ (n = 2) and $Bi_4Ti_3O_{12}$ (n = 3). Additional members can also be generated by allowing stacking with perovskite blocks of different n sizes. It is shown by many studies that BLSFs with even n only exhibit P_s along the a-axis but those with odd n can have a minor P_s along the c-axis or a major P_s along the a-axis. [2.32]–[2.35]

Figure 2.8 shows the crystal structure of $SrBi_2Ta_2O_9$ (SBT, n=2) as an example. SBT has a tetragonal structure and is paraelectric at high temperature. Below its Curie temperature at about 300°C, it becomes orthorhombic with lattice parameters a=0.5531nm, b=0.5534nm, c=2.498nm at room temperature. Because the difference between a and b is very small, its orthorhombic structure is sometimes regarded as pseudo-tetragonal. There are two oxygen octahedra between bismuth oxide layers. Ta occupies the center of the octahedra and Sr occupies the interspaces between the octahedra. It should be noted that the perovskite layers in neighborhood are not aligned together along the c-axis. In **Figure 2.8**, the P1/P2 octahedra are aligned to the Sr atom adjacent to the Q1/Q2 octahedra and vice versa. Therefore a unit cell of SBT includes two perovskite layers between three bismuth oxide layers.

The spontaneous polarization originates from rotation and tilt of the octahedra. When the octahedra tilt and rotate along the a-axis, a net polarization along the a-axis can occur. There are glide planes (mirror + translation) perpendicular to the b-axis between neighboring octahedral rows, so there is no net polarization along the b-axis. For BLSFs with even n, there are also mirror planes perpendicular to the c-axis between adjacent octahedra, for example between P1, P2 and between Q1, Q2 in **Figure 2.8**. Hence the net polarization along the

c-axis becomes zero, too. But for BLSFs with odd n, such mirror planes don't exist. A non-zero net polarization along c-axis is possible. [2.32][2.36]–[2.39]

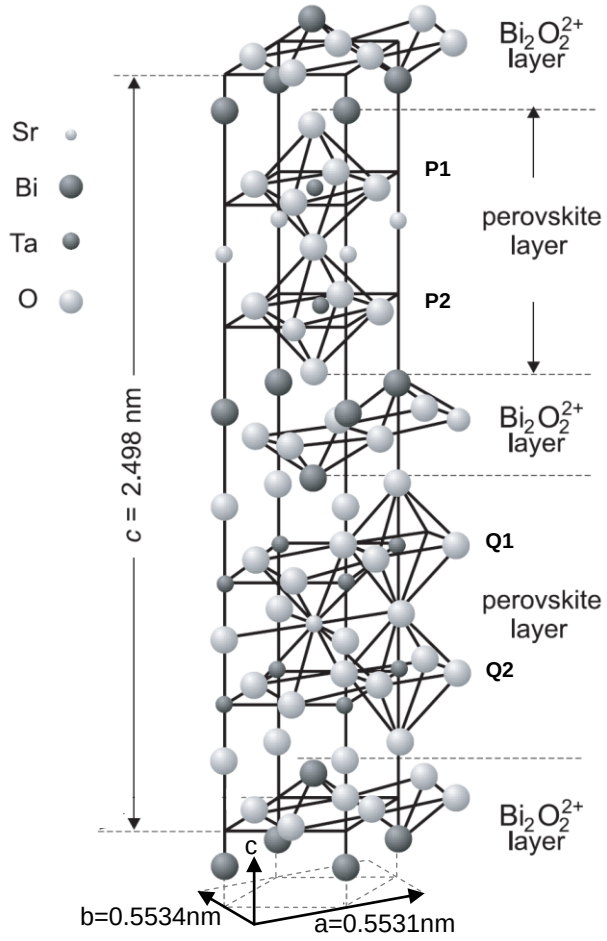


Figure 2.8 Crystal structure of SBT.

Bismuth titanate ($Bi_4Ti_3O_{12}$, BIT) is a prototype member of BLSF materials with n=3. Each perovskite layer of BIT comprises three layers of corner-sharing TiO_6 octahedra. At high temperature, the compound is paraelectric with tetragonal structure. Below the Curie temperature (~675°C), the structure is ferroelectric and can be described as a subtle monoclinic distortion of an essentially orthorhombic symmetry (a=0.5448nm, b=0.5411nm, c=3.283nm at 25°C).

2.7 Ferroelectric Capacitor for FeRAM Applications

Ferroelectric capacitors are the hearts of a FeRAM. The characteristic of ferroelectric capacitors plays the most important role for the performance of a FeRAM.

2.7.1 Two- and Three-Dimensional Ferroelectric Capacitors

At the beginning of the development of FeRAMs, a ferroelectric capacitor was integrated into a FeRAM memory cell by putting a two-dimensional parallel-plate ferroelectric capacitor on the field oxide directly adjacent to the cell transistor and making contact to top/bottom electrodes from the upper side. Such a memory cell is called offset cell and is shown in **Figures 2.9(a)** and **(c)**. The advantage of an offset cell is that the capacitor is made before contact formation and metallization in the process flow. Because deposition and post-deposition treatment of the ferroelectric film are usually under high temperature and high oxidizing ambience, making the ferroelectric capacitor before contact formation and metallization can prevent degradation of contacts/vias and metal interconnections. A serious drawback of the offset cell is the very large cell area. This kind of structure is only suitable for noncritical applications with low cell density and low memory capacity.

In order to reduce cell size and to achieve a high cell density and a high memory capacity, the ferroelectric capacitor must be stacked above the cell transistor such as the one shown in **Figures 2.9(b)** and **(d)**. The ferroelectric capacitor is usually stacked on top of a contact plug and under the first metal layer, but it's also possible to be stacked at higher layer. The requirement to realize a stacked ferroelectric capacitor is, at first, a suitable conductive oxygen barrier layer between contact plug and bottom electrode to protect the top side of the contact plug against oxidation and then to keep the contact plug at low electrical resistance. Some bottom electrode materials are inert to oxidation and can also work as oxygen barrier to protect the contact plug. In addition, a suitable diffusion barrier layer between contact plug and bottom electrode of the ferroelectric capacitor as well as between contact plug and source/drain of the cell transistor is necessary to prevent interdiffusion of materials from both sides at high temperature. These diffusion barrier and oxygen barrier layers protect the interconnection between bottom electrode and cell transistor during the deposition and

post-deposition treatment of ferroelectric film against high temperature and high oxidizing ambience and ensure the electrical function of the ferroelectric memory cell.

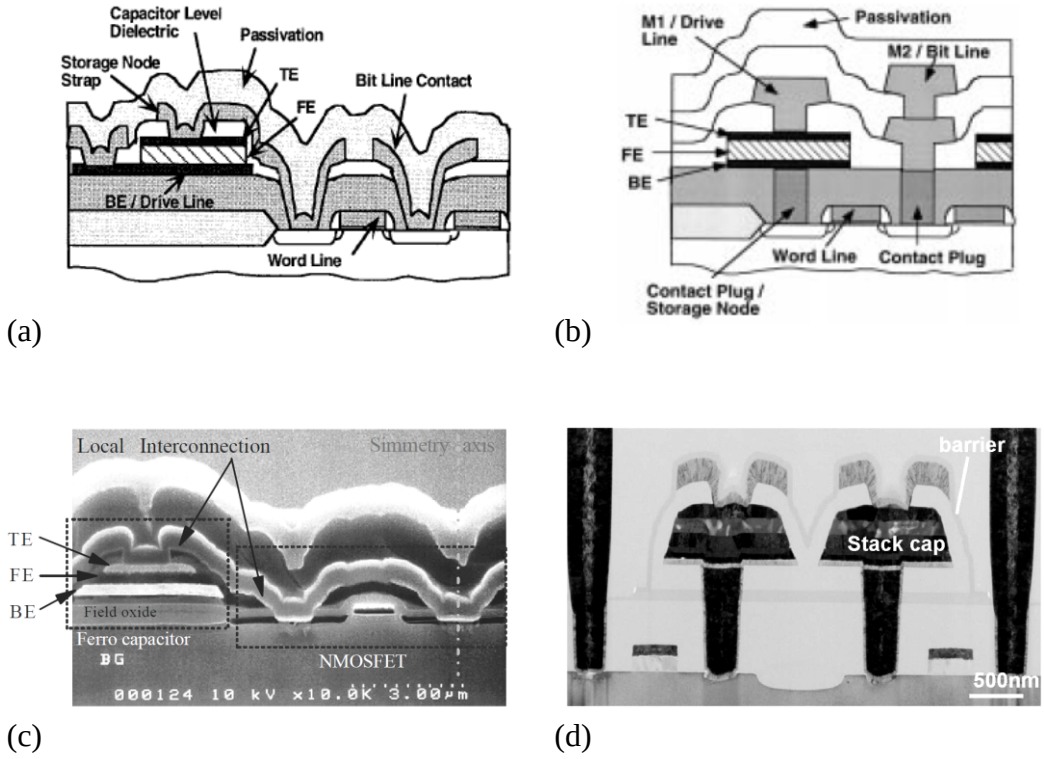
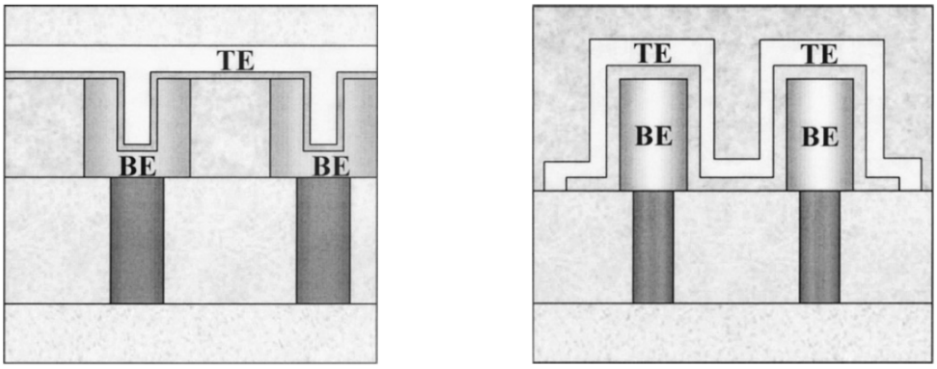


Figure 2.9 FeRAM memory cell with parallel-plate ferroelectric capacitors. (a)(c) offset cell, (b)(d) stacked cell. [2.40]–[2.42]

As the devices of integrated circuits are being scaled down more and more, the dimension of the ferroelectric capacitor is also forced to be miniaturized along with other devices on the chip. Meanwhile, the miniaturized ferroelectric capacitor must still have enough remanent polarization to provide enough signal difference between “0” and “1”. This situation causes a dilemma that a two dimensional parallel-plate ferroelectric capacitor cannot fulfill the demand of miniaturization and enough signal strength at the same time. The same problem has happened in DRAM development about 25 years ago; and the solution was to

use three-dimensional capacitor structures to obtain more area from vertical sidewalls. [2.43][2.44] The same solution may be applicable for FeRAMs.

Up to now, all the FeRAM chips in mass-production use two-dimensional parallel-plate capacitors as storage node. Three-dimensional ferroelectric capacitors are still under development. **Figure 2.10** shows two simple examples of three-dimensional structures for ferroelectric capacitors: cup-type and pin-type. In these examples bottom electrode, ferroelectric film and top electrode are defined with separate lithography process steps but it's possible to reduce necessary lithography steps by optimization of the real structure and process design. In DRAM technology there are also fin-type and crown-type structures which may be choices for FeRAMs, too. [2.44]



(a) (b)

Figure 2.10 Three-dimensional structures of ferroelectric capacitor. (a) cup-type, (b) pin-type. [2.45]

In order to realize a three-dimensional ferroelectric capacitor, a conformal deposition of the ferroelectric layer is absolutely necessary. For bottom/top electrode layers, a conformal deposition is not indispensable but still preferred. Characteristics and operating conditions of ferroelectric capacitors have a strong relation with ferroelectric film thickness. Only conformal ferroelectric films can ensure a reliable function of ferroelectric capacitors. **Figure 2.11** shows a prototype of a three-dimensional cup-type ferroelectric capacitor made by Samsung.

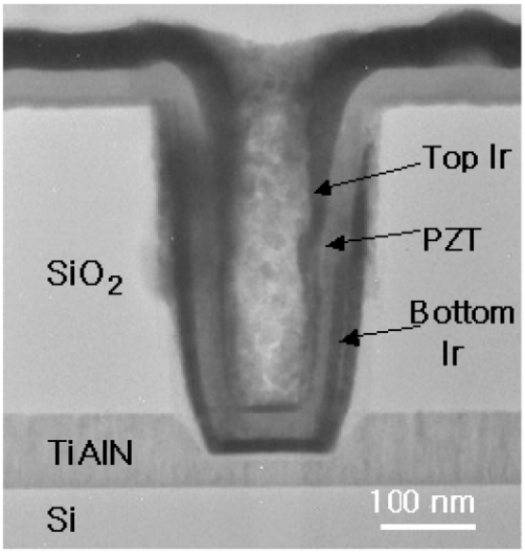


Figure 2.11 Completed Ir/PZT/Ir trench capacitor with hole diameter 0.18μm. (TEM image) [2.46]

2.7.2 Reliability Issues of Ferroelectric Capacitors

As the most important part of a memory cell in a FeRAM, ferroelectric capacitors are polarized over million, billion even much more cycles in their whole lifetime. Their properties degrade during polarization cycles. **Figure 2.12** shows the relation of remanent polarization of PZT film with switching cycles. It can be seen that after 10^4 cycles the remanent polarization begins to decrease and remains only 30% of the initial value after 10^7 cycles. Such a degradation after cycling is called fatigue. The loss of remanent polarization after repeated read/write cycles of ferroelectric memory cells causes a serious problem for sensing amplifier to distinguish between “0” and “1” of a memory cell. That means, a limited lifetime of FeRAM is strongly related to the fatigue property of the ferroelectric materials.

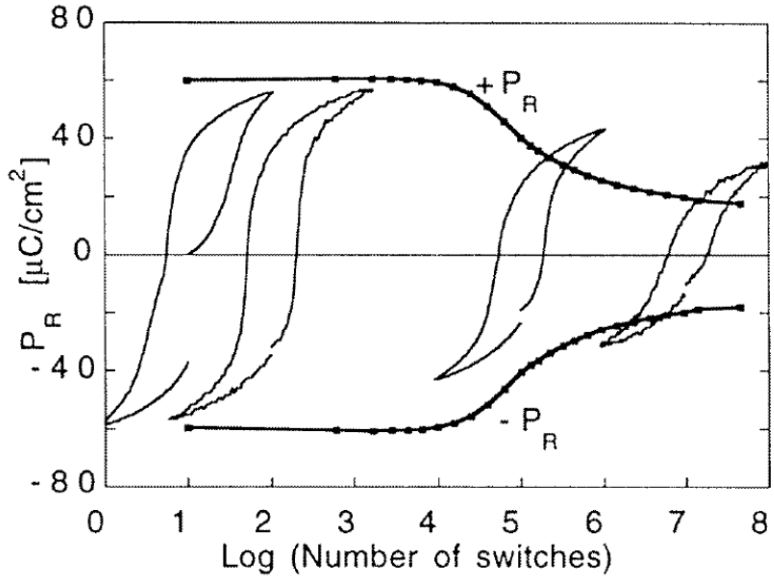


Figure 2.12 An example of polarization fatigue in a PZT film with Pt electrodes. [2.47]

Polarization fatigue can be considered with following possible factors: (i) reduction of the effective electrode area, (ii) reduction of the effective electric field and (iii) degradation of the ferroelectric film itself that makes polarization switching more difficult.

With a non-optimized process, electrode delamination or burn-out can be found after cycling. [2.48][2.49] Because the available electrode area becomes smaller, the effective capacitor area is smaller and therefore the remanent polarization becomes smaller.

In some studies it is supposed that appearance and growth of a thin low-dielectric-constant interface layer between electrode and ferroelectric material during cycling is responsible for fatigue. [2.50]–[2.52] As the interface layer grows with cycling, the effective external field seen by the ferroelectric material decreases and eventually becomes insufficient to switch the domains.

Many models are proposed to explain the fatigue phenomenon under the aspect of degradation of the ferroelectric film itself. Among them are: (1) Domain wall pinning, (2) Nucleation inhibition, (3) Local phase decomposition.

Warren et al. [2.53] and Scott et al. [2.54] thought, during read/write cycling, more and more domain walls are pinned. A domain is not switchable any more if it's surrounded by pinned domain walls. So, the remanent polarization degrades. It is believed that electronic charge trapped at domain walls and ionic defects such as oxygen vacancies are responsible for domain wall pinning.

Tagantsev et al. [2.55] proposed another model related to the nucleation inhibition. In this model it is assumed that polarization switching begins with nucleation seeds of reversed domains near the ferroelectric/electrode interface. These nucleation seeds are blocked during cycling by accumulated ionic or electronic defects, which can be created by charges injected from the electrode or by charges that can arrive from the bulk of the material as a result of electromigration by electric stressing during cycling.

The local phase decomposition model is proposed by Lou and his colleagues. [2.56] They showed that PZT thin films undergo a local phase decomposition from the perovskite structure to a pyrochlore-like phase (possibly containing Ti/Zr–O clusters) near an electrode during bipolar electrical fatigue. This local phase decomposition is initiated by switching-induced charge injection from an electrode. Because the decomposed region becomes pyrochlore and has a lower dielectric constant, the effective electric field applied to a ferroelectric region is reduced. Furthermore, the most probable locations where phase decomposition occurs are the domain nucleation sites. The collapse of nuclei and the decrease of the available nucleation sites during electrical cycling also make switching more difficult.

The hysteresis characteristic of ferroelectric capacitors is not always symmetric to both polarization states. Sometimes one polarization state is preferred to the other one, especially, after the ferroelectric material has been polarized and kept without external electric field for a long time. A shift of the hysteresis loop along the electric field axis with unequal coercive field for each polarization state can be observed. This phenomenon is called imprint which is shown in **Figure 2.13**. Imprint results in asymmetric switching and incomplete polarity reversal. The consequences are read/write failures if imprint is not controlled within a range which is acceptable by the sensing amplifier for correct read/write operations.

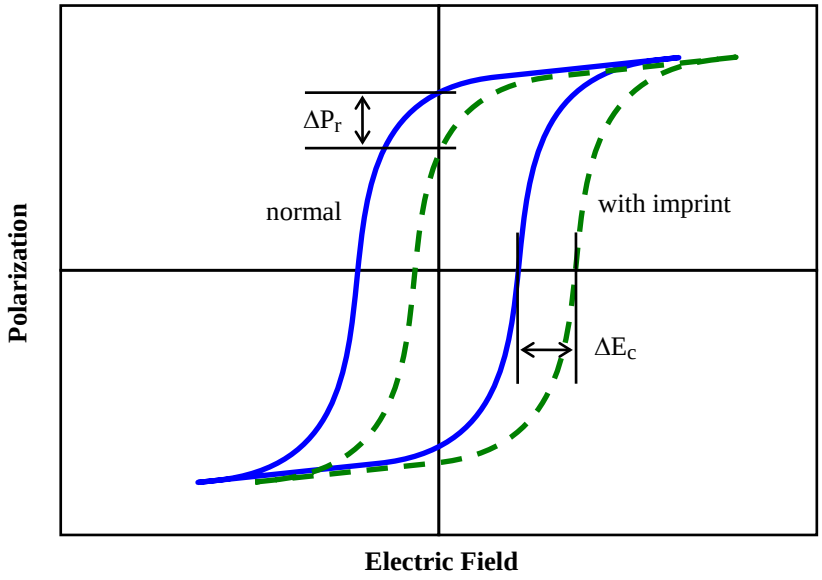


Figure 2.13 Imprint.

Several models have been proposed to explain the imprint phenomenon. [2.57]–[2.59] Warren and his colleagues proposed that defect dipoles associated with oxygen vacancies and acceptor ions are responsible for imprint. Mobile oxygen vacancies are very usual in perovskite crystals. The defect dipoles form an internal electric field in the ferroelectric materials and can be reoriented under an external electric field but much more slowly than ferroelectric switching. This internal electric field caused by defect dipoles is the origin of imprint. [2.60]–[2.63] Domain pinning caused by charge trapping near domain walls is also thought to be a possible mechanism to result in imprint. [2.64][2.65] In another model, Abe et al. proposed that a non-switching layer, which possesses irreversible polarization, is present between the bottom electrode and the ferroelectric layer in order to release lattice misfit stress in the early stage of the heteroepitaxial growth. The voltage shift of the hysteresis loop is caused by this layer. [2.66][2.67] A similar model has also been proposed by Grossmann et al., in which a residual depolarizing field causes charge emission from an electrode into the film or charge separation in the interior of a surface layer between electrode and ferroelectric film. If these charges are trapped at the interface between the ferroelectric and the surface layer they would also cause an internal bias. [2.59]

In addition to fatigue and imprint, retention is also an important property of ferroelectric materials, which relates to the ability of maintaining the polarization state in

absence of an external electric field. Retention failure means the loss of remanent polarization after certain duration without an external electric field. For the application as nonvolatile memory, the data in the memory cells should persist for a long enough time without supply of external electricity. The usual industrial criterion for retention is longer than 10 years. Generally, it is accepted that retention loss is caused by a depolarization field, which remains in ferroelectric films after the external voltage on the electrodes of ferroelectric capacitors is removed. The depolarization field exists because polarization induced bound charges at the surface of the ferroelectric material near electrodes are not completely compensated by free charges in conducting electrode. This field causes the relaxation of remanent polarization. [2.68][2.69]

2.7.3 Materials for Ferroelectric Capacitors

Up to now only PZT and SBT are used as ferroelectric materials for the fabrication of FeRAM either for mass production or for prototype demonstration.

Although $BaTiO_3$ is the first discovered ferroelectric perovskite oxide and is well investigated, it is not suitable for the application in nonvolatile memories as dielectric layer of ferroelectric capacitors. First of all, a $BaTiO_3$ thin film has a much lower remanent polarization than its bulk form, and in some researches $BaTiO_3$ thin films are even paraelectric. [2.70]–[2.72] Besides, the Curie temperature of bulk single crystal $BaTiO_3$ is around 130°C, and at 0°C there is a phase transition between tetragonal and orthorhombic phases. Near these transition temperatures the properties such as spontaneous polarization and relative permittivity show anomalous behavior and the read/write operation of a FeRAM can be disturbed if $BaTiO_3$ is used in the ferroelectric capacitor. The operation temperature of a FeRAM made of $BaTiO_3$ is, therefore, limited to be impractical.

There is an exception that strained heteroepitaxial $SrRuO_3/BaTiO_3/SrRuO_3$ structures or similar structures are found to be ferroelectric and exhibit a higher remanent polarization than bulk single crystal $BaTiO_3$. [2.73][2.74] This may give hope to $BaTiO_3$ thin films in the future to be used in FeRAMs.

Extensive researches have been carried out for PZT not only because of its superior ferroelectric properties but also because of its superior piezoelectric properties. PZT has a higher remanent polarization, needs lower process temperature than other materials. These merits are very important to realize the production of FeRAMs. Higher remanent polarization (15–55μC/cm^2) means a smaller capacitor is necessary and a higher memory density and memory capacity are achievable. A lower process temperature (400–600°C) makes PZT more compatible than other candidates to be integrated into conventional CMOS process technology on Si.

However, PZT undergoes serious fatigue after about 10^4 read/write cycles when metallic electrodes such as Pt are used. [2.75][2.76] This problem has been solved recently by using metal-oxide electrodes and will be discussed in the next section. Another problem is the environmental issue of toxic Pb in PZT. Scientists and engineers are still looking for a better candidate to replace PZT because of its toxicity.

SBT has its advocates because it has some important properties that PZT doesn't have. SBT has no fatigue problem, which exists on PZT with Pt electrode. After up to 10^{12} read/write cycles SBT shows almost no degradation of remanent polarization. [2.75]–[2.79] SBT is not toxic, so there is no environmental problem with SBT. But the remanent polarization of SBT is usually only 5–15μC/cm^2, which is much lower than for PZT. Furthermore, higher process temperatures (700–850°C) are necessary for crystallization of SBT. Such high temperatures make it difficult to integrate SBT into a conventional CMOS process. A comparison between PZT and SBT is shown in **Table 2.1**

Table 2.1 Comparison between PZT and SBT.

	PZT	**SBT**
Crystal structure	ABO_3 Perovskite	Bismuth-Layered Perovskite
Process temperature	400~600°C	700~850°C
Remanent polarization	15~55μC/cm^2	5~15μC/cm^2
Fatigue	Poor (Pt electrode) Good (metal oxide electrode)	Good

There are a few ferroelectric materials which can be potential candidates to be used in ferroelectric capacitor of FeRAMs. Bismuth titanate ($Bi_4Ti_3O_{12}$, BIT) is a member of the BLSF materials. Bulk single crystal BIT has a larger remanent polarization (~50μC/cm^2) [2.80] and a lower crystallization temperature (~650°C) than SBT. However, unlike SBT, BIT thin films show fatigue and have a much lower remanent polarization than its bulk form. [2.81] Some researchers suggested Lanthanoid and/or higher-valent cation substitution for Bi and Ti sites, for example, lanthanum-substituted bismuth titanate ($(Bi_{4-x}La_x)Ti_3O_{12}$, BLT). The improvements of remanent polarization and fatigue have been shown in several studies. [2.82]–[2.86]

Bismuth ferrite ($BiFeO_3$, BFO) is a new potential candidate in FeRAM application. The lattice structure of the single crystal BFO is rhombohedrally distorted perovskite. When the remanent polarization of an epitaxial BFO thin film was shown to be over 50μC/cm^2 in 2003, [2.87] it became one of the most attractive factors in addition to its lead-free composition for FeRAM application. The usual remanent polarization of BFO ranges from 50μC/cm^2 to 100μC/cm^2 and in some research can be even up to 150μC/cm^2.[2.88] Unfortunately, very high leakage currents are a serious problem of BFO. The very high remanent polarization can only be measured at very low temperature with liquid nitrogen cooling. Many efforts such as impurity substitution with rare earth or transition metal elements have been tried to improve leakage current and other properties of BFO and some of them seem to be promising. [2.89]–[2.92] Further studies for process development and properties improvement are still necessary in order to realize the application of BFO in FeRAMs.

2.7.4 Electrodes of Ferroelectric Capacitors

The selection of electrode materials is a challenge for ferroelectric capacitor applications. Many criteria must be fulfilled in order to obtain the required ferroelectric function of the capacitors:

1. The electrode materials must be inert under oxidizing environment and high temperature during processing, especially during the deposition process of the ferroelectric film. Or if it's not inert, the oxidized electrode material must be electrical conductive. Formation of

an insulating layer of the oxidized electrode material with a low dielectric constant can cause a reduced performance of the ferroelectric capacitor.

2. The electrode material may not react with the materials above and under the electrode. It is especially important to prevent the reaction between the ferroelectric film and the electrode. Otherwise degradation of the ferroelectric film can happen.
3. The electrode material should work as a diffusion barrier against oxygen which may diffuse from environment through the electrode into the contact/via material which is under the bottom electrode or over the top electrode. In addition, it should also work as a diffusion barrier to prevent the interdiffusion between ferroelectric film and contact/via material which is under the bottom electrode or over the top electrode.
4. The lattice mismatch between the electrode material and ferroelectric material must be taken into account. A smaller lattice mismatch is preferred in order to minimize mechanical strain and improve crystallization of the ferroelectric film.

Many electrode materials have been investigated according to the requirements mentioned above. They can be classified into two categories: metal based and conductive oxide based. Metal based materials include platinum, [2.75][2.93] iridium [2.94]–[2.97] and ruthenium. [2.98]–[2.100] Conductive oxide based materials include rutile-type conductive oxides such as iridium oxide IrO_2 [2.101]–[2.103] and ruthenium oxide RuO_2 [2.104]–[2.106] and perovskite-type conductive oxides such as strontium ruthenate $SrRuO_3$ (SRO), [2.103][2.107][2.108] lanthanum nickel oxide $LaNiO_3$ (LNO), [2.109]–[2.113] lanthanum strontium cobalt oxide $La_{(1-x)}Sr_xCoO_3$ (LSCO), [2.76][2.114]–[2.116] lanthanum strontium manganese oxide $La_{(1-x)}Sr_xMnO_3$ (LSMO), barium ruthenate $BaRuO_3$, barium lead oxide $BaPbO_3$ (BPO), and superconducting $YBa_2Cu_3O_{(7-x)}$ (YBCO). [2.117]–[2.119]

At the early stage of developing ferroelectric capacitor, platinum (Pt) was the most widely used electrode for PZT, SBT and other ferroelectric films. Even under high temperature Pt is still relative inert to oxygen. This was very beneficial because annealing at very high temperature (600–850°C) for crystallization of PZT, and especially SBT was necessary at that time. Another advantage of Pt is that Pt has a small lattice mismatch with PZT (~ –2.9%).

However Pt has disadvantages, too. Because of a high mechanical strain between Pt bottom electrode and substrate, hillocks form in the Pt film under high temperature and can

cause short-circuits. [2.120][2.121] Usually Ti is used as adhesion layer between Pt and the substrate in order to reduce strain and improve adhesion. It is found that Ti can diffuse through Pt to the electrode/ferroelectric film interface and form TiO_2 and Pt_3Ti under high temperature and oxidizing environment. The ferroelectric capacitor is, therefore, degraded. Oxygen can also diffuse from the ferroelectric film or environment through Pt to the adhesion layer and the contact/via materials. Adhesion layer and contact/via materials are hence oxidized, resulting in a higher resistance. Furthermore, it was also found that Pb in PZT films penetrates the Pt electrode and reacts with other materials. PZT films become Pb-insufficient and thus degrade.[2.102][2.120][2.122] All these phenomena show that Pt doesn't work well as a diffusion barrier.

In addition, during the back-end process of modern CMOS technology, which includes metallization, inter-metal-dielectrics deposition and passivation, wafers are often exposed to reducing ambience with hydrogen. Pt electrodes act as an effective catalyst to activate deoxidization of ferroelectric films and cause degradation of the remanent polarization. [2.123]–[2.125]

The most serious problem of ferroelectric PZT capacitor with Pt electrode is fatigue. In many studies fatigue can happen after only 10^4 read/write cycles.[2.75][2.94][2.102][2.104] This value is too low for memory application, in which a capability of at least 10^{12} to 10^{15} read/write cycles should be fulfilled.

Iridium has been considered as a candidate for electrodes for ferroelectric capacitors because it's thermally more stable than Pt. Ir doesn't react with Silicon and oxygen at high temperature. Ir itself acts as diffusion barrier to prevent diffusion of oxygen and Pb. [2.126]–[2.128] Improved fatigue properties of PZT ferroelectric capacitor with Ir electrodes was also shown by several studies.[2.94][2.101][2.129]

Ruthenium, Ru is another candidate for electrodes for ferroelectric capacitors. It has a merit that Pt and Ir don't have: Ru can be etched in a dry etching process. For Pt and Ir dry etching is difficult. The effect of Ru electrodes on fatigue properties is controversial. Some studies show improvement, some not. [2.98][2.99]

The use of conductive oxide electrodes has been suggested by many researchers in order to solve the polarization fatigue problem with Pt. The improvement is demonstrated with many types of conductive oxide electrodes such as IrO_2, RuO_2, LNO, LSCO and SRO. **Figure 2.14** shows some results of early studies.

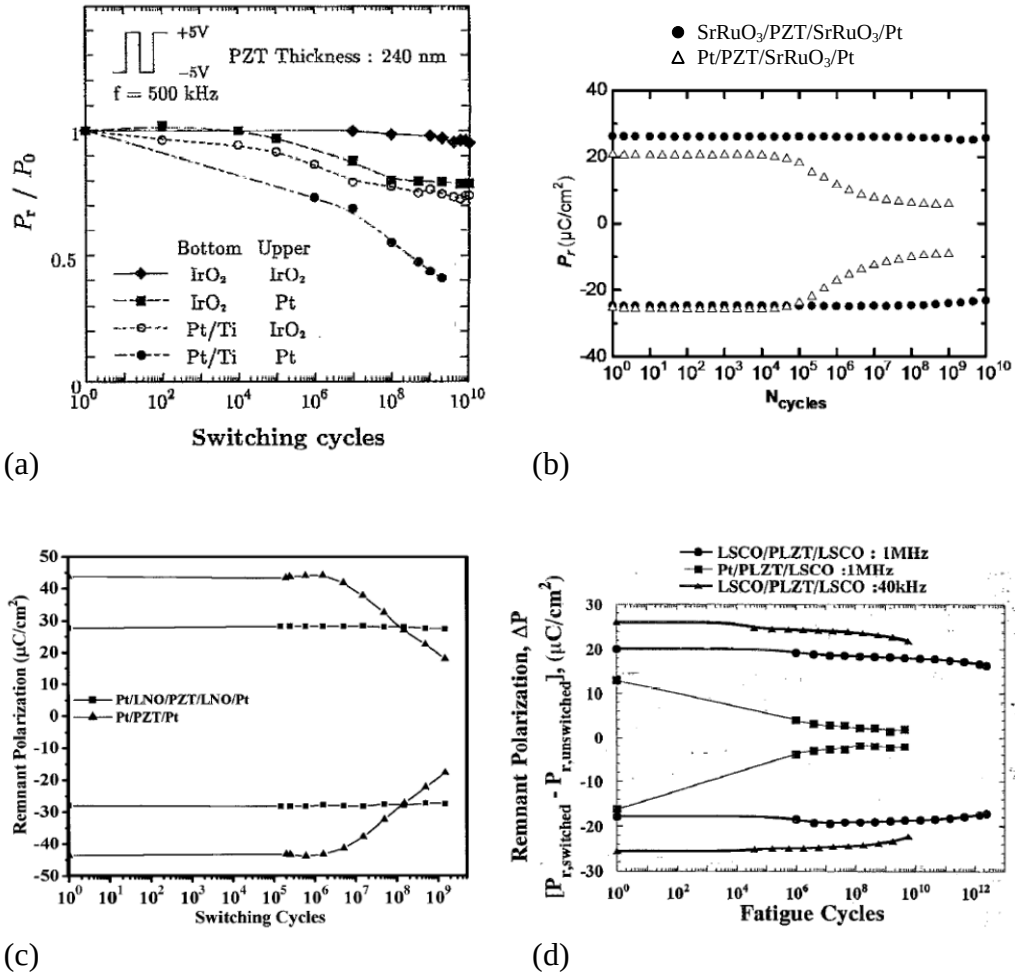


Figure 2.14 Fatigue properties of PZT and PLZT with various electrode materials: (a) IrO_2, [2.102] (b) SRO, [2.108] (c) LNO, [2.112] (d) LSCO. [2.114]

The phenomenon that PZT films with conductive oxide electrodes instead of metal electrodes do not fatigue after cycling gives an idea that oxygen vacancies may play an important role. It is believed that conductive oxide electrodes act as sinks for oxygen vacancies and prevent their accumulation at the PZT/electrode interface. Smaller concentrations of oxygen vacancies at the interface result in a reduced injection of electronic carriers from the electrodes into the ferroelectric film, and consequently reduce pinning of

domain walls and fatigue. [2.47] This model of oxygen vacancies for fatigue phenomenon is supported by a study of Auger microprobe at the interface of Pt/PZT.[2.130] It was found that after cycling the oxygen concentration in PZT near the Pt electrode decreased in comparison to that before cycling.

In addition to the function of oxygen vacancy suppression, IrO_2 as top electrode shows a further advantage: it works as a hydrogen barrier against the reducing ambience in back-end processes to prevent degradation of the ferroelectric film. [2.131]–[2.133]

At the interface between electrode and PZT, structural discontinuity can generate defects which contain plenty of dangling bonds, vacancies and trapped charges and cause degradation of the ferroelectric properties. Perovskite-type conductive oxide electrodes are supposed to have inherent advantage that they have a well matched structure and chemistry with regard to the ferroelectric perovskite PZT. They can promote nucleation and crystallization of PZT better than rutile-type IrO_2 and RuO_2. Many research results of LNO, LSCO and SRO are available. Among them, SRO is the most popular candidate in recent studies because SRO has a smaller lattice mismatch with PZT (~ –2.7%) than LNO (~ –5.4%) and LSCO (~ –5.2%).

However, it was found that PZT ferroelectric capacitors with conductive oxide electrodes, especially RuO_2 and SRO, have a higher leakage current density than with Pt electrodes.[2.103][2.105][2.107][2.134] Two models have been proposed to explain the higher leakage current density of PZT capacitors with conductive oxide electrodes. The first one supposes that the higher leakage current density is caused by a lower Schottky barrier height between PZT and the conductive oxide electrodes.[2.51][2.103] The charge carrier injection through the PZT/electrode interface is higher if the Schottky barrier height is lower and consequently a higher leakage current density occurs. The second model supposes the existence of an impurity phase in the PZT film, which forms a leakage path through the PZT film.[2.104][2.135] This model is supported by other studies, which showed outdiffusion of Ru and Sr from SRO into PZT with SIMS analysis.[2.128] In another study, a pyrochlore phase, which was assumed to be conductive $Pb_2Ru_2O_{7-X}$, was found in PZT under TEM.[2.105][2.136][2.137]

The state-of-the-art ferroelectric capacitors use generally a combination of SRO, Ir and IrO_2 as multilayer electrode to optimize the ferroelectric properties of PZT and to prevent

oxidation and interdiffusion of the materials which are in contact with the ferroelectric capacitor.[2.138][2.139]

2.7.5 Etching Process of Ferroelectric Capacitors

Reactive ion etching (RIE)/plasma etching is widely used in modern IC technology to form device structures, connections between devices and various patterns which are defined by photo lithography. However, applying this method to the formation of ferroelectric capacitors encounters many difficulties. Halogen-containing gases are often used in plasma etching processes to form volatile compounds of etched materials. Unfortunately, halides of the electrode materials Ir, Pt and many ferroelectric materials have high melting and boiling points, and, therefore, have low volatilities. The melting and boiling points of halides of some electrode and ferroelectric materials are shown in **Table 2.2**.

Table 2.2 Melting points and boiling points of halides of electrode and ferroelectric materials.[2.140]–[2.145]

Compound	mp (°C)	bp (°C)	Compound	mp (°C)	bp (°C)
PtF_4	600	-	PbF_2	855	1290
PtF_6	61.3	69.1	PbF_4	~600	-
$PtCl_2$	581	-	$PbCl_2$	501	954
$PtCl_3$	435	-	$PbCl_4$	-15	50
$PtCl_4$	370	-	$PbBr_2$	373	914
$PtBr_2$	250	-			
$PtBr_3$	200	-	ZrF_4	932	912
$PtBr_4$	180	-	$ZrCl_2$	727	1292
			$ZrCl_4$	437	331
IrF_3	250	-	$ZrBr_4$	450	357
IrF_6	44	53			
$IrCl_2$	>733	-	TiF_3	1200	1400
$IrCl_3$	763	-	TiF_4	284	-
$IrCl_4$	~700	-	$TiCl_2$	1035	1500
			$TiCl_3$	440	960
			$TiCl_4$	-24	136.5
			$TiBr_2$	>500	-
			$TiBr_3$	39	230
			$TiBr_4$	38	234

Low volatility of the etching products means low etching rates. In comparison to plasma etching of silicon with CF_4, the etching product SiF_4 has a melting point at –90.2°C and a boiling point at –86°C. It is apparent that iridium, platinum and PZT are more difficult to etch with reactive plasma than other usual materials in IC technology. The consequences are low etching rates, low sidewall slopes of etched structures and many etching residues. If the process parameters are not optimized, their etching rates are even lower than those of mask materials used for etching. [2.146]–[2.154]

Figure 2.15 shows some typical examples of electrode and ferroelectric materials after RIE processes. It can be seen in **Figures 2.15(a)** and **(b)** that fences form on top of the etched sidewall. Because of a low etching rate, higher DC bias and additional Ar gas are often used in RIE to enhance the etching rate by physical ion sputtering. The drawback is the redeposition of sputtered nonvolatile etching products on sidewalls of the etching mask and etched material. Redeposition on mask sidewalls causes the fence formation seen in **Figures 2.15(a)** and **(b)**.

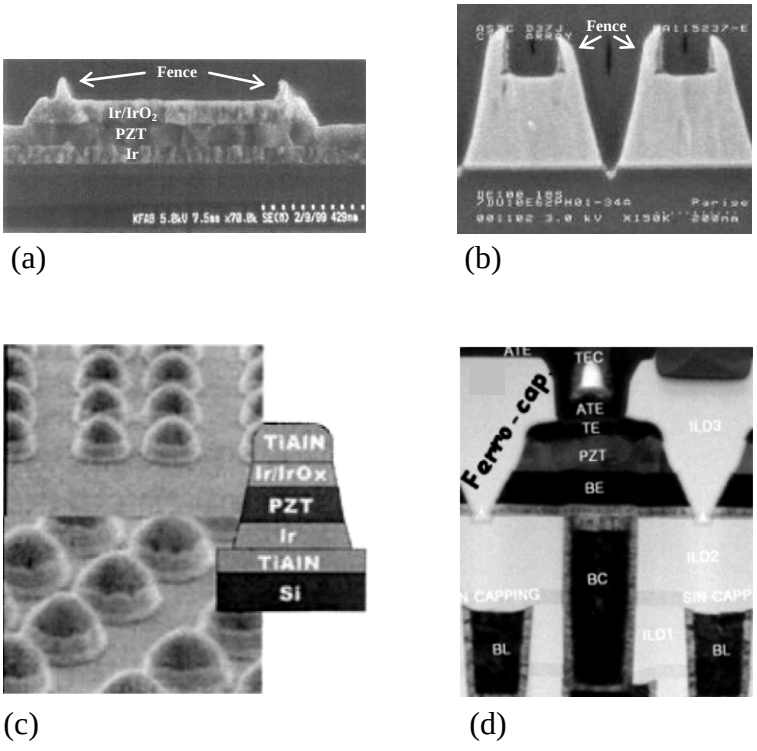


Figure 2.15 Electrode and ferroelectric materials after reactive ion etching. (a) Ir/IrO2, [2.155] (b) Pt, [2.156] (c) capacitor stack, [2.157] (d) complete ferroelectric capacitor. [2.158]

Redeposition on sidewalls of etched material results in sidewalls with lower slopes and deviations of structure dimensions. In RIE processes, not only the material which is supposed to be etched but also the mask material can be etched by reactive ions on both upper and lateral sides. Mask thickness and lateral dimensions decrease during etching. If the lateral dimension of an etching mask decreases very much during etching, the sidewall of etched material will have a low slope. In an ideal etching process, the selectivity (etching rate of target material/etching rate of mask) should be high enough to ensure a high slope sidewall. In the case of a ferroelectric capacitor, because of low selectivity, the sidewall slope is usually lower than 75° (**Figures 2.15(c)** and **(d)**). This causes a wasted area at the capacitor edge and makes scale down of ferroelectric capacitors more difficult.

A further problem can happen if the whole capacitor stack is etched at one time with a single mask process: redeposition of conductive etching residues from the electrodes onto sidewalls of ferroelectric material causes leakage currents between top and bottom electrodes. [2.159][2.160] A suitable dry/wet cleaning process is, therefore, necessary to remove such residues and prevent leakage. [2.160][2.161]

In some studies, it is also shown that RIE processes cause both high leakage currents and degradation of the remanent polarization even when there is no conductive residue on the sidewall. This degradation should be attributed to plasma damage, which includes bombardment of energetic charged particles on sidewalls of ferroelectric layers and charge accumulation on top electrodes. Bombardment of sidewalls by energetic charged particles changes the crystal structure and the composition of ferroelectric materials near the sidewall region. Charge accumulation on the top electrode can induce a high internal field in the ferroelectric film, causes charge injection and trapping. The ferroelectric film is hence degraded. [2.162]–[2.165] An annealing process after etching should be used to re-establish ferroelectric properties.

SiO_2, W, TiN and TiAlN are used as hard masks instead of photoresist to improve selectivity and achieve steeper sidewall. [2.150][2.166]–[2.168] In addition, high temperature etching processes have been developed to further increase the etching rate and to reduce nonvolatile residues. Because photoresist cannot sustain high temperature processes, a suitable hard mask material for high etching temperatures is also necessary. [2.156][2.157][2.159][2.169][2.170]

Unfortunately, high temperature etching processes don't always give advantages. In some studies the etching rate is lower at high temperature or capacitor properties degrade due to high temperature etching. [2.139][2.148][2.171][2.172]

2.7.6 Hydrogen Induced Ferroelectric Degradation

It is found that ferroelectric capacitors are severely degraded if exposed to a reducing environment containing hydrogen, which is very usual in back-end processes of CMOS technology, for example, conventional interconnection technologies (chemical vapor deposition of silicon nitride, silicon oxide and W) and forming gas annealing. As confirmed by many researches, the catalytic activity of top electrode materials is closely related to this degradation.[2.173][2.174] The mechanism how ferroelectric materials are degraded by hydrogen and catalytic electrode materials during anneal is still not completely clarified. In some researches destruction of Pb-O bond into metallic Pb in PZT film near the electrode interface has been found. The resulting compositional and structural change of PZT is the reason of this degradation.[2.175][2.176] Other studies propose the formation of polar OH^- bond of hydrogen with oxygen in PZT. This polar OH^- can suppress switching of ferroelectric materials or cause domain pinning by charge trapping. [2.177][2.178] The hydrogen induced degradation of SBT and BLT was also investigated in many studies. The study of Han and Ma [2.173] showed a loss of the remanent polarization. The studies of Im et al., [2.179] Yoon et al. [2.180] and Noh et al. [2.181] showed a higher leakage current. Decomposition of Bi-O bonds into metallic Bi is suspected to be the cause of hydrogen induced degradation of SBT and BLT. [2.179]–[2.182]

One solution against hydrogen induced degradation is using materials as top electrodes, which have a lower catalytic activity. IrO_2 is an excellent candidate as top electrode because it doesn't have a strong catalytic activity, and in addition, it can improve fatigue degradation of PZT. The effectivity of IrO_2 against hydrogen was already demonstrated in many studies. [2.131][2.133][2.183]–[2.185] Another approach is using a hydrogen barrier layer to encapsulate the ferroelectric capacitor. This layer should prevent the penetration of hydrogen into the ferroelectric film. Al_2O_3, TiO_2 and SiON are commonly used as encapsulating barrier layer for ferroelectric capacitors against hydrogen. [2.161][2.186]–[2.190]

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3 Fabrication of Ferroelectric PZT Thin Films by MOCVD

3.1 Status of PZT Thin Films Deposited by MOCVD

MOCVD is the most promising technology for deposition of ferroelectric thin films in comparison with other technologies such as sputter and chemical solution deposition (CSD) because it gives better film qualities with respect to electrical and material properties. The necessary process temperature (including film deposition and annealing for crystallization) of MOCVD is lower than those of sputter and sol-gel methods. Therefore, MOCVD is more compatible to backend processes of standard IC process technology. In addition, sputter and sol-gel methods are suitable only for two dimensional thin film deposition but MOCVD possesses better step coverage for deposition on three-dimensional structures, which is important for realization of high density FeRAM.

The deposition temperature of PZT by MOCVD is usually between 550°C and 650°C in order to obtain well crystallized thin film and good ferroelectric properties. In some studies lower deposition temperatures were used but followed by crystallization annealing at higher temperatures. Tokita et al. [3.1] achieved deposition at lower temperatures down to 415°C without following crystallization annealing. Their ferroelectric capacitors of 0.1mm diameter with deposited 250nm PZT films still show good remanent polarization. In chip level manufacturing of Samsung, a deposition temperature over 530°C is necessary because of the quality of PZT films. [3.2]–[3.4] Such process temperatures (deposition and annealing) are too high for backend processes of standard IC process technology. Further lowering of the deposition/annealing temperature is still a goal for a better process compatibility.

Film thickness reduction is also an important topic for scaling down in order to achieve high density and high capacity FeRAM. Ultra-thin PZT films are necessary especially for good filling into nano-scale three-dimensional capacitor structures. Tybell et al. have demonstrated by using atomic force microscopy (AFM), that single crystalline PZT films as

thin as 4nm are still ferroelectric. [3.5] Electrical measurements on capacitors of both, single crystalline and polycrystalline PZT films thinner than 50nm also showed good ferroelectric hysteresis loops. [3.6]–[3.8] Nevertheless, chip level verification showed serious degradation of remanent polarization as thickness was reduced below 100nm. [3.3] Therefore, the thickness of PZT films in chip level production is usually kept between 70nm–100nm.

3.2 MOCVD System and Precursors for PZT Thin Film Deposition

The difference between MOCVD technology and other CVD technologies is that metalorganic precursors are used as reactants in MOCVD technology. Because metalorganic precursors are usually in liquid or solid form rather than gaseous form, special systems are necessary in MOCVD equipment to convert precursors into gaseous form and to transport them into the reactor.

Conventionally, a bubbler system is used for precursor delivery in a MOCVD system. A simplified bubbler system is illustrated in **Figure 3.1(a)**. The bubbler is heated in order to obtain the desired vapor pressure of the precursor. If the precursor is solid at room temperature, the heating temperature should also be higher than the melting temperature of the precursor. An inert gas is used as carrier gas and is fed through a pipeline which is dipped into the precursor under the liquid level, usually near the bottom of the bubbler. Gas bubbles form in the precursor, emerge upward and bring the precursor vapor out. The concentration of the precursor vapor in the carrier gas depends on many factors such as bubbler temperature, bubbler pressure, carrier gas flow, bubble size, bubble quantity, liquid level, and so on. The disadvantage of a bubbler system is that the precursor flow is not easy to measure directly and is difficult to control. In addition, the precursor in the bubbler degrades with time under high temperature.

Some alternative methods are developed to improve precursor handling. One of them is called liquid delivery or direct liquid injection. In such a system pure liquid precursors or solutions of solid/liquid precursor are contained in isolated bottles. The bottles are similar to bubblers but are used in the opposite flow direction. The bottles are pressurized with inert gas to transport precursor solutions in liquid form through pipelines to a heated vaporizer. There

is an injector, an atomizer or a valve at the end of the pipelines to control precursor flow. Precursor solutions are then converted into small droplets or aerosol in order to be easily vaporized in the vaporizer. Afterward the gaseous precursor vapor can be transported to the location where the chemical reaction of the deposition process happens. The advantage of a liquid delivery system is that only a small portion of precursor which is close to reaction will be heated and vaporized. The majority of the precursor is kept at room temperature in the bottle. This prevents degradation of the precursor caused by high temperature. **Figure 3.1(b)** shows an illustration of a liquid delivery system.

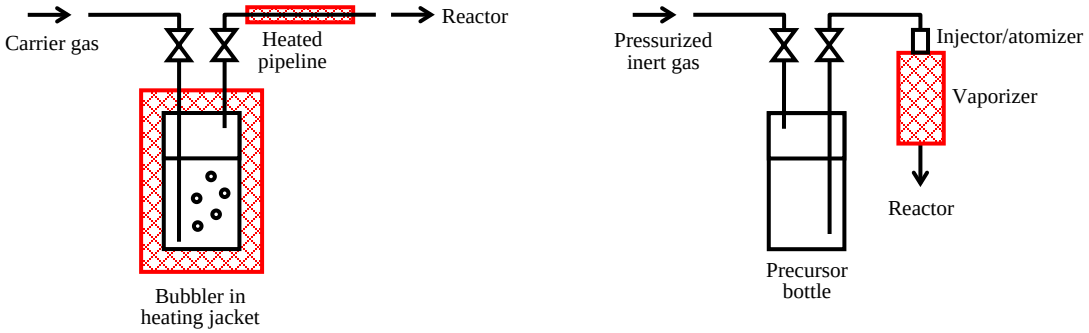


Figure 3.1 Handling of precursors in MOCVD technology :
(a) Bubbler system and (b) liquid delivery system.

Precursors are also a very important part of MOCVD technology. The properties of the precursor can affect, even limit process conditions and qualities of deposited films. An ideal MOCVD precursor should have the following properties: [3.9]–[3.12]

1. Adequate volatility to achieve acceptable deposition rates at moderate evaporation temperatures.
2. A sufficiently large temperature “window” between evaporation and thermal decomposition to assure precursor not to decompose before arriving at reaction location.
3. Suitable thermal decomposition/reaction temperature, not too high or not too low.
4. Clean evaporation without residues and clean decomposition without contamination of the growing film (e.g. by carbon)

5. Compatibility with other precursors in the multi-precursor process. (no pre-reaction between precursors, similar evaporation temperature range and similar decomposition temperature range)
6. Long shelf-life, stable in solution for liquid injection MOCVD applications.
7. Low hazard, low toxicity, nonflammable.
8. "Manufacturability" (high yield, high purity, low cost).

Usually, most of the precursors can fulfill only parts of these requirements. The precursors may often be toxic, unstable against air and moisture. Metal oxide precursors generally have a low vapor pressure, need to be heated for better evaporation; therefore, the temperature window between evaporation and thermal decomposition is often insufficient. It may happen that in a multi-precursor process evaporation and decomposition temperatures of each precursor don't match together or there is a pre-reaction between precursors. Precursor selection is always a compromise.

In earlier years tetraethyl lead [$Pb(C_2H_5)_4$], zirconium tert-butoxide [$Zr(OtBu)_4$] and titanium isopropoxide [$Ti(OiPr)_4$] were the most commonly used precursors for PZT thin film deposition by MOCVD. The advantage of these precursors is that they are liquids at room temperature and their vapor pressures are high enough. Therefore, it is easy to handle them either with a bubbler or with a liquid delivery system. But tetraethyl lead is very toxic and causes safety and environmental issues. Zirconium tert-butoxide and Titanium isopropoxide are air and moisture sensitive. Hydrolysis of these precursors often causes clogging of precursor lines and particles on deposited PZT films.

A new Pb precursor bis(2,2,6,6-tetramethyl-3,5-heptanedionato)lead [$Pb(thd)_2$] has been used since many years to replace the very toxic tetraethyl lead. $Pb(thd)_2$ is in solid form at room temperature and has a melting point at about 130°C. Although in many researches this precursor was used with a bubbler system, a liquid delivery system is more suitable for this solid precursor. The use of $Pb(thd)_2$, $Zr(OtBu)_4$ and $Ti(OiPr)_4$ for PZT thin film deposition was investigated by many researchers. [3.13]–[3.18] However, it was found that $Zr(OtBu)_4$ and $Ti(OiPr)_4$ appear to react with $Pb(thd)_2$ when they are prepared in a cocktail solution as well as when their vapors meet in the reactor. [3.19][3.20] This causes precursor degradation and particle generation and can affect the quality of deposited PZT thin films.

Many new Zr and Ti precursors were developed by replacing the alkoxide-ligand by other ligands such as thd- or mmp-ligands (1-methoxy-2-methyl-2-propoxy). $Zr(thd)_4$, $Ti(OiPr)_2(thd)_2$, $Zr(OiPr)_2(thd)_2$, $Zr_2(OiPr)_6(thd)_2$, $Zr(OtBu)_2(thd)_2$, $Ti(OtBu)_2(thd)_2$, $Zr(mmp)_4$, $Ti(mmp)_4$, are all examples of "tailoring" precursors in order to improve their compatibility with $Pb(thd)_2$. Many of them still have problems that they are not suitable to be integrated into PZT deposition processes. $Zr(thd)_4$ needs a high vaporization temperature (>300°C) and high deposition temperature (>600°C), so it doesn't match well with Pb and Ti precursors. [3.21][3.22] $Zr_2(OiPr)_6(thd)_2$ is found to match better with $Pb(thd)_2$ from the viewpoint of vaporization temperature and deposition temperature. But a ligand exchange reaction between $Zr_2(OiPr)_6(thd)_2$ and $Pb(thd)_2$ in a cocktail solution occurs gradually and leads to formation of $Zr(thd)_4$. [3.23] In general, $Ti(OiPr)_2(thd)_2$ works well with $Pb(thd)_2$. But at a lower deposition temperature the deposition rate is limited by $Ti(OiPr)_2(thd)_2$. [3.24]

3.3 Deposition and Characterization of PZT Thin Films

In this study an AIXTRON Tricent MOCVD system was used for deposition of PZT thin films. A simplified schematic diagram of this system is shown in **Figure 3.2**. The wafer for deposition lies on a graphite susceptor in the chamber. The susceptor can be heated up to 570°C by nine IR lamps under the susceptor. Gaseous reactant flows are introduced through a showerhead into the chamber from the upper side of the wafer. The susceptor is rotatable for better temperature and reactant flow uniformities.

A liquid delivery system is used together with the AIXTRON Tricent MOCVD system for precursor handling. This system is called TriJet and is made by Jipelec. In this system pure liquid precursors or solid/liquid precursor solutions are contained in isolated bottles. These bottles work like bubblers but are used in the reversed flow direction. They are pressurized with N_2 to transport precursor solutions in liquid form through metallic pipelines to the injectors. The injectors are usual gasoline fuel injectors of cars and are used here to inject precursor solutions into the vaporizer. An additional N_2 source is used as carrier gas and flows beside the injector nozzle together with injected precursor droplets into the vaporizer. Injected precursor droplets are heated and vaporized in the vaporizer and then flow to the showerhead. O_2 is fed to the showerhead as oxidant and mixed with precursor vapor in the showerhead. In

the original design of the TriJet system the injection is controlled by setting opening time and opening frequency of the injectors without monitoring the actual precursor flows. It was found that the experiment results were often unstable and difficult to reproduce. The precursor injection was proved to be unstable. The original TriJet system was, therefore, reconstructed to cascade with liquid flow meters. The precursor flows are monitored by a microcontroller and compared with the setting values. The opening time and opening frequency of each injector are adjusted dynamically by the microcontroller in order to keep stable flows.

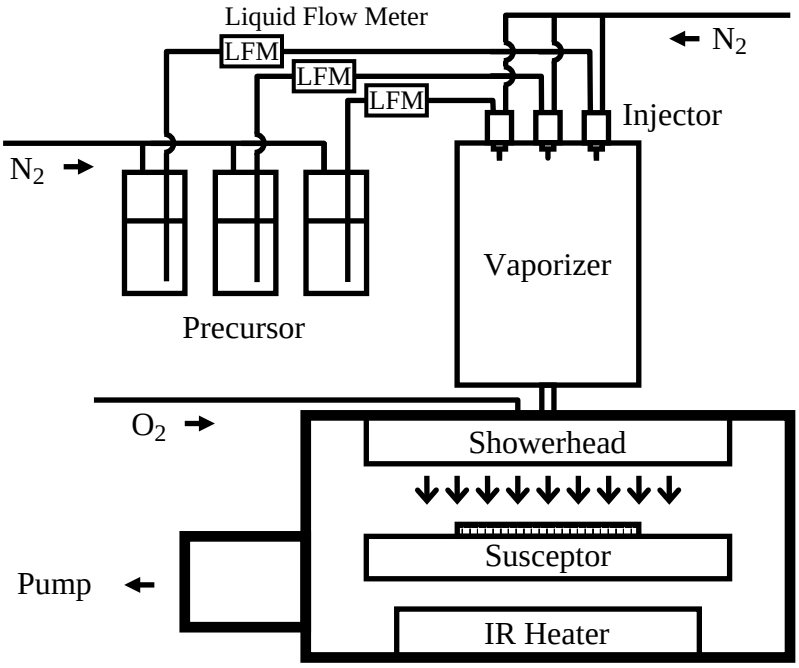


Figure 3.2 Schematic diagram of liquid delivery MOCVD system used in this study.

In this study, two novel precursors, Zirconium bis(isopropoxy) bis(1-methoxy-2-methyl-2-propoxy) [$Zr(OiPr)_2(mmp)_2$] and Titanium bis(isopropoxy) bis(1-methoxy-2-methyl-2-propoxy) [$Ti(OiPr)_2(mmp)_2$] are used together with $Pb(thd)_2$ for PZT thin film deposition. $Zr(OiPr)_2(mmp)_2$ and $Ti(OiPr)_2(mmp)_2$ are manufactured by Sigma-Aldrich. $Pb(thd)_2$ is available by Sigma-Aldrich, Strem Chemicals Inc. and many other suppliers. **Figure 3.3** shows the results of a thermal gravimetric analysis (TGA) for the three precursors which are provided by the manufacturer and can be found in literature. $Ti(OiPr)_2(mmp)_2$ is the

most volatile precursor of the three and $Pb(thd)_2$ has the lowest volatility. According to these TGA curves the vaporizer temperature should be at least 150°C or higher to ensure a better evaporation efficiency of $Pb(thd)_2$.

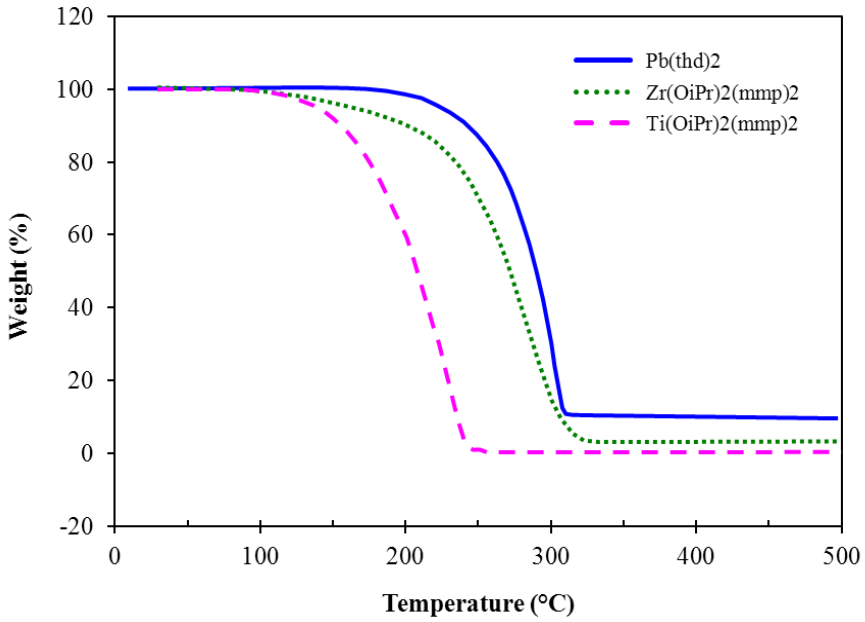


Figure 3.3 TGA results of $Pb(thd)_2$, $Zr(OiPr)_2(mmp)_2$ and $Ti(OiPr)_2(mmp)_2$.

More detailed experiments were performed to find out the optimum temperatures for precursor vaporization. These temperatures actually include the temperature of vaporizer, the temperature of the pipeline from the vaporizer to the showerhead and the temperature of the showerhead. The deposition rates of the single metal oxide of each precursor at various vaporization temperatures with a fixed substrate temperature at 500°C were measured. The metal oxide films were deposited on both Si and Ir substrates at the same time. The results are shown in **Figure 3.4**. The deposition rate of PbO with a vaporization temperature between 170°C and 220°C is similar. At the temperatures higher than 220°C the deposition rate decreases more and more with increasing vaporization temperature. It is supposed that at the temperature higher than 220°C, the Pb precursor either decomposes in the vaporizer or reacts with oxygen in the showerhead before arriving at the surface of the substrate because visible depositions are always found on inner surfaces of the vaporizer and inside/outside the

showerhead after a long term operation of many processes. The loss of Pb precursor in the vaporizer or in the showerhead causes a decrease of the deposition rate on the substrate. Similar results are obtained for Zr and Ti precursors. But they seem to be more thermally stable than the Pb precursor. The Ti precursor can resist temperatures up to 230°C and the Zr precursor is stable at temperatures up to 250°C. Under the view of precursor handling for the process, higher vaporization temperatures are preferred in order to vaporize the precursor as soon as possible. The precursor should not accumulate in the vaporizer for a long time before it is completely vaporized. Otherwise, the chemical vapor flow of precursors will not match with the controlled liquid flow of the precursors. On the other hand, decomposition of precursors in the vaporizer and the showerhead caused by overheating should also be prevented. Therefore, the compromised vaporization temperature for these three precursors was set to 220°C for processes in this study.

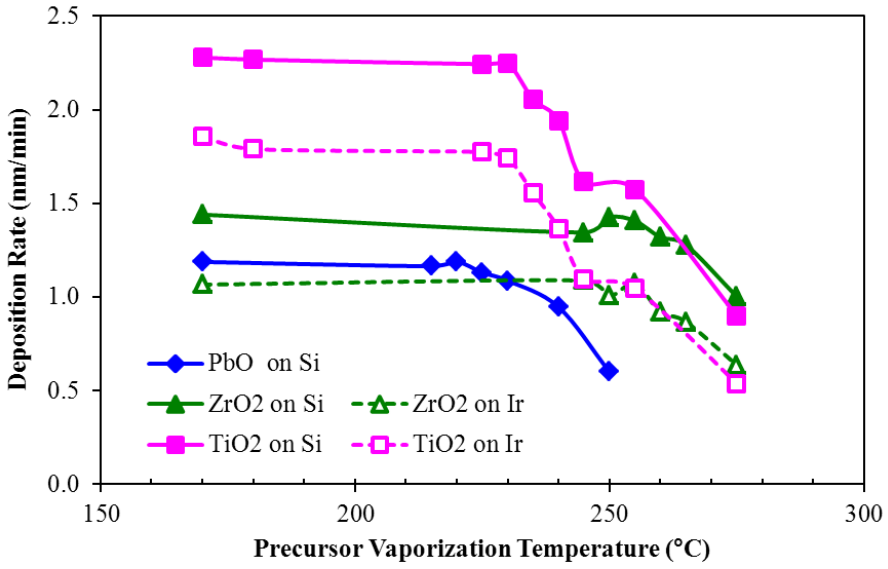


Figure 3.4 Deposition rate of the single metal oxide of each precursor at various vaporization temperatures.

The deposition rate of the single metal oxide of each precursor at various substrate temperatures ranging from 380°C to 550°C was also investigated. The results are shown in **Figure 3.5**. The deposition rate of PbO on Si substrates increases with increasing substrate

temperature from 400°C to 420°C and then keeps almost at a constant value between 420°C and 500°C. At a substrate temperature higher than 500°C the deposition rate decreases with increasing temperature. In many studies it is supposed that at the high temperature PbO is much more volatile and results in the decrease of the net deposition rate at higher temperature. In addition, the Pb loss must also be taken into consideration for high temperature annealing of PZT thin films. The deposition rate of ZrO_2 on Si increases, when substrate temperature increases from 380°C to 450°C. Between 450°C and 550°C the deposition rate is almost the same. Deposition of TiO_2 on Si shows also similar results. But the deposition of ZrO_2 and TiO_2 on Ir substrates is a little different from those on Si substrates. The deposition rates of ZrO_2 and TiO_2 on Ir substrates between 380°C and 550°C are approximately constant. Generally speaking, the deposition rates of PbO, ZrO_2 and TiO_2 have only a weak dependence on the substrate temperature between 400°C and 550°C. That means the process in this temperature range is rather mass transport limited than surface reaction limited. In order to have optimized ferroelectric property, the composition of Pb, Zr and Ti in the PZT films should be kept at a certain ratio. A deposition process limited by mass transport is preferred for easier composition control with variable precursor flow.

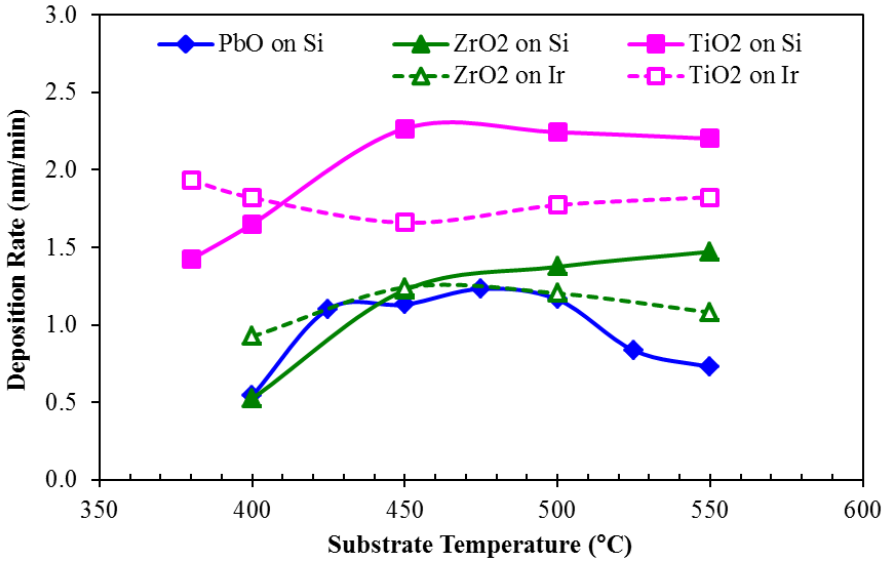


Figure 3.5 Deposition rate of single metal oxide of each precursor at various substrate temperatures.

It should be noted that the deposition of a ternary metal oxide such as PZT does not necessarily have a strong relation with the deposition of the single metal oxides of the three elements. Investigation of the deposition for each single metal oxide can only provide indirect information to find suitable process parameters by evaluating if they are comparably reactive and if the deposition rate is in an acceptable range.

The process conditions were defined according to the results above and summarized in **Table 3.1**. Two kinds of substrates were used in this study for PZT deposition. The first kind was p-type silicon wafers of ‹100› direction. The second kind was iridium substrates prepared as follows:

1. A thermal SiO_2 film of 200–500nm thickness was formed on the p-type ‹100› silicon wafers.
2. A thin Ti film of 10–20nm was then deposited by e-beam evaporation on the SiO_2. This Ti film was used to improve the adhesion of the following iridium deposition.
3. An iridium film of 100nm thickness was then deposited also by e-beam evaporation on TiO_2 as bottom electrode.

Table 3.1 Process conditions for PZT deposition.

Substrate		Ir/Ti/SiO_2/Si
		Si
Precursors	$Pb(thd)_2$	0.02–0.10M
	$Zr(OiPr)_2(mmp)_2$	0.02–0.10M
	$Ti(OiPr)_2(mmp)_2$	0.02–0.10M
Solvent	Octane	
Vaporizer temperature		220°C
Showerhead temperature		220°C
Gas lines temperature		220°C
Carrier gas (N_2) flow rate		800–1000sccm
O_2 gas flow rate		1100–1300sccm
Substrate temperature		450–550°C
Process pressure		0.5–5.0mbar

PZT films with a thickness close to 100nm were deposited at 450, 500 and 550°C on iridium and silicon substrates. In order to reduce the maximum temperature in the whole process flow, there was no crystallization annealing at higher temperatures after PZT deposition. The process temperature of the PZT deposition was the highest temperature in the whole process flow.

The film thickness was measured by using a spectroscopic ellipsometer or, sometimes, by scanning electron microscopy (SEM). The compositional analysis of PZT films was performed by using X-ray photoelectron spectroscopy (XPS) and energy dispersive X-ray spectroscopy (EDX). Crystal structure of the thin films and their crystallographic orientation were examined by X-ray diffraction (XRD) using Cu-Kα radiation and transmission electron microscopy (TEM). Surface morphologies of the PZT films were investigated by SEM and atomic force microscope (AFM).

For electrical characterization of the samples a further Ir film was deposited as top electrode to form an Ir/PZT/Ir capacitor stack. Circular Ir top electrodes were deposited on the PZT/Ir by e-beam evaporation through a shadow mask with many holes of various diameters ranging from 0.2 to 1mm. An IR heater heated the wafers to 250°C during evaporation. After top electrode deposition the samples were annealed at 300–400°C in atmosphere for 30–60 minutes. Because the whole Ir bottom electrode is covered by the PZT film during the deposition process, a small area of the PZT film is etched off with a chemical solution (6% HNO_3 + 2% HF + 1% HCl) in order to provide electrical contact to the bottom electrode. Ferroelectric properties, such as P-V hysteresis loops, of these capacitors were measured by using a ferroelectric test module TF ANALYZER 1000 (aixACCT Systems GmbH).

Figure 3.6 shows XRD patterns of as-deposited PZT films which were deposited at various substrate temperatures 450, 500 and 550°C with two different compositions. Some films have stoichiometric PZT composition with a Zr/Ti ratio close to 30/70. The other films contain 50% more Pb than the stoichiometric one.

It can be seen that the stoichiometric PZT film ($P_{1.0}Z_{0.3}T_{0.7}$) deposited at 450°C has very weak (101)/(110) peaks. The PZT film with 50% excess Pb ($P_{1.5}Z_{0.3}T_{0.7}$) deposited at 450°C has stronger (101)/(110) peaks than the stoichiometric one. In addition, very weak peaks at (001)/(100) and (112)/(211) are also visible. That means PZT films deposited at

450°C can be perovskite crystallized and may have ferroelectric properties. Both $P_{1.0}Z_{0.3}T_{0.7}$ and $P_{1.5}Z_{0.3}T_{0.7}$ films deposited at 500°C and 550°C are well crystallized and have clear (001)/(100), (101)/(110), (200) and (112)/(211) peaks. Some other peaks such as (002) and (102)/(201)/(210) are also visible. Because the Zr/Ti ratio is close to 30/70, the PZT films show the characteristic tetragonal splitting of (00*l*) and (*l*00) peaks. At the deposition temperatures of 500°C and 550°C, no clear relationship between crystallization orientation and Pb compositions is found in the XRD measurements.

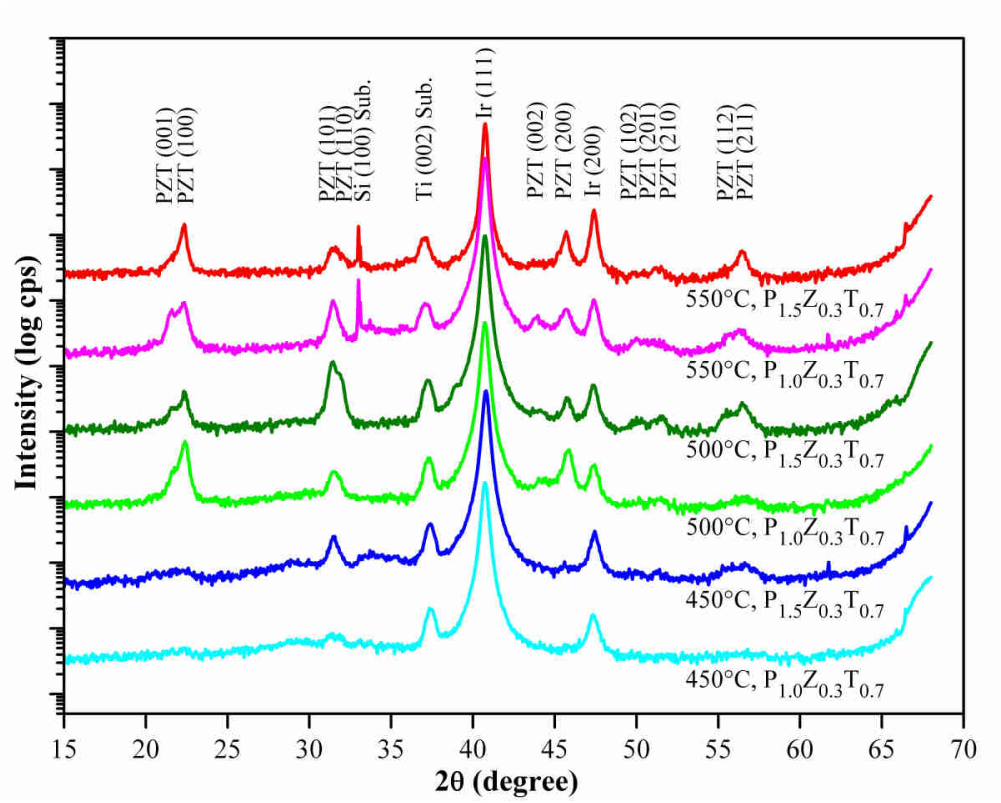
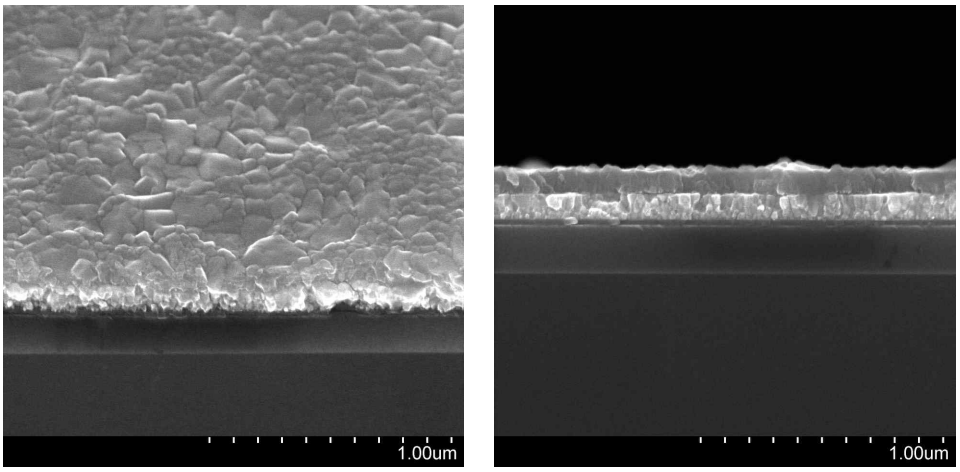


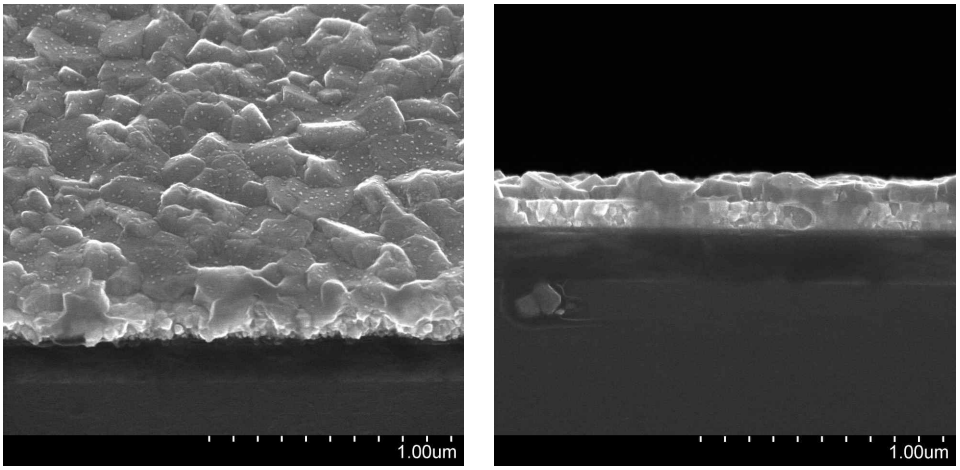
Figure 3.6 XRD patterns of PZT films deposited at various temperatures with various Pb contents.

Figure 3.7 shows SEM images of two PZT films deposited at 550C with a stoichiometric and a Pb-excess composition. The PZT films consist of grains in different size with clear facets and edges. It can be clearly seen that the Pb-excess PZT film is much rougher and has larger grains than the stoichiometric one. Quantitative analysis of the morphology was made by AFM measurement and is shown in **Figure 3.8**. The

root-mean-square value of surface roughness is 7.1 nm for the stoichiometric PZT film and 21.4 nm for the Pb-excess PZT film. It is suggested by many researchers that in addition to a higher deposition temperature, more Pb also helps for better crystallization and, hence, for better ferroelectric properties. Excess Pb plays especially an important role for crystallization at lower process temperatures. Therefore, in **Figure 3.6** at 450°C the $P_{1.5}Z_{0.3}T_{0.7}$ film has stronger PZT peaks than $P_{1.5}Z_{0.3}T_{0.7}$. And this is also the reason why in **Figure 3.7** and **Figure 3.8** the Pb-excess PZT film is rougher than the stoichiometric one.

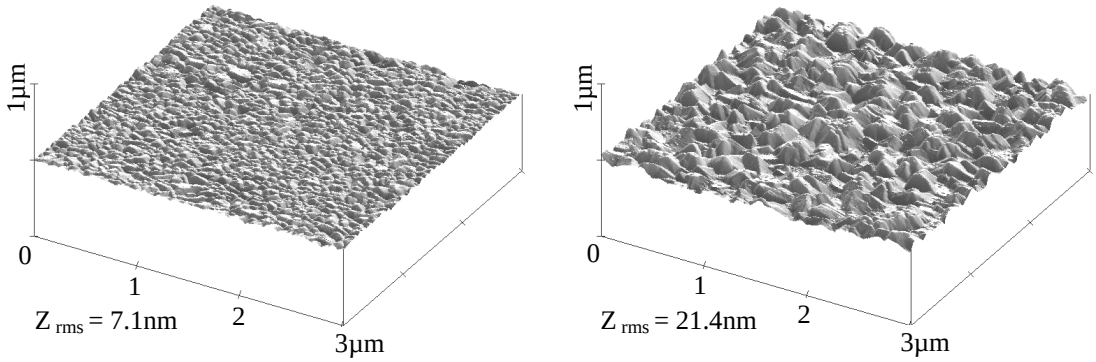


(a) Pb/(Zr+Ti)=0.94, Zr/(Zr+Ti)=0.38



(b) Pb/(Zr+Ti)=1.28, Zr/(Zr+Ti)=0.35

Figure 3.7 SEM images of PZT films deposited at 550°C with various compositions.



(a) Pb/(Zr+Ti)=0.94, Zr/(Zr+Ti)=0.38 (b) Pb/(Zr+Ti)=1.28, Zr/(Zr+Ti)=0.35

Figure 3.8 AFM surface morphology of PZT films deposited at 550°C with various compositions.

A phase separation is found in deposited PZT films. This phenomenon doesn't happen in all samples but is seen in the majority. **Figure 3.9** shows some typical examples of different phases inspected by SEM. **Figure 3.9(a)** shows many disk-shape areas on the PZT film. These disks consist of many grains and are much rougher than the surroundings. The center of the disk is rougher than edge of the disk and there are sometimes cluster of very large grains at the disk center. Qualitative EDX measurements of the PZT composition show that there is more Pb in rougher disks than in the surroundings. But no clear dependence of this disk phase on the process parameters can be found.

Wang and Choi [3.25][3.26] also found such a disk-shape phase in $PbTiO_3$. Their analysis with Auger electron spectroscopy (AES) revealed no composition difference between the disk region and the surroundings. They concluded that this disk phase must be a result of a partial crystallization of $PbTiO_3$, which was embedded in the amorphous matrix.

Figure 3.9(b) shows another type of phase separation. Two different phases form randomly on a PZT film and can be distinguished as brighter areas and darker areas in SEM working with secondary electron imaging (SEI) mode. This kind of phase separation forms more easily on Ir substrates than on Si substrates. The brighter areas are rougher with many crystal grains. The darker areas are smoother than the brighter areas and look like amorphous

at the lower process temperature (450°C) on Si substrates. But crystal grains are also visible in darker area at 450°C on Ir substrates, and at higher process temperature (500/550°C) on both Si and Ir substrates. The difference of brightness in SEM inspection is probably caused by different roughness, different crystallization or other factors.

The phase separation of rougher brighter and smoother darker areas shown in **Figure 3.9(b)** can also be found in the research of Otani et al. (Figure 11(a) in reference [3.27]) but no analysis was focused on this phenomenon in their publication.

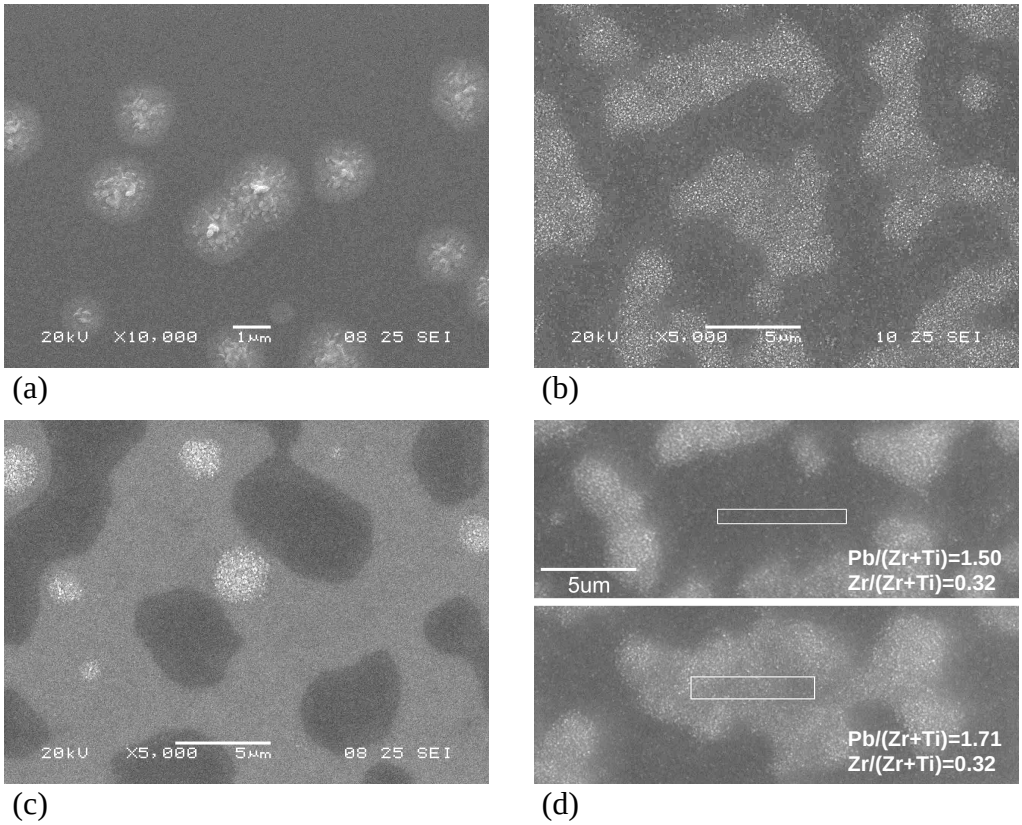
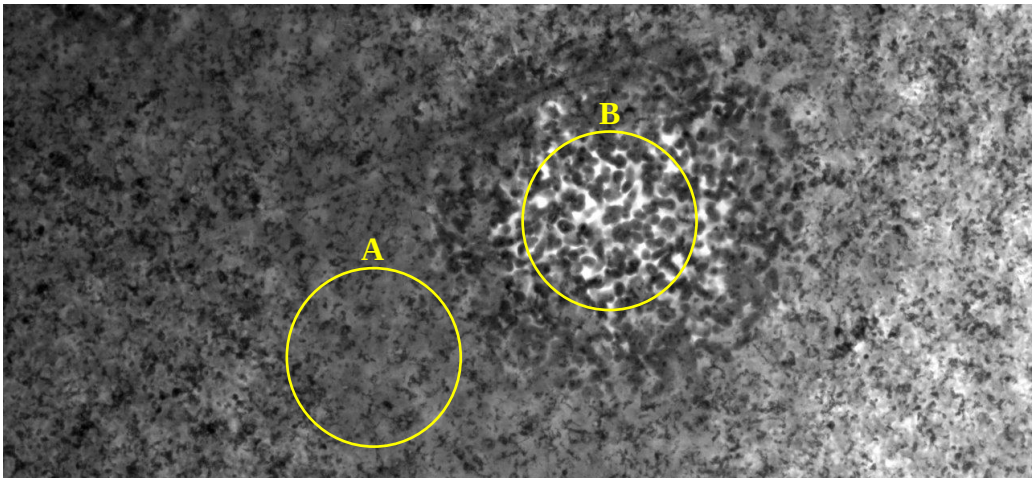


Figure 3.9 Phase separation in PZT films inspected by SEM: (a) disk rougher phase, (b) smoother phase (darker area) and rougher phase (brighter area), (c) mixture phase of (a) and (b), (d) EDX analysis.

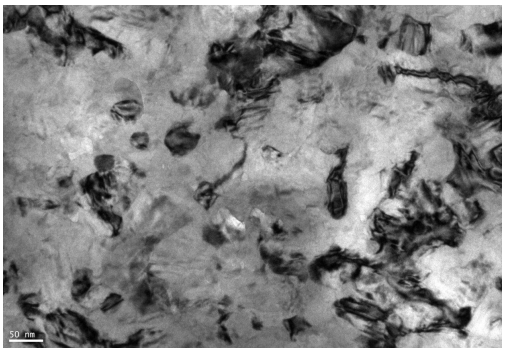
Figure 3.9(c) shows a mixture of phase separations shown in **Figure 3.9(a)** and **Figure 3.9(b)**. The rougher disks locate mostly on rougher brighter areas and seldom on

smoother darker areas. There seems to be some relationship between rougher disks and rougher brighter areas. **Figure 3.9(d)** shows quantitative EDX measurements of PZT composition for rougher brighter area and smoother darker area. The white rectangles are measured areas. In both areas the ratios of Zr/(Zr+Ti) are the same; but in the rougher brighter area the Pb/(Zr+Ti) ratio is 15% higher than that in the smoother darker area. This result reveals that the Pb composition may play some certain role for phase separation.

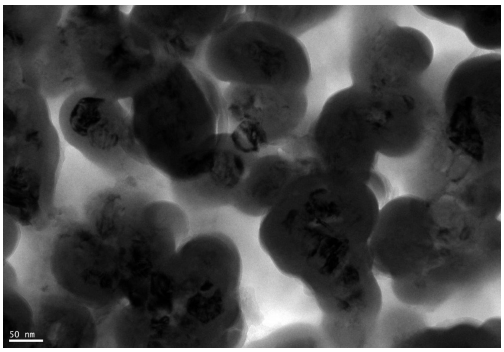
Further analyses of the disk rougher phase with TEM were shown in **Figure 3.10**. The normal phase region of the PZT film shown in **Figure 3.10(b)** has no apparent grain boundary while the disk rougher phase region shown in **Figure 3.10(c)** consists of many large grains of a size ranging from 100nm to 200nm. These grains have round corners without facets.



(a)



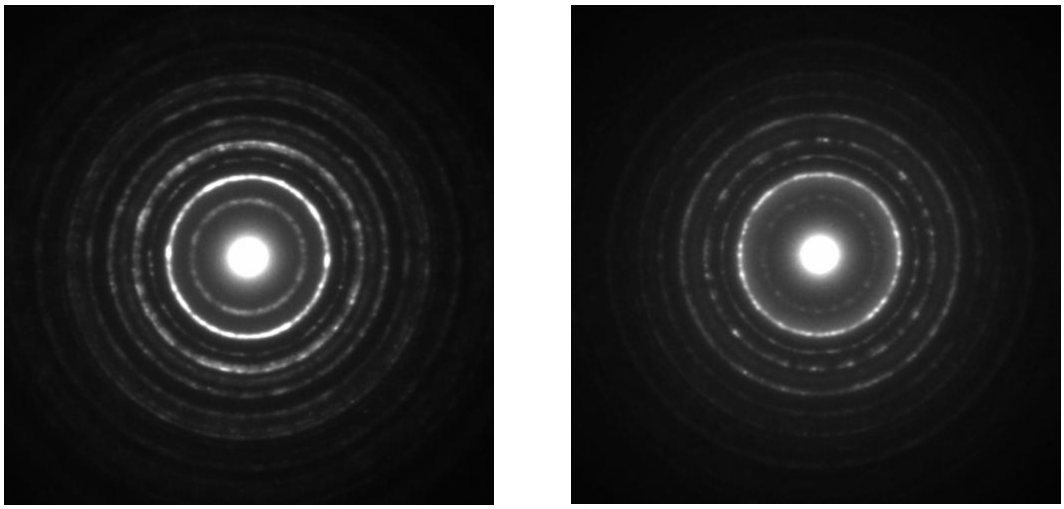
(b)



(c)

Figure 3.10 TEM images of the PZT film with disk rougher phase: (a) overview, (b) normal phase (region A), (c) disk rougher phase (region B).

Selected area electron diffraction (SAED) was performed on both regions for the normal phase and the disk rougher phase. The results are shown in **Figure 3.11**. Both phases have almost the same diffraction patterns. Under the qualitative aspect, both phases contain the same PZT crystal structures although more Pb was found in disk rougher phase according to EDX results and, also, their appearances under TEM and SEM are totally different. Because the very rough surface of the disk rougher phase region is combined with a large thickness variation of the PZT film, it may cause problems for electrical properties and reliability. The formation of such a phase should be avoided.



(a) (b)

Figure 3.11 Selected area electron diffraction (SAED) of disk rougher phase in PZT films: (a) normal phase (region A), (b) disk rougher phase (region B).

Electrical characteristics of ferroelectric capacitors such as hysteresis loops and current density responses vs. voltage were measured. **Figure 3.12** shows the results of ferroelectric capacitors with PZT films deposited at 450, 500 and 550°C. It can be seen that the capacitors with 500°C PZT and 550°C PZT show good hysteresis curves. The remanent polarizations of them reach about 35μC/cm^2. In the J-V characteristics, sharp pulses of the switch current near ±1V are visible. The capacitor of 450°C PZT has also smaller switch current pulses and exhibits a weak remanent polarization about 10μC/cm^2.

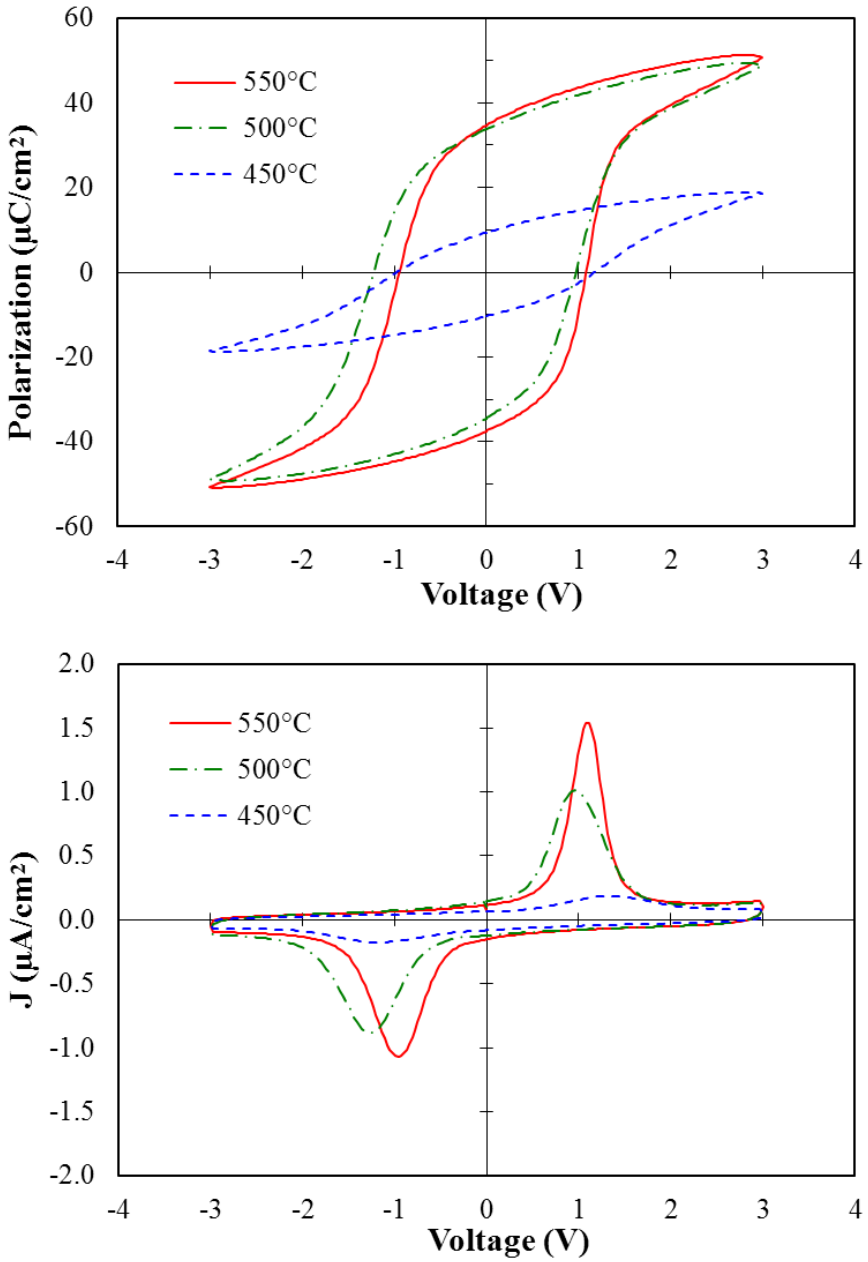


Figure 3.12 Hysteresis loops and current density responses of ferroelectric capacitors with PZT films deposited at various temperatures.

Figure 3.13 shows the hysteresis loops of capacitors with PZT films deposited at 550°C with different compositions. The one with nearly stoichiometric composition exhibits a very low remanent polarization of about 2μC/cm^2. Another one with a composition of about 30% excess Pb exhibits a better hysteresis loop with a remanent polarization at about 12μC/cm^2. Generally speaking, the PZT films with a higher Pb content have higher remanent

polarizations. The ferroelectric capacitors shown in **Figure 3.12** with PZT films deposited at 450°C and 500°C have compositions with excess Pb and exhibit better remanent polarization values than stoichiometric PZT films.

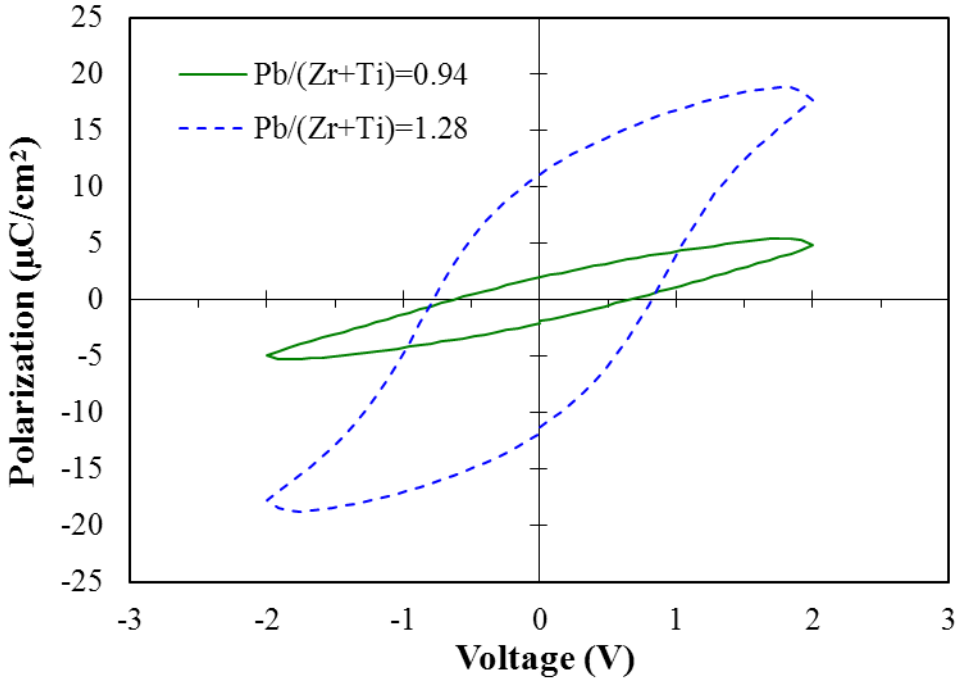


Figure 3.13 Hysteresis loops of ferroelectric capacitors with PZT films deposited at 550°C with various compositions.

3.4 Summary

In this chapter, MOCVD PZT thin film deposition with novel Zr and Ti precursors [$Zr(OiPr)_2(mmp)_2$ and $Ti(OiPr)_2(mmp)_2$] together with $Pb(thd)_2$ was investigated. Process conditions for these precursors were optimized. Well crystallized PZT thin films with good ferroelectric properties at deposition temperatures between 450 and 550°C could be achieved. Phase separation in PZT film was found and has probably a relation to Pb content in the PZT films.

3.5 Reference

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4 Reactive Ion Etching of Iridium Thin Films

4.1 Considerations for Reactive Ion Etching of Iridium Thin Films

As mentioned in previous chapters, applying RIE technology on formation of ferroelectric capacitors still encounters difficulties. Halogen-containing gases, which are often used in plasma etching process, form low volatile compounds with electrode materials Ir, Pt and many ferroelectric materials. The melting points and boiling points of halides of some electrode and ferroelectric materials are shown in **Table 4.1**. It can be seen that most of the halides in the table are nonvolatile at room temperature.

Table 4.1 Melting points and boiling points of halides of electrode and ferroelectric materials.[4.1]–[4.6]

Compound	mp (°C)	bp (°C)	Compound	mp (°C)	bp (°C)
PtF_4	600	-	PbF_2	855	1290
PtF_6	61.3	69.1	PbF_4	~600	-
$PtCl_2$	581	-	$PbCl_2$	501	954
$PtCl_3$	435	-	$PbCl_4$	-15	50
$PtCl_4$	370	-	$PbBr_2$	373	914
$PtBr_2$	250	-			
$PtBr_3$	200	-	ZrF_4	932	912
$PtBr_4$	180	-	$ZrCl_2$	727	1292
			$ZrCl_4$	437	331
IrF_3	250	-	$ZrBr_4$	450	357
IrF_6	44	53			
$IrCl_2$	>733	-	TiF_3	1200	1400
$IrCl_3$	763	-	TiF_4	284	-
$IrCl_4$	~700	-	$TiCl_2$	1035	1500
			$TiCl_3$	440	960
AlF_3	1290		$TiCl_4$	-24	136.5
$AlCl_3$	192.6		$TiBr_2$	>500	-
$AlBr_3$	97.5	255	$TiBr_3$	39	230
			$TiBr_4$	38	234

Higher temperature etching process for ferroelectric capacitor is, therefore, necessary in order to enhance etching rate. This demand results in a new problem that photoresist is not sustainable for high temperature etching. SiO_2, TiN and TiAlN have been used as hard masks instead of photoresist for high temperature RIE. [4.7]–[4.11] Unfortunately, although the etching rates of ferroelectric and electrode materials are improved in high temperature etching processes, the sidewall slope of ferroelectric capacitors after etching is still too low because of low selectivity between mask materials and ferroelectric/electrode materials.

The halides of aluminum are also shown in **Table 4.1**. It is found that its fluoride (AlF_3) has a much higher melting point than fluorides of iridium (IrF_3, IrF_6) and platinum (PtF_4, PtF_6). This is a hint that it may be possible to use Al or Al_2O_3 as hard mask with high selectivity for reactive ion etching of Ir and Pt under high temperature with fluorine-containing chemistries such as CF_4, SF_6 and NF_3. Aluminum is already used as metal wires in conventional CMOS process. Al_2O_3 is also used in FeRAM processes as hydrogen barrier layer and is proved to be compatible with conventional CMOS process technology.

Fluorocarbon plasmas have been widely used for Si and SiO_2 etching processes. They have also been investigated since many years. The mechanism of dissociation of CF_4 in the plasma is a very complicated procedure. Many kinds of reactions can happen in the plasma and many different radicals are generated by electron impact. **Equations (4.1)** to **(4.3)** are believed to be some of the main reactions happening in the plasma. [4.12]–[4.17] In RIE of Si and SiO_2, the dissociated fluorine atoms are responsible for etching. They react with Si and SiO_2 surface; form volatile SiF_4 which leaves the substrate surface thereafter.

$$CF_x + e^- \rightarrow CF_{x-1} + F + e^- \qquad (x=2\text{–}4) \qquad (4.1)$$

$$CF_x + e^- \rightarrow CF_{x-1} + F^- \qquad (x=2\text{–}4) \qquad (4.2)$$

$$CF_x + e^- \rightarrow CF_{x-1}^+ + F + 2e^- \qquad (x=2\text{–}4) \qquad (4.3)$$

It is well known that the addition of a small amount of O_2 into the CF_4 plasma can enhance the atomic fluorine concentration and therefore enhances the etch rate. The mechanism of dissociation becomes more complicated with the addition of O_2. **Equations (4.4)** to **(4.9)** are some of many possible reactions which can happen in the plasma. [4.17]–[4.20]

$$O_2 + e^- \rightarrow O + O + e^- \quad (4.4)$$

$$CF_x + O \rightarrow COF_{x-1} + F \quad (x=1–3) \quad (4.5)$$

$$CF_2 + O \rightarrow CO + 2F \quad (4.6)$$

$$COF_2 + e^- \rightarrow COF + F + e^- \quad (4.7)$$

$$COF_2 + O \rightarrow CO_2 + 2F \quad (4.8)$$

$$COF + O \rightarrow CO_2 + F \quad (4.9)$$

Earlier studies have reported that when O_2 addition starts increasing from 0%, the atomic F concentration also increases up to a maximum at a certain O_2 percentage. Further increasing of O_2 percentage causes a decrease of the F concentration. This decrease is probably caused by dilution. A strong relation between F concentration and etch rate of Si and SiO_2 was also found. [4.12][4.21][4.22]

In addition to the dissociation and reaction of CF_4 in the plasma, it should be noted that fluorocarbon radicals can form polymers on the substrate surface. The deposited polymer layer inhibits the etching by preventing fluorine atoms to reach the Si or SiO_2 surface. The added O_2 reacts with fluorocarbon radicals in the plasma to form CO and CO_2 and reduces the formation of fluorocarbon polymers. This is another benefit of adding O_2 in CF_4 plasma. Adding argon in plasma is also an alternative to remove the polymers by Ar ion bombardment.

The knowledge about RIE of Si and SiO_2 with fluorine-containing gases provides information about etching of iridium and aluminum with the same kind of gases. In this chapter RIE of iridium thin films under elevated process temperatures was investigated with thin aluminum films as etching mask and CF_4/O_2/Ar as etching gases.

4.2 Reactive Ion Etching of Iridium Thin Films with Al Mask and CF_4/O_2/Ar Gas Mixture

The experiments were conducted in an electron cyclotron resonance (ECR) enhanced reactive ion etching system which is shown in **Figure 4.1**. The ECR plasma was generated at the upper side of the chamber and introduced into the process chamber. The wafer was located on a resistor heated chuck. A DC bias at −200V was applied to the chuck by an RF generator with a matchbox. The total gas flow was kept at 50sccm. The process conditions are summarized in **Table 4.2**.

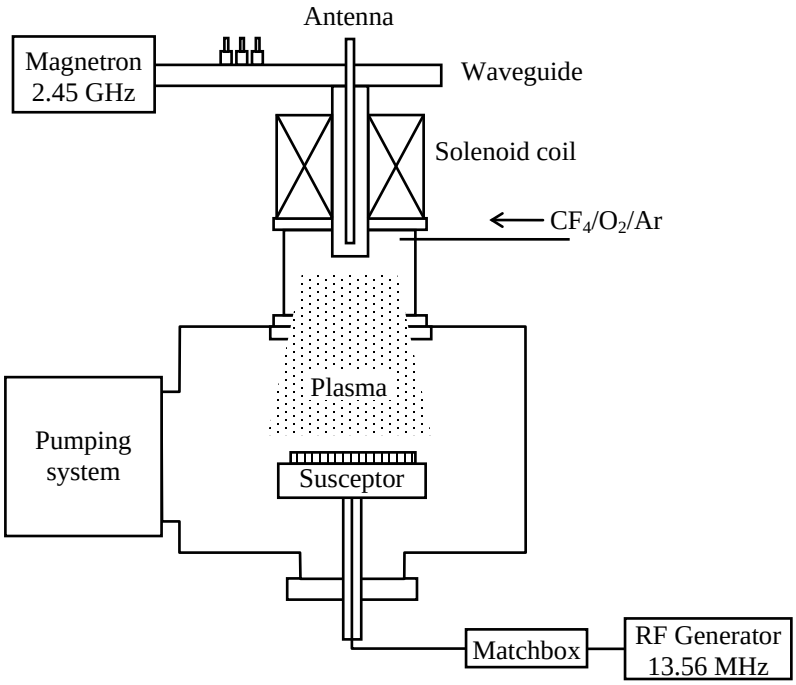


Figure 4.1 Schematic diagram of ECR-RIE system.

Table 4.2 Process conditions for iridium etching.

Substrate	$Al/Ir/Ti/SiO_2/Si$
	$Ir/Ti/SiO_2/Si$
Substrate temperature	25–350°C
Process pressure	0.006–0.013mbar
Co-reactant gases	$CF_4/O_2/Ar$
ECR microwave power	200–600W
RF DC bias	−200V
RF power (not independent)	20–70W

Iridium substrates used for these experiments were prepared on p-type ‹100› silicon wafers. The wafers were thermally oxidized to form 500nm SiO_2. A thin Ti film of 20nm thickness was then deposited by e-beam evaporation on SiO_2 and was used to improve the adhesion of the following iridium film. An iridium film of 150nm thickness was then deposited also by e-beam evaporation on the Ti film. The lift-off method was used to form Al patterns on iridium for use as etching mask. Photoresist was patterned on the Ir-covered wafers according to process parameters of the lift-off method. After performing this lithography process, a 100nm thick Al film was deposited on the wafers by e-beam evaporation. The wafers were afterwards soaked in acetone to remove photoresist and also the aluminum deposited on the photoresist. The aluminum which was deposited directly on iridium surface was not removed and stayed on the iridium as etching mask. An O_2 plasma treatment at 300°C for one hour was performed to remove the possible residue of photoresist on the surfaces of Ir and Al films. Wafers with 100nm Ir films but without Al etching mask were also used in the experiments for rough estimations of the Ir etching rate.

The etch rate was calculated with help of step height measurements by a Dektak Profilometer on the edge of Al mask patterns. The Al mask patterns for measurement are 10/10μm line/space structures. The Al mask thickness d_1 was measured at first before etching. The samples were then etched in the chamber for t minutes using various process conditions. After etching the samples were measured with the Profilometer for the second time and the step height determined was d_2. The Al etching mask on iridium was then removed by a wet etching process with a commercial Al etch solution (73.1% H_3PO_4 + 2.3% HNO_3 + 22.3% CH_3COOH) at room temperature without damaging the Ir surface because Ir is not attacked by any acids including aqua regia. After Al removal, the samples were measured by Profilometer for the third time and the step height d_3 was obtained. The etch rates of Ir and Al were then calculated as follows:

Ir etch rate = d_3/t

Al etch rate = $(d_1 + d_3 - d_2)/t$

Selectivity = Ir etch rate / Al etch rate

In the experiments the influence of various process parameters such as substrate temperature, pressure, ECR power and gas mixing ratio on the etch rate was investigated.

The influence of the $CF_4/O_2/Ar$ gas mixing ratio on the etch rate is shown in **Figure 4.2**. The samples were etched at 300°C and 0.01mbar with 400W ECR power and the total gas flow was kept at 50sccm. In **Figure 4.2(a)** the CF_4 flow rate was fixed at 40sccm and only O_2 and Ar flow rates were changed. The etch rate decreases when O_2 is replaced by Ar. Although both Ar and O_2 have the effect of reducing polymer deposition, the result shows that O_2 works better than Ar in the view of enhancing the etch rate. The reason may be the role of O_2 in enhancing the dissociation of CF_4 which results in a higher concentration of fluorine radicals.

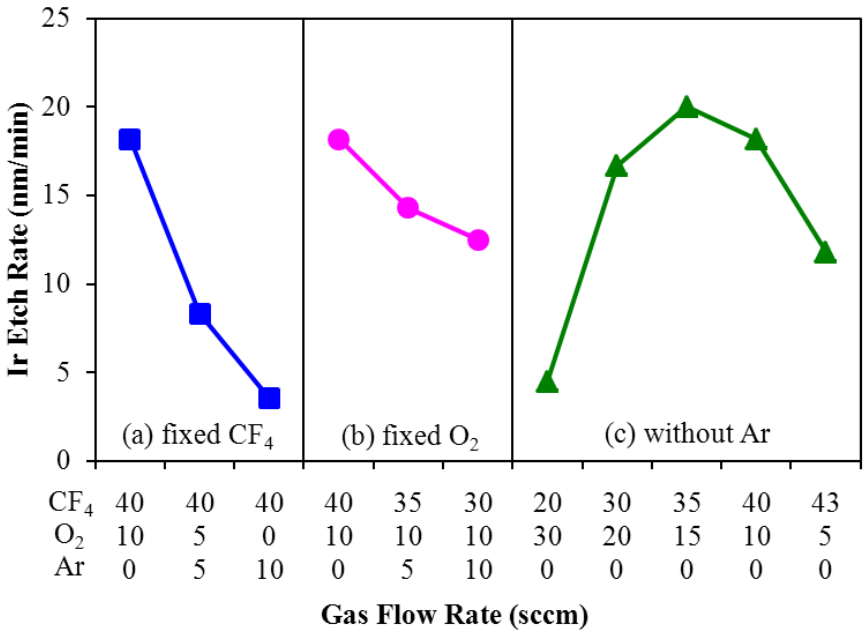


Figure 4.2 Effect of gas flow rates on etch rate of Ir in $CF_4/O_2/Ar$ plasmas.

In **Figure 4.2(b)** the flow rate of O_2 was fixed at 10sccm and CF_4/Ar flow rates are changed. Increasing the Ar flow rate and decreasing the CF_4 flow rate causes a decrease of the etch rate. It seems that the gain of etch rate by reducing polymer film growth with Ar ion bombardment is smaller than the loss of etch rate caused by replacing an equal amount CF_4 by Ar. The results of **Figures 4.2(a)** and **(b)** indicate that the addition of Ar in the CF_4/O_2 gas mixture may be profitless for Ir etching.

The gas mixing ratio of CF_4/O_2 without Ar was investigated and the result is shown in **Figure 4.2(c)**. The adding of O_2 up to 30% (CF_4=35sccm, O_2=15sccm) results in the highest etch rate. A further increase O_2 beyond 30% causes a decrease of the etch rate. This phenomenon is similar to the results found in earlier studies of Si/SiO_2 etching with CF_4/O_2 plasmas. [4.12][4.23][4.24]

The influence of the process pressure on the etch rate was also investigated, and the results are shown in **Figure 4.3**. The experiments were carried out at 300°C with an ECR power of 400W and gas flow rates CF_4=35sccm/O_2=15sccm. The results show that the etch rate increases with the pressure. Because the working pressure range of the equipment is designed to be between 5×10^{-4} mbar and 1×10^{-2} mbar, the process pressure in all other experiments was kept as a constant at 0.01mbar.

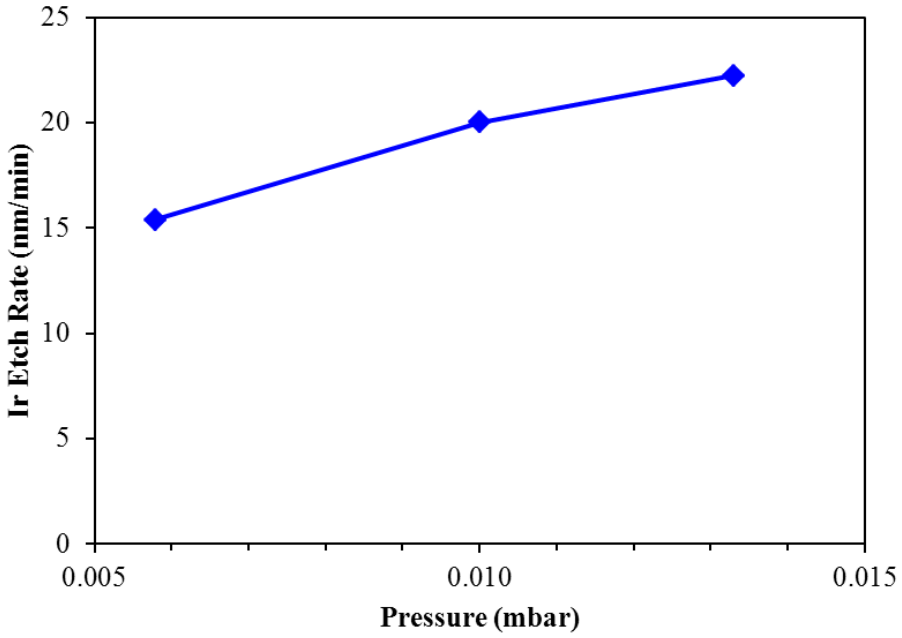


Figure 4.3 Effect of process pressure on the etch rate of Ir in CF_4/O_2 plasmas.

The ECR microwave power is also an important factor of the etching process. **Figure 4.4** shows the relation between ECR power and etch rate of Ir. The samples were etched at 300°C and 0.01mbar with gas flows CF_4=35sccm/O_2=15sccm. The etch rate of Ir increases

when ECR power increases from 200W and reaches a maximum in the range from 300W to 400W. Beyond 400W the etch rate decreases with increasing ECR power.

Increasing the ECR power increases the density of ions and radicals and causes usually an increase of the etch rate. In this experiment the etch rate doesn't increase monotonically with the ECR power but reaches a maximum value at a certain power. In the CF_4/O_2 plasma more fluorine atoms can increase etch rate but more fluorocarbon radicals can increase polymer generation and, therefore, decrease the etch rate. It is supposed that there exists a competition between F atom etching and fluorocarbon polymer deposition on the substrate surface. Increasing the ECR power changes the concentration of F atoms and fluorocarbon radicals which enhance etching and polymer deposition, respectively. The net effect is a maximum etch rate at an optimum ECR power. If the power is lower than the optimum value, the concentration of F atoms increases faster than the concentration of fluorocarbon radicals with increasing power. So the etch rate increases with increasing ECR power. If the ECR power is higher than the optimum value, the concentration of fluorocarbon radicals increases faster than the concentration of F atoms. Hence the etch rate decreases with increasing ECR power.

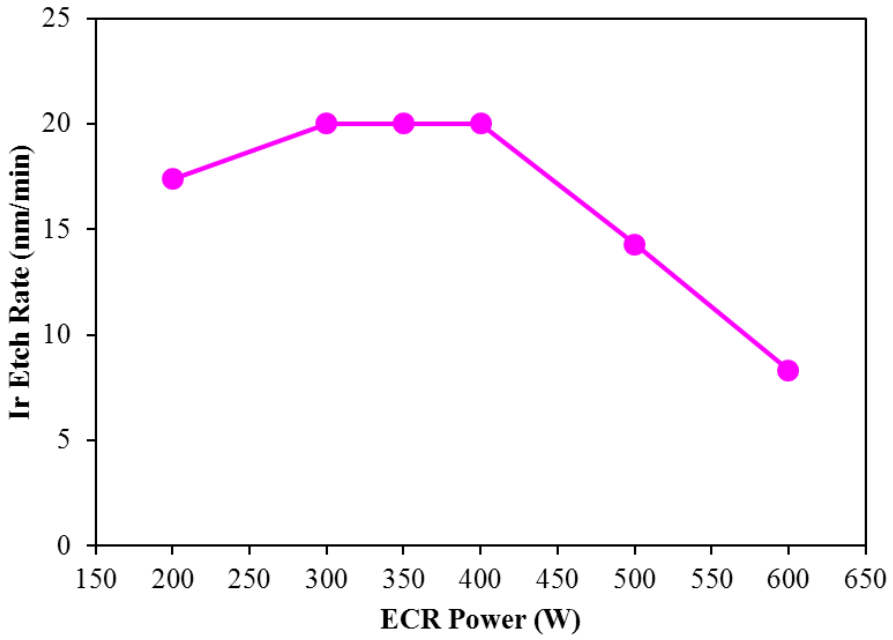


Figure 4.4 Effect of ECR power on etch rate of Ir in CF_4/O_2 plasmas.

The effect of substrate temperature on etch rate and selectivity is shown in **Figure 4.5**. The etch rate of Ir increases in general with increasing temperature. The etch rate is higher than about 25nm/min at 350°C and is about five times higher than the etch rate at room temperature. The selectivity (Ir/Al) at room temperature is nearly 70. The thickness loss of the Al mask after etching ($d_1 + d_3 - d_2$) is actually only one nanometer and is smaller than the measurement precision. Therefore, one can say that the etch rate of the Al mask is negligible and the selectivity is very high. At higher temperatures the thickness of the Al masks after etching is even a few nanometers higher than before etching. It is probably that a very thin polymer redeposition on the Al mask occurs at high temperature etching but it is also possible that these results are caused by measurement fluctuations. In comparison to the etch rate of Ir, the etch rate of Al mask is very low and the selectivity is very high. Good etching profiles at sidewalls of Ir should be achievable as long as the sidewall profile of the Al mask is good enough.

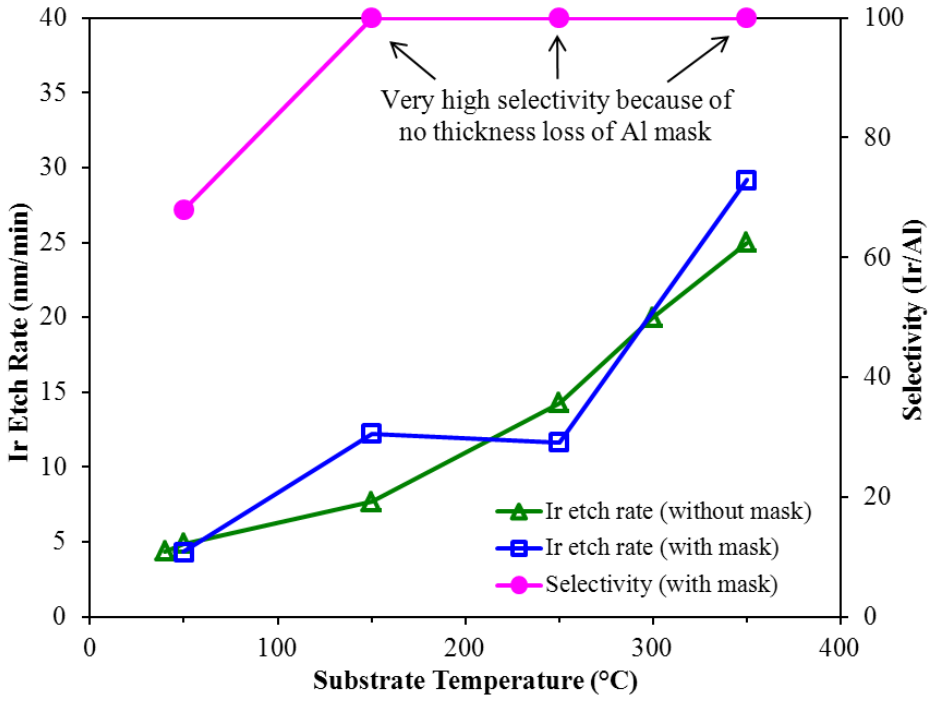


Figure 4.5 Effect of substrate temperature on etch rate of Ir in CF_4/O_2 plasmas.

Figure 4.6 shows an Arrhenius plot of the Ir etch rate in CF_4/O_2 plasmas. The temperature dependence of the etch rate seems to be non-Arrhenius. The whole etching reaction may consist of several mechanisms including absorption of reactants on the surface, surface reaction, inhibition caused by polymer deposition, ion-enhanced reaction, desorption of low volatile products from the surface, ion-assisted products/polymer removal from the surface, etc. In addition to the surface reaction rate, it is known that deposition of fluorocarbon polymer and desorption of low volatile products play also important roles for the etch rate in such a system. Due to the influence of so many factors, one can understand that the etch rate cannot be characterized by an Arrhenius equation with a single activation energy.

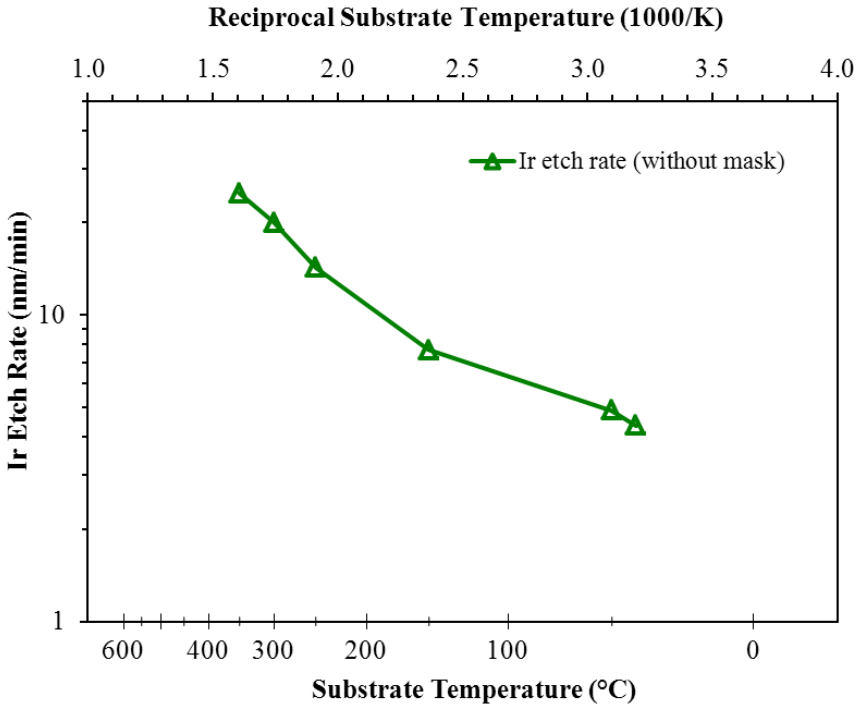


Figure 4.6 Arrhenius plot of the etch rate of Ir in CF_4/O_2 plasmas.

The samples were inspected with SEM after the experiments. A bird's view and a cross-sectional view of the Ir film and the Al mask before etching are shown in **Figure 4.7**. Unfortunately, the sidewall of the Al mask pattern made by the lift-off method is not vertical but shows a very low slope. A vertically etched sidewall is usually not possible with such an etching mask.

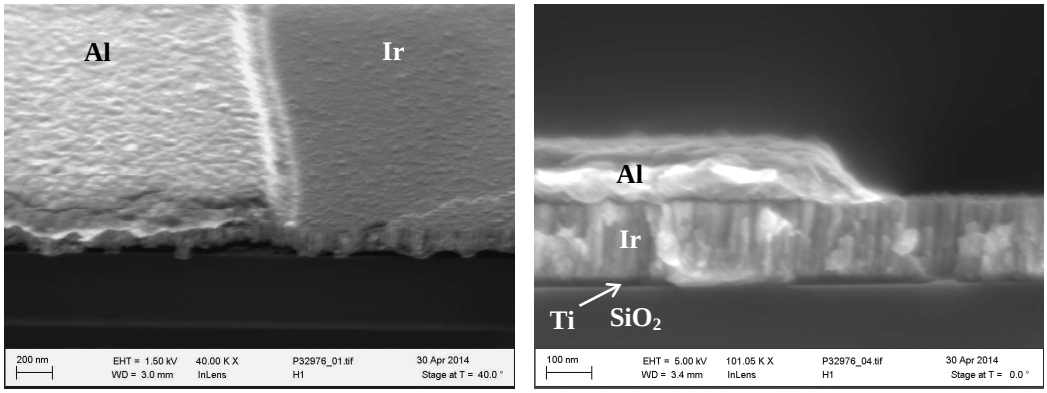
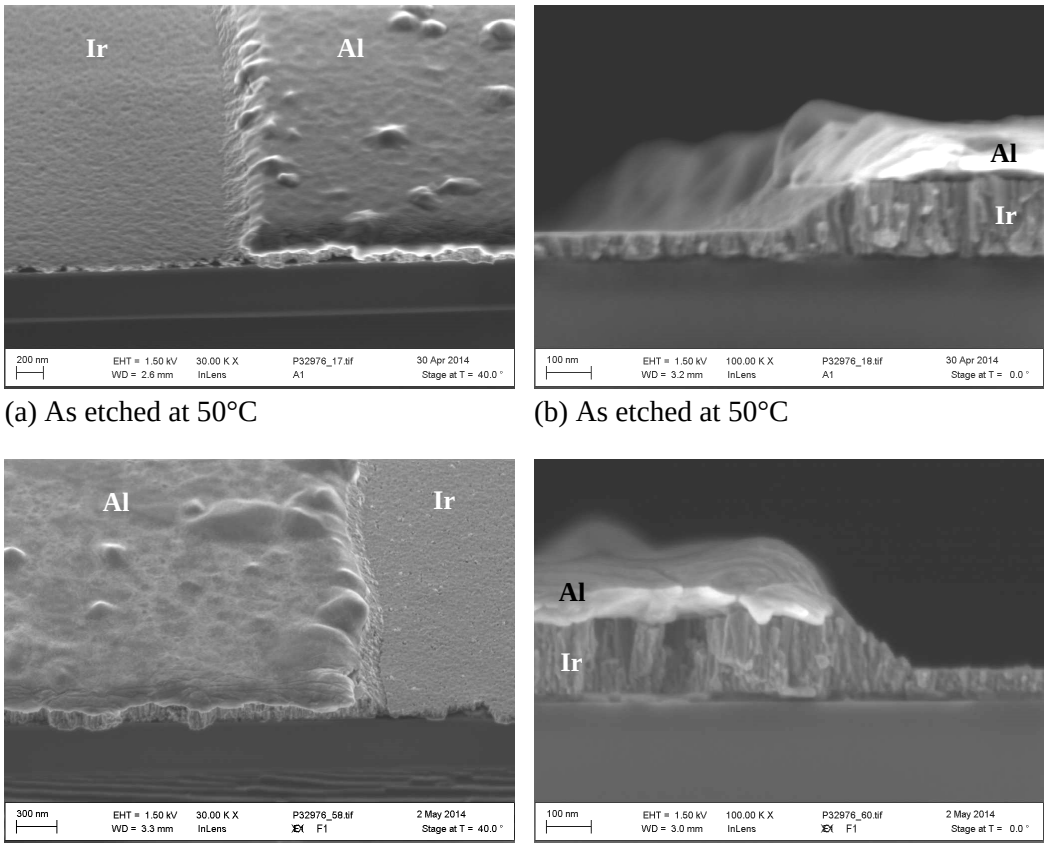


Figure 4.7 SEM images of the Ir film and Al mask before etching.

The samples etched at 50°C and 350°C are shown in **Figure 4.8**. Both Ir surface and Al surface are clean after etching. No fences or residues on the sidewalls are visible. The slope of the etched Ir sidewalls is around 45°. It is found that many hillocks form on the Al mask after etching. The reason is still unknown. As the hillock formation happens at low and high temperatures, the etching temperature should not be the key issue.



(a) As etched at 50°C (b) As etched at 50°C

(c) As etched at 350°C (d) As etched at 350°C

Figure 4.8 SEM images of Ir films and Al masks after etching.

The Ir film etched at 100°C after Al mask removal is shown in **Figure 4.9**. The whole surface, including the etched Ir area, the etched Ir sidewall and the unetched Ir area under the Al mask, is clean without any residue. The unetched Ir area under the Al mask is still smooth after etching and Al mask removal. That means the location of hillocks shown in **Figure 4.8** should be above the Ir film and the hillocks may not have anything to do with the Ir film under the Al mask.

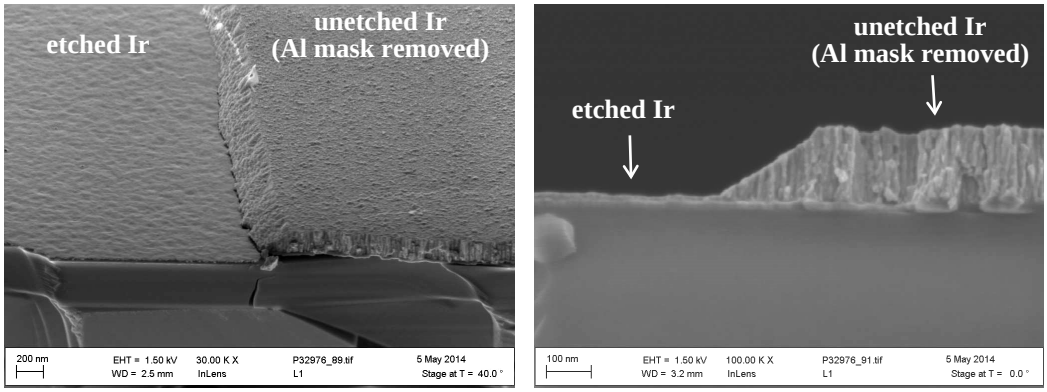


Figure 4.9 SEM images of the Ir film etched at 100°C after Al mask removal.

4.3 Summary

Reactive ion etching technology for iridium was developed and the results are shown in this chapter. CF_4/O_2/Ar gas mixtures were used with an aluminum film as hard mask for Ir etching at high temperatures. According to the results, the addition of Ar to the gas mixture seems to be profitless. The optimum gas mixing ratio is CF_4/O_2 = 35sccm/15sccm and the optimum ECR power is between 300W and 400W. The high process temperature at 350°C enhances the Ir etch rate to roughly 25nm/min, about five times higher than the etch rate at 50°C. All investigated processes at temperatures ranging from room temperature up to 350°C exhibit very high etching selectivities. Neither visible residues on the etched surfaces nor fences at the etched sidewalls could be detected. The surfaces of Ir and Al were clean after etching independent on etching temperature. Nevertheless, many hillocks formed on the Al mask after etching and the reason for it is still unknown.

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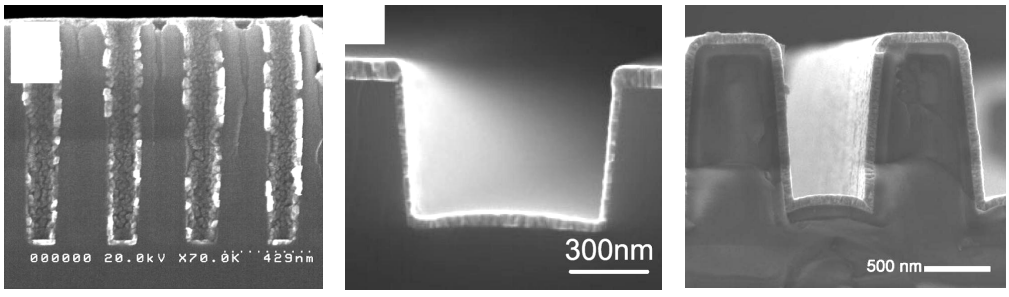
5 Deposition of Iridium Thin Films on Three-Dimensional Structures with MOCVD

5.1 Current Status of Iridium Thin Film Deposition in Three-Dimensional Structures

Up to now the commercialized FeRAM products are still made with planar capacitor structures. There are only a few studies on three-dimensional structures of ferroelectric capacitors and most of them are ferroelectric PZT films with Ir electrodes. Deposition of iridium and iridium oxide in three-dimensional structures with MOCVD or ALD (Atomic Layer Deposition) were investigated by a few research groups. [5.1]–[5.5] **Figure 5.1** shows some of the results in published papers. Generally speaking, conformal deposition of fine, thin Ir or IrO_2 films in three-dimensional trench holes is more difficult than that in trench lines especially with high aspect ratio. In this dissertation, iridium thin film deposition in trench holes and lines with MOCVD was studied as one of the steps of developing complete three-dimensional ferroelectric capacitor.



(a) (b) (c)

Figure 5.1 Deposition of Ir or IrO_2 thin films in trench holes and lines by (a) PEALD [5.3], (b) MOCVD [5.4], (c) ALD [5.5].

5.2 Deposition of Iridium Thin Films on Three-Dimensional Structures with Conventional MOCVD

In this study, deposition of iridium thin films in 3D trench structures was first developed with conventional MOCVD technology. 3D trench holes of 1μm depth and various widths from 0.3μm to 0.6μm were prepared on SiO_2/Si substrates which were provided by IHP (Leibniz-Institut für innovative Mikroelektronik) in Frankfurt (Oder), Germany. A thin titanium nitride (TiN) film of 20–50nm thickness was deposited by MOCVD on the SiO_2/Si substrates as adhesion layer before Ir deposition.

Figure 5.2 shows a schematic diagram of the deposition chamber for iridium and TiN in this study. TiN thin films were prepared using tetrakis(dimethylamido)titanium ($Ti[N(CH_3)_2]_4$, TDMAT) as precursor and NH_3 as reactants, N_2 gas was used as a carrier gas. The precursor flow was precisely controlled between 100–1000 mg/h by a liquid delivery system including a liquid flow controller (LFC) with an evaporator in series. The evaporator temperature was kept at 100°C. The flows of reactant gas and carrier gas were 100 sccm and 150 sccm, respectively. TiN was deposited at 300°C substrate temperature with a chamber pressure of 3 mbar.

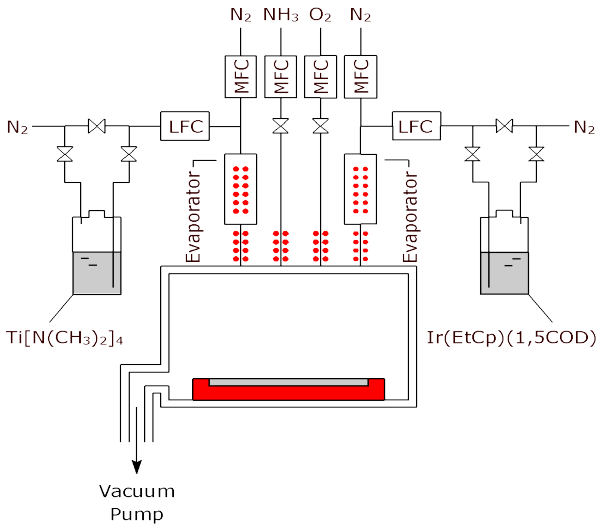


Figure 5.2 Schematic diagram of the conventional MOCVD system for TiN and Ir deposition.

In a subsequent process, Ir films were deposited on TiN at various substrate temperatures ranging from 300°C to 450°C using the same equipment. Ir(EtCp)(1,5COD) [iridium(ethylcyclopentadienyl)(1,5-cyclooctadiene)] was used as precursor and was diluted in toluene with a concentration of 0.1 M for liquid delivery. Oxygen was used as the co-reactant gas. Although oxygen may cause oxidation of the TiN layer, it is necessary for decomposition of the Ir precursor. Early experiments showed that no deposition of iridium films could be achieved without adding oxygen when Ir(EtCp)(1,5COD) was used as precursor. [5.6] The problem of oxidation of TiN must be solved in future studies. Details of the process parameters for both TiN and iridium deposition are summarized in **Table 5.1**.

Table 5.1 Process conditions for TiN and iridium deposition.

TiN	
Substrate	SiO_2 1µm/Si
Substrate temperature	300°C
Process pressure	3mbar
Evaporator temperature	100°C
Precursor	TDMAT 0.1M in toluene
Carrier gas	N_2 150sccm
Co-reactant gas	NH_3 100sccm
Iridium	
Substrate temperature	300–450°C
Process pressure	5–8mbar
Evaporator temperature	180°C
Precursor	Ir(EtCp)(1,5COD) 0.1M in toluene
Carrier gas	N_2 150sccm
Co-reactant gas	O_2 500sccm

Figure 5.3 shows the SEM cross-sectional views of Ir/TiN bottom electrodes in trench holes at various Ir deposition temperatures. There is no apparent difference of the Ir deposition in trench holes between 450°C and 400°C. Large iridium grains with many facets cause a high surface roughness. Grain size ranges from 10nm to 70nm in diameter. The step coverage of the deposited Ir films is rather poor, and is estimated to be less than 25%. Nevertheless, a full coverage of the structure was obtained. The deposition rate of Ir at 300°C is much lower than those at 400 and 450°C. A higher pressure (8mbar instead of 5mbar) was

used in order to increase the deposition rate. The Ir film deposited at 300°C looks different from those at 450°C and 400°C. The grains are bigger but with fewer facets. Such round grains are supposed to be less crystalline because of the lower deposition temperature. The surface morphology seems to be a little bit smoother than those at 450°C and 400°C. The step coverage at 300°C is only a little bit improved.

(a) 450°C

(b) 400°C

(c) 300°C

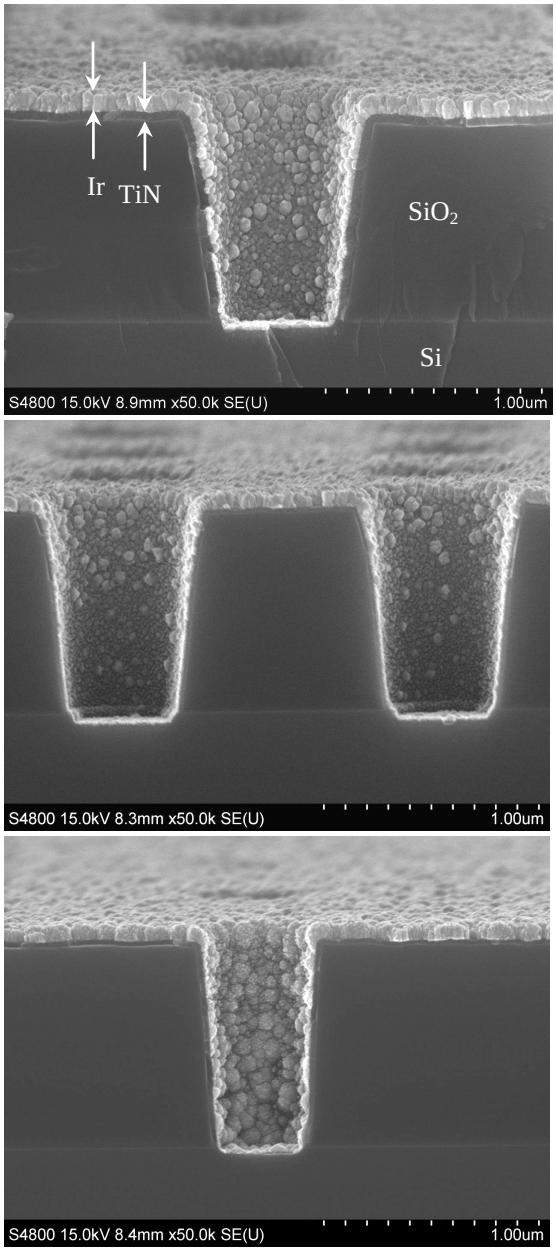


Figure 5.3 SEM cross-sectional views of Ir/TiN bottom electrode in SiO_2/Si trench holes at various Ir deposition temperatures : (a) 450°C, (b) 400°C, (c) 300°C.

A bottom electrode should provide a rather smooth surface to ensure a uniform deposition of the successive ferroelectric layer. According to the results shown in **Figure 5.3**, the roughness of the deposited Ir films in the trench holes is comparable to the thickness of the ferroelectric layer, which is usually about 70–100nm. The thickness uniformity of the ferroelectric film in trench holes could be strongly affected by such a roughness and in consequence, the ferroelectric properties could be degraded. An improvement of the surface morphology of the deposited iridium films is necessary.

5.3 Deposition of Iridium Thin Films on Three-Dimensional Structures with Plasma Enhanced MOCVD

A MOCVD chamber with plasma enhancement was used for further studies in order to improve iridium thin film deposition in three-dimensional structures. A schematic diagram of the equipment is shown in **Figure 5.4**. The same precursor Ir(EtCp)(1,5-COD) as in earlier studies was used but with a bubbler system instead of a liquid delivery system. The precursor is manufactured by Kojundo Chemical Laboratory Co., Ltd. According to the information provided by manufacturer, the melting point of Ir(EtCp)(1,5-COD) is 14 °C. At room temperature it is a yellow liquid. The vapor pressure from 333 to 393K can be calculated by $\log_{10} P = -4329/T+10.58$, where P is in mbar and T in K. The pure liquid precursor was heated in the bubbler to 100 °C and the precursor vapor was transported with Ar as carrier gas. The transport line between bubbler and chamber was kept at 200 °C. The precursor vapor was fed into the chamber and flows laterally to the substrate. An oxygen plasma was generated by electron cyclotron resonance (ECR) at the upper side of the chamber above the substrate. It was introduced into the chamber as oxidant to react with the Ir precursor. Silicon wafers with a SiO_2 film of 1 µm thickness were used as substrates in this study. Trench holes and trench lines of various sizes were generated on SiO_2 by photolithography and reactive ion etching. Thin Ti and TiN films were then deposited on these wafers and serve as adhesion layers for the iridium films. The wafers including the patterning process and the Ti/TiN deposition process were provided by IHP (Leibniz-Institut für innovative Mikroelektronik) in Frankfurt (Oder), Germany. Iridium thin films with thicknesses of about 50–300 nm were then deposited on these substrates under various process conditions. Some experiments were

performed with ECR plasmas and some without in order to analyze the effect of the plasma enhancement. Details of the process conditions are summarized in **Table 5.2**.

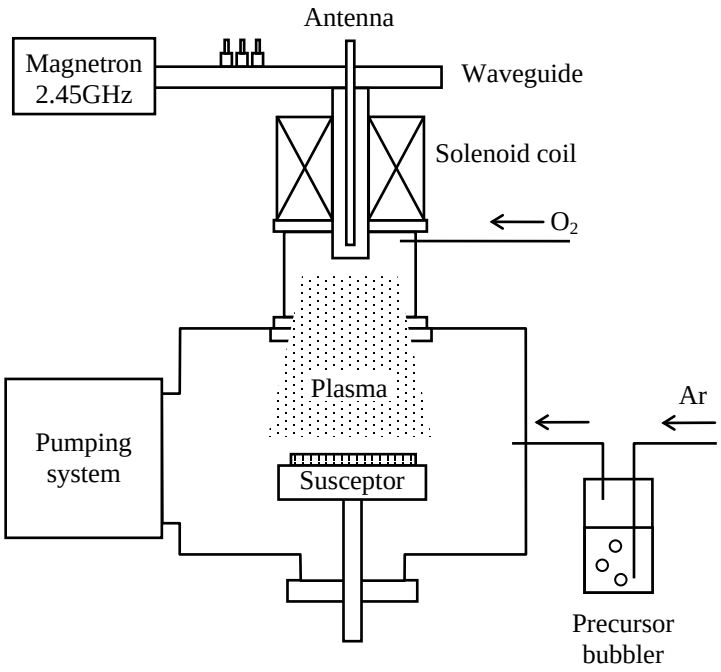


Figure 5.4 Schematic diagram of ECR-PE-MOCVD system.

Table 5.2 Process conditions for iridium deposition.

General parameters	
Substrate	TiN 25nm/Ti 20nm/SiO_2 1μm/Si
Substrate temperature	300–450°C
Bubbler temperature	100°C
Precursor line temperature	200°C
Carrier gas	Ar
Co-reactant gas	O_2
Conventional MOCVD	
Process pressure	0.2mbar
Ar flow	100sccm
O_2 flow	100sccm
ECR-PE-MOCVD	
Process pressure	0.01mbar
Ar flow	135–140sccm
O_2 flow	10–15sccm
ECR microwave power	200–350W

The crystal structure of the deposited iridium films was analyzed by X-ray diffraction (XRD), using a Bruker/AXS D5000 diffractometer. Step coverage and film geometry of the iridium films on different structures were evaluated by scanning electron microscopy (SEM) with a JEOL JSM-5900. The surface morphology of the films was additionally analyzed by atomic force microscope (AFM) using a Veeco Dimension 3100. Electrical resistivity of deposited Ir films was measured by four point probe method with a CDE ResMap 168.

Three substrate temperatures, 300 °C, 375 °C and 450 °C were used in various processes with and without plasma enhancement. The thickness distribution of the deposited Ir films over the wafer was very non-uniform and the distribution pattern varied with different substrate temperatures. It was affected by a non-uniform precursor flow from the lateral side because of the hardware constraints and was also sensitive to the O_2 flow and microwave power. Calculation and comparison of the deposition rate between different process conditions are therefore impractical. The experiments were performed for different process conditions with different process times in order to obtain Ir films that were thick enough for analysis at certain regions on the wafers. Generally speaking, the depositions at 450 °C and 375 °C without plasma enhancement were considerably faster than those with plasma enhancement. The reason is supposed to be related to the process pressure. For the depositions with plasma enhancement the pressure was much lower than for the conventional MOCVD process. At this pressure range the deposition rate decreases with decreasing pressure although the plasma can usually enhance deposition. The deposition rate also decreases with decreasing temperature. The deposition rate at 300 °C without plasma enhancement was too low. No iridium film could be found even after a deposition of six hours. Only with plasma enhancement a reasonable deposition rate at 300 °C was available. XRD scans (Bragg-Brentano with automatic slit system) of the layers grown under different process conditions are shown in **Figure 5.5**. All the deposited Ir films are polycrystalline with the evidence of (111) and (200) peaks. In the process at 300 °C substrate temperature with plasma the film is almost randomly oriented according to the intensity ratio of (111) and (200) peaks. A further annealing procedure at 450 °C in O_2 for 2 hours does not change the crystallization of the Ir film. At higher substrate temperatures the deposited Ir films become more (111) textured, as the results at 375 °C and 450 °C show. It can be seen in **Figure 5.5** that Ir films grown with plasma enhancement are more (111) textured than films without plasma at the same substrate temperature.

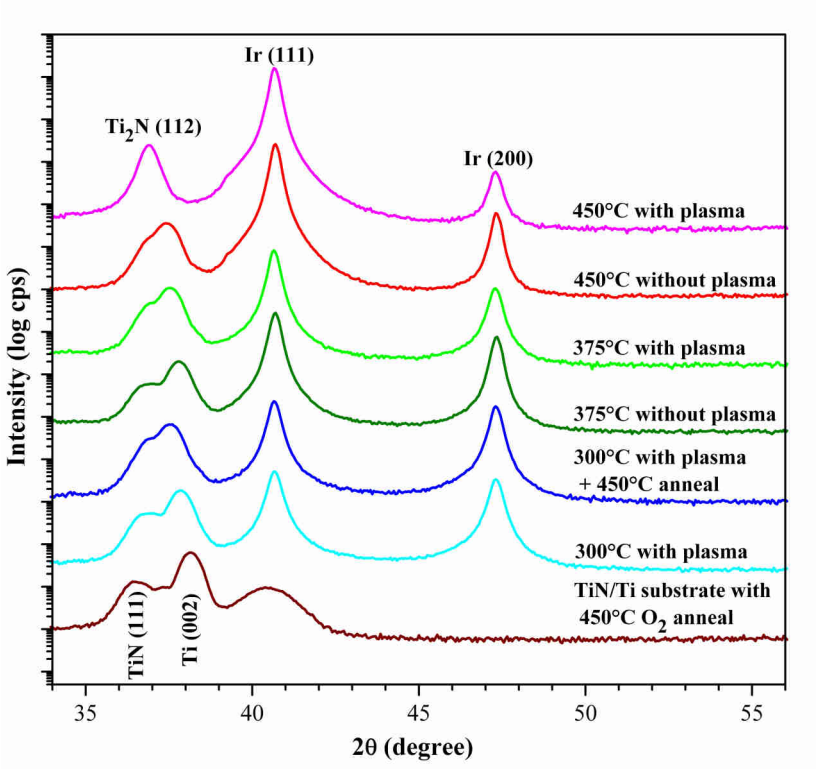


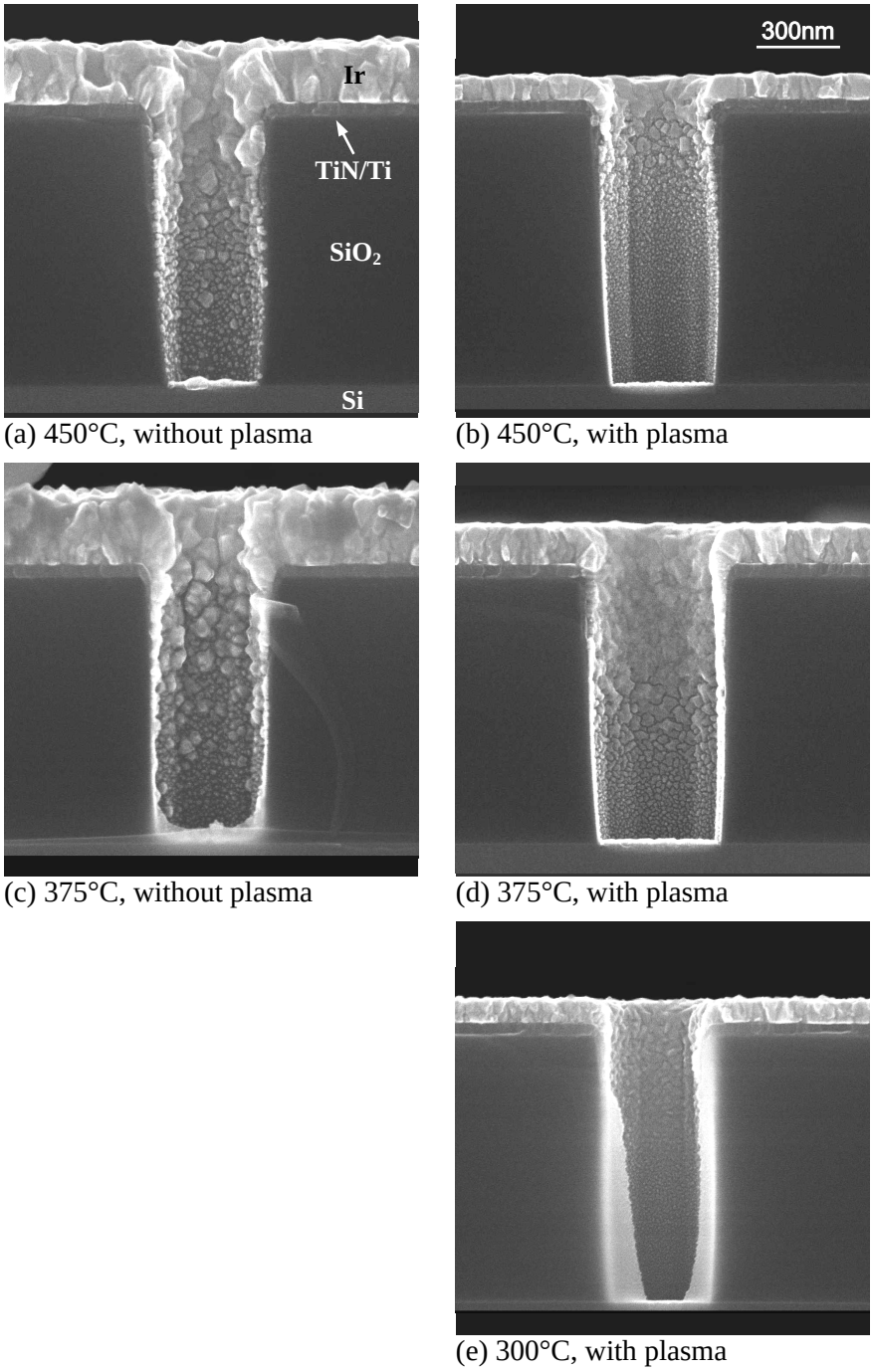
Figure 5.5 XRD patterns of iridium films deposited with various process conditions.

The XRD pattern of a substrate without the Ir film is also included in **Figure 5.5** as standard for comparison. TiN (111) and Ti (002) peaks are visible for this sample. These two peaks shift more closely to each other after iridium deposition. It seems that the deposition process can induce an interdiffusion of Ti and TiN. The higher the process temperature is, the closer these two peaks are. A sample of the Ir film deposited at 300 °C with plasma enhancement was annealed subsequently at 450 °C and a further peak shift is found. Samples grown with plasma enhancement show larger shifts than those without plasma enhancement. In the process at 450 °C with plasma enhancement, these two peaks merge into a single peak of Ti_2N (112). It should be noticed that the standard sample was also annealed in O_2 at 450 °C but it shows no peak mergence. That means the interdiffusion is not induced merely by the process temperature. The influence of iridium film and plasma plays also an important role. The influence of temperature together with mechanical stress resulting from lattice mismatch between the deposited Ir films and TiN/Ti layers is supposed to be a possible reason for the interdiffusion of Ti and TiN layers. The fact that Ir

films with plasma enhancement are more (111) textured affects the mechanical stress and, therefore, affects the interdiffusion as well.

The deposited iridium films are investigated with SEM. **Figure 5.6** shows images of cross-sections of deposited Ir films in trench holes. The holes have an oval shape with 0.3µm width, 0.6µm length and 1µm depth and are cut along the width direction. The aspect ratio along width direction is about 3. **Figures 5.6(a)** and **(c)** show films deposited at 450°C and 375°C without plasma enhancement. The grain size is very large and iridium grows into large grains on the sidewalls in the holes before forming a continuous film. Therefore, the Ir film is very rough inside the holes and also on the top surface outside the holes. **Figures 5.6(b)**, **(d)** and **(e)** show the results of depositions at 450°C, 375°C and 300°C with plasma enhancement. The films on the top surface as well as in the trench holes are obviously smoother than those without plasma enhancement. Although the films on the top surface are thick enough for electrodes, the films in trench holes are very thin. Especially on the lower part of the sidewalls, only discontinuous individual nuclei were grown. The Step coverage for all these process conditions is estimated to be less than 0.1. Deposition of a fine, uniform and continuous Ir films seems difficult in trench holes with aspect ratios at about 3.

The results of larger trench holes with a size of 0.6µm width × 1.2µm length are shown in **Figure 5.7**. The aspect ratio along width direction is about 1.7. In chemical vapor deposition on three dimensional structures, higher aspect ratios can limit the mass-transport of active reactants into trench holes. Trench holes with lower aspect ratio have usually better deposition performance in the holes than those with higher aspect ratio in the view of step coverage and film thickness on bottom and sidewalls. The filling of iridium films in these trench holes in **Figure 5.7** is improved in comparison to those trench holes in **Figure 5.6**. Films without plasma enhancement are still very rough with large grains, but it is possible to form continuous films in these trench holes. The benefit of plasma enhancement for the surface planarization can be seen here more clearly, especially in comparison to the narrower trench holes of **Figure 5.6**. It is shown in **Figure 5.7(e)** that the iridium film deposited at 300°C with plasma enhancement has a smoother surface with finer grains than films with other process conditions. The step coverage is improved to be about 0.2. This is still not a conformal deposition but it is acceptable for the application as electrodes in three dimensional structures.



(a) 450°C, without plasma

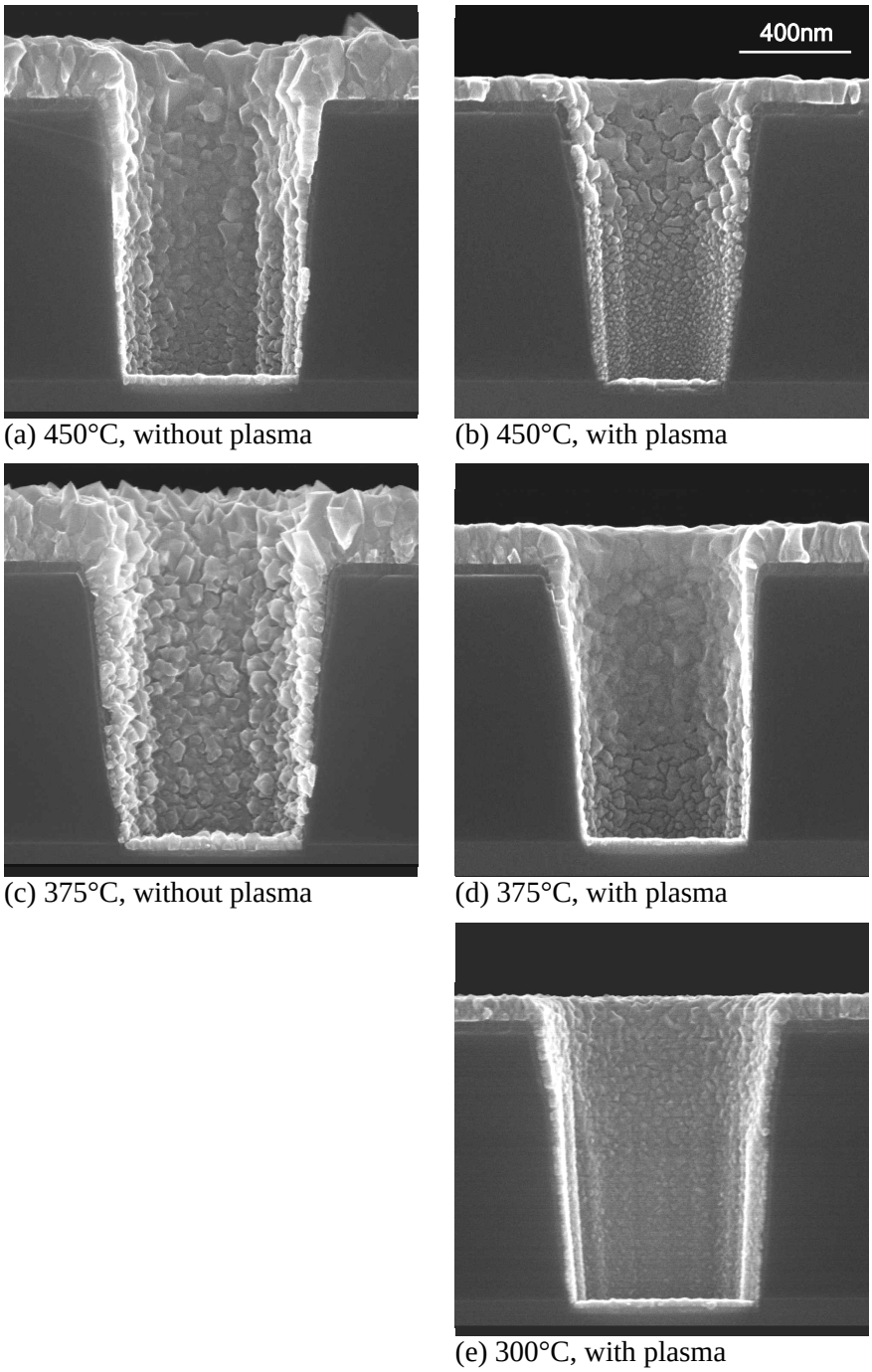
(b) 450°C, with plasma

(c) 375°C, without plasma

(d) 375°C, with plasma

(e) 300°C, with plasma

Figure 5.6 SEM cross-sectional views of iridium films deposited in trench holes of 0.3μm width.



(a) 450°C, without plasma
(b) 450°C, with plasma
(c) 375°C, without plasma
(d) 375°C, with plasma
(e) 300°C, with plasma

Figure 5.7 SEM cross-sectional views of iridium films deposited in trench holes of 0.6µm width.

A quantitative evaluation of the surface roughness was made by measurements with an AFM on the top surfaces near the trench holes. The results are shown in **Figure 5.8**. They also confirm the planarization effect of the plasma. The deposition at 375 °C without plasma has the roughest iridium film surface with a root-mean-square value of roughness Z_{rms} of

about 18.8 nm. The surface roughness of the iridium film deposited at 450 °C without plasma is 14.1 nm. The surface roughness of films grown with plasma enhancement at different deposition temperatures ranging from 300 °C to 450 °C is comparable and amounts to 5–6 nm. Although the iridium films deposited with plasma enhancement have similar levels of surface roughness, the film deposited at 300 °C has much finer grains than those at 375 °C and 450 °C, as can be seen in **Figure 5.8**. On the other hand, although plasma enhancement has the effect of surface planarization, the grain size of Ir films on the top surface looks similar to the Ir films deposited by conventional MOCVD at the same temperature. It seems that the grain size of Ir films in this study depends to a high extent on deposition temperature but at most marginally on plasma enhancement.

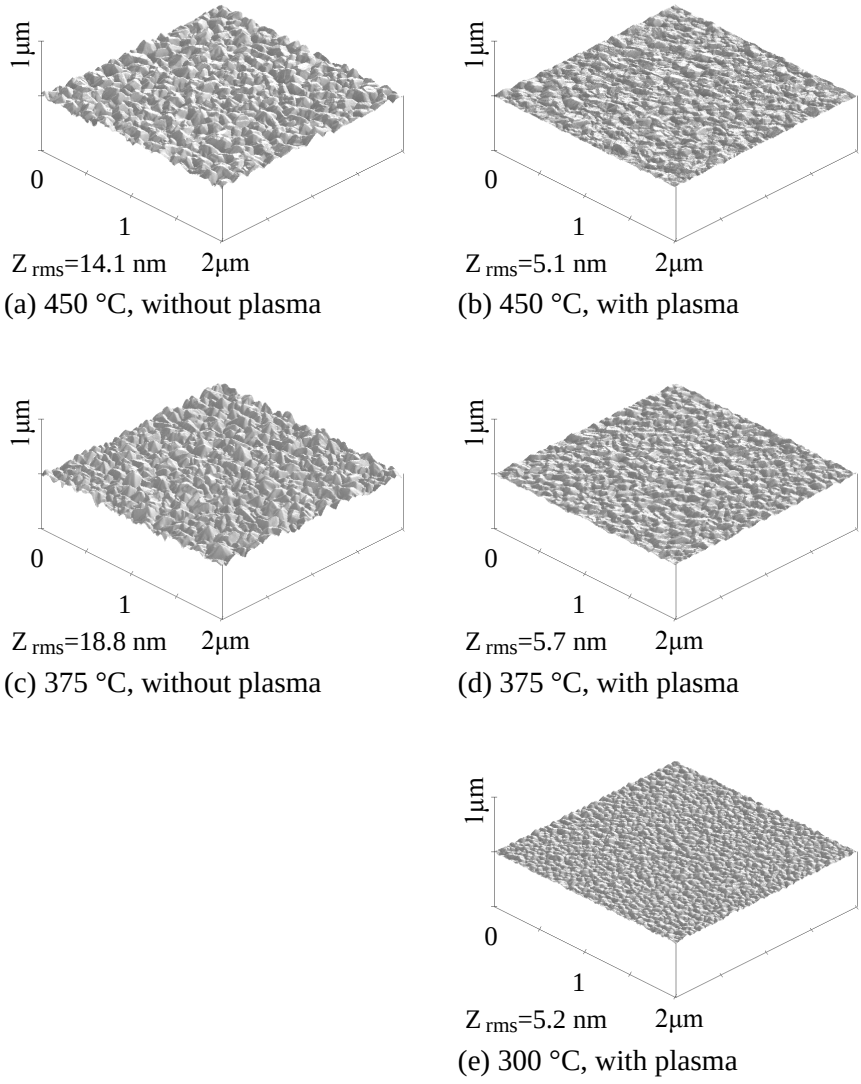


Figure 5.8 AFM surface morphology of iridium films.

An et al. [5.7] and Tseng et al. [5.8] demonstrated in their studies that plasma treatments can cause thin film surface planarization and densification. An et al. attributed the surface planarization to a filling of surface pores by surface adatoms that are excited by plasma ions, which results in a smoother surface. In order to clarify the effect of plasma in surface planarization, our Ir films deposited with conventional MOCVD were processed with a further plasma post treatment. The process conditions of the plasma post treatment were the same as the process conditions during the plasma-enhanced Ir film deposition but without precursor flow. The Ar carrier gas flowed through a bypass line into the chamber. The results of AFM measurements show that the surface roughness of Ir films deposited with conventional MOCVD did not significantly change after the plasma post treatment. That means a pure plasma treatment alone does not affect the planarization of Ir films in this study. The surface planarization is, therefore, not caused by pure physical sputtering effects of Ar and O_2 plasmas. The mechanism of surface reaction chemistry and nucleation in the deposition with plasma enhancement may be different from that of conventional MOCVD and is supposed to be the cause for planarization.

Figure 5.9 shows the results of a deposition in 0.7μm trench lines. Deposition of iridium without plasma enhancement seems to result in smoother surfaces in trench lines than in trench holes as can be seen by comparing **Figure 5.7(a)** and **Figure 5.9(a)**. The film deposited at 300°C with plasma enhancement has the finest grain and smoothest film morphology in comparison to processes with different conditions. For all process conditions the step coverage of the deposited iridium films is better in trench lines than in trench holes.

The electrical resistivity of the deposited Ir films was measured by four point probe method and is shown in **Figure 5.10**. The resistivity of Ir films at various process conditions ranges from 7 to 11 μΩ-cm. The Ir films deposited at 375°C have a little higher resistivity than the films deposited at 300 and 450°C. Plasma enhancement helps to reduce the resistivity. The variation of resistivity is supposed to be the result of combined effects of purity, density/porosity and grain size of Ir films.

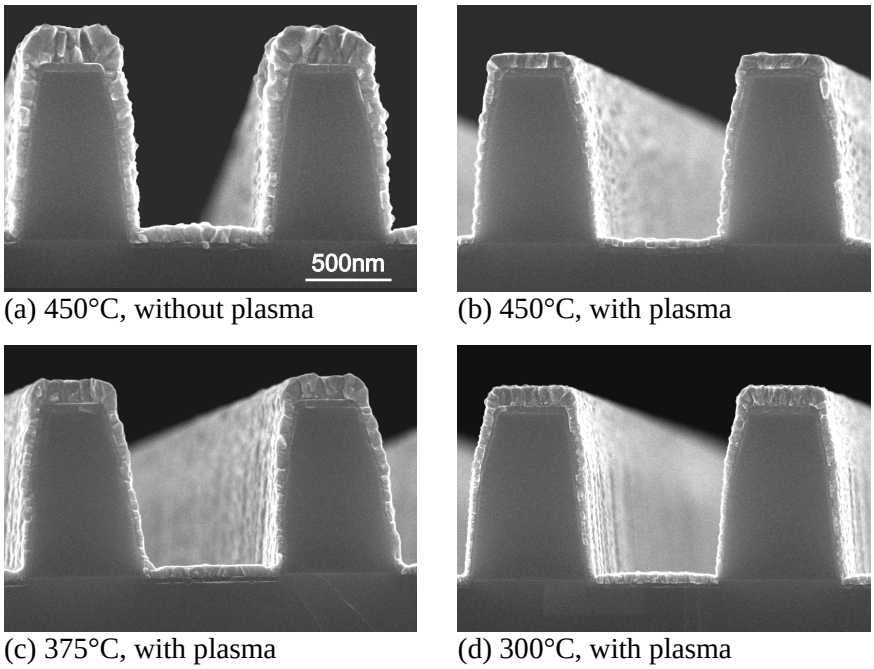


Figure 5.9 SEM cross-sectional images of iridium films deposited in trench lines of 0.7μm width.

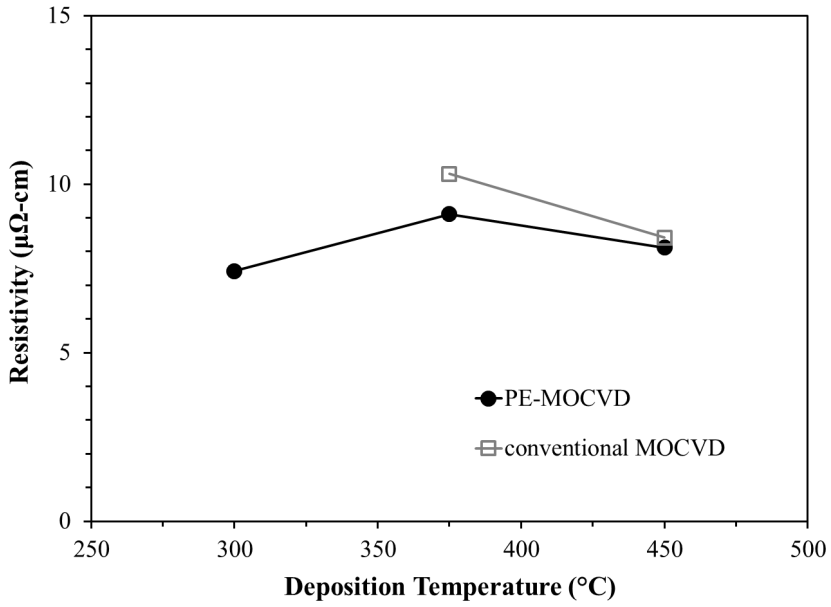


Figure 5.10 Electrical resistivity of deposited Ir films.

5.4 Summary

Summarizing the results of **Section 5.2** and **Section 5.3**, it can be concluded that the iridium thin film deposition with conventional MOCVD without plasma enhancement results in very rough iridium films with large grains especially on the sidewall in trench holes. Plasma enhancement during the deposition process seems to support planarization of the surface and results in smoother films. The deposition of uniform iridium films with fine grains in trench holes of 0.3µm width is difficult, but in trench holes of 0.6µm width and trench lines of 0.7µm width, iridium films with acceptable step coverage and surface morphology are achievable with a sufficient quality for the application as electrodes for three-dimensional capacitor structures.

5.5 Reference

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6 Fabrication of Three-Dimensional Ferroelectric Capacitors

6.1 Current Status of Three-Dimensional Ferroelectric Capacitors

FeRAM with three-dimensional ferroelectric capacitor structures have been studied by institutes and companies since many years. Most of them were based on PZT thin films. [6.1]–[6.8] The 3D ferroelectric capacitors based on SBT thin films were also investigated. [6.9][6.10] Up to now all the FeRAM chips in mass-production use two-dimensional parallel-plate capacitors as storage node. Three-dimensional ferroelectric capacitors are still in development. Neither mass-production nor test chip of FeRAM with 3D capacitors is available now.

6.2 Deposition of Ir/PZT/Ir Thin Films on Three-Dimensional Structures

After developing the technologies for deposition of PZT and Ir thin films which are described in **Chapter 3** and **Chapter 5**, the realization of three-dimensional ferroelectric capacitors was studied in this chapter.

Silicon wafers with a SiO_2 film of 1µm thickness were used as substrates in this study. Trench holes and trench lines of various sizes ranging from 0.3µm to 2µm were generated on SiO_2 by photolithography and reactive ion etching. A Ti film of 20nm thickness and a TiN film of 25nm thickness were deposited subsequently on these wafers and serve as adhesion layers for iridium films. After some experiments showed that these adhesion layers did not work very well, a single Ti layer of 40nm thickness was then used as adhesion layer. The wafers including the patterning process and the Ti/TiN deposition process were provided by IHP (Leibniz-Institut für innovative Mikroelektronik) in Frankfurt (Oder), Germany. According to the optimized results of **Chapter 5**, iridium thin films as bottom electrode were deposited on these substrates at 300°C with ECR plasma enhancement. PZT films with a

thickness about 100nm were then deposited at 450, 500 and 550°C on the iridium films. On some samples a further Ir film was deposited as top electrode to form Ir/PZT/Ir stacks. The other samples were left without Ir top electrode in order to investigate the surface morphology of PZT films. The details of the process conditions are summarized in **Table 6.1**. Step coverage, film geometry and film composition of the PZT/Ir and Ir/PZT/Ir thin film stacks were investigated by scanning electron microscopy (SEM), transmission electron microscopy (TEM) and scanning transmission electron microscopy (STEM).

Table 6.1 Process conditions for Ir/PZT/Ir deposition.

Substrate		$Ti/SiO_2/Si$ $TiN/Ti/SiO_2/Si$
Iridium bottom electrode		**ECR-PE-MOCVD**
Precursor	Ir(EtCp)(1,5-COD)	Pure in bubbler
Bubbler temperature		100°C
Precursor line temperature		200°C
Carrier gas		Ar, 135sccm
Co-reactant gas		O_2, 15sccm
Substrate temperature		300°C
Process pressure		0.01mbar
ECR microwave power		300W
PZT		**MOCVD**
Precursors	$Pb(thd)_2$	0.05M
	$Zr(OiPr)_2(mmp)_2$	0.02M
	$Ti(OiPr)_2(mmp)_2$	0.05M
Solvent	Octane	
Vaporizer temperature		220°C
Showerhead temperature		220°C
Gas lines temperature		220°C
Carrier gas		N_2, 800sccm
Co-reactant gas		O_2, 1100sccm
Substrate temperature		450/500/550°C
Process pressure		5.0mbar
Iridium top electrode		**ECR-PE-MOCVD**
The same as for the iridium bottom electrode		

For electrical characterization similar wafers were used as substrates but with different 3D structures. Two chips with different 3D structures were designed for electrical characterization. The first chip, 3DA, consists of parallel trench lines with 1µm width, 1µm distance and 1µm depth. The second chip, 3DB, consists of parallel trench lines with 2µm width, 2µm distance and 1µm depth. Both chips were fabricated on the substrates in neighborhood for 3D capacitors together with one additional chip, 2D, without any structures for 2D capacitors. All three chips were processed together at the same time in order to analyze the difference between 2D and 3D capacitors. For the samples with the purpose of electrical characterization, Ir bottom electrodes and PZT ferroelectric films were deposited using the same methods and process conditions as mentioned above. The Ir top electrodes were not prepared by ECR-PE-MOCVD because otherwise a RIE process for the Ir top electrodes would be necessary. Although the reactive ion etching technology of Ir has been developed in **Chapter 4**, it was not applied to our Ir/PZT/Ir stacks because the impact of the RIE process on the properties of the PZT films still needs to be investigated in detail. In this work, the Ir top electrodes for electrical characterization were prepared by e-beam evaporation at 250°C using a shadow mask with many holes of various diameters ranging from 0.2 to 1.0mm. Because thin film deposition by e-beam evaporation on 3D structures is strongly anisotropic, the samples were tilted to about 15° with rotation in order to enhance deposition at sidewalls of the trench lines. After top electrode deposition the samples were annealed at 300–400°C in atmosphere for 30–60 minutes before electrical measurements. Because the whole Ir bottom electrode is covered by the PZT film during the deposition process, a small area of the PZT film is etched off with a chemical solution (6% HNO_3 + 2% HF + 1% HCl) in order to provide electrical contact to the bottom electrode. Electrical properties, such as P-V hysteresis loops and leakage currents, of these capacitors were measured by using a ferroelectric test module TF ANALYZER 1000 (aixACCT Systems GmbH) and a Keithley 6430 source meter.

The cross sections of the 3D PZT/Ir and Ir/PZT/Ir thin film stacks were investigated by SEM. **Figure 6.1** shows the cross-sectional view of trench holes of width/length/depth =0.6µm/1.2µm/1µm. The PZT film was deposited at 450°C on the bottom Ir film. The step coverage of the PZT film is estimated to be about 0.4. The top/bottom iridium layers have poor step coverage but should be sufficient to work as electrodes.

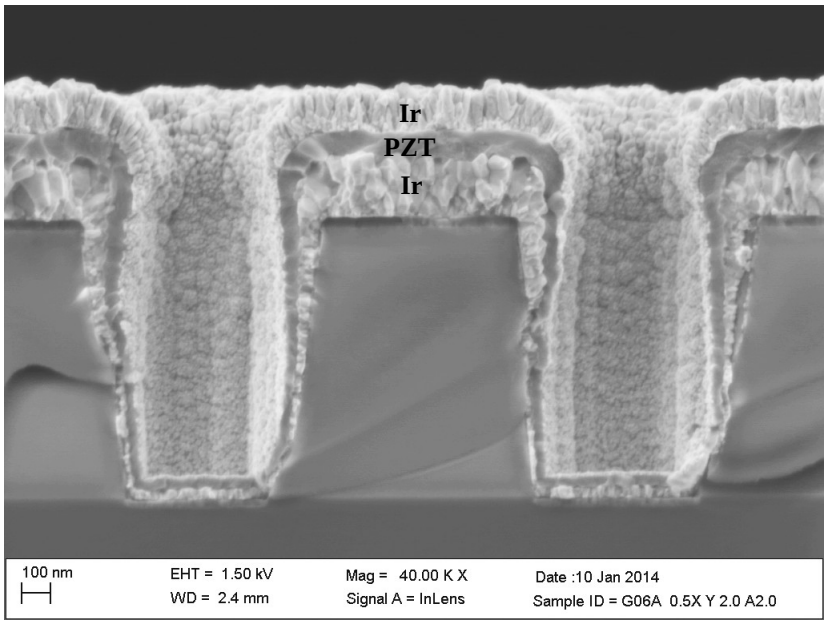


Figure 6.1 SEM cross-sectional view of the Ir/PZT/Ir film stack deposited in trench holes of 0.6µm width (450°C PZT).

The step coverage of the PZT film and the Ir films in trench lines are much better than those in trench holes. The PZT film deposited at 450°C in trench lines of width/distance/depth = 0.7µm/0.7µm/1µm has a step coverage of 0.57 (**Figure 6.2**). For the PZT deposition at 500°C the step coverage is further improved up to 0.66 (**Figure 6.3**).

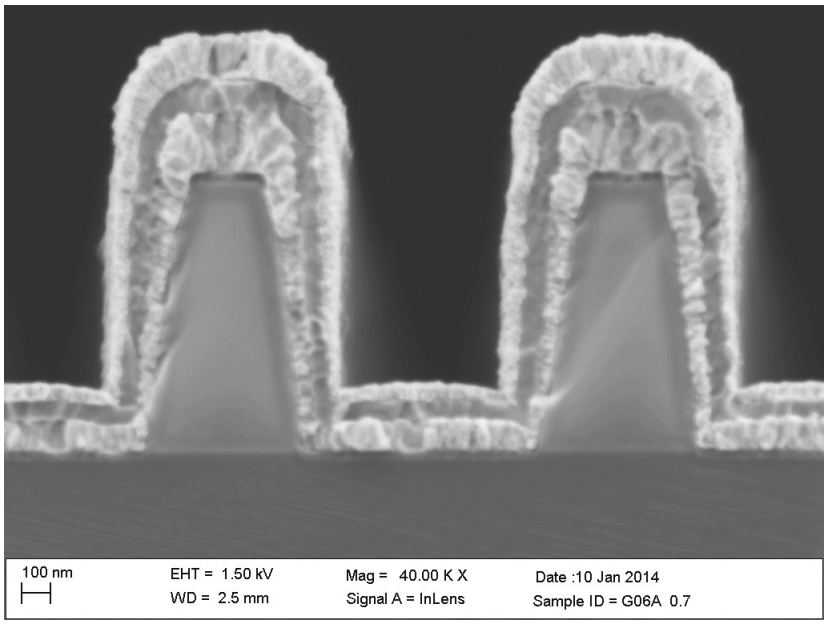


Figure 6.2 SEM cross-sectional view of the Ir/PZT/Ir film stack deposited in trench lines of 0.7µm width (450°C PZT).

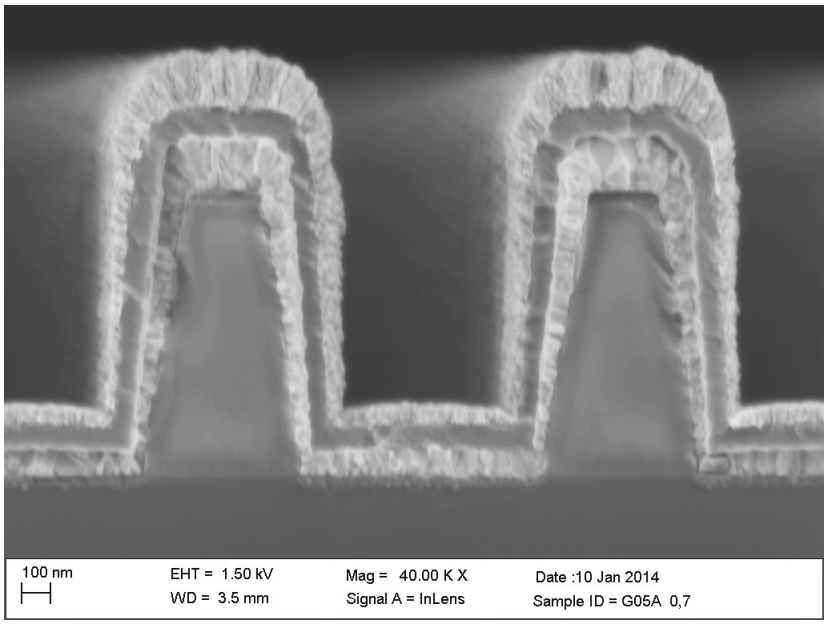


Figure 6.3 SEM cross-sectional view of the Ir/PZT/Ir film stack deposited in trench lines of 0.7µm width (500°C PZT).

The samples have 3D structures of various dimensions. The step coverage of PZT films deposited at 450°C in trench lines of width/distance ranging from 0.7µm/0.7µm to 2µm/2µm with Ir bottom electrodes is summarized in **Figure 6.4**. The PZT film thickness on top of the line and on bottom of the line strongly depends on the 3D dimensions. It is found that the difference of the thickness between top and bottom on 0.7µm/0.7µm (width/distance) trench lines is higher than for the other wider trench lines. If the line is wider, the thickness on bottom increases but the thickness on top decreases. The deposition on bottom of the trench lines depends on the aspect ratio of the structures, which affects mass transport of the chemical reactants. A narrower trench line has a higher aspect ratio, which makes mass transport more difficult to the bottom region of the lines. Therefore, deposition rate and thickness on bottom decrease with decreasing line width/distance. The step coverage becomes better on wider lines with a lower aspect ratio. On 1µm/1µm (width/distance) trench lines with 1µm depth (aspect ratio = 1) the step coverage reaches a value of 0.8. On 2µm/2µm (width/distance) trench lines with 1µm depth (aspect ratio = 0.5) the step coverage is close to 1. The PZT films are conformal and have uniform thicknesses on tops, sidewalls and bottoms of the trench lines of these dimensions.

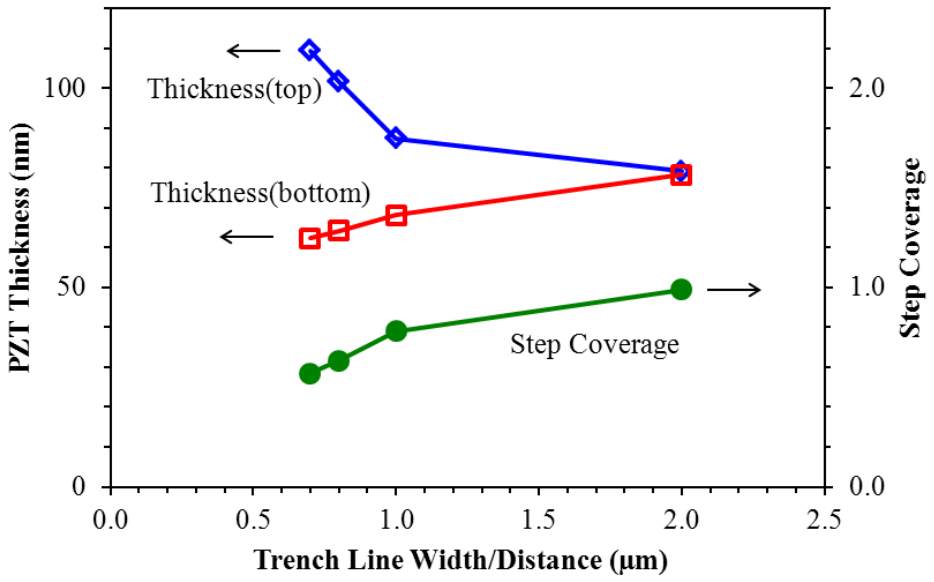


Figure 6.4 Step coverage of PZT films deposited at 450°C in trench lines with Ir bottom electrodes.

Phase separation is also found in PZT films on 3D structures. In **Figure 6.5** it can be clearly seen that the PZT film on the upper half of the sidewall in the hole and on the surface outside the hole looks very rough. The lower half of the sidewall in the hole appears to be smoother. A converse result can be found, too, and is shown in **Figure 6.6**. The PZT film on the lower part of the hole is rougher than the upper part and outside. A horizontal distribution of smoother/rougher phases happens as well and is shown in **Figure 6.7**. In **Figure 6.8** it can be seen that the sidewall of the line exhibits partially the smoother and partially the rougher phase. The disk rougher phase lies mostly on the bottom region. But it should be noted that in other samples the disk rougher phase can also be seen on the sidewall or the top of the lines. According to these results shown in **Figure 6.5** to **Figure 6.8**, it seems that there is no consistent relation between the profiles of the 3D structures and the formation of phase separation. 3D structures probably have no or only minor effects on the formation of phase separation by affecting mass transport of the chemical reactants. There should be other aspects which can affect formation of phase separation as well. Therefore, the influence of 3D structures becomes insignificant.

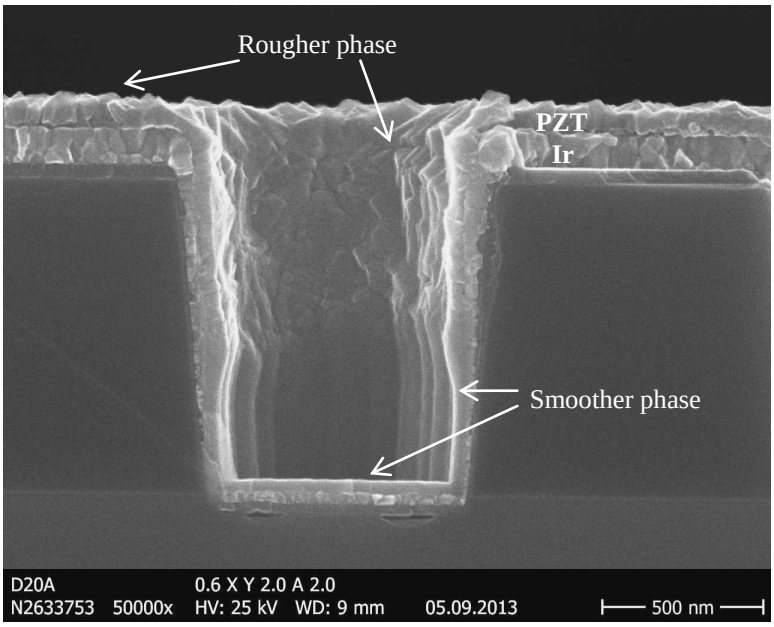


Figure 6.5 SEM image of PZT phase separation on 3D hole structures (vertical distribution).

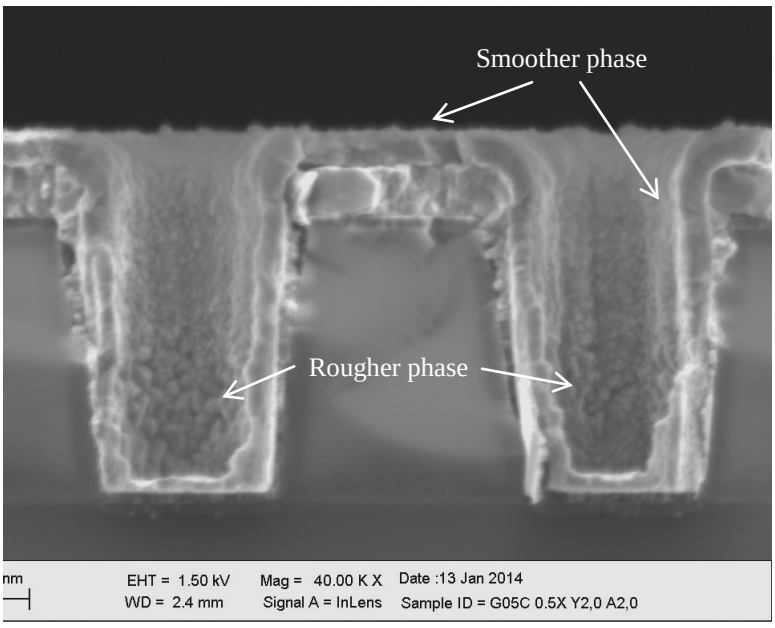


Figure 6.6 SEM image of PZT phase separation on 3D hole structures (vertical distribution).

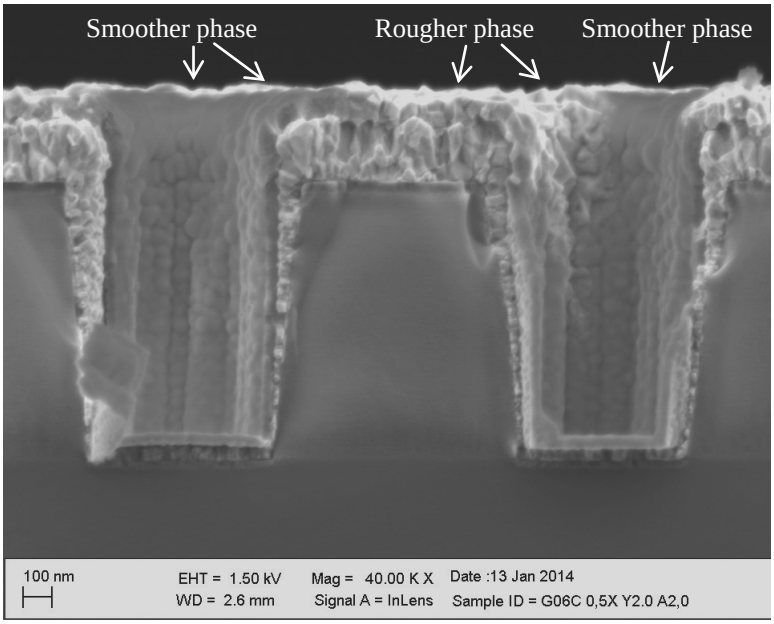
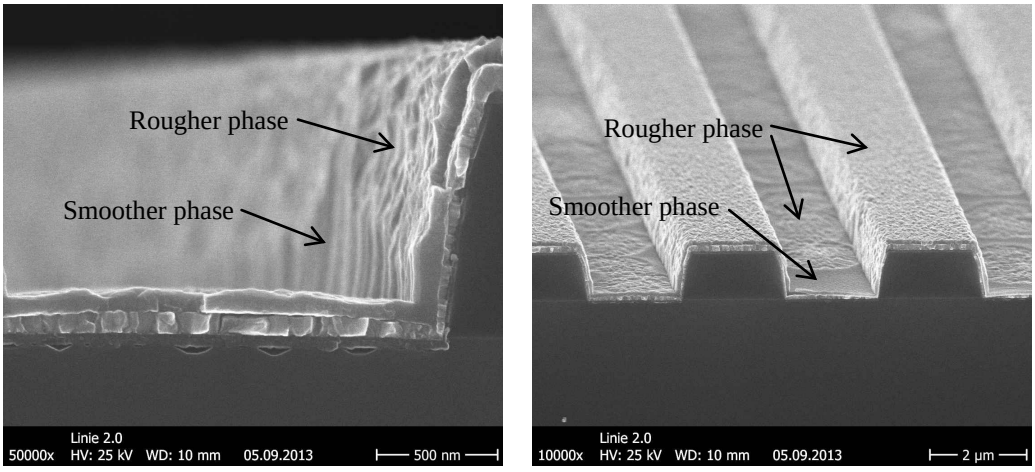


Figure 6.7 SEM image of PZT phase separation on 3D hole structures (horizontal distribution).



(a) (b)

Figure 6.8 SEM images of PZT phase separation on 3D line structures.

In the studies of Samsung, [6.4][6.5][6.8] phase differences of PZT films in trench holes were also recognized but their results differ from the results of this work. They found that a granular pyrochlore phase is prone to form on the lower part of the sidewalls in trench holes while a columnar perovskite PZT phase forms on the upper part of the sidewalls and on top surfaces outside the trench holes. The boundary between columnar phase and granular phase moved downward if the hole size increased or the process pressure increased.

STEM EDX line scans were performed to investigate the composition of the PZT films along the profile of 3D structures. The atomic composition is calculated with the Cliff-Lorimer method. In order to reduce the influence of other elements on composition percentage, the results are presented as Pb/(Zr+Ti) and Zr/(Zr+Ti) ratios. The composition of PZT films deposited at 500°C on 3D trench holes and trench lines are shown in **Figure 6.9** and **Figure 6.10**.

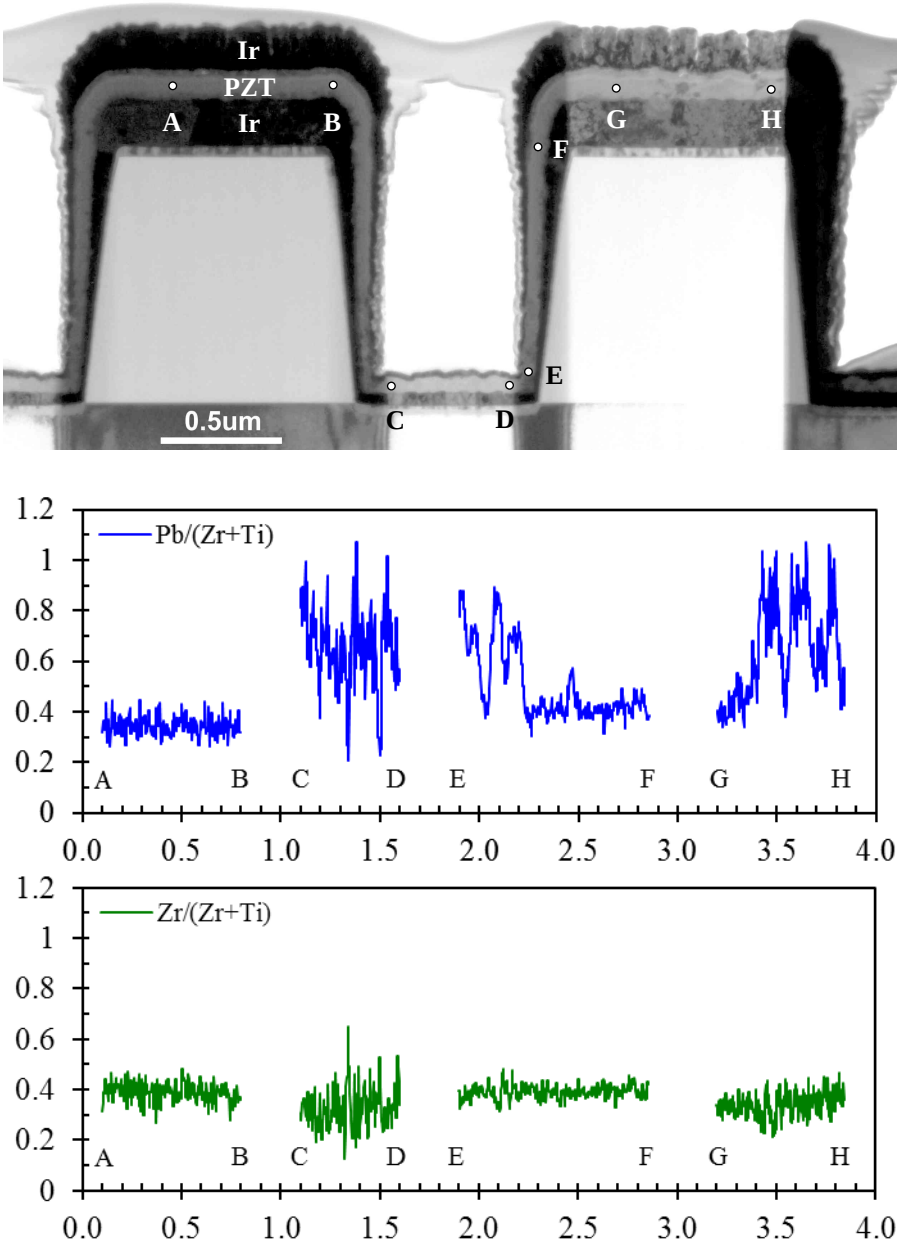


Figure 6.9 TEM cross-sectional view of Ir/PZT/Ir stack on 3D trench hole structures (width 0.6μm) and results of EDX line scans.

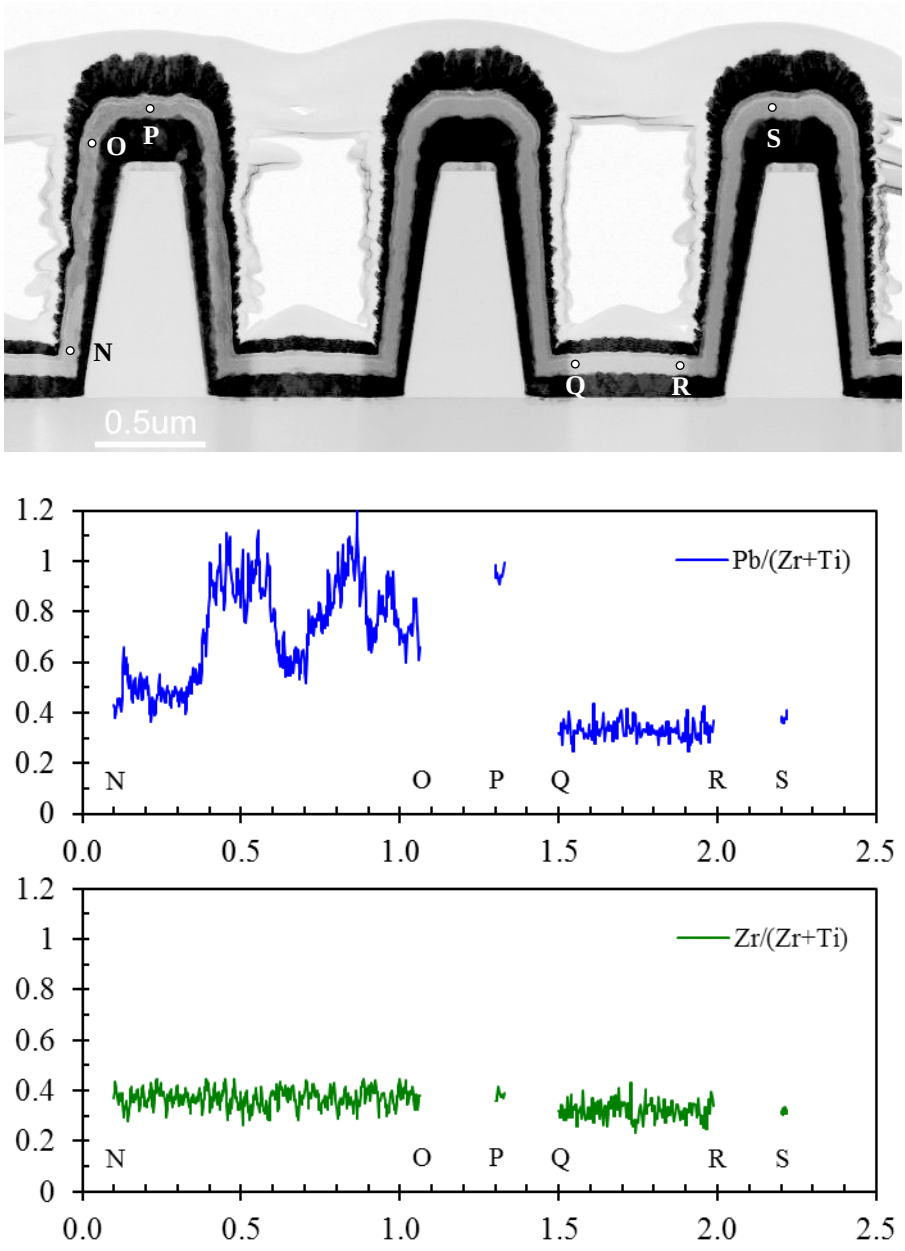
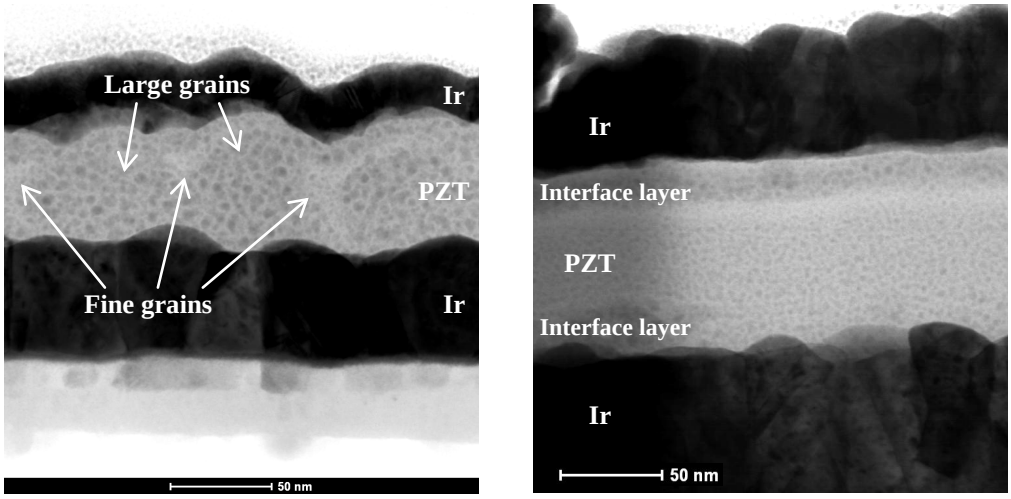


Figure 6.10 TEM cross-sectional view of Ir/PZT/Ir stack on 3D trench line structures (width/distance 0.7µm) and results of EDX line scans.

The Zr/(Zr+Ti) ratio stays stable close to 0.3–0.4 along the 3D profile on both trench hole and trench line structures. The Pb/(Zr+Ti) ratio is stable in some scan sections but very unstable in some other sections. There seems to exist a base value of Pb/(Zr+Ti) close to 0.4. In unstable regions the ratio varies strongly and can reach a value up to 1.1. By comparing TEM images with the line scans, it can be found that the variation of brightness in the images

matches with the variation of the Pb/(Zr+Ti) ratio. In scan sections E–F, G–H and N–O, the regions with higher Pb/(Zr+Ti) ratio are also darker than other regions. The darker brightness appears to be caused by more content of heavy Pb atoms in these regions.

Figure 6.11 shows a comparison of the STEM images of C–D and Q–R line scan regions with higher magnification. The top surface of PZT is rough in the C–D region but rather smooth in the Q–R region. This reveals that the C–D region has a rougher phase and the Q–R region has a smoother phase. The PZT film seems to be not well crystalized but consists of many small grains. In the C–D line scan region, grain size difference is quite obvious. Parts of the region contain large grains in the size between 5nm–10nm. The other parts contain finer grains of about 2nm–3nm. The ferroelectric property originates probably from these grains. The variation of grain size seems to have a relation with the variation of Pb/(Zr+Ti) ratio of the PZT films. A large variation of the grain size along the C–D scan line exhibits an unstable Pb/(Zr+Ti) ratio of the PZT films. A homogenous distribution of fine grains in the PZT film shows a stable Pb/(Zr+Ti) ratio of about 0.3–0.4 in the Q–R line scan region.



(a) Line scan section C−D (b) Line scan section Q−R

Figure 6.11 STEM cross-sectional view of the Ir/PZT/Ir stack on the bottom of 3D trench hole and line structures.

In **Figure 6.11(b)** interface layers are visible between PZT and Ir films including top Ir and bottom Ir films. The interface layers seem to be PZT but differ from the PZT in middle region. **Figure 6.12** shows a cross-sectional view of a PZT film in which interface layers are more clearly visible. The interface layers have grains a little bit larger than the grains near the middle of the PZT film and look darker than the middle region of the PZT film. Sometimes a brighter second interface layer can be seen between the first interface layer and the PZT film. Contrary, the second interface layer has finer grains and maybe less dense than the middle of the PZT film. The EDX line scan across the PZT film reveals that the darker interface layer contains much more Pb and less Zr, Ti than the middle of the PZT film. But in the brighter interface layer there is a little bit less Pb than in the middle of the PZT film. Although it is found that the content of Zr and Ti is smaller in the darker interface layer, the Zr/(Zr+Ti) ratio is nearly constant across the whole PZT film. The content of O and Ir does not differ in the interface layers. Pb seems to be the only element related to the interface layers.

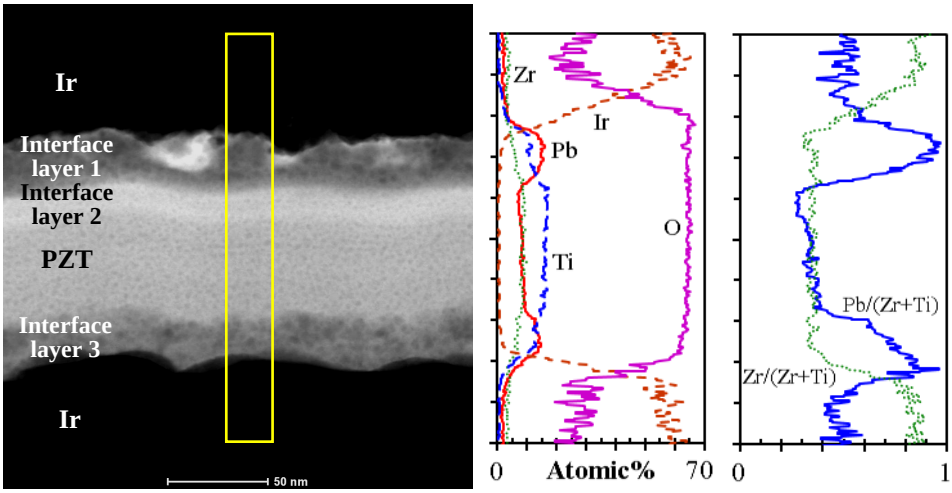


Figure 6.12 STEM cross section view of Ir/PZT/Ir stack and EDX line scan across PZT film in A–B region.

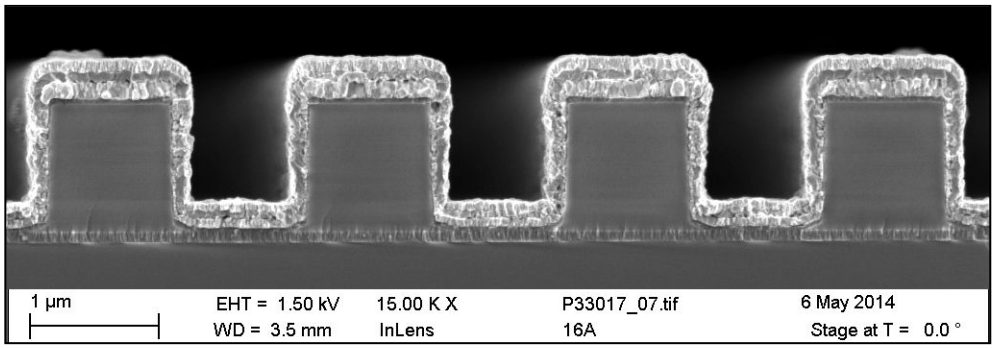
It is still unknown how these interface layers form. Because the interface layers are visible all over the 3D structures, they may have nothing to do with the 3D structures and probably can also be seen in 2D structures. According to the result of line scans across the

PZT films, this phenomenon seems to be a Pb accumulation in darker interface layers and a Pb depletion in the brighter interface layers. At the interface of PZT with the bottom Ir, it should be clarified whether the reaction rates of every element are constant during deposition. If these three precursors of PZT have different incubation times, an interface layer with a different composition can grow initially. At the interface of PZT with the top Ir, there may be another reason for the interface layers. A plasma damage may be one of the possible reasons. At the beginning of top Ir deposition the Ar plasma may perform a sputter etching effect on the PZT film. Such a sputter etching is usually selective depending on the elements. Therefore, the composition of PZT at the top surface is modified by the Ar plasma. Because the thickness of interface layer is about 20nm–30nm on each side, the influence of the interface layers on the ferroelectric properties may be very high and has to be taken into consideration.

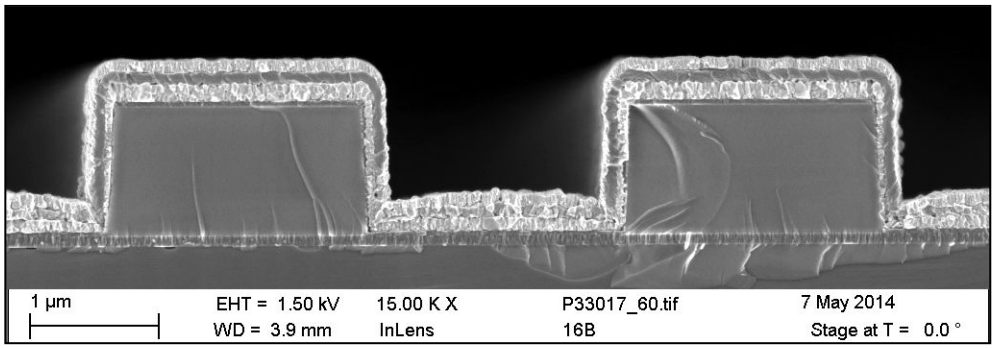
Generally speaking, no dependence of the PZT composition on the 3D profile can be found according to the results shown in **Figure 6.9** and **Figure 6.10**. The Pb composition is very non-uniform in the view of sub-micrometer dimensions. The ferroelectric capacitors in FeRAMs must have dimensions less than 0.5μm in order to compete with other memory devices. The non-uniformity may involve a large diversity of switching charges between memory cells resulting in function failures of FeRAMs.

6.3 Electrical Characterization of Three-Dimensional Ferroelectric Capacitors

As mentioned before, two kinds of 3D capacitors consisting of parallel trench line structures of width/distance/depth = 1μm/1μm/1μm and 2μm/2μm/1μm were used for electrical characterization. **Figure 6.13** shows their cross-sectional views under SEM. The capacitor area is determined by the area of the top electrode, which is deposited by e-beam evaporation through a shadow mask with many holes of various diameters ranging from 0.2 to 1.0mm. The type 3DA capacitors of width/distance/depth = 1μm/1μm/1μm have a 3D/2D area ratio of 2 and type 3DB capacitors of width/distance/depth = 2μm/2μm/1μm have a 3D/2D area ratio of 1.5.



(a) Type 3DA, width/distance/depth = 1µm/1µm/1µm



(b) Type 3DB, width/distance/depth = 2µm/2µm/1µm

Figure 6.13 SEM cross-sectional views of ferroelectric capacitors made of the Ir/PZT/Ir stack on 3D trench line structures.

Figure 6.14 shows typical P-V and J-V characteristics of 2D, 3DA and 3DB capacitors. The P and J values are converted according to the real capacitor areas. With suitable process conditions all 2D and 3D capacitors show ferroelectric properties. In general the 3D capacitors especially 3DA type have a higher leakage current than the 2D capacitors. Many 3D capacitors show even a short circuit. The hysteresis loop becomes fat and round because of the disturbance of leakage current. If leakage current is too high, it is difficult to monitor the ferroelectric property. Meyer et al. [6.11] have developed a method to extract the leakage current of ferroelectric capacitors by multiple measurements with different frequencies. This method was also used to analyze the leakage current in our ferroelectric capacitors. The leakage current in our ferroelectric capacitors consists of two main components. As the voltage increases from zero, the leakage current increases linearly with increasing voltage. This is the first component of the leakage current and is shown in **Figures 6.14(d)** and **(f)** as J_{L1}. After increasing the voltage beyond a threshold, the leakage current increases much faster. It looks like a breakdown but the capacitor does not really break down unless the voltage does exceed the threshold voltage too much. The component of fast

increasing leakage current beyond threshold voltage is shown in **Figures 6.14(d)** and **(f)** as J_{L2}. After the subtraction of leakage current, the P-V and J-V characteristics of 3DA and 3DB capacitors are shown as red dashed lines in **Figures 6.14(d)(e)(f)(g)**. The 3DA and 3DB capacitors show comparable remanent polarizations in comparison with 2D capacitors. That means, the sidewalls, bottoms of 3D structures seems to have comparable remanent polarizations with tops. But this result is based only on a few samples. More statistical investigations are necessary to confirm if 3D and 2D capacitors have the same ferroelectric properties.

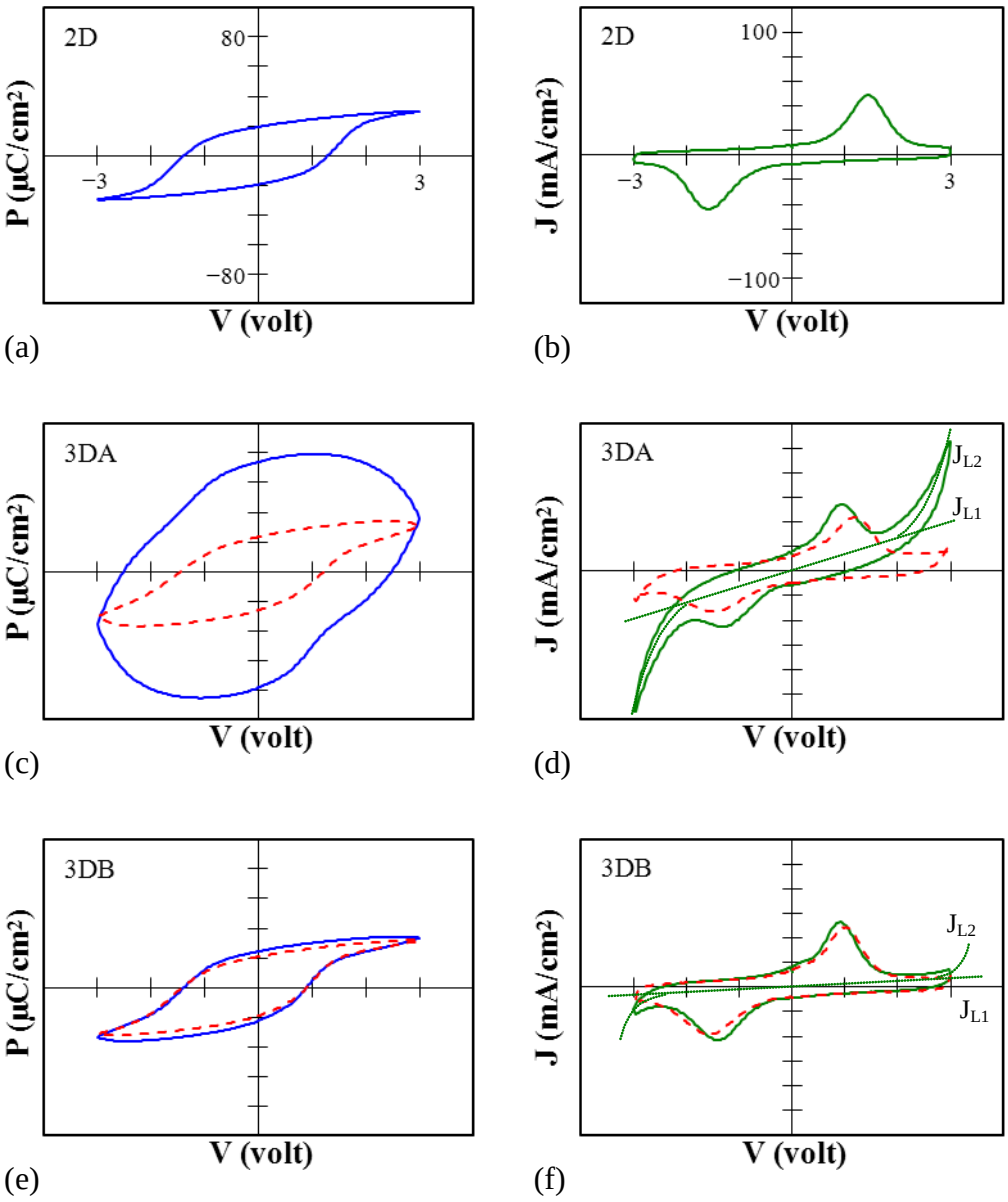


Figure 6.14 Hysteresis loops and current responses of 2D and 3D ferroelectric capacitors. (P, J values are converted according to real capacitor areas)

High leakage currents exist actually in our ferroelectric capacitors independent of their 2D or 3D structures. The leakage current level and the threshold voltage for J_{L2} vary in different ferroelectric capacitors and have a relation with PZT and top electrode deposition processes. Positive and negative threshold voltages are usually asymmetric. In 2D ferroelectric capacitors, good characteristics with low leakage current J_{L1} and high threshold voltage for J_{L2} have been obtained very often at selected process conditions. But in 3D ferroelectric capacitors the leakage current J_{L1} is often too high and the threshold voltage of J_{L2} is too low. Therefore, the capacitors have a rather high leakage current before reaching the voltage sufficient to switch the polarization. Hence a quantitative evaluation of 3D ferroelectric capacitors is very difficult.

The leakage currents of several typical 2D and 3D ferroelectric capacitors were measured and the results are shown in **Figure 6.15**. The leakage currents of the two 3DA capacitors are about three orders higher than those of the two 2D capacitors. One of the 3DB capacitors has the same leakage current level as 3DA capacitors and the other one has a leakage current level between 3DA and 2D capacitors. It is the general case in this work that the leakage current $I_{3DA} > I_{3DB} > I_{2D}$.

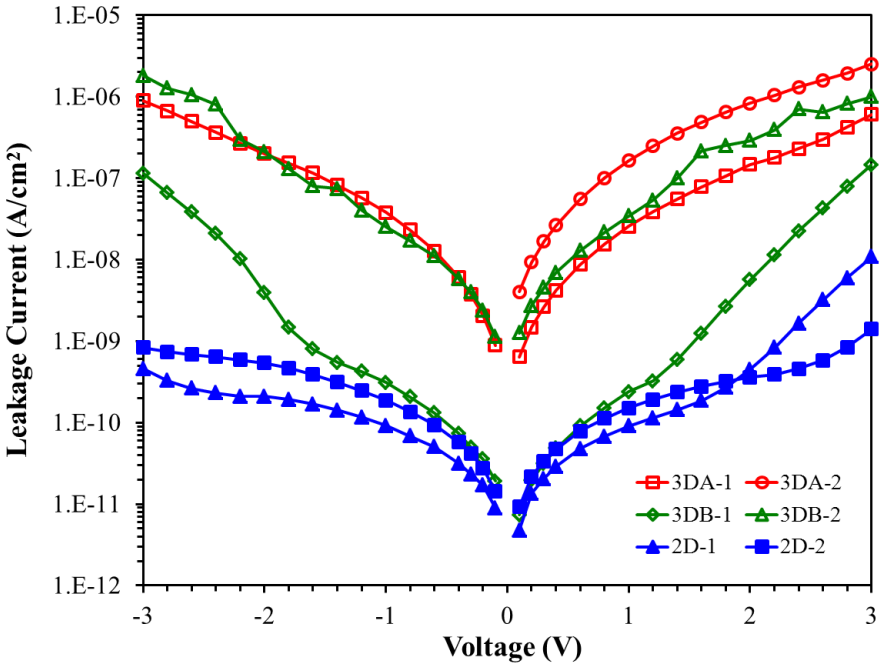


Figure 6.15 Leakage currents of 2D and 3D ferroelectric capacitors.

One possible reason is the PZT film thickness of the Ir/PZT/Ir capacitor stack on the sidewall and the bottom of the trench lines. According to the results shown in **Figure 6.4**, the PZT films on sidewalls and bottoms of the narrower trench lines are thinner than those of the wider trench lines. Thinner PZT films usually have higher leakage currents than thicker PZT films.

In addition, the mechanical stress between Ir, PZT and substrates is also suspected. Layer peeling of Ir/PZT/Ir stacks caused by high mechanical stress happened very often in the start-up period of this work. This problem caused high leakage currents and short-circuits of the capacitors. It was found that the deposition temperature of the e-beam evaporation process for Ir top electrodes played a very important role. Although the layer peeling problem was reduced by depositing the Ir top electrode at a higher temperature, it is believed that there still exists a high stress in the capacitor stacks. The geometric difference of the 3D/2D structures may cause accumulation of mechanical stress at certain sites of the capacitor stacks and results in more leakage current paths.

Although a high leakage current disturbs the 3D ferroelectric capacitors very much, some 3DB type capacitors have been found to be ferroelectric with a low leakage current. They were used for the cycling tests. **Figure 6.16** shows the degradation of the remanent polarization of three groups of 2D/3DB capacitors after cycling. The process conditions of different groups were different. The degradation of the remanent polarization between these groups differs severely. Group 1 started to fatigue only after 10^5 switching cycles and the remanent polarization decreased to less than 50% after 10^9 cycles. Group 2 could preserve the remanent polarization comparable to the initial value even after 10^9 cycles. The degradation of 2D and 3DB capacitors of the same group is similar. They have probably the same quality with respect to degradation of the remanent polarization. But there is a distinct difference between 3DB and 2D capacitors. During the cycling tests, leakage current jumps happened in two of the three 3DB capacitors. The leakage current decreased again after further cycling but one of the capacitor broke down after further cycling. Two of three tested 3DB capacitors broke down before finishing 10^9 switching cycles. This reveals that 3D capacitors tend to have failures caused by leakage current.

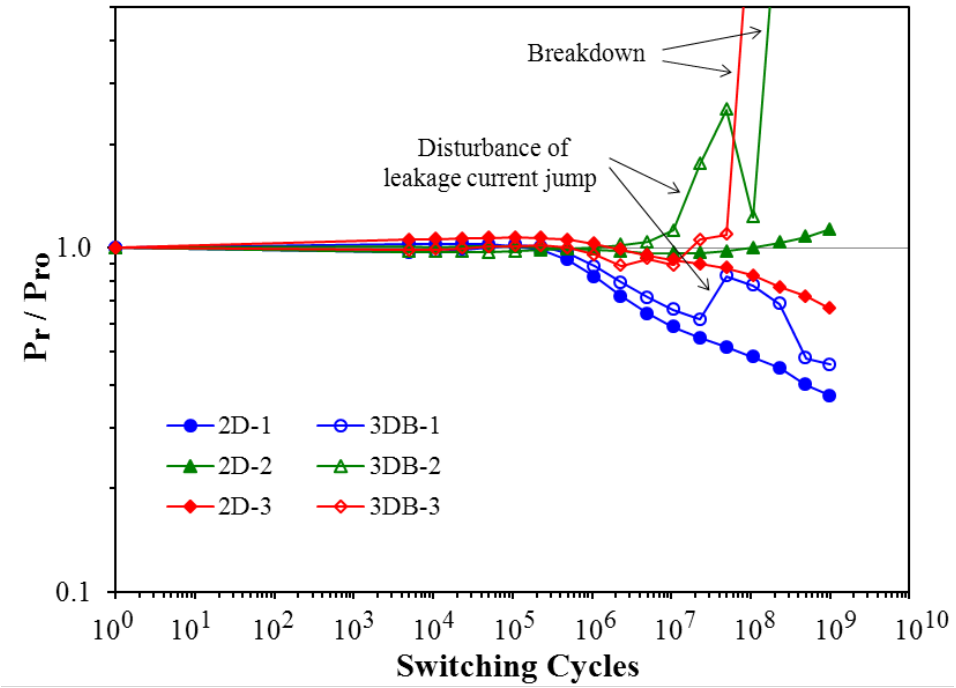


Figure 6.16 Degradation of remanent polarization vs. cycling.

6.4 Summary

The deposition of Ir/PZT/Ir ferroelectric capacitor stacks is investigated in this chapter. The step coverage of PZT films on trench holes of width/depth=0.6μm/1.0μm is about 0.4. For trench line structures with width/distance/depth from 0.7μm/0.7μm/1μm to 2μm/2μm/1μm, the step coverage of PZT films between 0.6 and 1 has been found. Phase separation, observed for 2D PZT deposition, has also been detected on 3D structures. No clear dependence of the crystallization of PZT on 3D profiles is found. STEM EDX line scans show a uniform Zr/(Zr+Ti) concentration ratio along the 3D profile but the Pb/(Zr+Ti) concentration ratio has a very large variation. Interface layers between PZT and top/bottom Ir layers are visible. EDX line scans across PZT films show large differences of Pb composition between middle regions of PZT films and interface layers. The PZT films appear to be not well crystalized but consists of many grains smaller than 10nm as revealed by TEM investigations. The grain size and its distribution seem to have a relation with the large variation of Pb composition in the PZT films.

3D ferroelectric capacitors have much higher leakage currents than 2D ferroelectric capacitors. Although the degradation of the remanent polarization between 2D and 3D capacitors is similar after 10^9 switching cycles, 3D ferroelectric capacitors tend to break down or to have leakage current jumps during cycling tests.

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7 Conclusions and Perspectives

The achievement in this thesis is listed below:

(1) A MOCVD PZT thin film deposition process with novel Zr and Ti precursors was developed on Ir substrates. The PZT films deposited at 450/500/550°C are ferroelectric and the films deposited at 500/550°C show good remanent polarization.

(2) Reactive ion etching of iridium with an Al mask and $CF_4/O_2/Ar$ gas mixtures was developed. Higher etch rates were achieved at elevated substrate temperatures. A high selectivity was obtained between iridium and the Al etching mask.

(3) An Ir thin film deposition process on 3D structures was developed using plasma enhanced MOCVD. Acceptable step coverage and surface morphology are achieved with sufficient quality for the application as electrodes of three-dimensional capacitor structures.

(4) Ir/PZT/Ir ferroelectric capacitor stacks on 3D structures were realized. The 3D capacitors show good ferroelectric properties comparable to 2D capacitors but have higher leakage currents than 2D capacitors and tend to fail during cycling tests.

After summarizing the results of this study, some conclusions can be drawn for the future work:

Although the PZT films deposited at 450°C are ferroelectric, their remanent polarizations are too low and need more improvement. Further reduction of the deposition temperature is still a benefit for better compatibility with the conventional CMOS process. Reduction of PZT film thickness below 50nm in 3D capacitors is necessary in order to compete with other memory devices. Non-uniform Pb contents, inhomogeneous microstructures and partially crystallized phases in PZT films can be deleterious to the ferroelectric properties. These are important issues to be solved before mass production.

A reactive ion etching process for Ir was developed in this study. Further investigations with Ir/PZT/Ir stacks are necessary to ensure its compatibility to PZT films. It is also worth to study Al_2O_3 thin films as hard mask for Ir etching with CF_4/O_2 gas mixtures.

Although the deposition technology of Ir thin films developed in this study is applicable to 3D ferroelectric capacitors, further improvements of step coverage are necessary. The deposition of Ir by ALD can be an alternative approach instead of MOCVD to achieve a better step coverage.

The reasons for high leakage currents of 3D ferroelectric capacitors as observed in this study need further detailed investigations. In addition, complex electrodes with conductive oxides such as $SrRuO_3$ and $LaNiO_3$ are inevitable against fatigue degradation. Conductive oxides should be integrated into 3D capacitor stacks as electrodes.

List of Abbreviations

AES	Auger electron spectroscopy
AFM	atomic force microscopy
ALD	atomic layer deposition
BFO	bismuth ferrite, $BiFeO_3$
BIT	bismuth titanate, $Bi_4Ti_3O_{12}$
BL	bit line
BLB	bit line bar
BLSF	bismuth layer structured ferroelectric
BLT	lanthanum-substituted bismuth titanate, $(Bi_{4-x}La_x)Ti_3O_{12}$
CD	compact disc
CMOS	complementary metal-oxide-semiconductor
CPU	central processing unit
CVD	chemical vapor deposition
DDR2	double-data-rate two
DRAM	dynamic random access memory
DVD	digital video disc, or digital versatile disc
EDX	dispersive X-ray spectroscopy
FeRAM	ferroelectric random access memory
FRAM	ferroelectric random access memory
ECR	electron cyclotron resonance
GST	GeSbTe, germanium-antimony-tellurium
IC	integrated circuit
Ir(EtCp)(1,5COD)	iridium(ethylcyclopentadienyl)(1,5-cyclooctadiene)
LNO	lanthanum nickel oxide, $LaNiO_3$
LSCO	lanthanum strontium cobalt oxide, $La_{(1-x)}Sr_xCoO_3$
mmp	1-methoxy-2-methyl-2-propoxy
MOCVD	metal organic chemical vapor deposition
MOS	metal-oxide-semiconductor
MPB	morphotropic phase boundary
MRAM	magnetic random access memory

MTJ	magnetic tunnel junction
NMOS	n-MOSFET, n-channel metal-oxide-semiconductor field-effect transistor
OiPr	isopropoxide
OtBu	tert-butoxide
PCRAM	phase change random access memory
PDA	personal digital assistant
PECVD	plasma enhanced chemical vapor deposition
PE-MOCVD	plasma enhanced metal organic chemical vapor deposition
PL	plate line
PMOS	p-MOSFET, p-channel metal-oxide-semiconductor field-effect transistor
PT	lead titanate, $PbTiO_3$
PZ	lead zirconate , $PbZrO_3$
PZT	lead zirconate titanate, $PbZr_xTi_{1-x}O_3$
RF	radio frequency
RIE	reactive ion etching
SAED	selected area electron diffraction
SBT	strontium bismuth tantalate, $SrBi_2Ta_2O_9$
SEM	scanning electron microscopy
SIMS	secondary ion mass spectroscopy
SRAM	static random access memory
SRO	strontium ruthenate, $SrRuO_3$
STEM	scanning transmission electron microscopy
STT-MRAM	spin-torque-transfer MRAM, or spin-transfer-torque MRAM
TDMAT	tetrakis(dimethylamido)titanium, $Ti[N(CH_3)_2]_4$
TEM	transmission electron microscopy
TGA	thermal gravimetric analysis
thd	2,2,6,6-tetramethyl-3,5-heptanedionato
TMR	tunnel magnetoresistance
WL	word line
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

List of Publications

1. C. P. Yeh, M. Lisker, V. Vezin, B. Seitzinger, P. K. Baumann, B. Garke, J. Bläsing, A. Krost, and E. P. Burte, *"Fabrication of Ferroelectric PZT Thin Films by Liquid Delivery MOCVD Using Novel Zr and Ti Precursors"*, Integrated Ferroelectrics, 2008, 104: 16–24

2. C.-P. Yeh, T. Grinys, M. Lisker, and E. P. Burte, *"Fabrication of Ferroelectric BLT Thin Films by Direct Liquid Injection MOCVD"*, Mater. Res. Soc. Symp. Proc., 2008, Vol. 1110, 1110-C03-20

3. M. Lisker, C. P. Yeh, S. Matichyn, and E. P. Burte, *"Deposition of PZT Thin Films on Three-Dimensional Trench Structures"*, Mater. Res. Soc. Symp. Proc., 2008, Vol. 1110, 1110-C03-22

4. Chia-Pin Yeh, Marco Lisker, Jürgen Bläsing, Oleksandr Khorkhordin, Bodo Kalkofen and Edmund P. Burte, *"Deposition of Iridium Thin Films on Three-Dimensional Structures with PE-MOCVD"*, Chemical Vapor Deposition, 2015, Vol. 21, Iss. 1-2-3, pp. 46–53

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