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Florian Wilhelmi: Gallium oxide (Ga_2O_3) Schottky diodes for power electronics

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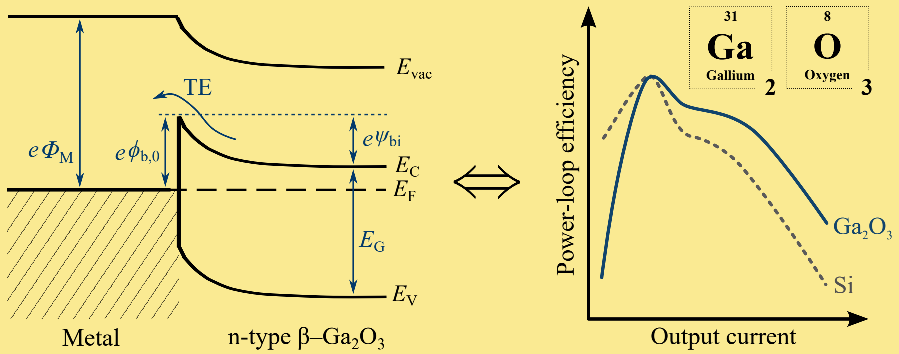
Florian Wilhelmi

On the characteristic electrical and thermal properties of beta-phase gallium oxide (β–Ga_2O_3) Schottky diodes in view of their potential application in power electronics



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Doktoringenieur

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Abstract

The semiconductor beta gallium oxide (β–Ga_2O_3) combines a 4.6–$4.9\,\mathrm{eV}$ wide band gap with the availability of melt-grown wafers and could help meet the growing demand for high-efficiency and low-cost power electronics. However, research still mostly focuses on basic device structures, and the low thermal conductivity raises concerns about potential thermal management problems. The objective of this work is to transition from fundamental device structure research to power electronics applications by experimentally and through simulation investigating the electrical and thermal characteristics of novel β–Ga_2O_3 diodes from a planned production line. A change of the conduction mechanism leading to an initial decrease and then increase of the conduction losses with rising temperature is observed for multiple but not all diodes. This seems to originate from the device processing rather than the intrinsic properties of β–Ga_2O_3. Despite a strong variation of the material properties between diodes of the same type, a lower increase in differential on-resistance with rising temperature is observed compared to silicon carbide (SiC) diodes, and measurements of the temperature-dependent ideality factors and Schottky barrier heights indicate stable junction properties. The heat dissipation in Ga_2O_3 diodes can be improved by thinning the currently $600\,\mu\mathrm{m}$ thick standard devices to thicknesses of $200\,\mu\mathrm{m}$. In contrast to SiC, however, cooling the devices from the junction side is found to be significantly more effective in reducing the junction temperature despite the smaller cooling area, if the entire anode area is covered with die-attach material. Combined with the potentially low conduction losses, it seems realistic for future Ga_2O_3 diodes to achieve similar junction temperatures as modern commercial SiC diodes at the same forward current. Even $600\,\mu\mathrm{m}$ thick diodes are successfully implemented in a $400\,\mathrm{V}$ buck converter operated at frequencies up to $350\,\mathrm{kHz}$. Peak voltage slew rates exceeding $100\,\mathrm{V/ns}$ are achieved, but in continuous operation the diodes exhibit a higher temperature rise than their SiC counterparts. Nevertheless, the efficiencies with a state-of-the-art silicon diode of similar size can be surpassed with the Ga_2O_3 diodes despite the still higher on-resistance, owing to the absence of recombination losses.

Zusammenfassung

Der Halbleiter beta-Galliumoxid (β–Ga_2O_3) vereint eine 4.6–$4.9\,\mathrm{eV}$ breite Bandlücke mit der Verfügbarkeit schmelzgewachsener Wafer und könnte dazu beitragen, den steigenden Bedarf an hocheffizienter und kostengünstiger Leistungselektronik zu decken. Jedoch konzentriert sich die Forschung derzeit noch hauptsächlich auf die grundlegenden Strukturen der Bauelemente. Außerdem weckt die geringe thermische Leitfähigkeit von Ga_2O_3 Bedenken hinsichtlich möglicher Probleme bei der Wärmeabfuhr. Ziel dieser Arbeit ist, einen Übergang von der bisherigen Forschung auf Bauelementestruktur-Ebene hin zur Anwendung in der Leistungselektronik zu schaffen, indem elektrische und thermische Eigenschaften neuartiger β–Ga_2O_3 Dioden aus einer geplanten Fertigungslinie experimentell und simulativ untersucht werden. Bei mehreren β–Ga_2O_3 Dioden ist eine Änderung des Leitmechanismus zu beobachten, die zu einer anfänglichen Abnahme und dann zu einem Anstieg der Leitungsverluste mit steigender Temperatur führt. Dies scheint jedoch auf die Herstellung der Chips zurückzuführen zu sein und nicht direkt auf die intrinsischen Eigenschaften von β–Ga_2O_3. Trotz einer starken Variation der Materialeigenschaften zwischen Dioden desselben Typs wird ein geringerer Anstieg des differentiellen Durchlasswiderstands mit steigender Temperatur im Vergleich zu Siliziumkarbid (SiC) Dioden beobachtet, und Messungen der temperaturabhängigen Idealitätsfaktoren und Schottky-Barrierenhöhen weisen auf stabile Sperrschicht- bzw. Grenzflächeneigenschaften hin. Die Entwärmung von Ga_2O_3 Dioden kann durch Abdünnen der derzeit $600\,\mu\mathrm{m}$ dicken Standardbauteile auf Dicken von $200\,\mu\mathrm{m}$ signifikant verbessert werden. Im Gegensatz zu SiC erweist sich jedoch die sperrschichtseitige Kühlung trotz der kleineren Kühlfläche als wesentlich effektiver bei der Senkung der Bauteiltemperatur, wenn die gesamte Anodenfläche mit Lot- bzw. Sinterpaste bedeckt ist. In Verbindung mit den potenziell geringen Leitungsverlusten scheint es realistisch, dass künftige Ga_2O_3 Dioden bei gleichem Durchlassstrom ähnliche Sperrschichttemperaturen erreichen wie moderne kommerzielle SiC Dioden. Selbst $600\,\mu\mathrm{m}$ dicke Dioden werden erfolgreich in einem $400\,\mathrm{V}$ Abwärtswandler eingesetzt, der bei Schaltfrequenzen von bis zu $350\,\mathrm{kHz}$ betrieben wird. Es werden maximale Anstiegsgeschwindigkeiten der Spannung von über $100\,\mathrm{V/ns}$ erreicht, aber im Dauerbetrieb weisen die Ga_2O_3 Dioden einen höheren Temperaturanstieg auf als die SiC Vergleichsbauteile. Dennoch können mit den Ga_2O_3 Freilaufdioden trotz des aktuell höheren Durchlasswiderstandes aufgrund der fehlenden Rekombinationsverluste die Effizienzen mit einer modernen Silizium-Diode ähnlicher Größe übertroffen werden.

Contents

Nomenclature

Acronyms and abbreviations

2DEG	**two**-**d**imendional **e**lectron **g**as
3D	**t**hree-**d**imensional
Ga_2O_3	**ga**llium **o**xide
AC	**a**lternating **c**urrent
Al_2O_3	**al**uminium **o**xide
AlN	**a**luminum **n**itride
B1...B4	**b**atch 1...**b**atch 4 of the studied diodes
C200	medium large **c**athode-side cooled 200 µm thin Ga_2O_3 die
C600	medium large **c**athode-side cooled 600 µm thin Ga_2O_3 die
C600LL	**l**argest **c**athode-side cooled 600 µm thin Ga_2O_3 die
CBL	**c**urrent **b**locking **l**ayer
CSC	**c**athode-**s**ide **c**ooled, **c**athode-**s**ide **c**ooling
CuMo	**c**opper **m**olybdenum
CVD	**c**hemical **v**apor **d**eposition
DC	**d**irect **c**urrent
DPC	**d**irect **p**lated **c**opper
EFG	**e**dge-defined **f**ilm-fed **g**rowth
FE	**f**ield **e**mission
FET	**f**ield-**e**ffect **t**ransistor
FOM	**f**igure **of** **m**erit
FP	**f**ield **p**late
GaN	**ga**llium **n**itride
GR	**g**uard **r**ing
HEMT	**h**igh-**e**lectron-**m**obility **t**ransistor
HfO_2	**h**afnium(IV) **o**xide
HV	**h**igh **v**oltage
HVPE	**h**alide **v**apor **p**hase **e**pitaxy
IGBT	**i**nsulated-**g**ate **b**ipolar **t**ransistor
J200	medium large **j**unction-side cooled 200 µm thin Ga_2O_3 die
JSC	**j**unction-**s**ide **c**ooled, **j**unction-**s**ide **c**ooling
L	second **l**argest anode size of the diodes under investigation
LL	**l**argest anode size of the diodes under investigation
MBE	**m**olecular **b**eam **e**pitaxy
ML	**m**edium **l**arge anode size of the diodes under investigation
MOCVD	**m**etal**o**rganic **c**hemical **v**apor **d**eposition

MOS	**m**etal–**o**xide–**s**emiconductor
MOSFET	**m**etal–**o**xide–**s**emiconductor **f**ield-**e**ffect **t**ransistor
MPS	**m**erged **P**iN **S**chottky
MS	**m**etal–**s**emiconductor
NiO	**ni**ckel **o**xide
PCB	**p**rinted **c**ircuit **b**oard
PFC	**p**ower **f**actor **c**orrection
PFE	**P**oole–**F**renkel **e**mission
PFOM	**p**ower **f**igure **o**f **m**erit
RMS	**r**oot **m**ean **s**quare
S377	cathode-side cooled $377\,\mu\mathrm{m}$ thin **S**iC reference die
SBD	**S**chottky **b**arrier **d**iode
Si	**si**licon
Si_3N_4	**si**licon **n**itride
SiC	**si**licon **c**arbide
SiO_2	**si**licon(IV) **o**xide
SMD	**s**urface-**m**ount **d**evice
SMT	**s**urface-**m**ount **t**echnology
TAT	**t**rap **a**ssisted **t**unneling
TE	**t**hermionic **e**mission
TEOS	**te**traeth**o**xy**s**ilane
TFE	**t**hermionic **f**ield **e**mission
TIM	**t**hermal **i**nterface **m**aterial
TSP	**t**emperature **s**ensitive **p**arameter
XS	smallest anode size of the diodes under investigation

Greek symbols

α	alpha polymorph of a semiconductor
α_{ref}	temperature coefficient of the differential on-resistance in relation to a certain reference temperature
α_{Z}	fitting variable to determine the junction-to-case thermal resistance
α_{300}	temperature coefficient of the differential on-resistance related to $300\,\mathrm{K}$
α_{373}	temperature coefficient of the differential on-resistance related to $373\,\mathrm{K}$
β	beta polymorph of a semiconductor
β_{Z}	fitting variable to determine the junction-to-case thermal resistance
Δ	change of a quantity
$\delta_{\mathrm{Z}}(Z_{\mathrm{th}})$	exponential trendline to determine the junction-to-case thermal resistance

ϵ_s	relative dielectric constant (low-frequency)	
ϵ_0	vacuum permittivity	$\mathrm{F/m}$
ϵ_∞	relative dielectric constant (high-frequency)	
η_p	power-loop efficiency	$\%$
λ_th	thermal conductivity	$\mathrm{W\,m^{-1}\,K^{-1}}$
μ_e	electron mobility	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
$\phi_\mathrm{b,0}$	Schottky barrier height	eV
$\phi_\mathrm{if,0}$	image force lowering	eV
Φ_M	work function of a metal	eV
ψ_bi	built-in potential	V
ρ	mass density	$\mathrm{kg/m^3}$
τ_i	time constant of the i-th component	s
ζ_fs	forward model shift parameter	
ζ_rb	reverse model bending parameter	
ζ_ri	reverse model inclination parameter	
ζ_rs	reverse model shift parameter	

Latin symbols

A	active area	$\mathrm{m^2}$
$A_\mathrm{ch,eff}$	effective chip size	$\mathrm{m^2}$
$a_\mathrm{i}(t)$	step-function response of the i-th component	
$a(t)$	step-function response	
A^{**}	Richardson constant	$\mathrm{A\,m^{-2}\,K^{-2}}$
B_i	bandwidth of the i-th measurement instrument	Hz
B_osci	bandwidth of an oscilloscope	Hz
C	capacitance	F
C_ds	drain–source capacitance	F
C_gd	gate–drain capacitance	F
C_gs	gate–source capacitance	F
C_j	junction capacitance of a diode	F
C_j0	junction capacitance of a diode at zero bias voltage	F
C_th	thermal capacitance	$\mathrm{W\,s/K}$
$C_\mathrm{th,i}$	thermal capacitance of the i-th component	$\mathrm{W\,s/K}$
c_th	specific heat capacity	$\mathrm{J\,kg^{-1}\,K^{-1}}$
D_1	diode	
E_br	critical electric field or breakdown field	$\mathrm{V/m}$
E_C	energy of the conduction band minimum	eV
$E_\mathrm{c,a}$	energy associated with the initial charging phase of the junction capacitance	J
$E_\mathrm{c,b}$	energy associated with the second charging phase of the junction capacitance	J

$E_{\mathrm{c,tot}}$	total capacitance energy associated with diode turn off	J
E_{F}	Fermi energy	eV
E_{off}	turn-off switching energy	J
$E_{\mathrm{Z}}(Z_{\mathrm{th}})$	linear trendline to determine the junction-to-case thermal resistance	
E_{on}	turn-on switching energy	J
E_{00}	characteristic tunneling energy	eV
E_{V}	energy of the valence band maximum	eV
γ_{T}	required drop of the on-resistance of Ga_2O_3 diodes below the SiC level	
I_{D}, i_{D}	current through a diode	A
$I_{\mathrm{D,ave}}$	average current through a diode	A
$i_{\mathrm{D,rm}}$	maximum reverse current during diode turn off	A
$I_{\mathrm{D,rms}}$	root-mean-square current through a diode	A
I_{f}	forward current	A
I_{L}	load current	A
I_{r}	reverse leakage current	A
$I_{\mathrm{r,TFE}}$	reverse thermionic-field emission current	A
I_{s}	saturation current	A
i_{s}	source current	A
J_0	reference current density	$\mathrm{A/m^2}$
$J_{\mathrm{r,TFE}}$	reverse thermionic-field emission current density	$\mathrm{A/m^2}$
J_{s}	saturation current density	$\mathrm{A/m^2}$
k	Boltzmann constant	$\mathrm{J/K}$
K_{bw}	measurement error due to bandwidth limitations	$\%$
L	inductance	H
$L_{\mathrm{p,loop}}$	parasitic commutation-loop inductance	H
m_{e}^*	electron effective mass	kg
m_{T}	slope of a linear fit of the transient temperature response	$\mathrm{K/s}$
$\mu_{\mathrm{e,sub}}$	electron mobility in the substrate	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
N_{C}	density of states in the conduction band	$\mathrm{m^{-3}}$
N_{D}	effective donor concentration	$\mathrm{m^{-3}}$
$N_{\mathrm{D,sub}}$	effective donor concentration in the substrate	$\mathrm{m^{-3}}$
n	ideality factor	
n_{if}	ideality factor with image force lowering	
n_{tun}	ideality factor with tunneling	
P_{cond}	conduction loss	W
P_{H}	heating power	W
h	Planck constant	$\mathrm{m^2\,kg/s}$
e	elementary charge	C
Q_{c}	capacitive charge	C

$Q_{\mathrm{c,a}}$	charge associated with the initial charging phase of the junction capacitance	C
$Q_{\mathrm{c,b}}$	charge associated with the second charging phase of the junction capacitance	C
$Q_{\mathrm{c,tot}}$	total capacitive charge associated with diode turn off	C
R	resistance	Ω
$\hbar$	reduced Planck constant	$\mathrm{m^2\,kg/s}$
$r_{\mathrm{epi,sp}}$	specific resistance of the epitaxial layer	$\Omega\,\mathrm{m}^2$
$R_{\mathrm{g,on}}$	external gate turn-on resistance	Ω
r_{o}	differential on-resistance	Ω
$r'_{\mathrm{o,sp}}$	fitted effective specific differential on-resistance	$\Omega\,\mathrm{m}^2$
$r_{\mathrm{o,sp}}$	specific differential on-resistance	$\Omega\,\mathrm{m}^2$
r_{sc}	ohmic resistance of a semiconductor layer	Ω
$r_{\mathrm{sub,sp}}$	specific resistance of the substrate	$\Omega\,\mathrm{m}^2$
R_{th}	thermal resistance	$\mathrm{K/W}$
$R_{\mathrm{th,die}}$	thermal resistance of the die	$\mathrm{K/W}$
$R_{\mathrm{th,i}}$	thermal resistance of the i-th component	$\mathrm{K/W}$
$R_{\mathrm{th,ja}}$	thermal resistance from junction to ambient	$\mathrm{K/W}$
$R_{\mathrm{th,jc}}$	thermal resistance from junction to case	$\mathrm{K/W}$
S_1, S_2	bidirectional switch	
T_{amb}	ambient temperature	K
$T_{\mathrm{a,exp}}$	experimentally determined rise time	s
$T_{\mathrm{a,sense,i}}$	inherent rise time of the i-th measurement instrument	s
$T_{\mathrm{a,true}}$	true impulse rise time of a signal	s
T_{epi}	temperature of the epitaxial layer	K
t	time	s
T_{j}	junction temperature	K
$T_{\mathrm{j,ave}}$	average junction temperature	K
$T_{\mathrm{j,max}}$	maximum junction temperature	K
$T_{\mathrm{j,min}}$	minimum junction temperature	K
T_{j0}	initial junction temperature	K
T_1	unidirectional switch	
T_{ref}	reference temperature	K
t_{ref}	reference time	$1\,\mathrm{s}$
V	voltage	V
V_{br}	breakdown voltage	V
V_{D}, v_{D}	voltage across a diode	V
V_{ds}	drain–source voltage	V
$V_{\mathrm{f@10mA}}$	forward voltage at a sensing current of $10\,\mathrm{mA}$	V
V_{gs}	gate–source voltage	V
V_0	knee voltage	V

V_0'	fitted effective knee voltage	V
V_{ref}	reference voltage	V
V_{th}	threshold voltage	V
z_{att}	thickness of the die-attach layer	m
z_{die}	thickness of the die	m
z_{epi}	thickness of the epitaxial layer	m
z_{sc}	thickness of a semiconductor layer	m
z_{sub}	thickness of the substrate of a die	m
Z_{th}	thermal impedance	K/W

Chapter 1

Introduction

1.1 Motivation and research goals

The demand for global electricity is expected to continuously grow from about $25\,000\,\mathrm{TWh}$ in the year 2021 to between $44\,000\,\mathrm{TWh}$ and $62\,000\,\mathrm{TWh}$ in the year 2050 [1]. The associated efficient transmission of electrical energy from the energy source to the consumer clearly determines daily life now and in the future. However, the electrical input quantities, such as current and voltage amplitude or frequency supplied by the source (e.g., a car battery), are generally different from the waveforms required at the electrical load (e.g., an electric motor). Power electronics concerns the corresponding transmission and conversion of electrical energy with the maximum possible efficiency. The underlying processes are based on semiconductor devices that can be switched either actively or passively between a conducting and a non-conducting state [2, 3].

While bipolar silicon (Si) semiconductor devices have been standard in all power electronics applications for years, recently power devices based on the wide-bandgap materials silicon carbide (SiC) and gallium nitride (GaN) have entered the market. Their wide bandgap and associated high breakdown fields allow the fabrication of unipolar high-voltage devices with lower on-resistances and switching losses than their Si counterparts [2–5]. This enables high switching frequencies and allows a reduction of the size and weight of passive components used to store the energy – a trend that is especially important also in the automotive industry [3, 4].

Vertical SiC power devices and modules up to several kV are commercially available already, and first SiC-based inverters have found their way into series production [3, 5, 6]. However, the growth of SiC wafers from the vapor phase is cost-intensive and hampers a widespread commercial implementation of SiC-based modules [5, 7, 8]. The less mature GaN technology, where the currently most promising devices are lateral GaN transistors grown on Si wafers, struggles to realize transistors with rated blocking voltages above $650\,\mathrm{V}$ [9, 10]. Nevertheless, it excels with fast switching transients and high switching frequencies at lower voltages [9, 10].

Recently, the transparent semiconductor gallium oxide (Ga_2O_3) has raised interest regarding a potential application in power electronics. While it occurs in different crystal structures, beta-phase gallium oxide (β–Ga_2O_3), which is the most stable of all polymorphs [11, 12], differs from Si, SiC, and GaN in that it combines two decisive properties: First, it exhibits an even wider bandgap than SiC or GaN, leading to a more than three times larger theoretical breakdown field than that of SiC [12]. Second, large β–Ga_2O_3 wafers can be grown from the melt using standard techniques such as the Czochralski method known from Si wafer technology [13–17]. As such, it holds potential for unipolar and vertical high-voltage power devices at a lower cost than comparable SiC devices [8, 12, 18].

Based on these properties, the on-resistance of a vertical $1.2\,\mathrm{kV}$ Ga_2O_3 transistor could theoretically be as low as one-tenth that of a SiC and about one-third that of a GaN counterpart [18]. At the same time, the charge × resistance figure of merit could theoretically be improved by a factor of 3 and 1.2 compared to SiC and GaN, respectively [18]. A Ga_2O_3 based $500\,\mathrm{kW}$ bi-directional charger was proposed in [19] through simulation and, from a purely electrical perspective, suspected to exceed the efficiencies of current SiC-based chargers by $3\,\%$ [19]. However, one major drawback of Ga_2O_3 that is often not considered in such studies is its low thermal conductivity – about one order of magnitude lower than that of SiC [12]. This limits heat dissipation and raises concerns about potential thermal management problems, but a “disproportionately small amount of work is addressing this sensitive issue” [8].

Today, the research into Ga_2O_3 substrate growth and device processing is steadily increasing [12]. The first research milestone was achieved in 2012 with the demonstration of a lateral Ga_2O_3 transistor cell grown on a native substrate [20]. Shortly after, in 2013, a vertical Ga_2O_3 Schottky diode was demonstrated [21]. Since then, research has intensified and the growth conditions and device structures have continuously improved. This resulted in another milestone in 2022, when first $6\,\mathrm{kV}$ and $8.3\,\mathrm{kV}$ vertical Ga_2O_3 diode cells on native substrates exceeding the theoretical unipolar on-resistance versus breakdown voltage limit of SiC were realized [22, 23]. However, the reported diodes are only several hundreds of micrometers large and thus still need to be scaled up to larger sizes. Furthermore, especially vertical transistors are significantly less developed although cells with several kV breakdown voltage have been developed already [24–26]. Hence, research still mainly focuses on the understanding and improvement of basic device structures.

One reason for this is that β–Ga_2O_3 cannot be p-doped and that it is highly anisotropic in its crystal structure and electrical and thermal properties [12, 27–29]. Therefore, intense research effort on a device level is still required. As a result, there are no established device concepts so far, power devices are not yet commercially available, and corresponding suitable packaging concepts are yet to be developed. In short: Ga_2O_3 power devices are still far from being integrable into real-world applications.

Taking this initial situation as a starting point, this work aims at building a bridge towards the use of Ga_2O_3 devices in power electronics. Although not yet commercially available, here the very first large-area Ga_2O_3 diodes from a planned manufacturing line are available for research of their basic properties and development towards potential applications. Through various electrical and thermal measurements, simulations, and theoretical considerations, the work addresses basic questions such as: What are characteristic similarities and differences between these novel Ga_2O_3 and commercial SiC diodes? Is the device quality sufficient to take the next steps towards an application in power electronics? Is an implementation in fast-switching power converters feasible despite the low thermal conductivity? What are the difficulties and potential methods to improve the application-relevant properties? By gradually examining the basic properties of novel large-area Ga_2O_3 diodes in an application-oriented manner, this thesis contributes to paving the way to Ga_2O_3 power electronics.

1.2 Structure of this thesis

In order to successively address the previously motivated research questions, the thesis is organized as follows:

Chapter 2 briefly introduces the basic concepts of power electronics, including the most important topologies and established semiconductor power devices. This forms the basis for understanding the theoretical advantages of β–Ga_2O_3 as a power semiconductor. Finally, the material properties of Ga_2O_3 are explained in more detail, and an overview of current state-of-the-art device structures and achievements is given. From this, the current research gaps are identified, and more detailed guiding questions are derived.

Chapter 3 covers the experimental methods used in this work. First, the packaging procedure of the devices under investigation is explained. Furthermore, the basic electric and thermal measurement techniques are introduced, and the associated measurement uncertainties are discussed. Since Ga_2O_3 devices are expected to exhibit fast-switching capabilities, it is crucial to capture the associated waveforms accurately. Therefore, novel current sensors are assessed and comparatively evaluated to find the most suitable sensors for further tests.

Before novel Ga_2O_3 devices can be tested in an application environment, their fundamental characteristics must be examined. **Chapter 4** therefore first studies the basic temperature-dependent electrical characteristics and junction properties that, as will be shown, can differ significantly from those of standard SiC diodes. Furthermore, the variation of characteristic device properties due to the early development stage is discussed, and Spice simulation models that allow a simple but effective replication of these characteristics are introduced.

After having gained insight into the basic properties, the heat dissipation in Ga_2O_3 diodes, which is identified as one of the major limitations, is studied in more detail in **Chapter 5**. The effectiveness of different thermal management strategies, such as substrate thinning, cooling from the junction-side, or the use of underfill materials, is studied experimentally and simulatively. In view of the potentially low on-resistance of Ga_2O_3 devices, it is discussed if junction temperatures similar to those of SiC counterparts can realistically be achieved in the future despite the low thermal conductivity.

Chapter 6 uses the newest generations of Ga_2O_3 diodes to assess their switching properties in an application-oriented environment. To this end, the samples are subjected to double pulse tests and, for the first time, also studied in a $400\,\mathrm{V}$ buck converter application. The switching waveforms, power-loop efficiencies, and thermal behavior are compared to that of Si and SiC reference diodes and connected to the findings of the previous chapters.

Chapter 7 summarizes key findings of this work and provides a brief outlook on potential future research activities.

Note that several results obtained as a part of this work have been published previously in [253–260]. Furthermore, the student work [249–252] has been supervised by the author during the course of this thesis.

Chapter 2

Basics and state-of-the-art of gallium oxide power electronics

2.1 Chapter overview

This chapter summarizes the state-of-the-art of Ga_2O_3 power electronics. Section 2.2 briefly introduces the general principles of power electronics, including the buck converter as a central topology and a basic overview of the structure of common commercialized semiconductor power devices. Section 2.3 then introduces Ga_2O_3 as a material for power electronics. Section 2.3.1 first motivates the use of Ga_2O_3 by comparing basic figures of merit of different power semiconductors. Building on this, Section 2.3.2 describes the most important structural, electrical, and thermal properties and challenges of gallium oxide in more detail. Section 2.3.3 discusses the different methods to grow β–Ga_2O_3 bulk crystals and high-quality epitaxial layers. These methods enable the fabrication of Ga_2O_3 power devices, whose structures and current state of research are covered in Section 2.3.4 (diodes) and Section 2.3.5 (transistors). Section 2.4 summarizes key aspects and formulates the corresponding research questions.

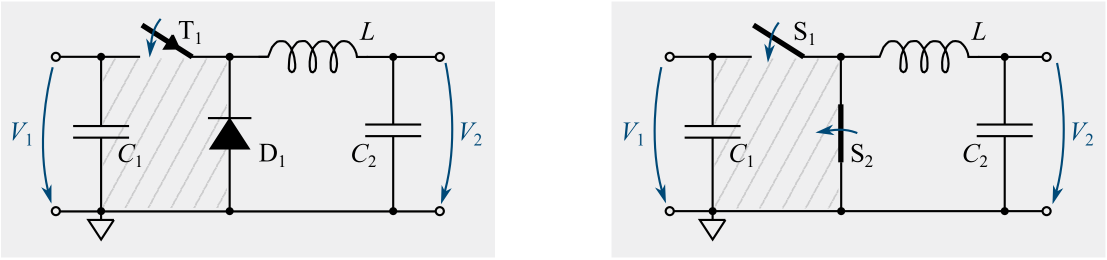
2.2 Basics of power electronics

2.2.1 Basic principles of power conversion

The buck converter topology shown in Fig. 2.1a is a central element that can be found in various types of power converters. In its simplest form, it consists of a unidirectional active switch T_1 that can be periodically opened and closed through a control circuit, a diode D_1, and an inductance L [30].

D_1 blocks the current in the reverse direction but provides a freewheeling path when T_1 is open, and the magnetized inductance L acts as a current source. By controlling the ratio of the switch-on and switch-off time, the so-called duty cycle, the input voltage V_1 is consequently stepped down to a voltage $V_2 \leq V_1$ at the output. The input capacitance C_1 decouples the circuit from the input voltage supply and the output capacitance C_2 can be added to stabilize the output waveforms [30].

When T_1 and D_1 are replaced by two bidirectional switches S_1 and S_2 as shown in Fig. 2.1b (either by combining a unidirectional switch and an antiparallel diode, or by using intrinsically bidirectional switches), stepping up the voltage in the opposite direction is also possible. First, the voltage source V_2 magnetizes the inductance L when S_2 is closed. When opening S_2 and closing S_1, the stored energy is transferred to the capacitor C_1, leading to an output voltage $V_1 > V_2$. The resulting topology is called a half bridge [30].



(a) (b)

Figure 2.1: (a) The buck converter in its simplest form consists of a unidirectional switch T_1, a diode D_1, and an inductance L. (b) When T_1 and D_1 are replaced by two bidirectional switches S_1 and S_2, a half-bridge topology is obtained. Based on [30].

The current commutates between the different switches with a high frequency of typically several kHz to several hundreds of kHz. The corresponding current loop, the so-called commutation loop, is shaded in Fig. 2.1. In reality, parasitic inductances that exist in this loop (e.g., caused by the current traces, package leads, or bond wires) can lead to strong oscillations or voltage and current overshoots and limit the commutation speed. The commutation-loop inductance must therefore be kept as low as possible [31].

Generally, increasing the switching frequency is targeted as it translates to a smaller amount of energy that needs to be stored in the passive components per cycle, thus enabling to use smaller and lighter inductances and capacitors. In reality, however, the switching frequency is limited. The main reason (apart from additional losses such as core losses in the passive components) is that real semiconductor devices exhibit switching losses and generate heat during switching events [30, 31]. The basic properties of these semiconductor devices will be covered in the following section.

2.2.2 Semiconductor power devices

Power diodes

One of the most common diode structures found in power electronics is the bipolar silicon PiN diode shown in Fig. 2.2a. It consists of a lightly (n^-) doped drift region that is surrounded by a p-region and a heavily doped n^+-region. The p-region and n^+-region are metallized to allow an electrical connection to the circuit and constitute the anode and cathode of the device [32].

In forward direction, when the anode potential is higher than the cathode potential (defined as $V_D > 0\,V$ in the following), the lightly doped drift region is flooded by charge carriers from the outer zones. Consequently, both holes and electrons contribute to the current flow that can be described by the Shockley equation [32, 33]. In blocking direction ($V_D < 0\,V$), the drift region is depleted from charge carriers and only a small leakage current (typically in the order of µA at the specified reverse voltage) flows in reverse direction [32].

The strength of the electric field that is built up in the drift zone increases with rising reverse voltage. At a certain reverse voltage, the so-called breakdown voltage V_{br}, the electric field is strong enough to accelerate charge carriers to such an extent that they can create new electron–hole pairs by impact ionization, which themself gain enough kinetic energy to create additional electron–hole pairs. This process is called avalanche multiplication or avalanche breakdown. The critical field strength E_{br} at which this happens is one of the most important parameters for semiconductor devices [32].

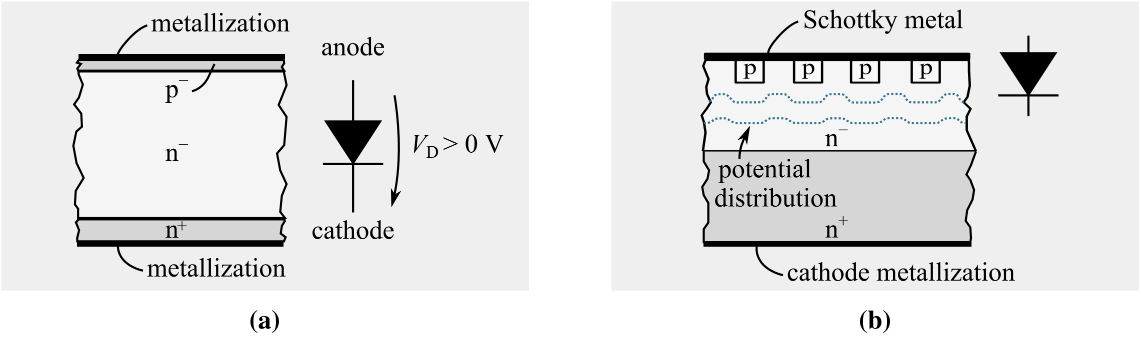


Figure 2.2: Schematic structure of (a) a bipolar PiN diode and (b) a merged PiN Schottky (MPS) diode composed of a Schottky junction with merged p-areas to improve the blocking characteristics and the surge-current capability. Based on [32, 34].

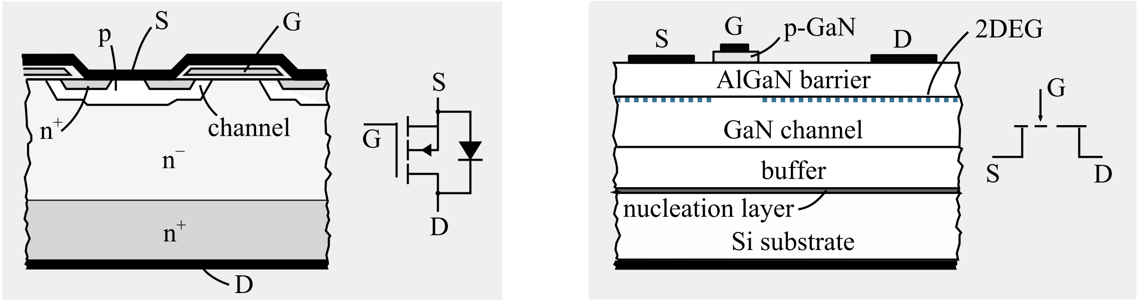
Wide-bandgap semiconductors such as SiC, GaN, or Ga_2O_3 exhibit a significantly higher critical electric field than Si (see Section 2.3.1). This allows the thickness of the drift zone to be reduced and the doping concentration to be increased, which reduces the differential on-resistance at a given breakdown voltage. In addition, purely unipolar diodes with a direct metal–semiconductor (MS) contact, also called Schottky contact, become available for high blocking voltages [34].

A substantial advantage of such unipolar devices is apparent when the device is turned off, i.e., switched from the forward to the blocking state. The charge removal and recombination of minority carriers in the case of bipolar diodes causes a high reverse current before the full blocking state is reached. This reverse current and the associated reverse recovery charge lead to power losses that increase significantly with rising current, current slope, and temperature. In the case of unipolar diodes, however, only majority carriers are involved in the charge transport. Therefore, only their removal is necessary to build up a blocking voltage in the drift region, which is associated with a certain displacement current. This process is temperature-independent and causes negligible power losses in the diode, making unipolar devices favorable for fast-switching applications [34].

Commercial Schottky diodes for high-voltage applications are typically made from SiC. One of the most common structures is the merged PiN Schottky (MPS) diode shown in Fig. 2.2b. Instead of a pure MS contact it consists of additional p-type areas distributed across the entire junction area. The exact diode properties depend critically on the density and doping level of these merged p-regions. Generally speaking, the structure can bring two main improvements: In blocking direction, the p-areas can effectively shield the Schottky junction from high electric fields. The reduced electric field lowers the reverse leakage current and prevents premature breakdown close to the junction [34–36]. In forward direction, the p-areas can be activated and inject holes at sufficiently large forward voltages above the normal operation area. This effect can reduce the resistance and improve the surge-current capability significantly [34, 37]. Both Si PiN diodes and SiC Schottky diodes are used as benchmarks throughout this thesis.

Power transistors

The metal–oxide–semiconductor field-effect transistor (MOSFET) is a voltage-controlled switch that is either normally-off (enhancement mode) or normally-on (depletion mode) when no control voltage is applied [38]. In power electronics, normally-off MOSFETs are preferred and will also be used in this thesis as active switches.



(a) **(b)**

Figure 2.3: Basic structure and circuit symbol of (a) a vertical n-channel power MOSFET and (b) a lateral GaN HEMT with p-GaN gate to achieve enhancement-mode operation. Based on [38, 39].

As shown in Fig. 2.3, the drift region of the MOSFET is typically formed by a lightly n-doped epitaxial layer grown on a heavily n-doped substrate. It blocks the entire voltage when the MOSFET is turned off and a positive voltage is applied between drain and source ($V_{ds} > 0$). The source contact is formed by a metallized heavily doped n-region that is surrounded by a p-area. To avoid a turn-on of the resultant parasitic npn-transistor, the p-area is also connected to the source metallization. The gate, usually heavily doped poly-silicon, is electrically insulated from the source pad and the drift region by a thin oxide layer such as SiO_2. When the gate–source voltage V_{gs} is larger than a certain threshold voltage V_{th} ($V_{gs} > V_{th} > 0\,V$ for normally-off transistors), an inversion layer with an accumulation of electrons is created in the p-type area below the gate. A forward current can now flow through this n-channel when a drain-source voltage $V_{ds} > 0\,V$ is applied. A parasitic diode, the so-called body diode, is formed between the p-area, the n^- drift layer, and the n^+ substrate. When the MOSFET is reverse biased ($V_{ds} < 0\,V$), the diode is forward biased and can thus serve as an internal freewheeling diode [38].

An improvement of the MOSFET technology was achieved by moving from planar structures to trench designs. In SiC MOSFETs, e.g., the gate is often formed at a trench that is etched into the lightly doped drift region between the source contacts [38, 40]. This structure offers an improved channel mobility, which reduces the on-resistance. In addition, a higher number of trench gates can be formed in a given area in comparison to the planar gate structure, which increases the current density [38, 40]. For other commonly used power devices such as insulated-gate-bipolar transistors (IGBTs), where the n^+ layer at the drain side is basically replaced by a p-type layer that can inject holes into the drift region, it is referred to [41] for more details as they will not be used in this work.

The device structures are associated with parasitic internal capacitances that have to be charged and discharged during the switching events. These are the gate–source capacitance C_{gs}, the gate–drain capacitance C_{gd}, and the drain–source capacitance C_{ds}. Minimizing these capacitances is crucial to enable fast switching [41]. SiC power MOSFETs will be used in this thesis to build a hybrid buck converter with Ga_2O_3 Schottky diodes in Chapter 6.

HEMT

Transistors based on the wide-bandgap semiconductor gallium nitride (GaN) have recently been commercialized. A thorough technology review can be found in [39]. As shown in Fig. 2.3b, a low-cost Si wafer typically provides the basis for the following fabrication steps.

First, a heteroepitaxial AlN nucleation layer is grown on the substrate, which mainly prevents the diffusion of gallium into the wafer. To avoid excessive mechanical strain resulting from the difference in lattice parameters and thermal expansion between Si and GaN, several $Al_xGa_{(1\text{-}x)}N$ buffer layers are grown on the nucleation layer. The central part of the device is formed at the interface between a GaN/AlGaN heterostructure. Strong polarization and piezoelectric effects at the interface associated with a strong bending of the conduction band below the Fermi level lead to the formation of a two-dimensional electron gas (2DEG). This enables a lateral current flow with high carrier mobility, which is why the device is called a high-electron-mobility transistor (HEMT). As a consequence, the device is inherently normally-on. Several methods exist to create an enhancement-mode operation. The GaN HEMTs that will be used in this thesis have a p-GaN or p-AlGaN gate structure. The p-layer increases the channel potential below the gate and depletes it from charge carriers at zero bias voltage. Other common ways to achieve normally-off behavior are cascode structures with normally-off Si MOSFETs [42], a recessed gate metal–insulator–semiconductor structure to interrupt the 2DEG [43], or HEMTs with fluorine implanted AlGaN layer [44].

Due to the symmetrical structure, the GaN HEMT can conduct current both in forward and reverse direction, if the potential at the gate in relation to drain or source is high enough. Compared to power MOSFETs, the parasitic capacitances C_{gs}, C_{gd}, and C_{ds} are significantly smaller. Combined with the high electron mobility, this enables faster switching transients [39]. Therefore, GaN HEMTs will be used to study new high-bandwidth current sensor concepts in Section 3.4. Due to the lateral structure, however, it is difficult to achieve voltage ratings above $650\,\mathrm{V}$ [39].

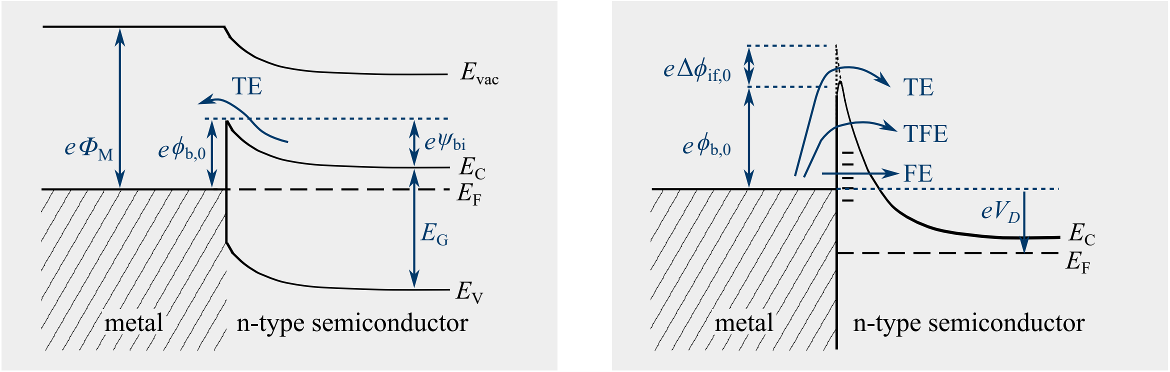
2.2.3 Physical basics of Schottky diodes

Figure 2.4a shows the band structure of a Schottky contact with an n-type semiconductor, which is the central part of the diodes studied in this work. In thermal equilibrium, when the gradient in the electrochemical potential is zero, the conduction band at the metal–semiconductor (MS) junction bends upwards and a region that is depleted from charge carriers is formed. The energy difference between the conduction band minimum E_{C} and the Fermi energy E_{F} at the junction is called Schottky barrier height $\phi_{\mathrm{b,0}}$. It depends critically on the band-gap energy E_{G} and doping concentration N_{D} of the semiconductor, the work function Φ_{M} of the metal, and defect states at the interface. The bending in the conduction band is described by the built-in potential ψ_{bi} [45].

The thermionic emission (TE) model is widely used to describe the current flow in forward direction for Si Schottky diodes [45], but also for MS contacts with wide-bandgap semiconductors such as SiC [46, 47], GaN [48], or Ga_2O_3 [21]. From the Fermi-Dirac statistics it follows that for temperatures above $0\,\mathrm{K}$ there will always be a number of electrons above the Schottky barrier giving rise to a saturation current I_{s} and the associated current density [45]

$$J_{\mathrm{s}} = \frac{4\pi e m_{\mathrm{e}}^{*} k^2}{h^3} \cdot T_{\mathrm{j}}^{2} \exp\left(-\frac{e\phi_{\mathrm{b,0}}}{kT_{\mathrm{j}}}\right) = A^{**} \cdot T_{\mathrm{j}}^{2} \exp\left(-\frac{e\phi_{\mathrm{b,0}}}{kT_{\mathrm{j}}}\right) \tag{2.1}$$

with e the elementary charge, k the Boltzmann constant, h the Planck constant, m_{e}^{*} the effective electron mass, T_{j} the junction temperature, and A^{**} the Richardson constant. When the external voltage is increased (potential at Schottky metal positive in relation to potential at semiconductor), the electrons gain additional energy and a current with the current density [45]



(a) **(b)**

Figure 2.4: Band structure of a Schottky contact in (a) thermal equilibrium and (b) when a reverse voltage is applied. The forward current can often be described by the thermionic emission (TE) model. In reverse direction, different conduction mechanisms such as thermionic-field emission (TFE), field emission (FE), or a combination of different processes can dominate depending on the semiconductor properties. Based on [45].

$$J_{\mathrm{D}} = J_{\mathrm{s}} \left[\exp\left(\frac{eV_{\mathrm{D}}}{nkT_{\mathrm{j}}} \right) - 1 \right] \tag{2.2}$$

can flow in forward direction. The dimensionless ideality coefficient n is 1 for an ideal diode and > 1 when tunneling and recombination processes are present at the junction. Equation 2.2 holds true only for low currents when the series resistance of the diode can be neglected. The series resistance is given by the sum of contact resistances the resistances of the auxiliary parts (bondwires, contact resistance, etc.), the ohmic contact, the substrate, and the drift zone, i.e., the epitaxial layer [31, 34]. The resistance of a semiconductor layer with thickness z_{sc} can be calculated directly from its electron mobility μ_{e}, effective doping concentration N_{D}, and current-conducting area A according to [34]

$$r_{\mathrm{sc}} = \frac{z_{\mathrm{sc}}}{e\mu_{\mathrm{e}}N_{\mathrm{D}}A}. \tag{2.3}$$

The substrate is usually heavily doped, leading to a rather small specific resistance. It can be reduced, e.g., by using thinner substrates and improving the electron mobility at high doping levels. The resistance of the lightly doped drift layer usually makes up the major part of the device resistance. As the drift layer is responsible for blocking the voltage during reverse operation, it needs to have a minimum thickness of $z_{\mathrm{epi}} = 2V_{\mathrm{br}}/E_{\mathrm{br}}$ when a triangular field is assumed. Materials with high E_{br} such as Ga_2O_3 thus allow the reduction of the drift layer thickness and a reduction of the specific differential on-resistance $r_{\mathrm{o,sp}}$ for a given breakdown voltage [34].

In reverse direction, the drift zone is depleted from charge carriers. With rising reverse voltage, the depletion region extends further into the drift layer, giving rise to a space charge Q_{c} and an associated parasitic junction capacitance [49]

$$C_{\mathrm{j}}(V_{\mathrm{D}}) = \frac{\partial Q_{\mathrm{c}}}{\partial V_{\mathrm{D}}} = A\sqrt{\frac{e\epsilon_0\epsilon_{\mathrm{s}}N_{\mathrm{D}}}{2(\psi_{\mathrm{bi}} - V_{\mathrm{D}})}}\,, \tag{2.4}$$

where ϵ_0 is the vacuum permittivity and ϵ_s is the relative dielectric constant of the semiconductor. This parasitic junction capacitance is (dis-)charged during every switching event in a converter operation. Despite the absence of bipolar recombination this results in a non-negligible current undershoot during diode turn-off [34].

In blocking direction, high electric fields can occur at the Schottky junction. This can lead to a substantial image force lowering $\Delta\phi_\mathrm{if,0}$ of the Schottky barrier, and the (at least partial) tunneling of charge carriers through the barrier can become increasingly dominant [45]. This is shown schematically in Fig. 2.4b. Here, field emission (FE) is a pure tunneling process of charge carriers through the Schottky barrier, which can occur especially at very high doping concentrations. Thermionic-field emission (TFE) describes the tunneling of thermally excited electrons through the barrier, which appears thinner at higher energies [45]. This theory has been found to accurately describe the reverse conduction mechanism of many MS contacts, including wide-bandgap semiconductors such as SiC [50], GaN [51], and $\mathrm{Ga_2O_3}$ [52]. Often, however, especially defects and traps at the interfaces can lead to a variety and even combination of different conduction mechanisms, such as Poole–Frenkel emission (PFE), i.e., the thermal emission of electrons trapped at the MS interface into the conduction band [53, 54], or the tunneling of electrons through trap states at the MS interface, called trap-assisted tunneling (TAT) [53, 55]. Both conduction mechanisms have been identified previously in wide-bandgap devices such as GaN [56] or $\mathrm{Al_x(Ga_{1-x})_2O_3}$ [57] diodes. Clearly, the properties of the semiconductor and the MS interface critically determine the behavior of the resulting power devices. The following section will therefore cover the material properties of $\mathrm{Ga_2O_3}$ and the related power devices in more detail.

2.3 Gallium oxide as power semiconductor

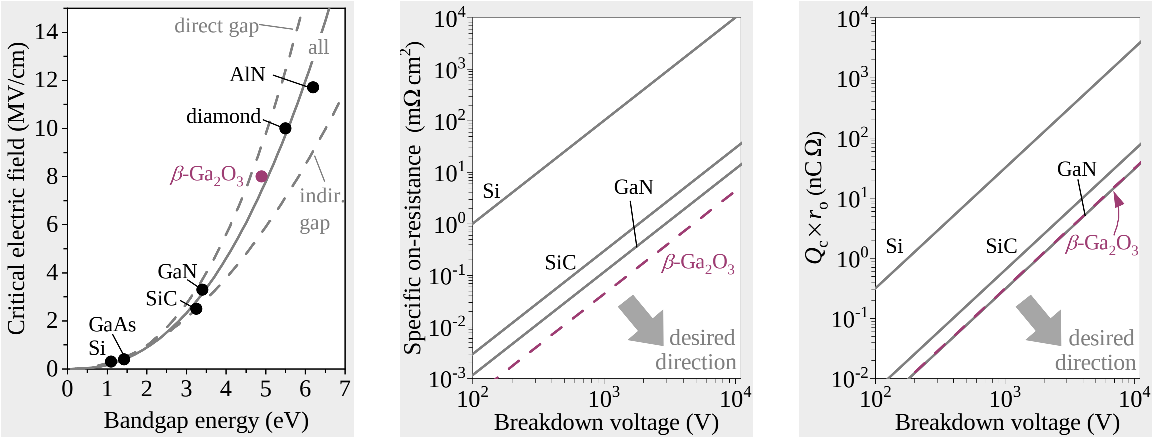
Gallium oxide is a transparent oxide semiconductor with five different known modifications of the crystal structure. These five polymorphs (or phases), designated as α–, β–, γ–, δ–, and ϵ–$\mathrm{Ga_2O_3}$ differ in mechanical, electronic, and optical properties. The most important polymorphs regarding an application in power electronics are β–$\mathrm{Ga_2O_3}$ and α–$\mathrm{Ga_2O_3}$. Relevant material properties are discussed in the following.

2.3.1 Important figures of merit

As explained in Section 2.2.3, the band-gap energy E_G and the associated critical electric field strength E_br belong to the essential material parameters for power semiconductor devices. The critical electric field can empirically be expressed directly as a function of the bandgap energy according to [58]. Figure 2.5a shows this relationship for semiconductors with direct and indirect bandgap, as well as the generalized relationship for all semiconductors. β–$\mathrm{Ga_2O_3}$ can be considered as a material with a quasi-direct bandgap of about $4.8\,\mathrm{eV}$ leading to a theoretical critical electric field of about $8\,\mathrm{MV/cm}$, which compares to $2.5\,\mathrm{MV/cm}$ for 4H-SiC and $3.3\,\mathrm{MV/cm}$ for GaN [12]. In the unipolar limit, the specific resistance of the drift layer with thickness z_epi can be calculated from [45]

$$r_\mathrm{o,sp} = \frac{z_\mathrm{epi}}{e\mu_\mathrm{e}N_\mathrm{D}\,A} = \frac{4{V_\mathrm{br}}^2}{\epsilon_0\epsilon_\mathrm{s}\mu_\mathrm{e}{E_\mathrm{br}}^3}\,, \tag{2.5}$$

where $N_\mathrm{D} = \epsilon_0\epsilon_\mathrm{s}{E_\mathrm{br}}^2/(2eV_\mathrm{br})$ is the maximum allowed doping concentration necessary to achieve the breakdown voltage V_br. Note that $r_\mathrm{o,sp}$ scales inversely with the third power of



(a) **(b)** **(c)**

Figure 2.5: (a) Based on the relationship between bandgap energy and critical electric field E_{br} for semiconductors with direct or indirect band gap, a high E_{br} of about $8\,\mathrm{MV/cm}$ is typically assumed for Ga_2O_3. In the unipolar limit, this theoretically leads to (b) a specific on-resistance of one-seventh of that of SiC and (b) a charge × resistance FOM similar to that of GaN. Based on [20, 34, 58] and Tab. A.1.

E_{br}. Critical other material parameters are the electron mobility and the relative dielectric constant of the semiconductor, which are summarized in Tab. A.1. Note that Eq. 2.5 does not consider the electric field dependence of μ_{e}, the dependence of E_{br} on N_{D}, temperature dependences, or more practical concerns such as necessary junction terminations and current spreading or crowding [34, 59]. Bearing this in mind, Fig. 2.5b illustrates that the $r_{\mathrm{o,sp}}$ of Ga_2O_3 devices can potentially be as low as a seventh of the $r_{\mathrm{o,sp}}$ of SiC, and almost one-third of the $r_{\mathrm{o,sp}}$ of GaN. A deeper physical comparison deviating from this rather generalized view was carried out in [60]. By analyzing the impact-ionization coefficients and dielectric properties of different semiconductors, it was shown that a wide bandgap does not necessarily result in a in a high critical electric field and breakdown voltage. Regarding Si, SiC, GaN, and Ga_2O_3, however, the same trend as shown in Fig. 2.5b was found [60]. The ratio ${V_{\mathrm{br}}}^2/r_{\mathrm{o,sp}}$ will be referred to as power figure-of-merit (PFOM) in the following.

As discussed in Section 2.2.3, the charge Q_{c} stored in the drift region affects the turn-off behavior of the diode. The theoretical trade-off between r_{o} and Q_{c} can be expressed by [34]

$$Q_{\mathrm{c}} r_{\mathrm{o}} = \frac{4{V_{\mathrm{br}}}^2}{\mu_{\mathrm{e}} {E_{\mathrm{br}}}^2} \,. \tag{2.6}$$

Due to the rather low electron mobility of $200\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [61] compared to $1000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for 4H-SiC or $1200\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for GaN [12], the theoretical advantages are less pronounced than expected only from the on-resistance. As illustrated in Fig. 2.5c, however, the $r_{\mathrm{o}} \times Q_{\mathrm{c}}$ FOM for Ga_2O_3 can theoretically still be approximately half that of SiC and similar to that of GaN. It must be noted that slightly varying values for μ_{e}, ϵ_{s}, and E_{br} are used for Ga_2O_3 in literature. This is partially related to varying physical properties based on the anisotropy of the β–Ga_2O_3 crystal structure which, together with other important material properties, will be discussed in the following section.

2.3.2 Material properties

Crystal structure

The α phase of Ga_2O_3 has a corundum structure with six Ga_2O_3 formula units per crystallographic cell and all Ga^{3+} ions being coordinated to the O^{2-} ions in an octahedral geometry [28, 62, 63]. This intrinsic crystal symmetry leads to rather isotropic electronic and thermal properties [64–66]. However, α–Ga_2O_3 is metastable and undergoes a phase transition to β–Ga_2O_3 at temperatures above $600\,°C$ in dry air and $300\,°C$ under hydrothermal conditions [11]. An important consequence is that it is not possible to grow α–Ga_2O_3 wafers from the melt. Therefore, α–Ga_2O_3 devices must be fabricated on non-native substrates such as α–Al_2O_3 [67–69] and will not be investigated in this thesis.

The β-phase is the thermodynamically most stable one of all Ga_2O_3 polymorphs and is obtained when heating any other phase of gallium oxide above a certain critical temperature between $300\,°C$ and $1000\,°C$ [11]. This also enables the fabrication of melt-grown β–Ga_2O_3 bulk substrates and corresponding homoepitaxially grown vertical devices. β–Ga_2O_3 has a monoclinic crystal structure with four Ga_2O_3 formula units in each crystallographic cell. The Ga^{3+} ions are coordinated both in an octahedral and in a tetrahedral geometry to the O^{2-} ions, which means there are two types of nonequivalent gallium ions and three types of non-equivalent oxygen ions. The interionic Ga–O and O–O distances differ for the respective coordinations [28, 62]. This intrinsic anisotropy in the crystal structure causes the optical, electronic, and thermal properties to vary along different crystal directions [27–29] and ultimately also affects the fabrication and processing of power devices as well as the resulting device characteristics significantly.

Electronic structure and doping

For β–Ga_2O_3, multiple theoretical and experimental studies find a fundamental indirect band gap in the range of 4.66 to $4.86\,eV$ [28, 70, 71] as well as a some $10\,meV$ larger direct band gap of 4.69 to $4.91\,eV$ [28, 70–73]. Due to the anisotropy of the crystal structure, the bandgap energy also depends on the crystal direction [74].

Similarly, a fundamental indirect bandgap of 5.03 to $5.19\,eV$ [28, 64, 70] and a several $10\,meV$ larger direct bandgap of 5.08 to $5.40\,eV$ [28, 64, 66, 70] has been determined for α–Ga_2O_3. This makes both α– and β–Ga_2O_3 semiconductors with a quasi-direct band gap, where corundum Ga_2O_3 seems to exhibit a slightly larger bandgap than its monoclinic counterpart. According to Fig. 2.5a, this leads to a higher theoretical breakdown field of up to 9 to $10\,MV/cm$ for α–Ga_2O_3.

The structures of both α–Ga_2O_3 and β–Ga_2O_3 allow for further adjustment of the bandgap energy. The corundum structure of α–Ga_2O_3 makes the combination with other corundum structured materials of similar lattice constant such as α–Al_2O_3 or α–In_2O_3 possible. This, in principle, allows tuning the bandgap in almost any range between $3.8\,eV$ and $8.8\,eV$, whereas the experimental realization is difficult due to the meta-stability of α–Ga_2O_3 and α-In_2O_3 [67]. Alloys with Al_2O_3 have opened the possibility to further increase the bandgap also for the β phase of Ga_2O_3. In [75], e.g., a bandgap energy of $5.7\,eV$ was experimentally determined for β–$(Al_{0.47}Ga_{0.53})_2O_3$ films.

The valence band of both α–Ga_2O_3 and β–Ga_2O_3 is rather flat, which results in a generally low hole mobility. In addition, polarons (quasi-particles describing the interaction between electrons and atoms in a solid) can significantly decrease the electron mobility in semiconductors. In the specific case of Ga_2O_3, holes tend to form localized polarons, i.e., they tend to be trapped by localized lattice distortions [76]. This phenomenon is often referred to as the self-trapping of holes, and it was concluded from a theoretical perspective that for this reason no p-type conductivity should occur in Ga_2O_3 [76]. Combined with the fact that potential acceptor states in Ga_2O_3 are located deep within the bandgap, i.e., no shallow acceptors have been found so far, Ga_2O_3 is generally considered as a material that cannot be p-doped [18, 76, 77].

Despite these considerations, NiO in p-NiO/n-Ga_2O_3 heterostructures has recently been experimentally shown to be capable of injecting holes into the Ga_2O_3 layers at sufficiently large forward voltages, which is referred to as conductivity modulation [23]. However, the associated hole mobility was estimated to be rather low (1.9 to $8.3\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) [23]. On the other hand, n-type doping in Ga_2O_3 can easily be achieved with effective donor concentrations ranging from $10^{15}\,\mathrm{cm^{-3}}$ [78] to $10^{20}\,\mathrm{cm^{-3}}$ [79]. Typical impurities that act as shallow donors in Ga_2O_3 are Sn [80], Si [81], or Ge [77].

According to Eq. 2.5, the electron mobility in a semiconductor material directly determines its specific resistance. The electron mobility in β–Ga_2O_3 at $300\,\mathrm{K}$ and a doping concentration below $10^{18}\,\mathrm{cm^{-3}}$ is generally limited to $200\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ due to phonon scattering [61]. High values of $194\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ at room temperature approaching this theoretical limit have already been achieved experimentally [82]. In this respect, it is interesting to note that the formation of a 2DEG can be achieved at $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterojunctions [83]. The electron mobility is expected to be much higher in these structures, which could enable the fabrication of $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ HEMTs for high-frequency applications [61].

The drift velocity of charge carriers in a semiconductor is another central property. At low electric fields, it increases linearly with rising electric field strength. At high electric fields, electrons lose energy by the emission of optical phonons. Therefore, the drift velocity approaches a maximum value, the so-called saturation drift velocity. When devices are blocking, high fields are present in the space-charge region. Thus, it can be assumed that charge carriers in the space-charge region move with the saturation velocity, which therefore affects the switching behavior of the devices [84]. In β–Ga_2O_3, the saturation velocity was calculated to reach a peak of $2.0 \times 10^7\,\mathrm{cm/s}$ at an electric field of $0.2\,\mathrm{MV/cm}$, and then slightly decrease to about $1.5 \times 10^7\,\mathrm{cm/s}$ at higher electric fields, where minor variations resulting from the crystal anisotropy are present [85]. This value is slightly lower than that of 4H-SiC, where about $2.0\,\mathrm{MV/cm}$ are approached at high electric fields [12, 86].

Thermal properties and cooling methods

The thermal conductivity in β–Ga_2O_3 was found to vary between $(10.9 \pm 1.0)\,\mathrm{W\,m^{-1}\,K^{-1}}$ in the [100], $(14.7 \pm 1.5)\,\mathrm{W\,m^{-1}\,K^{-1}}$ in the [001], and up to $(27.0 \pm 2.0)\,\mathrm{W\,m^{-1}\,K^{-1}}$ in the [010] crystal direction [29]. Other studies report slightly varying values [87–89]. Based on these values, the thermal conductivity is typically assumed to be in the range of 10 to $30\,\mathrm{W\,m^{-1}\,K^{-1}}$ [12], which is at least one order of magnitude lower than that of SiC (about $270\,\mathrm{W\,m^{-1}\,K^{-1}}$ at room temperature [12]).

In addition, it was shown that oxygen vacancy defects can increase phonon scattering, which ultimately leads to a reduction of the thermal conductivity [90, 91]. Simulations in [92] suggest that the effect of Ga vacancies might be even stronger, with a reduction of the thermal conductivity of $15\,\%$ for $1\,\%$ oxygen vacancies and $28\,\%$ for $1\,\%$ gallium vacancies in Ga_2O_3

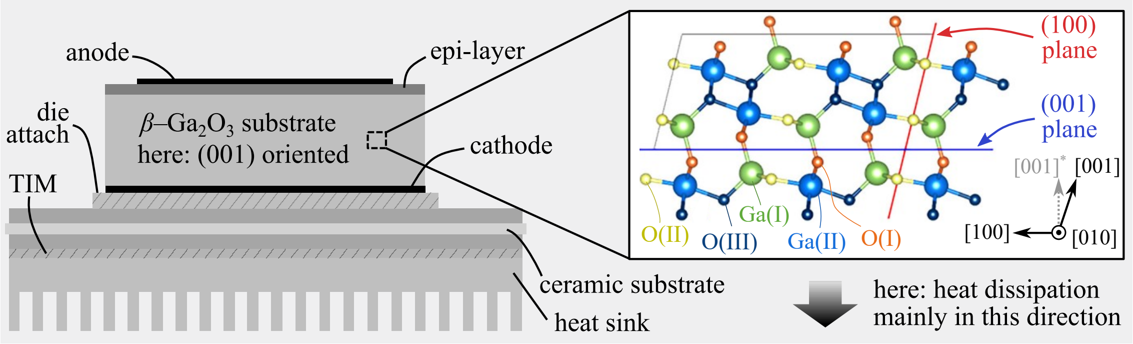


Figure 2.6: The thermal conductivity of β–Ga_2O_3 depends on the crystal direction, which is also expected to affect the heat dissipation in corresponding power devices. Diodes studied in this thesis are based on (001) oriented wafers. Therefore, the direct (vertical) cooling path, referred to as [001]*, is about $14°$ off of the [001] crystal direction. Image of the crystal structure adapted from [93].

thin films. A similarly strong effect on the thermal conductivity was found when inducing linear defects into the crystal [92]. Note that these results are based on β–Ga_2O_3 thin films, whose thermal conductivity is generally lower than that of corresponding bulk crystals [92]. Nevertheless, the crystal quality could potentially also affect the thermal conductivity of thick Ga_2O_3 layers, which is important for the thermal studies conducted on power devices in this thesis.

The low thermal conductivity of Ga_2O_3 limits the heat dissipation through the substrate significantly and leads to a heat concentration at the anode side (i.e., the junction side) of the devices [94]. Furthermore, due to the strong anisotropy of the thermal conductivity in β–Ga_2O_3, the crystal orientation of the corresponding power devices can be expected to have a direct effect on the thermal management. As illustrated in Fig. 2.6, the devices studied in this thesis are based on (001) oriented wafers. Due to the slightly tilted crystal structure, the direct cooling path is not in [001] direction but about $14°$ off of this crystal direction, which will be referred to as [001]* in the following. Therefore, the thermal conductivity along the direct cooling path may differ from the above summarized literature values.

Some studies focusing on the issue of low thermal conductivity have been published recently. By transferring β–Ga_2O_3 thin films onto a SiC wafer, e.g., Ga_2O_3-on-SiC diodes were realized in [95]. Compared to diodes fabricated on bulk Ga_2O_3 wafers, the increase in junction temperature was reduced by one-quarter [95]. However, a procedure based on SiC substrates may contradict the potential cost and quality advantage of Ga_2O_3 resulting from the availability of native substrates.

Instead, cooling the devices from the junction side was suspected to be potentially effective for Ga_2O_3 [94]. During the course of this thesis, junction-side cooling of Ga_2O_3 diodes was reported to enable a junction-to-case thermal resistance of $1.48\,\mathrm{K/W}$ for a die with an anode area of $9\,\mathrm{mm}^2$ sintered to a copper-molybdenum-copper substrate [96], and $0.5\,\mathrm{K/W}$ for a diode with the same anode area that was sintered to a silver plate [97]. Clearly, the reported values vary significantly. The different packaging methods and the fact that no reference devices with similar chip area were assembled in the same way in these studies prevents a thorough understanding of the effectivity of different cooling methods, let alone a comparison with other technologies such as SiC. Generally, as pointed out in [8], the heat dissipation in large-area Ga_2O_3 power devices is critical both from a performance and cost point-of-view, but rarely studied in the literature. Therefore, parts of this thesis target a comparable analysis of different thermal management methods for Ga_2O_3 power diodes.

In the case of α–Ga_2O_3, the thermal conductivity seems to be rather isotropic according to first principle calculations [65]. However, the calculated values of $11.6\,\mathrm{W\,m^{-1}\,K^{-1}}$ in [100] direction, $9.4\,\mathrm{W\,m^{-1}\,K^{-1}}$ in [010] direction, and $8.9\,\mathrm{W\,m^{-1}\,K^{-1}}$ in [001] direction are slightly lower than for β–Ga_2O_3. This might result from the bond strength of Ga and O atoms in α–Ga_2O_3, leading to stronger phonon scattering processes [65].

Thermomechanical properties

The coefficient of thermal expansion (CTE) was also found to be highly anisotropic for β–Ga_2O_3. In the range of 300 to $700\,\mathrm{K}$, CTEs of $1.5 \times 10^{-6}\,\mathrm{K^{-1}}$ in [100] up to $3.2 \times 10^{-6}\,\mathrm{K^{-1}}$ in [001] and $3.4 \times 10^{-6}\,\mathrm{K^{-1}}$ in [010] direction were reported in [98]. Slightly higher values were determined in [99]. Due to the limited number of available large-area devices, it has not yet been studied if the anisotropy of the CTE affects, e.g., the assembly and packaging procedure or reliability of the devices. As a comparison, the CTE of GaN increases from about 2.8 to $6.1 \times 10^{-6}\,\mathrm{K^{-1}}$ [100] and the CTE of 4H-SiC from 2.2 to $4.5 \times 10^{-6}\,\mathrm{K^{-1}}$ [101] in the same temperature range, respectively.

The mechanical properties of the semiconductor are critical not only from a reliability point-of-view but also regarding the device fabrication and wafer handling. One important mechanical property, the microhardness as measured by the Vickers indentation method also indicates a certain anisotropy in β–Ga_2O_3. The reported values are in the range of about $6.4\,\mathrm{GPa}$ for (010) oriented substrates [102], 8.3 to $8.9\,\mathrm{GPa}$ for (100) oriented substrates [102, 103], $10.1\,\mathrm{GPa}$ for (001) oriented substrates [102], and up to a maximum hardness of $12.5\,\mathrm{GPa}$ as specified by a substrate manufacturer for $(\bar{2}01)$ oriented substrates [231]. It should be noted that the determined hardness depends on the force applied during the test as cracks and cleavages in certain crystal planes can form even at rather low test forces [104]. The values are similar to those typically reported for Si (about 9 to $10\,\mathrm{GPa}$ [105]) and significantly lower than those of 4H-SiC (about $32\,\mathrm{GPa}$ [106]). A similar observation is made for the Young modulus, which characterizes the stiffness of a material. It is about $230\,\mathrm{GPa}$ in β–Ga_2O_3 substrates [103, 231], which compares to about $160\,\mathrm{GPa}$ for Si [105, 107] and about $500\,\mathrm{GPa}$ for 4H-SiC [107, 108].

The comparison of Young's modulus and the microhardness shows that Ga_2O_3 is a rather soft material that, in contrast to 4H-SiC, can in principle be processed with standard tools known from Si wafer technology (such as cutting with a diamond saw). However, Ga_2O_3 is rather brittle and fragile in certain crystal directions. Associated cleavage planes with weak atomic bonds make the handling and dicing of Ga_2O_3 wafers with certain orientations such as (010) difficult [104], which is a new challenge for Ga_2O_3 device technology. Nevertheless, β–Ga_2O_3 wafers with or without high-quality epitaxial layer have been fabricated using different methods that will be summarized in the next section.

2.3.3 Growth and metal–semiconductor contacts

While SiC wafers need to be grown from the vapor phase at high temperatures above $2000\,^{\circ}\mathrm{C}$ [109], and for the same reason GaN devices are mostly based on hetero-epitaxially grown GaN layers on Si or sapphire substrates (see Section 2.2.2) [39], β–Ga_2O_3 wafers can be grown from the melt with standard methods known from Si technology [18]. In this section, fundamental steps to fabricate basic vertical power devices, i.e., bulk growth, epitaxial growth, and the formation of ohmic and Schottky contacts, are discussed.

Wafer growth

The Czochralski (CZ) method is a well-understood standard method for the fabrication of large-area Si, sapphire, Ge, or GaAs wafers, and has been successfully adapted to grow β–Ga_2O_3 substrates [13, 14]. Due to high growth temperatures of $1800\,°\mathrm{C}$, an Ir crucible is required to contain the Ga_2O_3 melt. This is associated with high cost [8] and the possibility of introducing impurities to the melt [110]. Furthermore, to scale up CZ-grown bulk crystals to sizes beyond 4 inches, a current challenge is to achieve a sufficiently high oxygen concentration in the entire melt [110]. Nevertheless, high-quality crystals have been fabricated at typical growth rates of 1 to $2.5\,\mathrm{mm/h}$ [13].

Edge-defined film-fed growth (EFG) is a standard method to grow large sapphire ribbons. For Ga_2O_3, it is especially appealing due to fast growth rates of currently 6 to $15\,\mathrm{mm/h}$ [15, 18]. EFG-based Ga_2O_3 substrates were the first ones to be commercialized [231] and device-quality wafers with a diameter of up to 6 inches have been realized [111, 232]. All Ga_2O_3 devices studied in this thesis are fabricated on EFG-grown wafers. Although an Ir crucible is used to contain the Ga_2O_3 melt, it seems to be less susceptible to oxidation and melt volatilization than in the case of CZ growth [18].

The two previously described methods are currently the most commonly applied ones to fabricate β–Ga_2O_3 wafers. Nevertheless, β–Ga_2O_3 substrates have also been grown using other techniques such as vertical Bridgman (VB) [16, 112] or optical floating zone (FZ) [17, 113]. While FZ-growth is feasible in principle as no crucible is required and a high oxygen atmosphere is possible, scaling up the wafer size beyond 1 inch seems to be hampered by difficulties in achieving sufficient heating of the material [18, 113]. The number of studies on VB-grown substrates is limited, although it was concluded in [18] that this method might hold a certain potential. So far, substrates with a diameter of 2 inches have been achieved, where the growth took place in ambient air without a seed crystal [112]. However, with $0.5\,\mathrm{mm/h}$ the growth rate was rather low [16]. The availability of β–Ga_2O_3 substrates fabricated by one of these methods constitutes the basis for the subsequent growth of homo-epitaxial Ga_2O_3 drift layers.

Epitaxial growth

Device-quality epitaxial Ga_2O_3 layers can be grown by a number of standard methods such as molecular beam epitaxy (MBE) [80], halide-vapor-phase epitaxy (HVPE) [114], metalorganic chemical vapor deposition (MOCVD) [115], low-pressure chemical vapor deposition [116], pulsed-laser deposition [117], physical vapor deposition [118], and mist chemical vapor deposition (mist-CVD) [119]. A thorough overview and comparison of the different techniques can be found, e.g., in [18] and [120]. Here, only the most important aspects will be covered.

The first gallium oxide power devices were fabricated by MBE [80]. Since then, the layer quality was improved significantly, and MBE was also employed to grow high-quality $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures forming a 2DEG [83]. Due to low growth rates below $0.5\,\mathrm{\mu m/h}$ [121], MBE is rather interesting for lateral Ga_2O_3 devices that do not require a thick drift layer [18]. Although an ultra-high vacuum is required, MBE is expected to enable uniform and large Ga_2O_3 epitaxial layers that are scalable for production [18].

Epitaxial layers grown by MOCVD have achieved very low unintentional doping, leading to record electron mobilities exceeding $190\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ at room temperature [82]. With up to $10\,\mathrm{\mu m/h}$ [122], the growth rates significantly exceed those achieved with MBE. Therefore, MOCVD of Ga_2O_3 thin films could be scalable for production of both lateral and vertical β–Ga_2O_3 power devices [18].

Even higher growth rates of $25\,\mu m/h$ on β–Ga_2O_3 substrates [123] and up to $250\,\mu m/h$ on sapphire substrates [124] are possible with HVPE while achieving reasonable electron mobilities [18]. Therefore, HVPE is also a potential candidate for large-volume production of vertical Ga_2O_3 power devices with thick drift layers. A challenge for HVPE is high deposition temperatures that can trigger a diffusion of atoms between the epitaxial layer and the substrate or lead to the incorporation of Si or Cl impurities originating from the quartz reactor and precursor [18, 123, 125, 126]. It was suspected that this could affect the electrical properties of HVPE-grown films [126], as Cl is assumed to be a shallow donor in β–Ga_2O_3 [127]. These considerations are important because all devices studied in this thesis were fabricated by HVPE on EFG-grown substrates.

Ohmic and Schottky contacts to Ga_2O_3

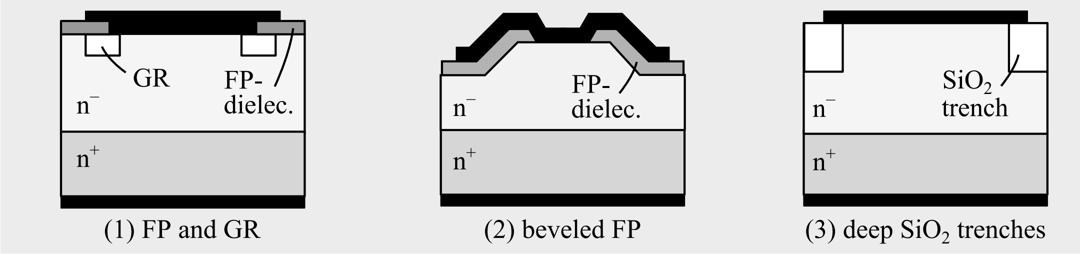
Taking the availability of epitaxial wafers as a starting point, the next step towards the fabrication of gallium oxide power devices is the formation of ohmic and Schottky contacts to Ga_2O_3 as an integral part of every power device (see also Section 2.2.3). The properties of these contacts depend on the metal work function but also on the doping concentration of the semiconductor and the interface quality of the MS contact [128]. It was shown that defect states at the Ga_2O_3 surface can actually have a stronger impact on the contact properties than the metal work function itself [129, 130]. Furthermore, owing to the anisotropy of the β–Ga_2O_3 crystal structure, basic properties such as the barrier height depend strongly on the Ga_2O_3 wafer orientation [130].

Ohmic contacts to β–Ga_2O_3 are almost exclusively formed using Ti/Au, where Ti forms the ohmic contact and Au acts as a capping and protection layer [22, 23, 129, 131–135]. Compared to other metals (such as In, Ag, Sn, or Zr) it shows a high temperature stability and low specific contact resistances [129]. In [136], e.g., a specific contact resistance as low as $8.3 \times 10^{-7}\,\Omega\,cm^2$ was achieved on highly n-doped Ga_2O_3.

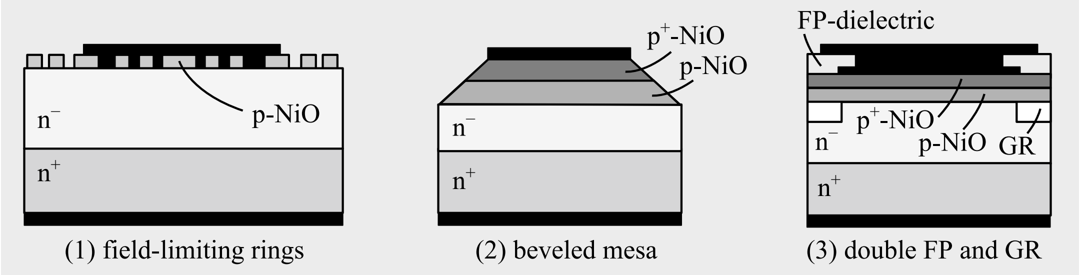
The formation of Schottky contacts to Ga_2O_3 is possible with a variety of metals, including W, Cu, Ni, Ir, Pt [130], Au [137], or Mo [138]. The barrier height is then typically in the order of 1 to $1.5\,eV$ [120, 130, 131, 134, 139]. In most Ga_2O_3 devices Ni [22, 23, 134, 140] or Pt [134, 140–142] is used as a Schottky metal. This lays the foundation for the fabrication of Ga_2O_3 power diodes, the concepts of which are discussed below.

2.3.4 Diode concepts

β–Ga_2O_3 diodes based on native substrates have been fabricated on a lab scale with various lateral and vertical structures. Currently, β–Ga_2O_3 power devices are not commercially available, and research is mostly restricted to the on-wafer characterization and analysis of basic structures with lateral dimensions of several hundreds of μm [18, 134]. In this thesis, first diced and partly standard molded diode chips from a planned production line that significantly exceed these dimensions and thus enable more application-oriented tests will be investigated. The most promising diode concepts, including the structures of the diodes under investigation in this thesis, are summarized in the following.



(a) Unipolar vertical β–Ga_2O_3 Schottky diodes.



(b) Vertical p-NiO/β–Ga_2O_3 heterojunction diodes.

Figure 2.7: Overview of promising vertical β–Ga_2O_3 diode structures based on lightly doped epitaxial layers deposited on heavily doped native substrates. Both (a) fully unipolar and (b) heterojunction devices have been fabricated with ion-implanted guard rings (GR), field plates (FP), and beveled structures. Some of the diodes studied in this thesis have a structure as shown in (a)-(1). Adapted from [22, 23, 131–133, 149].

Vertical planar diodes and edge terminations

The first β–Ga_2O_3 diode introduced in 2013 consisted of simple planar structures without edge termination [21]. The diode was based on an unintentionally doped FZ-grown substrate without an additional epitaxial layer and showed a basic rectifying behavior [21]. As shown in Fig. 2.7, most diodes developed since then consist of a heavily doped melt-grown β–Ga_2O_3 substrate, typically with an effective donor concentration in the range of 10^{18} cm^{-3} to more than 10^{19} cm^{-3} that is followed by a high-quality epitaxial layer which is usually around $10\,\mu m$ thick and exhibits an effective donor concentration in the order of 10^{16} cm^{-3} [22, 131, 132, 134, 135, 143]. Ohmic and Schottky contacts are typically formed with Ti/Au and Ni/Au or Pt/Au, respectively, as explained in Section 2.3.3, which leads to knee voltages typically in the range of around 0.8 to $1\,V$ [52, 131, 142, 144–148] but also up to $1.8\,V$ have been reported [149].

Without edge termination, the peak electric field at the edge of the anode is substantially higher than in the volume of the drift layer, which leads to a premature reverse breakdown of the device. To fully exploit the high theoretical breakdown field of gallium oxide, different edge termination structures such as field plates [150], guard rings [149], floating potential rings [132, 151], or beveled structures [131] that lead to a reduction of the peak electric field and an enhancement of the breakdown voltage have been implemented successfully.

Figure 2.7a–(1) shows a planar Schottky diode with field plates and guard rings. In this thesis, planar diodes without and with such kind of edge termination are studied. Field plates are often based on SiO_2 [254, 134, 149, 150] or Al_2O_3 [134, 139, 152]. Guard rings have been fabricated by N-ion [134, 149] or Mg-ion implantation [134, 153], but p-AlGaN structures [154] or the thermal oxidation of the anode edge region [146] have also been reported to be effective methods. As shown in Fig. 2.7b, also beveled structures with spin-on-glass and SiO_2 field plates have been successfully realized [131]. Figure 2.7a–(3) shows a rather simple structure, with deep SiO_2 trenches [22]. With all of these structures, breakdown voltages exceeding $1\,\mathrm{kV}$ and PFOMs of several hundreds of MW/cm^2 have been achieved. The structure with deep SiO_2 trenches (anode diameter of $180\,\mu\mathrm{m}$) enabled a low $r_{\text{o,sp}}$ of $3.4\,\mathrm{m\Omega\,cm^2}$ at a V_{br} of $6\,\mathrm{kV}$. The corresponding PFOM of $10.6\,\mathrm{GW/cm^2}$ exceeds the unipolar limit of SiC and GaN [22]. Recently, a Ga_2O_3 diode with a V_{br} of $1720\,\mathrm{V}$ and a high PFOM of $1.32\,\mathrm{GW/cm^2}$ was realized even without edge termination. This was achieved by plasma etching to remove donor-like impurities at the surface of the drift layer [144].

Due to the absence of p-type doping in Ga_2O_3 (see Section 2.3.2), other p-type semiconductors can be implemented to form edge terminations or heterojunctions. In this respect, p-type NiO has recently gained the most interest. The diode shown in Fig. 2.7b–(1), e.g., consists of alternating Ni/n-Ga_2O_3 Schottky contacts and p-NiO/n-Ga_2O_3 heterojunctions, as well as field-limiting p-NiO rings as edge termination. At a still reasonable knee voltage of $1.1\,\mathrm{V}$ a V_{br} of $1.89\,\mathrm{kV}$ and an $r_{\text{o,sp}}$ of $7.7\,\mathrm{m\Omega\,cm^2}$ were achieved [132]. For full p-NiO/n-Ga_2O_3 heterojunction diodes, the knee voltage increases to typically about 1.8 to $1.9\,\mathrm{V}$ [23, 133, 155]. However, such structures have achieved high PFOMs. The heterojunction diode in Fig. 2.7b–(3) with two differently doped p-NiO layers, Mg-implanted guard rings and SiO_2 double field plates, and an anode diameter of $150\,\mu\mathrm{m}$ achieved a record PFOM of $13.2\,\mathrm{GW/cm^2}$ [23]. The corresponding $r_{\text{o,sp}}$ of $5.24\,\mathrm{m\Omega\,cm^2}$ at a V_{br} of $8.32\,\mathrm{kV}$ is about one third of the unipolar SiC limit [23].

Recently, first rudimentary switching tests have been conducted for Ga_2O_3 Schottky and heterojunction diodes [96, 133, 155–158]. The studies proved the basic benefits of unipolar Ga_2O_3 Schottky diodes, such as the absence of reverse recovery. All devices that could sustain application-relevant reverse voltages of at least $400\,\mathrm{V}$ were limited to lateral dimensions of only some hundreds of $\mu\mathrm{m}$ up to a maximum anode area of $1\,\mathrm{mm^2}$ for a heterojunction diode in [133, 155]. Although a first diode operation in a PFC circuit was demonstrated, the achieved current slew rates were well below $1\,\mathrm{A/ns}$ [133, 155]. Furthermore, other application-critical parameters, such as the voltage slew rates and waveforms, were not studied and a comparison to mature technologies such as SiC is missing. This motivates the thorough and comparable investigation of switching properties of novel $600\,\mathrm{V}$ rated Schottky diodes with anode areas up to $10\,\mathrm{mm^2}$ performed in this thesis.

Vertical trench diodes

In Schottky barrier diodes there is an intrinsic trade-off between the reverse leakage current and the forward knee voltage, both of which are determined by the Schottky barrier height in an opposite manner. Furthermore, the maximum electric field E_{max} occurs at the Schottky junction and directly determines the leakage current. Since basic MPS structures such as in the case of SiC (see Section 2.2.2) cannot be implemented to resolve this issue due to the lack of p-Ga_2O_3, fabricating trench-MOS structures such as illustrated in Fig. 2.8 is another promising concept for Ga_2O_3 diodes [159–161].

Basically, the additional vertical PN junctions found in MPS diodes are replaced by MOS junctions at the sidewalls of the vertical trenches. Because of that, the depletion region formed during blocking operation does not only extend vertically but also horizontally. As a consequence, the electric field at the surface E_{surf} is reduced and the peak electric field is shifted towards the volume of the chip. Therefore, the effect is often referred to as reduced surface field (RESURF) effect [160, 162] and can be quantified by the field reduction factor $\mathcal{R} = E_{\text{surf}}/E_{\text{max}}$ [160]. The exact field distribution and diode properties depend critically on

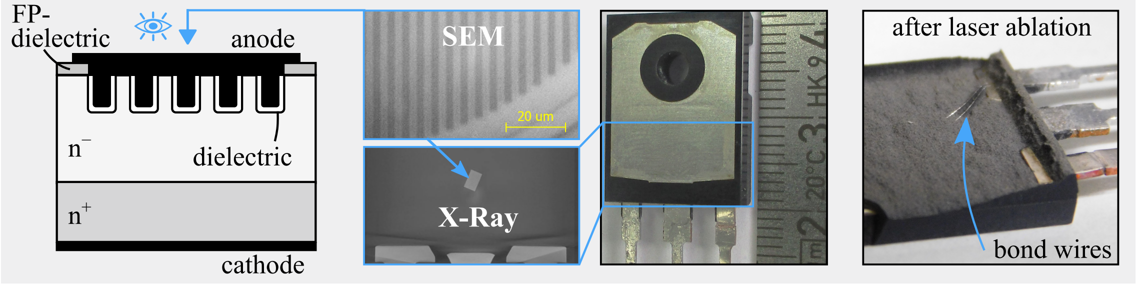


Figure 2.8: (Left) Basic structure of a field-plated β–Ga$_2$O$_3$ trench MOS diode. (Middle) The top-view SEM and X-ray images of a trench MOS diode studied in this thesis show the field plates and the about 3 µm wide trenches of a diced chip that is bonded by soldering and wire-bonding in a TO247 package. (Right) Two Al bond wires can be seen after removing the mold mass with a laser. Adapted from [254].

the trench depth, width, distance, crystal orientation, the doping profile, and the dielectric that needs to withstand high electric fields [160, 163, 164].

In [152] a Ga$_2$O$_3$ trench diode with field plates and Al$_2$O$_3$ dielectric achieved a breakdown voltage of $2.89\,\mathrm{kV}$ and an $r_{\mathrm{o,sp}}$ of $8.8\,\mathrm{m\Omega\,cm^2}$, resulting in a promising PFOM of $0.95\,\mathrm{GW/cm^2}$. So far, however, the small number of Ga$_2$O$_3$ trench diodes that have been subjected to temperature-dependent analysis in the literature showed strong junction inhomogeneities as characterized by a large change of ideality factor and barrier height with temperature [165, 166].

Therefore, a temperature-dependent characterization of a trench diode with HfO$_2$ instead of Al$_2$O$_3$ dielectric is performed in this thesis. The scanning electron microscopy (SEM) image in Fig. 2.8 clearly shows the trench and field-plate structure of this type of diode. As can be seen from the X-ray images, the chip is located in the center of a fully molded TO247 package. More information on the structure is provided in the respective chapters.

Lateral diodes

Several lateral β–Ga$_2$O$_3$ diodes have also been demonstrated. In [139] the existence of certain cleavage plane in β–Ga$_2$O$_3$ (see Section 2.3.3) was used to exfoliate 600 to $650\,\mathrm{nm}$ thin nano-membranes simply by using scotch tape and transfer them to a sapphire substrate, motivated by their low cost but better thermal conductivity. The resulting diode with Al$_2$O$_3$ field plates achieved a PFOM of $500\,\mathrm{MW/cm^2}$ at a breakdown voltage of $2.25\,\mathrm{kV}$. In [167] native substrates were used to grow lateral NiO/(Al$_x$Ga$_{1\text{-}x}$)$_2$O$_3$/Ga$_2$O$_3$ heterojunction diodes. The corresponding devices achieved high breakdown voltages above $7\,\mathrm{kV}$, however, at low PFOMs below $1\,\mathrm{MW/cm^2}$. A significantly higher PFOM of $1.34\,\mathrm{GW/cm^2}$ at a breakdown voltage of $1.5\,\mathrm{kV}$ was achieved by fabricating lateral diodes with trench-MOS structures on native substrates [168]. Given the focus of this thesis is on vertical diodes, which are typically preferred in power electronics, please refer to the respective publications for more details.

2.3.5 Transistor concepts

Transistors based on Ga$_2$O$_3$ are currently at a significantly earlier stage of development than Ga$_2$O$_3$ diodes. Nevertheless, both vertical and lateral β–Ga$_2$O$_3$ transistor cells with lateral dimensions of some tens to some hundreds of µm have been fabricated. Two vertical transistor structures that are currently considered promising candidates are planar FETs with a current blocking layer (CBL) and FETs with a trench structure.

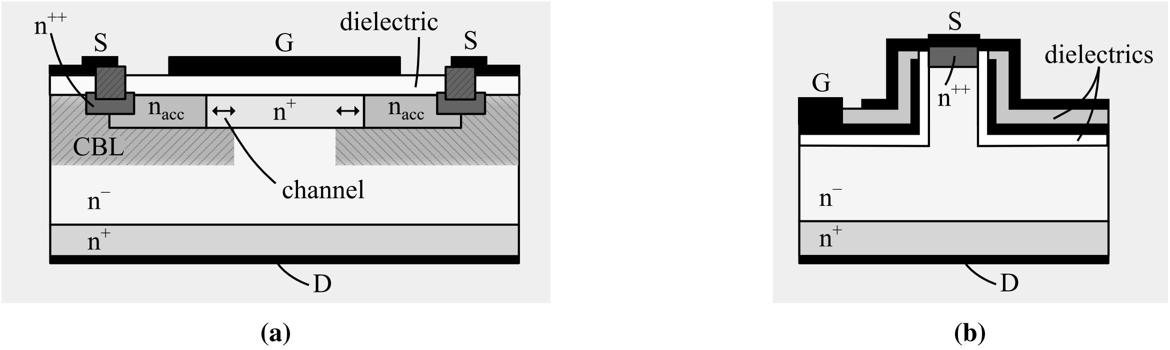


Figure 2.9: Schematic structures of promising vertical β–Ga$_2$O$_3$ enhancement mode transistor concepts. (a) Planar FET with N-ion or Mg-ion implanted current blocking layer (CBL). (b) FinFETs with optimized trench structure have achieved the highest PFOMs and breakdown voltages so far. Adapted from [24, 169, 170].

Fig. 2.9a shows the basic structure of a planar MOSFET that was introduced in [169]. Since Ga$_2$O$_3$ cannot be effectively p-doped, N-ion or Mg-ion implantation is used instead to create a high-resistive CBL below the heavily n-doped source contacts. It electrically isolates the drain from the source contact, thus limiting the drain–source leakage current, and forms the conductive aperture through which the current flows. The N^{++}-region an the n-doped Si^{+} implanted channel region basically form a PN junction that fully depletes the channel from charge carriers if the donor concentration in the channel is sufficiently low, thus resulting in a normally-off behavior. Due to the simple planar structure with implantation steps, the device is attractive from a mass production point-of-view. However, it only reached a V_{br} of $263\,\mathrm{V}$ at a $r_{\mathrm{o,sp}}$ of $135\,\mathrm{m\Omega\,cm^2}$ [169]. A recent news release claimed a V_{br} exceeding $1\,\mathrm{kV}$ for a similar structure [233].

Higher breakdown voltages and PFOMs have been achieved with trench or FinFET structures exemplarily shown in Fig. 2.9b. Initial FinFETs with normally-off behavior showed breakdown voltages exceeding $1\,\mathrm{kV}$ and PFOMs of $125\,\mathrm{MW/cm^2}$ [170, 171]. By introducing a post-deposition annealing step, the channel mobility was significantly increased to about $130\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, leading to PFOM of $280\,\mathrm{MW/cm^2}$ at a breakdown voltage of $2.66\,\mathrm{kV}$ [24]. Although other promising structures such as the vertical trench U-gate FET [172] or lateral FETs with trench gate [25] were demonstrated, the PFOMs of diodes are not yet achieved, and only one group has demonstrated a large-area (gate width $10\,\mathrm{mm}$) MOSFET with lateral structure [173, 174]. First switching tests indicated a dynamic increase in on-resistance preventing experiments above DC link voltages of $300\,\mathrm{V}$ [173] and $400\,\mathrm{V}$ [174], respectively. Since Ga$_2$O$_3$ transistors are not available in this thesis, the reader is referred to the corresponding publications for more information.

2.4 Summary and basic research questions arising

The current state of knowledge and the main issues that form the guiding questions for this work can be summarized as follows:

1. β–Ga$_2$O$_3$ is a highly anisotropic material that combines a high critical electric field with the availability of melt-grown and comparatively soft wafers. So far, no particular device structures have prevailed.

2. Research mostly concerns basic structures with lateral dimensions of some hundred $\mu\mathrm{m}$ and lacks application-oriented analyses. Especially the switching properties and the impact of low thermal conductivity are essential, but have hardly been examined so far.
3. The following aspects are thus identified as critical for the path towards application:
    a) understanding the basic properties of novel device structures with respect to their potential application in power electronics
    b) examination of the thermal properties and the effectiveness of different heat dissipation strategies
    c) transition to large-area devices that allow first application-oriented studies of the switching properties

In this work, the first β–Ga_2O_3 diodes from a planned industrial wafer and device fabrication line are analyzed. This allows the formulated problems to be addressed gradually.

Chapter 3

Experimental methods: sample preparation, measurement, and evaluation

3.1 Chapter overview

This chapter introduces the main experimental methods used to study a wide range of characteristics of Ga_2O_3 diodes, from basic physical properties to application-oriented parameters. To this end, Section 3.2 first introduces the various Ga_2O_3 diodes under investigation and their different packaging and assembly processes. Section 3.3 briefly discusses the measurement of forward and reverse current–voltage profiles and the junction capacitance, as well as the corresponding evaluation procedures. Diodes that can sustain sufficiently large reverse voltages can be subjected to double pulse tests in order to study their switching behavior. Capturing the associated short switching transients is challenging but vital to draw sound conclusions about the semiconductor properties. In Section 3.4, novel current sensor technologies are therefore evaluated and the most suitable ones are selected for further studies. For any continuous operation, the thermal resistance of the power devices is a central aspect. Section 3.5 therefore examines the forward voltage drop as a temperature-sensitive parameter to estimate the junction temperature and introduces the transient thermal measurement methods applied to Ga_2O_3 diodes. Parts of this chapter have been published in [255, 260] by the author during the course of this thesis.

3.2 Packaging and overview of the investigated samples

Assembly on custom substrates

Gallium oxide devices are not yet commercially available and as such cannot be purchased in standardized packages. While some diodes were already assembled on TO247 lead frames by the device manufacturer, other samples were received as bare dies that require further packaging. Therefore, a suitable custom substrate was designed that enables all types of planned measurements, and in particular fulfills the following requirements: First, it should enable the assembly of bare dies with different thicknesses, lateral dimensions and surface metallizations. Second, the package should enable effective cooling via different methods such as standard cathode-side cooling but also junction-side cooling, and thermal imaging of the bare die should be possible for these setups. Third, the package must allow a low-inductive assembly on a printed circuit board to enable fast switching tests. Fourth, the package should be easy to handle (e.g., with regard to mounting on a circuit board, connection to test fixtures, or mounting on heat sink) and at the same time protect the die sufficiently.

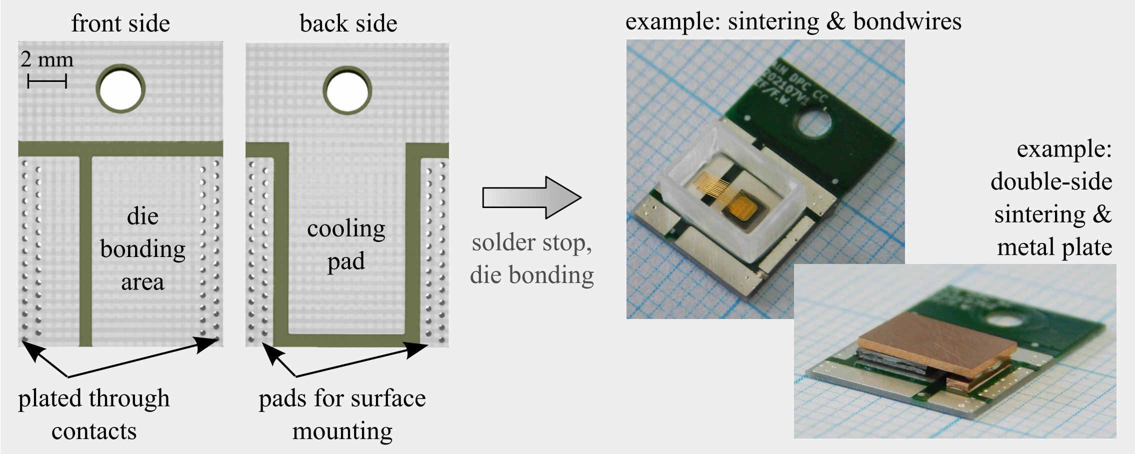


Figure 3.1: Custom package used to enable a wide range of different experiments. It is based on an aluminum nitride ceramic substrate with silver-plated copper pads on both sides. Plated through contacts at the sides of the substrate allow for a low-inductive SMD assembly on a printed circuit board. The silver plating facilitates different assemblies with either the cathode or the anode facing downwards. The terminal that is facing upwards can either be connected with bond wires in case of bottom-side cooling, or a metal plate can be attached to enable top-side or double-side cooling. A solder stop layer and 3D-printed plastic frame protect the die, while a mounting hole can be used to attach the package to a heat sink.

To meet the requirements, a package based on an aluminum nitride ceramic is designed. The manufacturing of the substrate is done externally by a contractor. The basic structure and two examples with an assembled Ga_2O_3 die are shown in Fig. 3.1. Aluminum nitride is the ceramic of choice for high thermal conductivity with about $170\,\mathrm{W\,m^{-1}\,K^{-1}}$ compared to about 30 to $70\,\mathrm{W\,m^{-1}\,K^{-1}}$ for Si_3N_4 or 20 to $30\,\mathrm{W\,m^{-1}\,K^{-1}}$ for Al_2O_3, combined with high electrical insulation capabilities (dielectric strength about 14 to $20\,\mathrm{kV/m}$) [175–177]. The high thermal conductivity reduces the effect the package has on the junction-to-case thermal resistance, which is helpful when studying the thermal properties of different dies.

The total package exhibits lateral dimensions of $10.7\,\mathrm{mm} \times 16\,\mathrm{mm}$. The ceramic is $0.3\,\mathrm{mm}$ thick and has $70\,\mathrm{\mu m}$ thick direct-plated copper tracks on both sides. The copper tracks are silver metallized, which prevents oxidation and simplifies silver sintering while also enabling standard wire bonding with aluminum or gold bond wires. In this way, a large degree of freedom for different surface metallizations of the die is achieved.

The front side consists of three different copper areas. The upper pad provides mechanical support and contains an M2 mounting hole to attach the substrate to a heat sink with a screw. The bottom right pad constitutes the die bonding area. Here, one electrode of the die can be bonded directly to the substrate, e.g., using soldering or sintering methods. In this way, an electrical and thermal coupling with the substrate is established. The bottom left hand pad serves as electrical connection to the second electrode of the diode, e.g., by wire-bonding or by attaching copper clips via soldering or sintering.

A solder stop layer is deposited on the front side to prevent solder from flowing to the die and potentially harming it. Optionally, a 3D-printed plastic frame is glued around the chip to facilitate safe handling and to enable silicone potting if required. The polarity of the die bonding pad changes depending on whether the cathode or anode is bonded to it. This in turn also changes the polarity of the package terminals. Therefore, an almost identical second version of the substrate was designed. It only differs in the fact that the two electrode pads on

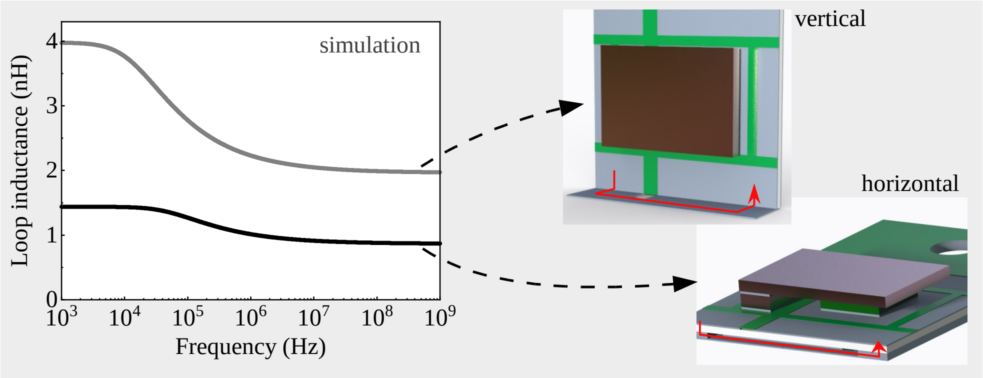


Figure 3.2: The custom package can be mounted either horizontally or vertically on a printed circuit board. Simulations in Ansys Q3D for the assembly method with a metal plate show that a parasitic inductance as low as 0.9 to $1.4\,\mathrm{nH}$ for frequencies between $1\,\mathrm{GHz}$ and $1\,\mathrm{kHz}$ can be achieved with the horizontal assembly, which enables fast switching experiments.

the front side are mirrored. As a result, when choosing the appropriate package for a certain assembly, the polarity of the package terminals remains the same.

The back side of the ceramic substrate also consists of three different copper pads. The large copper pad in the middle is electrically isolated and can serve as a connection to a heat sink in order to dissipate the heat created in the chip. Two narrow copper pads at the sides are connected to the two diode pads by copper plated through contacts through the ceramic. These two pads enable a low-inductive surface mounting of the package on a printed circuit board to enable fast switching. In such a surface mount assembly, the die can either be cooled from the bottom side, or from the top side when a metal plate is attached to the top-side of the die as shown on the right in Fig. 3.1. Alternatively, the package can be assembled on a circuit board in a vertical way, similar to a TO220 package without leads.

The parasitic inductance of the package is estimated using the Ansys Q3D Extractor [234]. To this end, a $3\,\mathrm{mm} \times 3\,\mathrm{mm}$ large and $0.6\,\mathrm{mm}$ thick die that is assembled with a $0.5\,\mathrm{mm}$ thick copper plate according to Fig. 3.1 is assumed. As shown in Fig. 3.2, the electrical loop is closed $200\,\mu\mathrm{m}$ below the backside of the substrate by a $70\,\mu\mathrm{m}$ thin copper plate to model the horizontal assembly. In this case, the area that is enclosed by the loop is rather small and thus a comparably low inductance is expected. In case of the vertical assembly the loop is closed at the front side of the substrate, which should increase the parasitic inductance. In both cases, a drop in inductance for increasing frequencies is expected as the proximity effect leads to a concentration of the current distribution at the inward-facing surface of the conductor [178, 179]. In agreement with these considerations, the simulated stray inductance for frequencies between $1\,\mathrm{kHz}$ and $1\,\mathrm{GHz}$ is 1.4 to $0.9\,\mathrm{nH}$ for the horizontal, and 4.0 to $2.0\,\mathrm{nH}$ for the vertical assembly. Note that the exact assembly method (such as assembly with bond wires instead of a metal plate, or size, thickness and position of the die) can affect the calculated parasitic inductance. Yet, the achieved inductance is several times lower than that of a standard TO220 package, which is in the range of 5 to $8\,\mathrm{nH}$ per lead [180]. Low-inductive switching tests are therefore possible with the introduced assembly method.

The functionality of the package is verified by assembling commercial $650\,\mathrm{V}/10\,\mathrm{A}$ rated SiC diode chips (Cree CPW2-0650-S010B [235]) using either soft soldering or pressureless silver sintering to attach the die to the substrate, and aluminum wire bonding to electrically connect the anode. The resulting temperature-dependent forward and reverse current–voltage characteristics and capacitance–voltage profiles are in agreement with the datasheet specifications

Table 3.1: Overview of β–Ga_2O_3 devices studied in this thesis. The samples differ in junction structure, edge termination, i.e., field plates (FP) or guard rings (GR), substrate thickness z_{sub}, the characteristic anode size (XS, ML, L, and LL) and metallization, and the packaging, i.e., either on a TO247 lead frame or the custom direct plated copper (DPC) ceramic substrate.

Batch no.	**Junction structure**	**Edge term.**	z_{sub} **(µm)**	**Die size (mm)**	**Anode size (mm)**	**Size code**	**Anode metal**	**Package type**
B1	trench	FP	500	–	$\varnothing = 0.3$	XS	Al	TO247
B2a	planar	none	200	2.2×3.8	1.6×1.6	ML	Ni/Au	TO247
B2b	planar	none	200	2.2×2.2	1.6×1.6	ML	Ni/Au	DPC
	planar	none	200	2.2×3.8	1.6×1.6	ML	Ni/Au	DPC
B2c	planar	none	600	2.2×2.2	1.6×1.6	ML	Al	DPC
	planar	none	600	3.8×3.8	3.2×3.2	LL	Al	DPC
B3	planar	FP, GR	600	3.4×4.2	1.6×1.6	ML	Ni/Au	TO247
B3	planar	FP, GR	600	3.3×3.3	2.4×2.4	L	Ni/Au	TO247
B3	planar	FP, GR	600	4.1×4.1	3.2×3.2	LL	Ni/Au	TO247
B4	planar	FP, GR	200	3.4×4.2	1.6×1.6	ML	Al	DPC
B4	planar	FP, GR	200	4.2×4.2	3.2×3.2	LL	Al	DPC

(see also Section 3.3). In addition, double pulse tests are carried out in Section 3.4.6 to confirm the suitability for low-inductive switching tests.

Overview of the types of investigated samples

Table 3.1 provides an overview of the different types of β–Ga_2O_3 diodes studied in this thesis, starting with the first batch received (B1) and ending with the final batch received (B4). The basic structure of state-of-the-art β–Ga_2O_3 diodes is explained in Section 2.3.4. For all samples that have an edge termination, field plates (FP) are based on SiO_2 and guard rings (GR) are nitrogen-ion implanted. The junction is completely unipolar for all samples, i.e., no p-type structures (such as p-NiO) are implemented.

While all samples are Ni/Au metallized on the cathode side of the chip, the anode metallization is either Ni/Au or Al. This affects the assembly process of the dies: On Ni/Au surfaces, soldering and pressureless silver sintering can be performed easily in addition to gold wire bonding [181]. For aluminum metallized surfaces, a thin oxide layer on the metal surface prevents the formation of a bond with conventional soldering or sintering methods [181, 182]. Therefore, only aluminum bond wires are used to electrically connect aluminum metallized anodes.

The first sample received (B1) has a Mo-Ga_2O_3 Schottky contact and a circular anode with a diameter of $0.3\,\mathrm{mm}$. All other diodes have a Ni-Ga_2O_3 Schottky contact and a square anode with one of the sizes ML ($1.6\,\mathrm{mm} \times 1.6\,\mathrm{mm}$), L ($2.4\,\mathrm{mm} \times 2.4\,\mathrm{mm}$), or LL ($3.2\,\mathrm{mm} \times 3.2\,\mathrm{mm}$). Note that some ML-size samples were diced out in a rectangular instead of a square shape. As will be shown in Section 5.2, this has no significant influence on the electrothermal properties. All samples that were obtained as bare dies were assembled on AlN substrates in one of the previously presented ways, depending on the type of available diode and the measurement goal.

Other samples were received already in TO247 packages. Among these samples, only diode B1-XS was attached directly to the lead frame via soldering (cathode) and wire bonding (anode). For all other TO247 packaged samples, the die is soldered to a $0.5\,\mathrm{mm}$ thick CuMo spacer, which itself is soldered to the lead frame. Such spacers can serve as a buffer layer to

Table 3.2: Overview of commercial reference devices used in this thesis. For TO packaged devices, the die and anode size were estimated by optical microscopy after removing the mold mass with a laser. Bare dies were assembled on custom direct plated copper (DPC) ceramic substrates.

Type/ no.	Diode rating	Part number	Die size (mm)	Anode size (mm)	Package type	Ref.
SiC-A	650 V/10 A	CPW20650S010B	1.92×1.92	1.65×1.65	DPC	[235]
SiC-B	650 V/16 A	STPSC16H065A	2.45×2.00	2.25×1.80	TO247	[236]
Si-A	600 V/10 A	DHG20C600PB	3.00×3.00	1.80×1.80	TO220	[237, 238]

reduce thermal strain due to differences in the thermal expansion between die and lead frame. Furthermore, all samples of batch B3 and one sample of batch B2a were sealed with silicone gel instead of being fully molded. More specific information about the diode structure or the assembly process can be found in the respective chapters, if relevant.

In addition to the Ga_2O_3 samples, commercial diodes listed in Tab. 3.2 are used as reference devices to investigate characteristic similarities and differences between them. To determine the die and anode size of the TO packaged diodes, their mold mass was removed by laser ablation and the corresponding dimensions were determined by optical microscopy. The anode sizes of the reference diodes are similar to those of the Ga_2O_3 samples in Tab. 3.1, which enables a fair analysis and comparison of their electrical and thermal properties. This is particularly important for the results derived in Chapters 5 and 6, as will be discussed in more detail in the respective places. Important measurement procedures to examine the basic features of the corresponding devices are explained in the following sections.

3.3 Evaluation of static electrical properties

General remarks

Many characteristic diode properties can be analyzed by measuring their forward and reverse current–voltage characteristics and the capacitance–voltage profiles. In this work, a Keysight B1505A power device analyzer [239] is used for this purpose. As this device is widely known, only the most important measurement and evaluation procedures will be explained in the following by the example of the commercial reference diode SiC-A. This on the one hand validates the measurement settings and on the other hand verifies the functionality of the AlN-DPC package introduced in Section 3.2.

For temperature-dependent measurements, the samples are heated with air in a closed chamber using a Temptronic ATS-545 Thermostream and a k-type thermocouple to determine the temperature. In case of the TO-packaged samples, the thermocouple is placed on the metal lead frame below the presumed chip location. A thin heat conductive sheet is used to electrically isolate the sensor from the lead frame. In the case of bare dies assembled on AlN-DPC substrates, the sensor is placed on the electrically isolated back side cooling pad below the die. After reaching a $\pm 0.5\,\mathrm{K}$ window around the target temperature, a waiting period of $15\,\mathrm{min}$ is initiated. This ensures a uniform temperature and allows the assumption that the junction temperature is equal to the temperature measured with the thermocouple.

Current–voltage (I–V) characteristics

Regarding the forward characteristics, two different types of measurements are performed. The first one shown in Fig. 3.3a is performed under dc conditions, which provides the highest resolution (typically $100\,\mathrm{pA}$) at low currents below the knee voltage. Under the assumption of current transport via thermionic emission, such measurements can be used to gain insight into the basic junction properties. When plotting the data semi-logarithmic, the saturation current I_s and the corresponding saturation current density $J_\mathrm{s} = I_\mathrm{s}/A$, where A is the active area of the device, can be determined from the intercept of a fit to the linear part of the low-current region below the knee voltage but at voltages larger than $3kT_\mathrm{j}/e$ [45]. The Schottky barrier height $\phi_\mathrm{b,0}$ is then calculated from the saturation current density according to [45]

$$\phi_\mathrm{b,0} = \frac{kT_\mathrm{j}}{e} \cdot \ln\left(\frac{A^{**} \cdot T_\mathrm{j}^2}{J_\mathrm{s}}\right), \tag{3.1}$$

where k is the Boltzmann constant, T_j is the junction temperature, e is the elementary charge, and A^{**} is the Richardson constant. For β–$\mathrm{Ga_2O_3}$, A^{**} is assumed to be $41\,\mathrm{A\,cm^{-2}\,K^{-2}}$, which is calculated from its effective electron mass m_e^* of 0.34 times the electron rest mass [21, 28]. The ideality coefficient n results from the slope [45]

$$n = \frac{e}{kT_\mathrm{j}} \frac{d\,V_\mathrm{D}}{d\ln(J_\mathrm{D}/J_0)}, \tag{3.2}$$

of the fit where V_D is the diode voltage, J_D is the current density, and J_0 is a reference current density of $1\,\mathrm{A/m^2}$. The built-in potential ψ_bi across the junction without image-force lowering then follows from [45, 183]

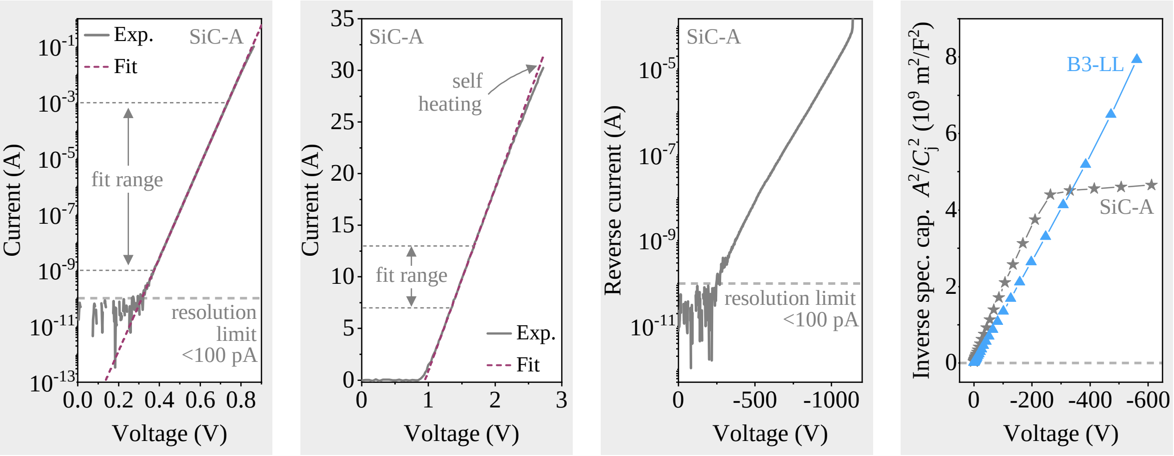
$$e\psi_\mathrm{bi} = e\phi_\mathrm{b,0} - (E_\mathrm{C} - E_\mathrm{F}) = e\phi_\mathrm{b,0} - kT_\mathrm{j}\ln\left(\frac{N_\mathrm{C}}{N_\mathrm{D}}\right), \tag{3.3}$$

where E_F is the Fermi energy, E_C is the energy of the conduction band minimum, and $N_\mathrm{C} = 2(2\pi m_\mathrm{e}^* kT_\mathrm{j}/h^2)^{3/2}$ is the effective density of states in the conduction band. The effective donor concentration N_D can be calculated from capacitance–voltage measurements, as will be discussed in more detail later.

The second type of measurement shown in Fig. 3.3b concerns the high-current region of the forward characteristics. Here, only $200\,\mathrm{\mu s}$ short voltage pulses are applied within a pulse period of $200\,\mathrm{ms}$. This pulse length, which is also commonly found in commercial datasheets [240], is long enough for oscillations in the current and voltage waveforms to fade but short enough to prevent excessive self-heating of the device. The differential on-resistance is obtained from the slope of a straight line fitted to the profile. For $\mathrm{Ga_2O_3}$ diodes, current ratings or other datasheet specifications are not yet defined by the manufacturer and thus not known. The fitting interval is therefore chosen to be within the linear part of the profile, i.e., above the knee voltage but well below the point where self-heating at high currents causes a rise in differential on-resistance. If not specified otherwise, a fitting range from 2 A to 4 A for ML-size diodes, 3 A to 6 A for L-size diodes, and 6 A to 10 A for LL-size diodes is chosen.

Finally, the reverse current–voltage characteristics are measured via a dc voltage sweep. Figure 3.3c shows a typical profile, indicating that the current resolution for this type of measurement is at least $100\,\mathrm{pA}$. In Fig. 3.3c , the reverse bias was increased until breakdown occurred at a voltage of $V_\mathrm{br} = -1140\,\mathrm{V}$. For an ideal planar Schottky diode with a triangular electric field, the average breakdown field can then be calculated from [34]

$$E_\mathrm{br} = \sqrt{2eN_\mathrm{D}V_\mathrm{br}/(\epsilon_0\epsilon_\mathrm{s})}, \tag{3.4}$$



(a) (b) (c) (d)

Figure 3.3: (a) Forward current–voltage (I–V) measurements at low currents with a resolution of about $100\,\mathrm{pA}$ are used to determine the saturation current, ideality factor, and Schottky barrier height. (b) The differential on-resistance r_o is calculated from a linear fit to the pulsed forward I–V profiles above the knee voltage but below the onset of substantial self-heating. (c) The current resolution for reverse I–V measurements is about $100\,\mathrm{pA}$. (d) The effective donor concentration is proportional to the square of the inverse junction capacitance, which allows conclusions about differences in doping profiles. Comparing the profiles measured with the SiC-A reference diode with the datasheet validates the measurement settings and confirms the functionality of the custom AlN-DPC package.

if the effective donor concentration N_D is known. Here, ϵ_0 is the vacuum permittivity and ϵ_s is the relative permittivity of the semiconductor (10 to 12 for β–Ga$_2$O$_3$ [184]).

Capacitance–voltage (*C*–*V*) characteristics

For voltage-dependent capacitance measurements, a reverse dc bias voltage is superimposed upon an ac measurement voltage. The change dV in the ac voltage signal leads to a displacement dQ of the charge stored in the depletion region, through which the associated capacitance is determined [45]. If not specified otherwise, the measurement frequency and amplitude are set to $1\,\mathrm{MHz}$ and $25\,\mathrm{mV}$. Based on the C–V profile, the associated capacitive charge Q_c and capacitance stored energy E_c can be calculated from

$$Q_\mathrm{c}(V_\mathrm{D}) = \int_0^{V_\mathrm{D}} C_\mathrm{j}(V'_\mathrm{D})\,\mathrm{d}V'_\mathrm{D} \tag{3.5}$$

$$E_\mathrm{c}(V_\mathrm{D}) = \int_0^{V_\mathrm{D}} C_\mathrm{j}(V'_\mathrm{D})V'_\mathrm{D}\,\mathrm{d}V'_\mathrm{D}\,, \tag{3.6}$$

where V_D takes negative values. Capacitance–voltage measurements can also be used to determine the effective donor concentration N_D of the epitaxial layer of the investigated samples. When the reverse bias voltage –V_D is increased, the depletion region extends further into the epitaxial layer. From Eq. 2.4 it follows that N_D can directly be determined from the slope of a C_j^{-2} versus V_D plot [183]

$$N_\mathrm{D} = \frac{-2}{e\epsilon_0\epsilon_\mathrm{s}A^2} \cdot \left(\frac{dC_\mathrm{j}^{-2}}{dV_\mathrm{D}}\right)^{-1}. \tag{3.7}$$

Figure 3.3d shows the corresponding plot exemplarily for a SiC-A reference diode and a B3-LL type Ga_2O_3 diode. To take into account the difference in the active area, the capacitance is normalized to the respective anode area. For various analyses, only the background doping concentration near the Schottky junction is of interest. If not specified otherwise, the fitting interval is therefore restricted to the low voltage region up to $-3\,\mathrm{V}$. In case of the Ga_2O_3 diodes, this is also reasonable as the practically constant slope up to $-600\,\mathrm{V}$ suggests a rather homogeneous doping concentration through the entire thickness of the epitaxial layer. Taking the SiC-A reference diode as another example, the slope decreases drastically for voltages below $-200\,\mathrm{V}$, which suggests an increase in the effective donor concentration.

Once the basic electrical properties of the Ga_2O_3 samples are known and it is confirmed that they can sustain a sufficiently large reverse voltage, they can be subjected to switching tests. As shown in the following section, these tests require advanced sensor technologies to achieve reliable results.

3.4 Capturing nanosecond switching transients

3.4.1 General basics of double pulse testing

Basics and motivation

The dynamic electrical properties of power semiconductor devices can be studied by assembling them in a buck converter or half-bridge topology (see Fig. 2.1a) and performing double pulse tests. The probes used to capture the transients can significantly affect the measurement accuracy. Current sensors are especially critical components, as they have to be placed in the current path of the commutation loop. This affects the commutation-loop inductance and with that also the behavior of the switching cell. To enable a sound analysis of the switching properties of novel Ga_2O_3 diodes, it is therefore vital to select a sensor with an acceptable tradeoff between parasitic inductance and bandwidth. An additional galvanic isolation of the sensor is advantageous to facilitate potential-independent measurements. Since common current sensors do not provide all necessary features to accurately capture switching transients in the range of just some nanoseconds, this section investigates novel current sensors. Parts of Section 3.4 have been published in [257] during the course of this thesis.

Measurement uncertainty considerations

The true impulse rise time $T_{\text{a,true}}$ of a signal, usually defined between $10\,\%$ and $90\,\%$ of the final value, can only be determined with a certain accuracy. The inherent rise times $T_{\text{a,sense,i}}$ of the measurement instruments lead to an experimentally determined rise time of $T_{\text{a,exp}} = (T^2_{\text{a,true}} + \Sigma_i T^2_{\text{a,sense,i}})^{1/2}$ [185, 186]. The error associated with the measurement can therefore be expressed by [186]

$$K_{\text{bw}} = \frac{T_{\text{a,exp}}}{T_{\text{a,true}}} - 1 = \sqrt{1 + \frac{\Sigma_i T^2_{\text{a,sense,i}}}{T^2_{\text{a,true}}}} - 1\,. \tag{3.8}$$

Instead of $T_{\text{a,sense,i}}$, often the equivalent $-3\,\mathrm{dB}$ bandwidth B_{i} of the components, which is related to the rise time by $B_{\text{i}} = 0.35/T_{\text{a,sense,i}}$ [185, 186], is specified by the manufacturers. Assuming a bandwidth of the oscilloscope of 1 GHz (which is given for the equipment used in this thesis), the expected measurement uncertainty expected for different sensor bandwidths

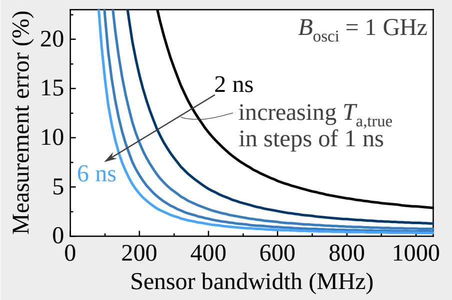


Figure 3.4: Estimation of the measurement error K_{bw} associated with the sensor's bandwidth when capturing switching transients with a true rise time between $2\,\text{ns}$ and $6\,\text{ns}$ using an oscilloscope with a bandwidth B_{osci} of $1\,\text{GHz}$.

according to Eq. 3.8 is shown in Fig. 3.4. To achieve an uncertainty K_{bw} of less than $5\,\%$ for a $3\,\text{ns}$ short transient, e.g., the bandwidth of the sensor should be at least $400\,\text{MHz}$. In addition, ringing caused by the LC circuit of junction capacitance and loop inductance $L_{\text{p,loop}}$ can be in the range of several hundreds of MHz (e.g., $356\,\text{MHz}$ for $L_{\text{p,loop}} = 5\,\text{nH}$ and $C_{\text{j}} = 40\,\text{pF}$ for SiC-A at $400\,\text{V}$) and needs to be resolved properly.

3.4.2 Experimental procedure to assess novel current sensors

Current sensors under investigation

Table 3.3 provides an overview of the current sensors under investigation. The coaxial shunt is commonly used to capture fast switching transients due to its claimed bandwidth of up to $2\,\text{GHz}$ for the SDN-414-05 version used here [241]. Although its inner measurement path is optimized to prevent disturbances by high-frequency effects [187], it was shown that the actual $3\,\text{dB}$ bandwidth can be less than one-tenth of the specified one [188, 189]. Furthermore, the external leads or alternative screw connectors that are used to mount the shunt on a PCB add parasitic inductances of several nH to the commutation loop [190], which affects the switching transients significantly. Nevertheless, since it is widely used, the coaxial shunt is chosen as a well-known reference for all other sensors studied here.

The resistive shunt RL7520WT consists of several paralleled resistors that are combined into a footprint that is short in the direction of the current flow and wide perpendicular to it. Since it is surface mounted on the PCB, it is expected to enable a significantly lower parasitic inductance than the coaxial shunt. However, previous measurements indicate that the inner stray inductance of such types of shunts (but not the exact one used here) can cause the measured current to exceed the actual one substantially [191]. Another resistive shunt that targets a low insertion inductance, high signal fidelity, and high maximum energy input by enhanced power dissipation is the M-shunt [187, 192]. An analysis of the 2016 version of the shunt indicated the combination of an inner stray inductance of several $10\,\text{pH}$ in combination with parasitic inductances as low as $0.4\,\text{nH}$. Here, the updated version from 2021 is studied, for which an insertion inductance of $1.1\,\text{nH}$ was estimated in [193].

Inductive sensors such as the standard Rogowski coil offer an intrinsic galvanic isolation. Although commonly used, Rogowski coils exhibit a maximum bandwidth of only $30\,\text{MHz}$ [243]. Depending on the setup, the coil can be placed around the current-carrying trace, which means that no parasitic inductance is added. Another inductive sensor, which will be referred to as IPM sensor [242] in the following, is formed by a rod-shaped coil that is inserted into a brass cylinder bridging a $20\,\text{mm}$ wide and $0.5\,\text{mm}$ long slit in the current carrying path.

Table 3.3: Characteristic properties (galvanic isolation, insertion inductance, bandwidth) of the different resistive and inductive current sensors under investigation [241, 190, 192–194, 242, 243]. Note that the actual 3 dB bandwidth of the coaxial shunt has been shown to be potentially lower than the one claimed by the manufacturer [188, 189]. Adapted from [257].

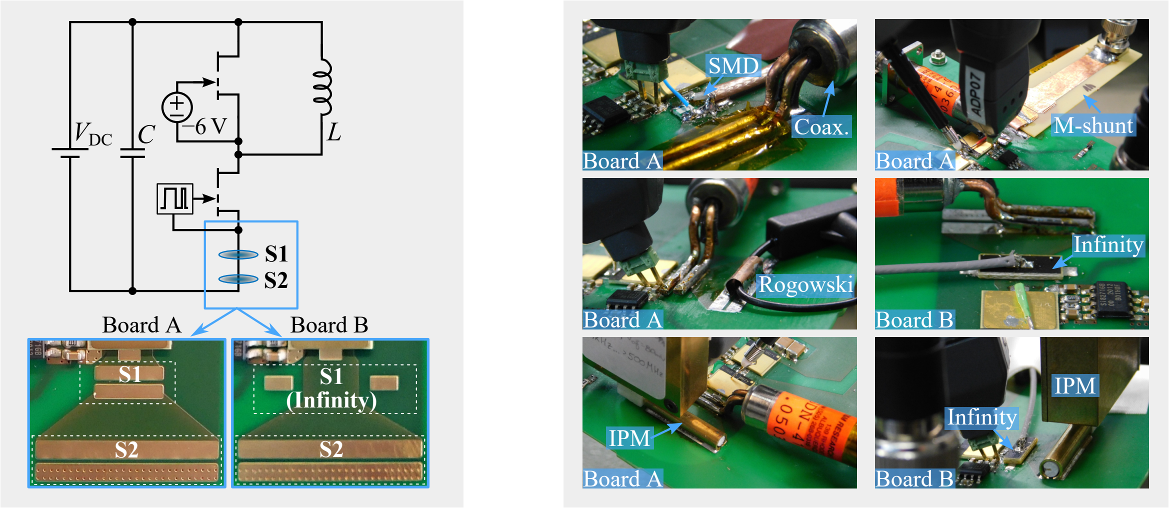
Sensor	Version / Name	Type	Isolation	Inductance (nH)	Bandwidth (MHz)	Manufacturer
Coaxial shunt	SDN-414-05	resist.	no	3–8	2000 (claimed)	T&M Research
SMD shunt	RL7520WT-R050-F	resist.	no	0.3–0.6	not specified	Susumu
M-shunt	Version 2021	resist.	no	0.7–1.1	not specified	Bremen University
Rogowski coil	CWTUM/1x	induct.	yes	≥ 0 (setup-dependent)	30	PEM
Infinity sensor	Generation 1	induct.	yes	0.2	> 225	Bristol University
IPM sensor	Generation 4	induct.	yes	0.3	> 475	Fraunhofer IZM/ ipmdesign

The signal that is picked up by the coil is pre-processed by a built-in analog integrator but requires further bandpass correction. The correction is performed in MATLAB after the measurement with a script provided by the manufacturer [242]. The specific sensor used here was custom-made and optimized for high bandwidth. A tradeoff, however, is that the associated built-in integrator saturates at currents of about $40\,\mathrm{A}$ (the exact value depends on the signal history). In contrast to the IPM sensor, the Infinity sensor [194] allows an inductive current measurement by placing the sensor above the current-carrying trace instead of having to interrupt it. Only the additional space needed on the PCB causes an insertion inductance of about $0.2\,\mathrm{nH}$. The magnetic field is sensed by horizontally aligned coils. The output signal is measured by soldering a coaxial cable directly to the measurement terminals and corresponds to the derivative of the source current [194]. The final waveforms are obtained by integration in MATLAB.

Measurement procedure

To investigate the different current sensors, two double pulse test boards A and B shown in Fig. 3.5a are designed. Each of the two PCBs can fit two current sensors in the commutation loop between DC minus and the transistor. Their layout is identical except for one sensor footprint. By mounting the well-known coaxial reference shunt on either test board A or test board B together with one of the sensors listed in Tab. 3.3, a direct comparison of the captured waveforms is possible.

Two $650\,\mathrm{V}$/$60\,\mathrm{A}$ GaN HEMTs in half-bridge topology are used as switches to enable fast transients exceeding $100\,\mathrm{V/ns}$. The inductance of the vertical commutation loop when modeling the decoupling capacitors as copper blocks is estimated to be between 1.8 to $1.3\,\mathrm{nH}$ in the frequency range of $1\,\mathrm{MHz}$–$1\,\mathrm{GHz}$ using Ansys Q3D. The gate–source voltage (V_{gs}) of the high-side GaN HEMT is kept at $-6\,\mathrm{V}$ while the low-side GaN HEMT is actively switched between a V_{gs} of $-6\,\mathrm{V}$ and $+6\,\mathrm{V}$ using external gate resistors of $1.0\,\Omega$ (turn-off) and $5.1\,\Omega$ (turn-on). Load currents I_{L} between $5\,\mathrm{A}$ and $60\,\mathrm{A}$ are set by varying the duration of the first turn-on time of the low-side GaN HEMT at a constant DC link voltage of $400\,\mathrm{V}$. The sensors are analyzed regarding basic waveforms during turn-on and turn-off, the corresponding current slopes $\mathrm{d}i_{\mathrm{s}}/\mathrm{d}t$ (measured between $10\,\%$ and $90\,\%$ of the load current) as they directly reflect the capability to capture fast switching transients, and the respective switching energies E_{on} and E_{off} as defined in the IEC 60747-9 standard [195]. Differences in the propagation delays



(a) **(b)**

Figure 3.5: (a) Two PCBs with GaN HEMTs in half bridge configuration are designed in a way that each one can fit two current sensors S1 and S2 at the same time. Their layout is identical except for one sensor footprint. (b) This allows to pair each sensor under investigation with the coaxial shunt, which is used as a reference for all measurements. Adapted from [257].

between the current and voltage probes must be considered and deskewed as they significantly affect the determination of the switching energies. Here, this is done by measuring the differences in the propagation delays and precisely aligning the onset of the drop in drain–source voltage ($\Delta V_{\rm ds}$) during turn-on with the onset of the rise in $i_{\rm s}$. Nevertheless, uncertainties in the range of $10\,\%$ can be expected. Since noise or peaks in the waveforms can additionally influence the calculations, e.g., by shifting the integration limits, 15 turn-on and 15 turn-off pulses are captured for each load current and the corresponding median values with the median absolute deviation as error bars are shown in the respective figures.

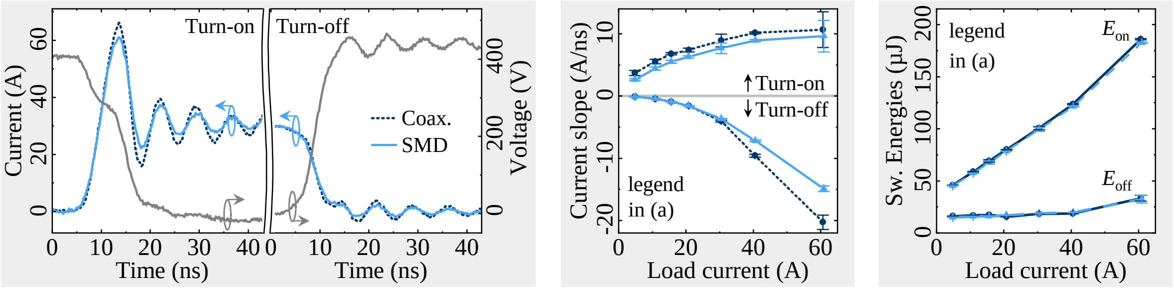
The oscilloscope used is a LeCroy Waverunner 104Xi with a bandwidth of $1\,\mathrm{GHz}$ and a sample rate of 5 GS/s. The drain–source voltage $V_{\rm ds}$ is measured with a $500\,\mathrm{MHz}$ LeCroy PP006-WR passive probe. Note that the passive probe offers high bandwidth but has a defined ground reference. To suppress ground loop effects when performing measurements with two non-isolated current sensors, the ground reference is set between the current sensors for all probes. The current slopes, switching energies, and exemplary waveforms at $I_{\rm L} = 30\,\mathrm{A}$ are discussed in the following for each sensor combination.

3.4.3 Exemplary analysis of switching waveforms

SMD shunt and coaxial shunt

The SMD shunt and the coaxial shunt are mounted together on test board A. The turn-on and turn-off waveforms in Fig. 3.6a show that short transient times in the order of several nanoseconds associated with high turn-off voltage slew rates of $60\,\mathrm{V/ns}$ are achieved at $I_{\rm L} = 30\,\mathrm{A}$. Generally, up to $110\,\mathrm{V/ns}$ are realized at $I_{\rm L} = 60\,\mathrm{A}$. This enables the targeted analysis of the different sensors.

The parasitic commutation loop inductance $L_{\rm p,loop}$ causes ringing with a frequency of about $135\,\mathrm{MHz}$ and a drop $\Delta V_{\rm ds}$ in the drain–source voltage during turn-on when the current rises,



(a) (b) (c)

Figure 3.6: Coaxial shunt and SMD shunt. (a) The captured waveforms during turn-on and turn-off are similar, but the turn-on peak current and the oscillation amplitude are slightly lower with the SMD shunt. (b) The turn-on and turn-off current slopes are also slightly lower, but (c) the calculated switching energies are almost identical. Adapted from [257].

visible as a plateau at about $10\,\mathrm{ns}$. As confirmed by the subsequent measurements, this drop is mainly caused by the insertion inductance of the coaxial shunt. Using

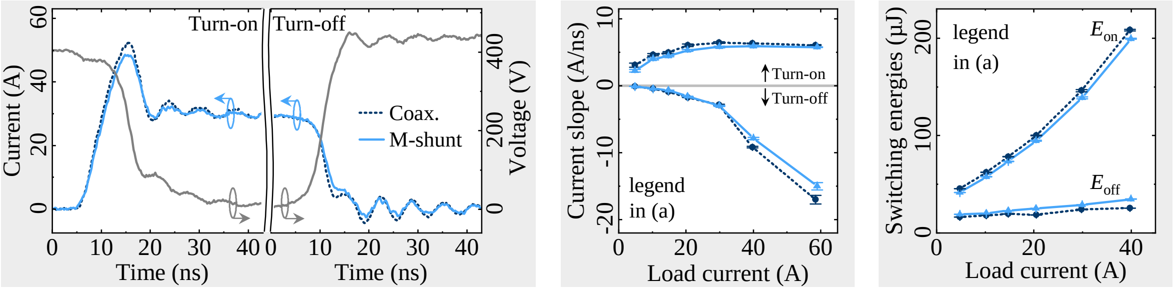
$$\Delta V_{\mathrm{ds}} = L_{\mathrm{p,loop}} \cdot \frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} \tag{3.9}$$

and subtracting the insertion inductance of the SMD shunt as well as the simulated commutation loop inductance yields an insertion inductance of about 5 to $8\,\mathrm{nH}$ for the coaxial shunt, which is consistent with literature [190].

The waveforms captured by the two current sensors are similar in general. The peak turn-on current measured with the coaxial shunt is about $5\,\mathrm{A}$ higher than determined with the SMD shunt. Both sensors capture the oscillations, but the amplitude is slightly higher with the coaxial shunt. The difference is related to the bandwidth of the sensors, or more precisely their specific frequency response, and will be discussed in more detail throughout this section. Note that in contrast to previous reports with other SMD shunts [191] no current overshoot is observed here. This is most likely due to the wide footprint of the SMD shunt with its multiple paralleled resistors, leading to a sufficiently low inner stray inductance.

Sharp transitions in the current waveforms tend to appear rather rounded for sensors with low bandwidth. Since the current slopes are defined between $10\,\%$ and $90\,\%$ of the load current (not the peak turn-on current), this translates to a high sensitivity of the measured $\mathrm{d}i_{\mathrm{s}}/\mathrm{d}t$ to the first hundreds of picoseconds of the transients. Additional peaks or spikes in the waveforms can thus have a significant impact on the calculated $\mathrm{d}i_{\mathrm{s}}/\mathrm{d}t$. In Fig. 3.6b, where the turn-on and turn-off current slopes are depicted, this leads to median absolute deviations of up to $2.5\,\mathrm{A/ns}$ at a median current slope of $9.6\,\mathrm{A/ns}$. This shows that capturing multiple rather than just one switching transient helps to achieve more meaningful results.

The turn-on $\mathrm{d}i_{\mathrm{s}}/\mathrm{d}t$ are slightly lower in case of the SMD shunt for all load currents. During turn-off, the absolute $\mathrm{d}i_{\mathrm{s}}/\mathrm{d}t$ are similar up to $4\,\mathrm{A/ns}$ at $I_{\mathrm{L}} = 30\,\mathrm{A}$ but lower than determined with the coaxial shunt at higher load currents. As will be discussed in Section 3.4.5, this is connected to the change in switching time in combination with the sensor bandwidth. Figure 3.6c shows that the turn-on and turn-off switching energies agree well despite the slight difference in the switching waveforms.



(a) **(b)** **(c)**

Figure 3.7: Coaxial shunt and M-shunt. (a) The turn-on and turn-off waveforms are similar. The slightly lower peak turn-on current in case of the M-shunt, and (b) the slightly lower current slopes lead to (c) a miniscule lower turn-on energy and a minuscule higher turn-off energy. Adapted from [257].

M-shunt and coaxial shunt

Figure 3.7a shows the exemplary turn-on and turn-off waveforms at $I_{\mathrm{L}} = 30\,\mathrm{A}$ as captured with the M-shunt and coaxial shunt assembled on test board A. The waveforms are similar and the ringing (frequency about $150\,\mathrm{MHz}$) is less pronounced than previously observed with the SMD shunt in Fig. 3.6a. This indicates a reduction of the parasitic commutation-loop inductance. Using Eq. 3.9 and the same procedure as before, i.e., subtracting the parasitic insertion inductance of the M-shunt and the simulated commutation-loop inductance, the insertion inductance of the coaxial shunt is now estimated to be about $3\,\mathrm{nH}$. This is significantly lower than the previously estimated 5 to $8\,\mathrm{nH}$, the reason being that the exact way of positioning the coaxial shunt on the PCB affects its insertion inductance and the corresponding waveforms significantly.

The amplitude of the oscillations is slightly lower with the M-shunt than with the coaxial shunt, and with a difference of about $3.5\,\mathrm{A}$ this also applies to the peak turn-on current. In [189], measurements of the transfer functions showed that the M-shunt increasingly attenuates signals above about $60\,\mathrm{MHz}$, reaching the $-3\,\mathrm{dB}$ limit at around $200\,\mathrm{MHz}$. A $400\,\mathrm{MHz}$ coaxial shunt version used in this study showed the opposite trend of increasingly amplifying signals, reaching the $+3\,\mathrm{dB}$ limit already at $45\,\mathrm{MHz}$ [189], which agrees with observations made in [188]. This suggests that the true current waveform may be "in between" that of the coaxial shunt and the M-shunt.

This also explains the difference in current slopes shown in Fig. 3.7b. During turn-on, they are about 1 to $1.5\,\mathrm{A/ns}$ lower in case of the M-shunt. During turn-off, the absolute current slopes are similar up to $3\,\mathrm{A/ns}$ at $I_{\mathrm{L}} = 30\,\mathrm{A}$ (i.e., at low $\mathrm{d}i_{\mathrm{s}}/\mathrm{d}t$ and thus low frequencies associated with the transients) but slightly lower at higher load currents. Consequently, the turn-on energies are slightly lower and the turn-off energies are slightly higher than determined with the coaxial shunt, but still agree well (see Fig. 3.7c).

Rogowski probe and coaxial shunt

Next, the Rogowski probe and the coaxial shunt are mounted together on test board A. To mount the Rogoswki coil, a small cylinder of copper foil is soldered to the PCB, and the probe is inserted into it. The oscillations after turn-on and turn-off (frequency about $140\,\mathrm{MHz}$) and the drop in V_{ds} during turn-on (Fig. 3.8a) are again mainly caused by the inductance of the coaxial shunt.

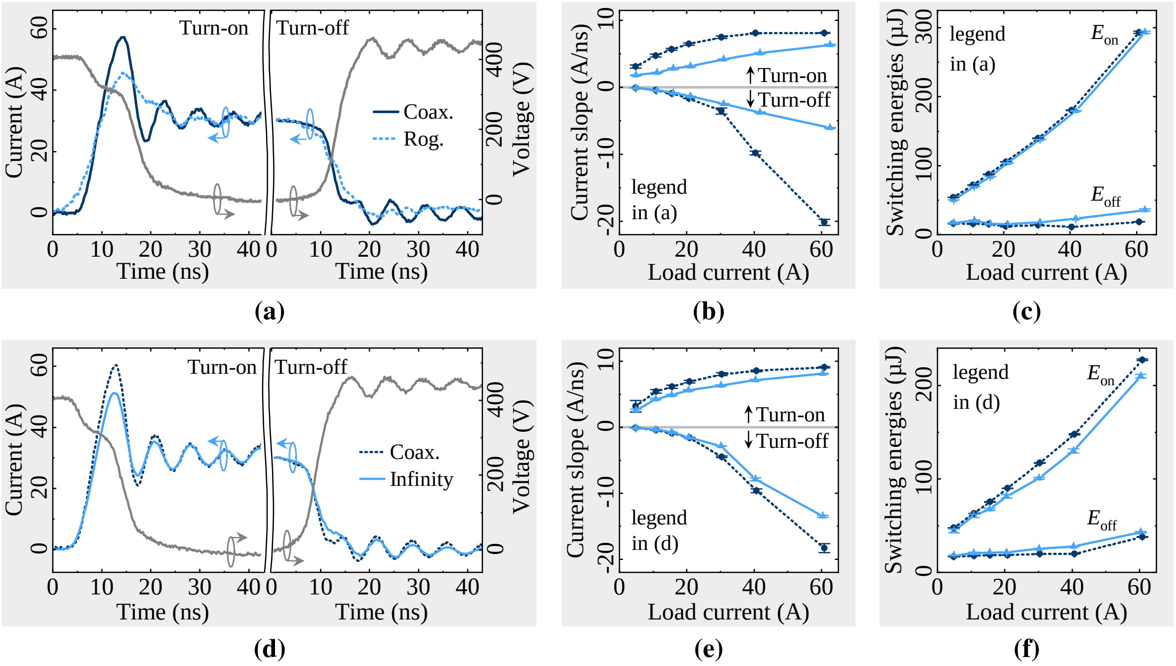


Figure 3.8: (a)–(c) Coaxial shunt and Rogowski probe. (a) The Rogowski probe cannot capture the peak current and ringing accurately and (b) the corresponding absolute turn-on and turn-off current slopes are significantly lower. (c) The switching energies are similar only because of the specific deskew setting: During turn-on, e.g., the energy is overestimated during the first, but underestimated during the second half of the transient. (d)–(f) Coaxial shunt and Infinity sensor. (d) The Infinity sensor can resolve the peak current and ringing more accurately. The slightly lower peak turn-on current in case of the Infinity sensor, and (e) the slightly lower absolute current slopes lead to (f) a slightly lower turn-on energy and a slightly higher turn-off energy. Adapted from [257].

In contrast to the previous measurements, the waveforms measured with the two current sensors differ significantly. The turn-on current peak is broadened in case of the Rogowski probe and the peak turn-on current is approximately $12\,\mathrm{A}$ lower than with the coaxial shunt. Furthermore, the oscillations triggered by the switching transients are not resolved properly both during turn-on and turn-off. The absolute current slopes during turn-on and turn-off (Fig. 3.8b) are significantly smaller with the Rogowski probe (at $\mathrm{d}i_\mathrm{s}/\mathrm{d}t = 10\,\mathrm{A/ns}$, e.g., the difference is about $60\,\%$). It is noticeable that the difference in the measured current slopes increases with rising load current during turn-off, but it decreases during turn-on. This is related to the actual transient time and will be discussed in Section 3.4.5.

Figure 3.8c shows that despite the considerable differences, the calculated switching energies are almost identical. This is solely caused by the specific deskew setting, which is somewhat arbitrary for sensors with low bandwidth: By using the coaxial shunt as a reference, the signal is adjusted in a way that the turn-on peaks and the onset of the oscillations after the turn-on transient (at about $25\,\mathrm{ns}$) are aligned. As the current slope appears too flat due to the low bandwidth, this leads to an overestimation of the switching energy during the first half of the turn-on transient, and an underestimation during the second half. Here, both effects balance each other out. The opposite is the case during turn-off. If in the absence of the reference signal the deskew were set such that the rise in i_s coincided with the drop in V_ds, this would result in E_on being severely underestimated, and E_off being considerably overestimated.

Infinity sensor and coaxial shunt

Figure 3.8d shows the turn-on and turn-off waveforms with the Infinity sensor and the coaxial shunt mounted on test board B at $I_\mathrm{L} = 30\,\mathrm{A}$. As observed before, the ringing (frequency about $140\,\mathrm{MHz}$) and drop in V_ds are mainly caused by the coaxial shunt. The infinity sensor itself does not affect the commutation-loop inductance, however, the necessary slight enlargement of the commutation cell adds about $0.2\,\mathrm{nH}$ [194].

The oscillations after the switching transients are resolved accurately with the amplitude being slightly lower compared to the coaxial shunt, and the peak turn-on current being about $10\,\mathrm{A}$ lower with the Infinity sensor. Again, the absolute current slopes captured with the Infinity sensor are lower than those captured with the coaxial shunt. However, with a difference of about $18\,\%$ at $10\,\mathrm{A/ns}$, the deviation is substantially lower than observed previously with the Rogowski probe.

The similarity of the waveforms shows that the bandwidth of the Infinity sensor is significantly increased (simulated bandwidth: $225\,\mathrm{MHz}$ [194]) compared to the Rogowski probe without having to interrupt the commutation loop. Nevertheless, the slight underestimation of the $\mathrm{d}i_\mathrm{s}/\mathrm{d}t$ leads to slightly higher turn-off and slightly lower turn-on energies, with differences in the range of 5 to $15\,\%$.

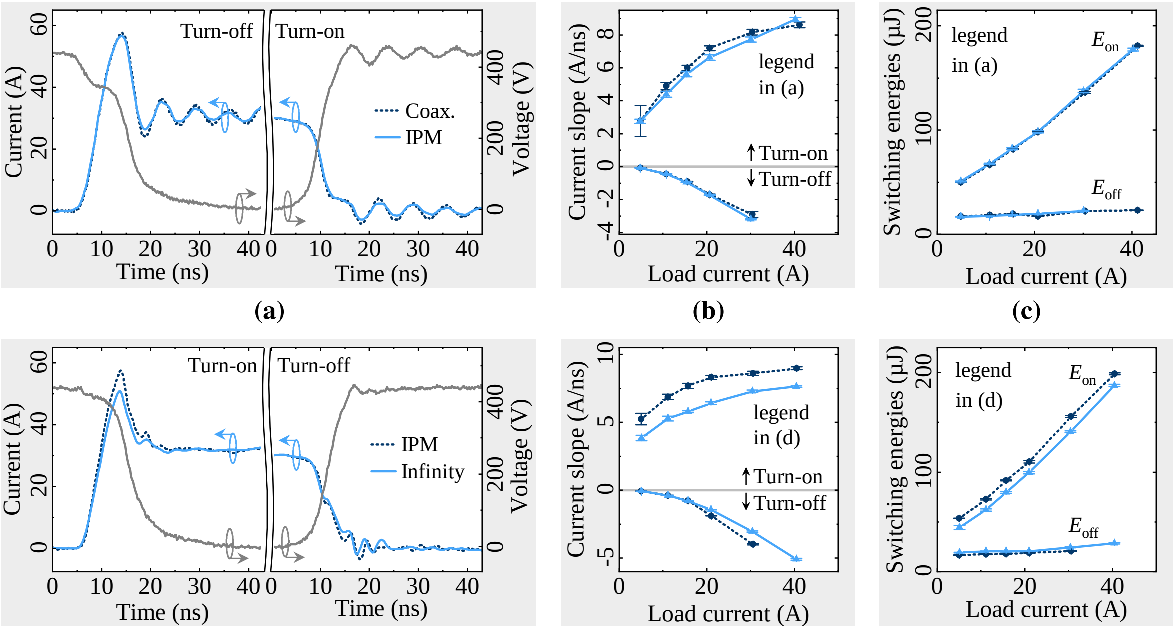
IPM sensor and coaxial shunt

Lastly, the IPM sensor is compared to the coaxial shunt on test board A. The waveforms at $I_\mathrm{L} = 30\,\mathrm{A}$ (Fig. 3.9a) are almost identical, including the plateau at $13\,\mathrm{ns}$ during turn-off. The peak turn-on current as captured with the IPM sensor is about 1 to $2\,\mathrm{A}$ lower than measured with the coaxial shunt, and the amplitude of the oscillations (frequency about $140\,\mathrm{MHz}$) following the switching transients are marginally lower. Again, the drop in V_ds and the ringing is mainly caused by the coaxial shunt, since the assembly with wide brass cylinder in case of the IPM sensor is expected to add only about $0.3\,\mathrm{nH}$ to the loop inductance [242]. The absolute current slopes (Fig. 3.9b) during turn-off are similar. During turn-on, they are slightly lower with the IPM sensor. Note that the sensor saturates at too high currents and current slopes. For this reason, measurements are performed only up to $30\,\mathrm{A}$ for the turn-off, and $40\,\mathrm{A}$ for the turn-on. As shown in Fig. 3.9c, the switching energies are practically identical.

Comparing the results with the previous measurements with M-shunt and coaxial shunt in Fig. 3.7a, it can be seen that the waveforms with IPM sensor deviate from the waveforms with the coaxial shunt in the same direction as observed with the M-shunt, albeit to a lesser extent. Bearing in mind that, as discussed earlier, the coaxial shunt might tend to amplify high frequencies while the M-shunt tends to attenuate high frequencies, this suggests that the IPM sensor could be the closest to the true current waveform.

IPM sensor and Infinity sensor

The previous results identify the IPM sensor and Infinity sensor as two promising galvanically isolated current sensors. The turn-on and turn-off waveforms at $I_\mathrm{L} = 30\,\mathrm{A}$ when mounting the two sensors together on test board B (Fig. 3.9d) differ significantly from the previous ones: First, the drop in V_ds during turn-on is only weakly pronounced. Second, only miniscule oscillations are visible after turn-off and no oscillations are induced after turn-on. This confirms the low-inductive design of the commutation loop and demonstrates the combination of high bandwidth and low insertion inductance achieved with the two novel sensors.



(a) (b) (c)

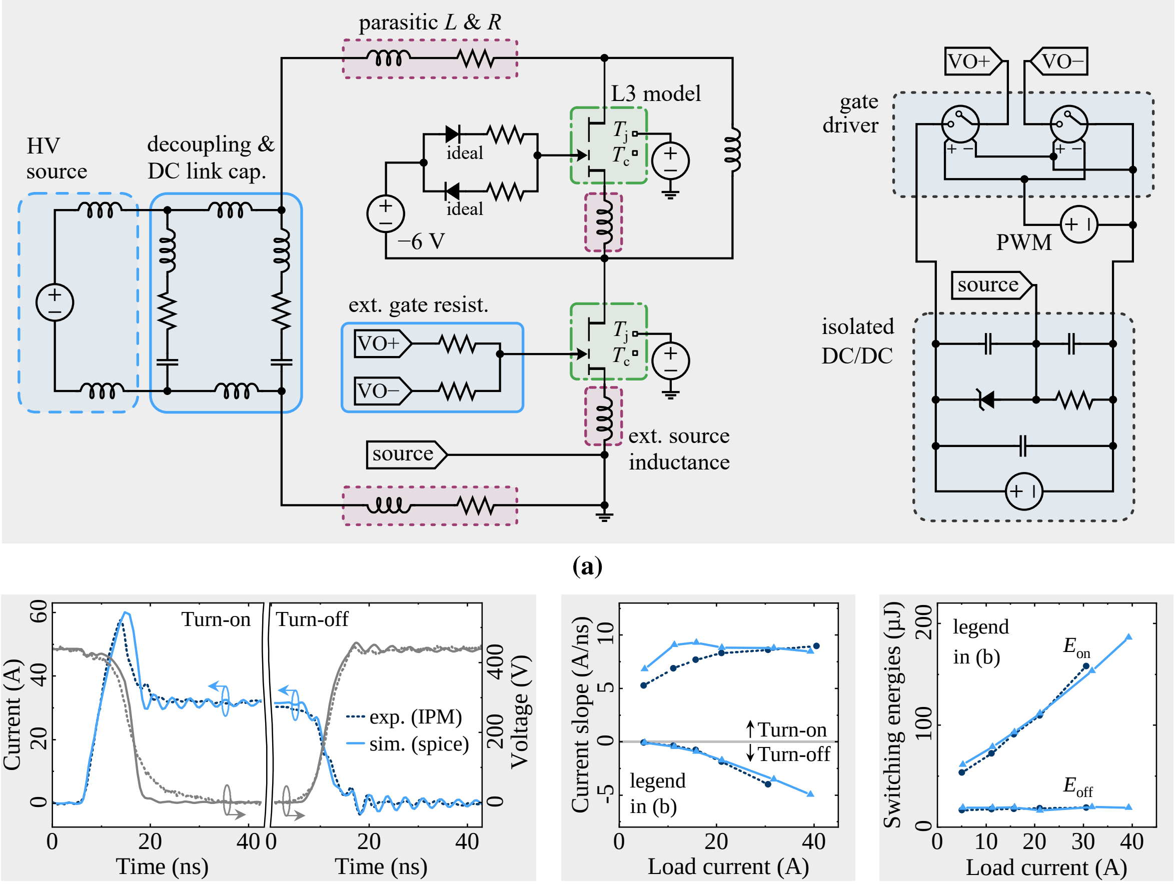
(d) (e) (f)

Figure 3.9: (a)–(c) Coaxial shunt and IPM shunt. (a) The captured waveforms during turn-on and turn-off are almost identical. The turn-on current slopes are slightly lower with the IPM sensor, but the difference in switching energies is negligible. (d)–(f) When IPM and Infinity sensor are mounted on one board, (d) the previously observed ringing and drop in V_{ds} during turn-on vanish, which demonstrates their low parasitic inductance. In agreement with the previous measurements, the turn-on peak current and (e) the current slopes are slightly lower with the Infinity sensor, leading to (f) slight differences in the switching energies. Adapted from [257].

The captured current waveforms are similar. As expected from the previous measurements, the peak turn-on current with the IPM sensor is about $7\,\mathrm{A}$ higher. The current slopes (Fig. 3.9e) with the Infinity sensor are slightly lower (about $1\,\mathrm{A/ns}$ difference at $I_{\mathrm{L}} = 30\,\mathrm{A}$), leading to about 9 to $15\,\mu\mathrm{J}$ lower turn-on and 2 to $4\,\mu\mathrm{J}$ higher turn-off energies (Fig. 3.9f). In comparison with the previous measurements with IPM sensor and coaxial shunt (Figs. 3.9a to 3.9c), E_{on} is slightly increased (e.g., $156\,\mu\mathrm{J}$ here versus $137\,\mu\mathrm{J}$ with coaxial shunt, both at $I_{\mathrm{L}} = 30\,\mathrm{A}$). The reason is that replacing the coaxial shunt with the Infinity sensor leads to a substantial reduction of the commutation-loop inductance. Using Eq. 3.9, it is now estimated to be about $2\,\mathrm{nH}$, which agrees well with the simulated value. During turn-on, this increases the $\mathrm{d}i_{\mathrm{s}}/\mathrm{d}t$ (difference about $0.9\,\mathrm{A/ns}$ at $I_{\mathrm{L}} = 30\,\mathrm{A}$), but also reduces the drop in V_{ds}. The latter aspect leads to a rise in turn-on energy, which agrees with simulations reported in [196].

3.4.4 Simulative validation of measured waveforms

In order to validate the previous measurement results, the experimental setup is replicated in LTspice. The circuit model of the power loop shown in Fig. 3.10a is based on [244] and considers the simulated commutation-loop inductance as well as the wires leading to the high-voltage power supply. The central element is a level 3 model of the GaN HEMT provided by the manufacturer. Various parameters used an input for the simulation are not known precisely but affect the switching waveforms. As discussed previously, even the exact way the sensors are positioned can affect the results. Therefore, to obtain the unaffected ideal waveforms and switching energies, the sensors are not specifically considered in the simulation. However,



(a)

(b) (c) (d)

Figure 3.10: (a) The experimental setup is modeled in LTspice using a level 3 model of the GaN HEMT and considering the simulated parasitic inductances in the commutation loop as well as the connections to the high-voltage source according to [244]. The gate driver model includes the output resistances specified in the datasheet. The corresponding simulation and measurement (the data is taken from the measurement with IPM sensor in Figs. 3.9d to 3.9f) are in agreement regarding (a) the waveforms (b) the current slopes and (c) the switching energies. Adapted from [257].

an additional external common source inductance of 0.1 nH is implemented. This common source inductance critically influences the turn-on and turn-off waveforms. The right part of Fig. 3.10a shows the model of the gate drive circuit. As in the experimental setup, an isolated voltage is supplied and divided into +6 V and −6 V. The gate driver is modeled by two switches with pull-up and pull-down resistances taken from its datasheet (Silicon Labs SI8271GB-ISR).

Figure 3.10b shows the simulated turn-on and turn-off waveforms at $I_L = 30$ A. In addition, the data captured with the IPM sensor in Fig. 3.9a is shown. In this measurement, the IPM sensor was mounted together with the Infinity sensor, providing the lowest additional stray inductance of all setups and making it a reasonable reference. The rising (turn-on) and falling (turn-off) edges of the simulation and measurement almost coincide. With about 57.6 A, the measured peak turn-on current is slightly lower than the simulated one of 60.0 A. Furthermore, the simulated peak is broader than the measured one. The fact that the Infinity sensor in Fig. 3.9a also shows a rather sharp turn-on peak, and an additional verification measurement with IPM sensor and SMD shunt also exhibits the same shape (not shown here), suggests slight inaccuracies in the simulation model rather than the measurements.

As shown in Fig. 3.9b, the turn-off current slopes agree well. During turn-on and at load currents below $15\,\mathrm{A}$, the simulated slopes are about 1.5 to $2.0\,\mathrm{A/ns}$ higher than the measured ones. As discussed before, the data are highly sensitive to roundings of the waveforms at the onset of the rise in i_s. This effect is especially prominent at low load currents and associated short transient times (see also Fig. 3.12). Again, inaccuracies in the LTspice model might cause a certain deviation. As will be discussed in Section 3.4.5, however, it is also likely that the current sensors underestimate the current slopes under these conditions. As shown in Fig. 3.10d, the turn-on and turn-off switching energies are in agreement despite these differences.

Bearing in mind that the simulation results should not be considered as an ideal reference because of the discussed influence of not exactly known circuit parameters, the similarity of measurement and simulation confirms the experimental results. Based on this simulative validation, a comparative analysis of the experimental data is performed in the next section.

3.4.5 Comparison of characteristic quantities

Method of comparing the data

As discussed previously, the current flow in the commutation cell depends on the loop inductance. It is affected by the sensors themselves (even the exact way of positioning the sensor), which complicates the accurate comparison of the sensor properties. With regard to switching energy, even small differences in signal propagation times between the voltage and current probe can affect the results. In addition, the deskew settings are somewhat arbitrary for sensors with low bandwidth, even if the results presented here agree well. Therefore, the switching energies are not suitable to compare the sensor properties.

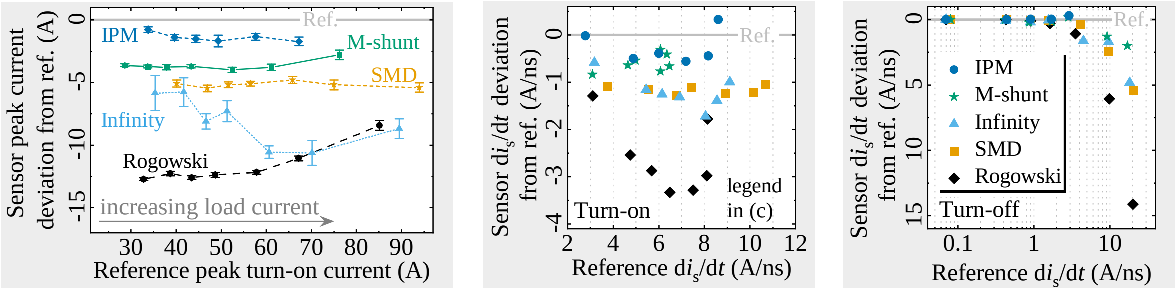
A comparison based solely on characteristic parameters of the captured current waveforms, such as slope and peak, is more meaningful. Due to the different stray inductances, these quantities also differ considerably between the different setups, even when the same measurement conditions are applied. For example, the current slopes and turn-on peak currents differ even with the same load current and gate resistance. Therefore, the coaxial shunt is used as a general reference in the following. All parameters measured with the different sensors are only considered in relation to the value measured by the coaxial shunt in the respective measurement setup. This allows a fair comparison.

Comparison of captured peak currents

Accurate recording of the peak turn-on current is essential, e.g., when investigating the turn-off behavior of the freewheeling diode or the current sharing between paralleled devices. Being aware of the differences between the individual sensors is therefore critical.

When the load current is increased, the peak turn-on current also increases. Figure 3.11a shows how much the turn-on peak current measured with the different sensors deviates from the value measured with the coaxial shunt. The data is interpreted in the following way: If, e.g., the coaxial shunt measured a peak turn-on current of about $60\,\mathrm{A}$ (which is the case at different load currents for the different setups), the M-shunt captured an about $3.8\,\%$ lower and the Infinity sensor and about $10.6\,\%$ lower peak current.

For all sensors and in all measurements, the peak currents are lower than the reference values. This might be connected to the previously discussed potential tendency of the coaxial shunt to



(a) **(b)** **(c)**

Figure 3.11: (a) For all current sensors and for all measurements, the captured peak turn-on currents are lower than the ones determined with the reference coaxial shunt. This might be connected to its potential tendency to amplify high frequencies even below the specified bandwidth. The differences in the current slopes between coaxial shunt and sensors under investigation (b) remain mostly constant during turn-on, but (c) increase substantially during turn-off with rising reference di_s/dt (i.e., with rising load current). This is caused by the opposing change of the transient times. Adapted from [257].

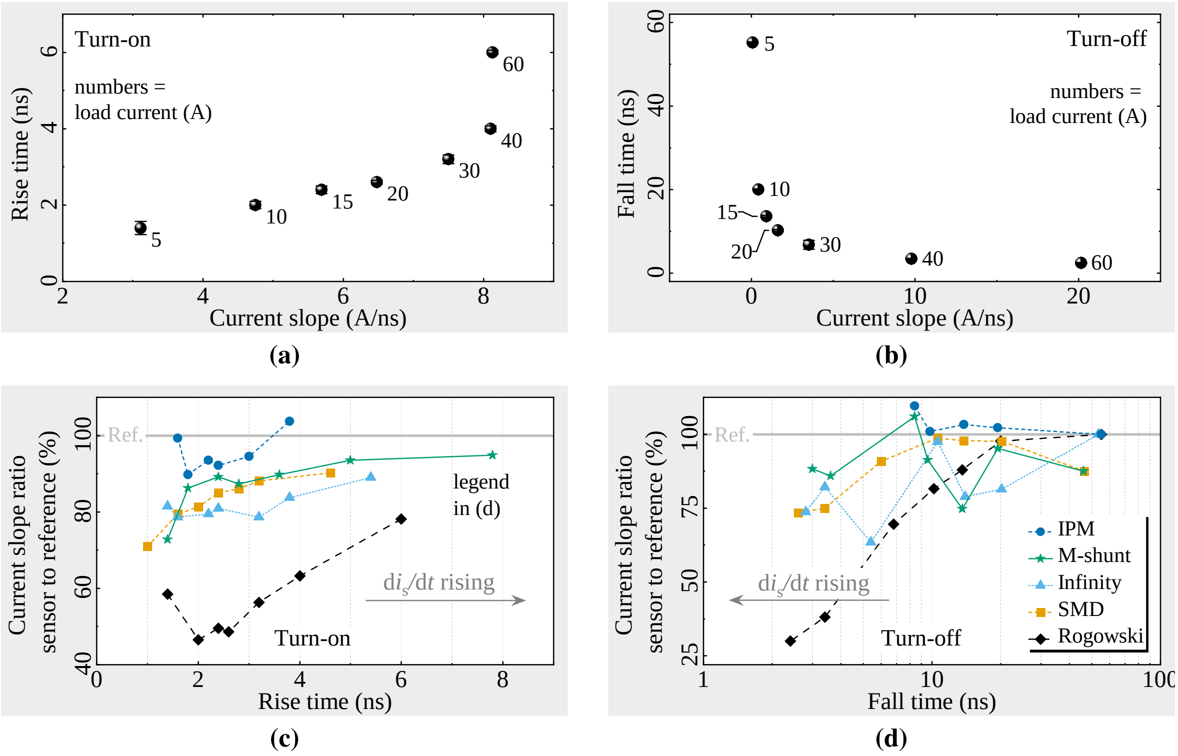
amplify high frequencies even below the specified maximum bandwidth [189]. The M-shunt, on the other hand rather attenuates high frequency signals [189]. At low turn-on currents the deviation increases in the order IPM sensor, M-shunt, SMD shunt, Infinity sensor, Rogowski probe. Regarding the IPM sensor, the M-shunt, and the SMD shunt, the difference is almost independent of peak current. For the Infinity sensor it tends to increase, while it decreases for the Rogowski probe.

Comparison of captured current slopes

Next, the deviation between the current slope measured with the reference coaxial shunt and the various sensors under investigation is compared in the same way as the peak currents. During turn-on (Fig. 3.11b), the current slopes captured with the Rogowski probe are up to $3\,\mathrm{A/ns}$ lower than the reference value, which corresponds to a deviation of more than $50\,\%$. However, the difference shrinks to about $20\,\%$ for the highest di_s/dt, i.e., the highest load currents. For both the SMD shunt and Infinity sensor, the current slopes are about 1 to $1.5\,\mathrm{A/ns}$ lower than the reference ones and rather independent of the reference di_s/dt. With a difference of about $-0.5\,\mathrm{A/ns}$, the IPM sensor and M-shunt show the lowest deviation.

Since the turn-off current slopes change over a large range from $< 0.1\,\mathrm{A/ns}$ to $> 20\,\mathrm{A/ns}$, they are displayed logarithmically in Fig. 3.11c. In contrast to the turn-on, the differences now increase with rising di_s/dt for all sensors. In case of the Rogowski probe, the differences become even larger, with a $70\,\%$ lower slope than the reference when the latter measures $20\,\mathrm{A/ns}$. With about 26 to $27\,\%$ below the reference, Infinity and SMD shunt again exhibit similar results, while with about $-22\,\%$ the M-shunt is again closer to the reference (all at a reference di_s/dt of about 17 to $20\,\mathrm{A/ns}$). The IPM sensor shows the lowest deviation, with a maximum difference of $+0.3\,\mathrm{A/ns}$ at a reference di_s/dt of $3\,\mathrm{A/ns}$.

Taking the coaxial shunt as a reference, it seems that as di_s/dt rises, the ability to resolve fast transients deteriorates at turn-off, but remains the same or even improves at turn-on. To understand this, the change in actual transient times must be taken into account. Figures 3.12a and 3.12b show the rise (turn-on) and fall (turn-off) time as a function of the current slope and the directly connected load current as determined with the coaxial shunt in the setup with Rogowski probe (see Figs. 3.8a to 3.8c). During turn-on (Fig. 3.12a), the current starts to rise



(a) (b)

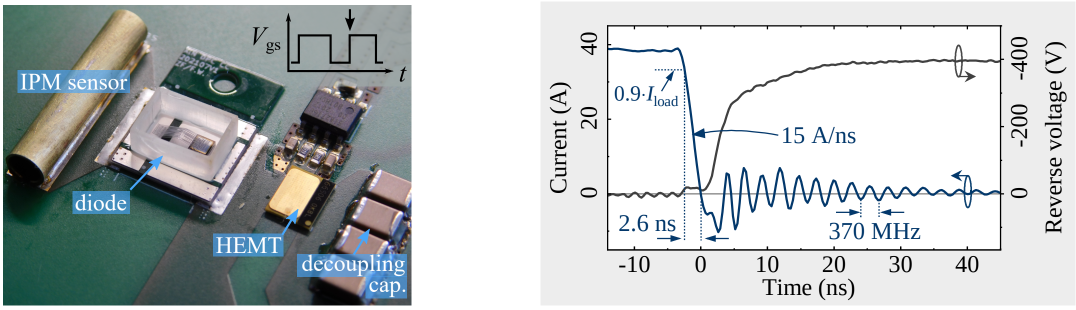
(c) (d)

Figure 3.12: When increasing the load current, (a) the rise time during turn-on increases slightly, but (b) the fall time during turn-off drops substantially. (c)–(d) Deviation of current slew rates measured with the different sensors with respect to the slew rate and transient time determined with the reference coaxial shunt. The deviation decreases with increasing transient time, which corresponds to (c) an increasing current slope during turn-on, but (d) a decreasing current slope during turn-off. Adapted from [257].

after the V_{gs} reaches the threshold voltage and the channel of the low-side becomes conductive. A higher load current results in a steeper rise of the current through the channel. The time required to reach higher load current also grows, resulting in an increase of the current rise time from $1.4\,\mathrm{ns}$ at $I_{\mathrm{L}} = 5\,\mathrm{A}$ ($\mathrm{d}i_{\mathrm{s}}/\mathrm{d}t = 3\,\mathrm{A/ns}$) to $6\,\mathrm{ns}$ at $I_{\mathrm{L}} = 60\,\mathrm{A}$ ($\mathrm{d}i_{\mathrm{s}}/\mathrm{d}t = 8\,\mathrm{A/ns}$). During turn-off, the output capacitance of the HEMT has to be charged by the load current. Increasing load currents reduce this charging time significantly. Therefore, the current slope increases and the current fall time decreases significantly when raising the load current, in the example in Fig. 3.12b from $55\,\mathrm{ns}$ and $\mathrm{d}i_{\mathrm{s}}/\mathrm{d}t = 3\,\mathrm{A/ns}$ at $I_{\mathrm{L}} = 5\,\mathrm{A}$ to $2.4\,\mathrm{ns}$ and $\mathrm{d}i_{\mathrm{s}}/\mathrm{d}t = 20.6\,\mathrm{A/ns}$ at $I_{\mathrm{L}} = 60\,\mathrm{A}$.

As explained in Section 3.4.1, such changes in the transient time directly affect the measurement error associated with the limited bandwidth of the sensors. To consider this effect, Figs. 3.12c and 3.12d compare the current slopes relative to the reference current slopes as a function of the reference current rise and fall time. This way, when taking the coaxial shunt as a reference, an overall either increase of the capability to capture fast $\mathrm{d}i_{\mathrm{s}}/\mathrm{d}t$ or an approximately constant level is visible when the transient time rises. Variations between the sensors are caused by their different internal structures (and potential signal processing units such as electronic integrators in case of the Rogowski probe and the IPM sensor), leading to deviating signal rise times and bandwidths.

The results illustrate the following: During turn-off the transient time decreases and the current slope increases with rising load current, which poses high requirements on the current sensor. During turn-on, however, higher current slopes at high turn-on currents (i.e., longer rise times)



(a) **(b)**

Figure 3.13: (a) The SiC-A reference diode is packaged on an AlN DPC substrate and mounted on a PCB in a buck converter configuration together with a GaN HEMT. (b) Double pulse tests with short switching transients $< 3\,\mathrm{ns}$ and current slew rates of $15\,\mathrm{A/ns}$, as well as a commutation-loop inductance of $4.6\,\mathrm{nH}$ including sensor, diode, HEMT, and decoupling capacitors (estimated from the oscillation frequency after diode turn-off) validate the sensor choice an demonstrate the functionality of the low-inductive package design and assembly procedure.

may actually be captured more reliably than similar or even lower current slopes at lower turn-on currents (i.e., shorter transient times). When evaluating switching transients, this effect must be considered.

3.4.6 Sensor selection and fast switching with custom package

The comparative analysis shows that both the resistive (SMD and M-shunt) and the inductive (IPM and Infinity sensor) current sensors can capture nanosecond switching transients reliably while at the same time achieving a significantly lower stray inductance than the standard coaxial shunt. The sensor choice depends on the application target. The Infinity sensor offers a small footprint with the lowest parasitic inductance. However, a substantial offset can occur at longer time windows with increased DC components (typically longer than about 60 to $100\,\mathrm{ns}$ after the switching transient). The data also show that short transients may not be captured as accurately as, e.g., with the custom-made IPM sensor. Based on the combination of low insertion inductance ($0.3\,\mathrm{nH}$) and high bandwidth ($475\,\mathrm{MHz}$) without excessively attenuating or amplifying high-frequency components, the sensor is used in the following to capture single switching transients.

Figure 3.13a shows a corresponding exemplary setup of a double pulse test with a $50\,\mathrm{m\Omega}$/$650\,\mathrm{V}$ GaN HEMT (GaN Systems GS66508T) and the SiC-A diode (see Tab. 3.2) packaged on a custom AlN DPC substrate (see Section 3.2) and assembled in a buck converter topology (see Fig. 2.1a). The IPM sensor is placed between the anode contact of the diode and HV– potential, similar to Fig. 3.5a. The measurement at a low $R_{\mathrm{g,on}}$ of $2.2\,\Omega$ displayed in Fig. 3.13b shows the turn-off behavior of the diode when the HEMT is turned-on at a load current of about $40\,\mathrm{A}$ and a DC-link voltage of $400\,\mathrm{V}$. The $370\,\mathrm{MHz}$ ringing caused by the LC circuit of diode capacitance ($40\,\mathrm{pF}$ determined with C–V measurements) and loop inductance can be used to estimate the latter one. This way, a low value of about $4.6\,\mathrm{nH}$ is obtained for the loop including the current sensor, the diode, the HEMT, and the decoupling capacitors. Current fall times of $2.6\,\mathrm{ns}$ associated with slew rates of $15\,\mathrm{A/ns}$ demonstrate that fast transients can be achieved with the setup and confirm the functionality of the low-inductive package design. According to Fig. 3.4, a measurement error K_{bw} below $5\,\%$ is expected for the IPM sensor, while a 200 MHz sensor would cause an error of up to 20 %. This consideration further validates the sensor choice.

The slightly lower bandwidth of the M-shunt compared to the IPM sensor and its tendency to attenuate high-frequency components result in a somewhat flatter representation of the switching transients. However, it offers a DC capability as well as higher energy dissipation and lower insertion inductance than the coaxial shunt. Therefore, the M-shunt is used for all applications with continuous current in the following. The SMD shunt is attractive as an easy-to-use and low-cost alternative with comparatively low insertion inductance. Compared to the M-shunt, however, the heat dissipation capability is significantly reduced, and it seems to be slightly inferior in terms of resolving fast transients accurately. Therefore, it is not used in this thesis.

When the devices are operated continuously instead of being subjected to individual pulses only, their temperature rises and their transient thermal properties must be taken into account. The corresponding measurement and evaluation procedures applied to the Ga_2O_3 diodes under investigation will be explained in the next section.

3.5 Evaluation of transient thermal properties

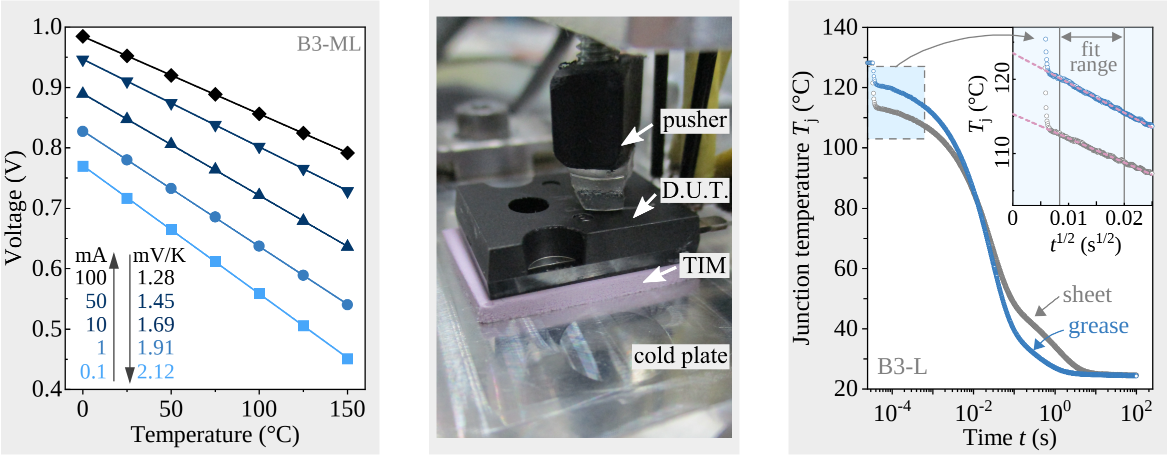
General remarks

During their operation, semiconductor power devices create a considerable amount of heat that must be dissipated to a heatsink. The entire thermal path between the junction, where a major part of the heat is created, and the ambient causes a certain thermal resistance called junction-to-ambient thermal resistance ($R_{\mathrm{th,ja}}$). It affects the thermal management strategy of power converters and determines the maximum possible current and power rating. Measurements of the thermal properties are of special interest for devices made from Ga_2O_3 due to its low thermal conductivity (see Section 2.3.2). All transient thermal measurements are carried out in compliance with the JEDEC JESD51-14 standard [197]. Parts of this section are based on [255].

Temperature-sensitive parameter for Ga_2O_3 diodes

The measurement method is based on a temperature-sensitive parameter (TSP) to determine the junction temperature of the device. In the case of diodes, the forward voltage drop at a certain suitable sensing current is usually used [197]. The temperature T_{j} determined in this way corresponds to the average temperature of the junction area [198].

In order to examine whether the forward voltage drop is a suitable TSP also for Ga_2O_3 diodes, different sensing currents between $0.1\,\mathrm{mA}$ and $100\,\mathrm{mA}$ are applied and the corresponding forward voltage drop is measured for temperatures between $0\,°\mathrm{C}$ and $150\,°\mathrm{C}$. Figure 3.14a shows the results exemplarily for a B3-ML type Ga_2O_3 diode. A linear relationship between the forward voltage drop and the junction temperature is observed for all sensing currents. The corresponding slope, the so-called K-factor, increases with decreasing sensing current. While a high K-factor is desirable in principle, the associated low sensing currents lead to a low signal-to-noise ratio. On the other hand, a too-high sensing current must be avoided to prevent self-heating of the device and ensure a sufficiently high sensitivity. For all further measurements a sensing current of $10\,\mathrm{mA}$ is chosen, leading to a sensitivity of about $1.7\,\mathrm{mV/K}$ for all investigated Ga_2O_3 diodes. This value is similar to that of commercial SiC diodes (e.g., K-factors of $1.61\,\mathrm{mV/K}$ and $1.65\,\mathrm{mV/K}$ at $10\,\mathrm{mA}$ are determined for the reference samples SiC-A and SiC-B, respectively) and allows to use the forward voltage drop as a TSP for thermal resistance measurements.



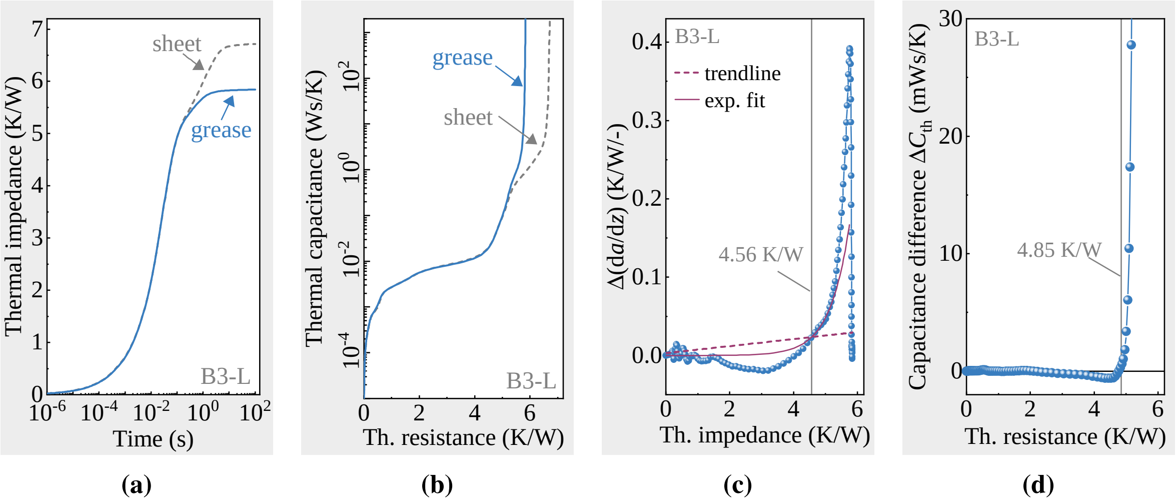
(a) (b) (c)

Figure 3.14: (a) A linear relationship between forward voltage and junction temperature is observed at different sensing currents between $0.1\,\mathrm{mA}$ and $100\,\mathrm{mA}$. The forward voltage at a sensing current of $10\,\mathrm{mA}$ provides sufficient sensitivity and is used as a temperature sensitive electrical parameter. (b) Setup for thermal resistance measurements: A rubber stud presses the device down onto a thermal interface material (TIM) between case and water-cooled heatsink. (c) Temperature response after heating a Ga_2O_3 B3-L type diode for $100\,\mathrm{s}$ with two different TIMs, showing that a measurement duration of $100\,\mathrm{s}$ is sufficient to reach thermal equilibrium. The inset shows the determination of the initial junction temperature using the $\sqrt{t}$-method. Parts adapted from [255].

Transient thermal measurement and evaluation procedure

A T3Ster thermal transient tester from Mentor is used to study the transient thermal properties in accordance with the JEDEC JESD51-14 standard [197]. All related calculations discussed below are performed using Mentor's standard-compliant T3Ster Master software [245]. The experimental setup for all transient thermal measurements is shown in Fig. 3.14b. The samples are mounted in the center of a water-cooled aluminum heatsink (cooling area $47.5\,\mathrm{mm} \times 47.5\,\mathrm{mm}$) with a coolant temperature of $25\,^\circ\mathrm{C}$ and a flow rate of $10\,\mathrm{l/min}$. A rubber stud is screwed down onto the diode with a torque of $60\,\mathrm{cN\,m}$, pressing it down onto a thermal interface material (either a thermally conductive sheet or thermal grease) between casing and heat sink.

During the actual measurement phase, a constant forward current of several amperes corresponding to a heating power P_H is applied and heats up the diode. Then, the heating power is switched off abruptly, and the time-dependent junction temperature $T_\mathrm{j}(t)$ during the subsequent cooling phase is recorded using the previously calibrated TSP. The duration of the cooling phase is equal to the duration of the heating phase. Figure 3.14c shows the temperature response exemplarily for two measurements with a B3-L type Ga_2O_3 diode: one with thermal grease at a heating current of $6.0\,\mathrm{A}$, and one with a heat conductive sheet at a heating current of $5.3\,\mathrm{A}$. The power loss leads to a rise in junction temperature of about 90 to $100\,\mathrm{K}$ for both samples. Since the transients associated with switching off the heating current disturb the measurement signal during the first 50 to $100\,\mathrm{\mu s}$ of the cooling phase, the initial junction temperature T_j0 cannot be determined directly. Instead, it is estimated with the $\sqrt{t}$-method [197]. To this end, the temperature response is plotted against $\sqrt{t}$ and a straight line is fitted to the profile (see inset in Fig. 3.14c). The initial junction temperature then follows from an extrapolation to $t = 0\,\mathrm{s}$.



(a) **(b)** **(c)** **(d)**

Figure 3.15: (a) Thermal impedance profiles and (b) structure functions obtained from transient thermal measurements with a B3-L type Ga_2O_3 diode and two different TIMs. The splitting point of the two curves marks the $R_{\mathrm{th,jc}}$. It is calculated either from (c) the difference of the derivatives of the thermal impedance profiles or (d) the difference of the thermal structure functions according to the JEDEC JESD51-14 standard [197].

It can also be seen that it takes several seconds longer for the setup with heat conductive sheet to reach a steady temperature. However, in both cases the temperature remains nearly constant between $30\,\mathrm{s}$ and $100\,\mathrm{s}$ (temperature difference $< 0.2\,\mathrm{K}$), indicating that a thermal equilibrium is reached within this time. Thus, a heating and cooling time of $100\,\mathrm{s}$ is used for all further transient thermal measurements unless explicitly stated otherwise. With that, the thermal impedance $Z_{\mathrm{th}}(t)$ can be calculated directly from the temperature response [197]:

$$Z_{\mathrm{th}}(t) = \frac{T_{\mathrm{j0}} - T_{\mathrm{j}}(t)}{\Delta P_{\mathrm{H}}} \tag{3.10}$$

Figure 3.15a shows the corresponding thermal impedance profiles with the two different TIMs exemplarily for the B3-L type Ga_2O_3 diode. As explained in detail in [199, 200], the recorded temperature profile basically represents a step-function response $a(t)$ that can be regarded as a sum of single response functions $a_{\mathrm{i}}(t) \propto (1 - \exp(t/\tau_{\mathrm{i}}))$, each with an individual time constant τ_{i}. The individual time constants mathematically correspond to those of individual parallel RC elements, and thus the whole system can be understood as a series connection of individual parallel RC circuit elements. This purely mathematical model based on a one-dimensional heat flow is called Foster model. A transformation to the equivalent Cauer model is helpful to obtain a one-dimensional thermal network with an actual physical meaning. In this model, all capacitances are connected to ground, and each RC section corresponds to a certain element in the experimental setup with its respective thermal capacitance $C_{\mathrm{th,i}}$ and thermal resistance $R_{\mathrm{th,i}}$ (see also Fig. 4.12 in Section 4.4). A common representation of the corresponding heat flow path from the heat source to the heat sink is the so-called structure function, where the cumulative thermal capacitance is plotted against the cumulative thermal resistance [199, 200]. Figure 3.15b shows the corresponding structure functions with two different TIMs exemplarily for the B3-L type Ga_2O_3 diode.

When two measurements with different thermal interface materials are performed, the junction-to-case thermal resistance ($R_{\mathrm{th,jc}}$) can be determined from the splitting point of the two thermal impedance profiles or structure functions following the JEDEC standard [197]. The first procedure relies on the difference of the derivatives of the two thermal impedance curves and is shown for the previously discussed measurement in Fig. 3.15c. When defining $a(z) = Z_{\mathrm{th}}(t_{\mathrm{ref}} \cdot \exp(z))$ with $z = \ln(t/t_{\mathrm{ref}})$ and $t_{\mathrm{ref}}=1\,\mathrm{s}$, the difference of the derivatives follows as $\Delta(\mathrm{d}a/\mathrm{d}z) = (\mathrm{d}a_1/\mathrm{d}z)–(\mathrm{d}a_2/\mathrm{d}z)$. In the next step, an exponential curve of the form $\delta_{\mathrm{Z}} = \alpha_{\mathrm{Z}} \cdot \exp(\beta_{\mathrm{Z}} Z_{\mathrm{th}})$ is fitted to the data, where α_{Z} and β_{Z} are free variables. The $R_{\mathrm{th,jc}}$ then follows from the intersection of this curve and a linear trendline $E_{\mathrm{Z}}(Z_{\mathrm{th}}) = 0.0045 \cdot Z_{\mathrm{th}} + 0.003$. The second procedure is based on the difference of the structure functions and illustrated in Fig. 3.15d. The $R_{\mathrm{th,jc}}$ is defined as the point where the difference ΔC_{th} “clearly starts to rise” [197]. In some cases, the difference rises monotonically. The critical difference used to specify the $R_{\mathrm{th,jc}}$ is then defined as $0.05\,\mathrm{mW\,s/K}$. In other cases, the difference fluctuates around zero before it is followed by a distinct rise (e.g., in [255]). In this case, the last zero-crossing point of ΔC_{th} is defined as $R_{\mathrm{th,jc}}$. The general accuracy of the measurement procedure was verified by measuring the $R_{\mathrm{th,jc}}$ of commercial SiC diodes and comparing them with the datasheet value.

As the two thermal impedance profiles and structure functions split gradually over a certain range, the definition of the separation point is still somewhat arbitrary and the junction-to-case resistances determined by both methods usually differ by a few percent (see also Fig. 3.15) [197]. In addition, the geometry of the die and package strongly affects the structure function and thermal impedance profile [201]. In combination with uncertainties in the exact determination of the initial junction temperature and potential numerical artifacts arising from the various analysis steps, this can result in the two profiles not splitting up precisely at the actual case-to-TIM interface and lead to an inherent uncertainty of up to $15\,\%$ associated with the determination of the $R_{\mathrm{th,jc}}$ [201]. Nevertheless, the method helps to match different sections of the structure function with the corresponding part in the experimental setup, especially when combined with thermal simulations. This constitutes the basis for the investigations in Section 4.3 and Chapter 5.

Summary

The section establishes that the forward voltage drop at a certain sensing current is a suitable temperature-sensitive parameter for Ga_2O_3 diodes. Transient thermal measurements are feasible for the samples under investigation within the general non-negligible inherent measurement uncertainties. Further measurement issues that may result from specific types of Ga_2O_3 diodes will be discussed in the respective sections.

3.6 Chapter conclusion

This chapter introduces the experimental methods used to study Ga_2O_3 diodes. The main aspects can be summarized as follows:

1. While some Ga_2O_3 devices under investigation are TO247 packaged by the manufacturer, other diodes were received as bare dies. A low-inductive package has been designed and an assembly procedure has been developed to allow a variety of different experiments for bare chips with different sizes and surface metallizations.

2. Static electrical measurement procedures to investigate basic junction properties of Ga_2O_3 diodes have been introduced, and typical measurement resolutions have been discussed.

3. To enable a sound analysis of the switching properties of Ga_2O_3 diodes, novel current sensors are evaluated. The IPM sensor is selected to resolve fast transients due to its combination of low insertion inductance and high bandwidth. A measurement error $\leq 4\,\%$ is expected for transients $\geq 3\,\mathrm{ns}$.
4. The forward voltage at a certain sensing current was found to be a suitable temperature-sensitive parameter to determine the junction temperature of Ga_2O_3 diodes. An experimental setup to measure transient thermal properties is established, but inherent uncertainties of up to $15\,\%$ associated with the determination of the junction-to-case thermal resistance have to be taken into account.

The results lay the foundation for further detailed studies on Ga_2O_3 diodes, with a focus on their general characteristic properties in Chapter 4, their thermal properties in Chapter 5, and their switching properties in Chapter 6.

Chapter 4

Basic characteristics of gallium oxide Schottky diodes

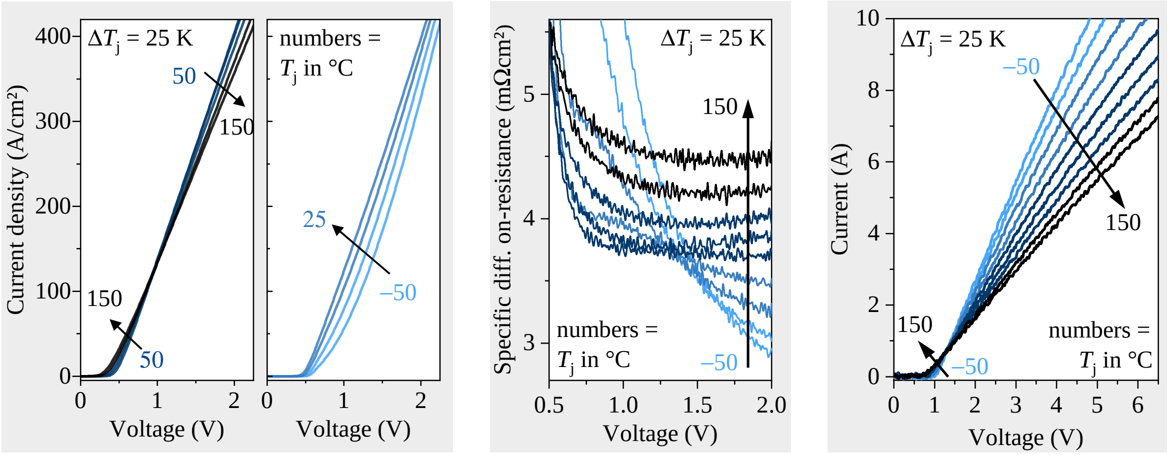
4.1 Chapter overview

Despite noticeable progress in the fabrication of β–Ga$_2$O$_3$ devices, many of their basic characteristics are still not well understood, and especially research on application-relevant large-area devices is lacking. As a first step towards the application of Ga$_2$O$_3$ power diodes, their fundamental properties must be investigated to provide the necessary understanding and basis for more application-oriented experiments. In Section 4.2, physical properties of the Schottky junction are derived from forward and reverse current–voltage and capacitance–voltage profiles. In addition, it is discussed how the diode characteristics can differ between different devices — either because of their intrinsically different structure, or due to a variation of material properties across the wafer as a result of the early level of maturity. Many of the electrical properties are discussed by the example of two different types of TO247 packaged β–Ga$_2$O$_3$ diodes (see overview of devices in Tab. 3.1): an early generation small-area trench MOS diode (B1-XS), and one of the more recently obtained large-area planar diodes (B3-ML). The TO247 package is one of the most commonly used ones in power electronics and serves as a vehicle to enable first measurements. Note that it is known to deteriorate the switching behavior due to its large parasitic inductance of up to about $10\,\mathrm{nH}$ [31, 180], but it does not influence the results presented here. Section 4.3 provides basic considerations on the thermal resistance of Ga$_2$O$_3$ diodes and Section 4.4 introduces a simple method to precisely reproduce unusual electrical characteristics observed for some diodes in the common simulation tool LTspice. Based on the results, further research questions that will be investigated in Chapters 5 and 6 are derived. Parts of the findings presented in this chapter have been published by the author in [253–255, 258] during the course of this thesis.

4.2 Basic electrical properties

4.2.1 Forward conduction characteristics and junction properties

Initial investigations concern the forward current–voltage characteristics. Measurements in the high-current regime show how the standard forward conduction profiles can vary between different diodes, while measurements in the low-current regime allow statements about the junction properties (see Section 3.3).



(a) Sample B1-XS. **(b)** Sample B1-XS. **(c)** Sample B3-ML.

Figure 4.1: The forward current–voltage characteristics at junction temperatures T_j between $-50\,^\circ\mathrm{C}$ and $150\,^\circ\mathrm{C}$ can show significant differences. A change in temperature-coefficient of the forward voltage and a non-constant differential on-resistance at low temperatures is observed for various diodes, as shown exemplarily for a trench MOS diode in (a) and (b). Other diodes exhibit the typical characteristics known from SiC Schottky diodes, as shown exemplarily for a field-plated planar diode in (c). Parts adapted from [253, 254].

Varying forward conduction profiles

First, the forward characteristics of the small-area β–Ga_2O_3 trench MOS diode (B1-XS) are discussed [254]. The basic structure and benefits of this type of diode are explained in Section 2.3.4. For this specific diode, the EFG-grown Ga_2O_3 substrate is $500\,\mu\mathrm{m}$ thick and the HVPE-grown epitaxial layer is approximately $7\,\mu\mathrm{m}$ thin with an effective donor concentration of about 5 to $6 \times 10^{16}\,\mathrm{cm}^{-3}$ after doping with Si. The trenches are approximately $1.5\,\mu\mathrm{m}$ deep and $3\,\mu\mathrm{m}$ wide, the mesas between the trenches are about $2\,\mu\mathrm{m}$ wide. The junction is terminated by a $50\,\mathrm{nm}$ thin HfO_2 layer and $300\,\mu\mathrm{m}$ thick and $75\,\mu\mathrm{m}$ long TEOS-SiO_2 field plates serve as edge termination. The aluminum metallized anode with a diameter of $300\,\mu\mathrm{m}$ yields an active area of about $0.071\,\mathrm{mm}^2$, which is used to calculated all area-related quantities shown in the following.

Figure 4.1a shows the forward current–voltage profiles at junction temperatures between $-50\,^\circ\mathrm{C}$ and $150\,^\circ\mathrm{C}$. The basic functionality at all temperatures confirms that undergoing a standard packaging procedure seems to be feasible for β–Ga_2O_3 devices despite the brittleness. Nevertheless, the forward characteristics show an interesting behavior. Above a junction temperature of $50\,^\circ\mathrm{C}$, the typical characteristics known from SiC Schottky diodes are observed: At low currents the forward voltage decreases with rising temperature (negative temperature coefficient of the forward voltage) because the electron density in the conduction band increases and thus more electrons can gain an energy sufficient to overcome the Schottky barrier [32]. At high currents the forward voltage increases with rising temperature (positive temperature coefficient of the forward voltage) because enhanced phonon scattering decreases the electron mobility in Ga_2O_3 [61] and thus increases the differential on-resistance. As a result, a crossing point with a temperature coefficient of zero is obtained at a current density of about $120\,\mathrm{A/cm}^2$.

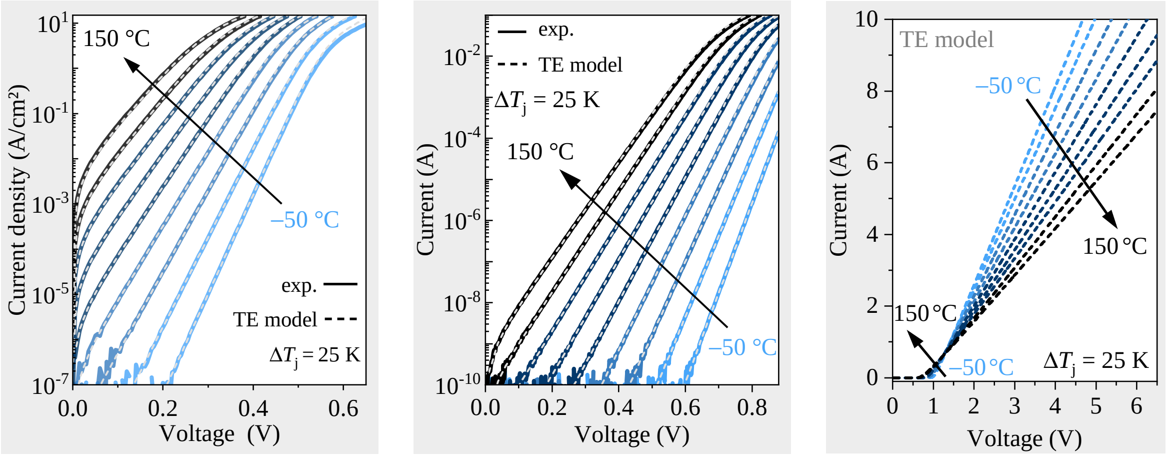
Between $-50\,^\circ\mathrm{C}$ and $50\,^\circ\mathrm{C}$, however, the forward voltage and with that also the conduction losses decrease with rising temperature over the entire voltage and current range. Furthermore, the profile is considerably curved at junction temperatures below $0\,^\circ\mathrm{C}$, which can also be seen from the non-constant differential on-resistance in Fig. 4.1b. For temperatures above about $50\,^\circ\mathrm{C}$ it reaches a constant value above about $150\,\mathrm{A/cm^2}$. For low temperatures, it continues to decrease with higher currents. Such curved current–voltage profiles with negative temperature-coefficient of the forward voltage are typical for bipolar diodes [202, 203]. As explained in Section 2.3.2, however, β–Ga$_2$O$_3$ cannot effectively be p-type doped and the investigated device does not contain a different p-type semiconductor (such as p-NiO) in its structure.

Such curvature and change of sign of the temperature coefficient are observed for multiple (but not all) Ga$_2$O$_3$ diodes under investigation in this thesis that differ in substrate thickness (e.g., $200\,\mu\mathrm{m}$ or $600\,\mu\mathrm{m}$), size (i.e., small-area and large-area diodes), structure (e.g., trench diode or planar diode), and packages (e.g., molded TO package or assembly on AlN substrate without further sealing, wire-bonded or double-side sintered). The junction temperature at which the temperature coefficient changes can differ but is usually found to be between $50\,^\circ\mathrm{C}$ and $100\,^\circ\mathrm{C}$. SiC reference diodes packaged in the same way do not exhibit this behavior (see also Fig. 3.3).

A decrease in on-resistance and a negative coefficient of the forward voltage with rising temperature was also observed for a planar β–Ga$_2$O$_3$ diode in [141] and a β–Ga$_2$O$_3$ trench diode in [166] for junction temperature up to $200\,^\circ\mathrm{C}$. It was supposed that this could result from thermal lattice vibrations: Since the vibrations increase with rising temperature, electrons could gain a sufficient amount of energy to overcome the Schottky barrier [141, 166]. In both studies, however, no change in the direction of the shift, i.e., the sign of the temperature coefficient is reported, and no curvature of the forward current–voltage profile (i.e., higher than expected differential on-resistance at low temperatures and low forward voltages) is mentioned.

For other Ga$_2$O$_3$ diodes in this thesis, the temperature coefficient of the forward voltage at high current densities is positive for all temperatures. An example of a large-area planar β–Ga$_2$O$_3$ diode with field plates (B3, ML type) is shown in Fig. 4.1c. The diode was fabricated on a $600\,\mu\mathrm{m}$ thick EFG-grown substrate and has a $1.6\,\mathrm{mm} \times 1.6\,\mathrm{mm}$ large gold metallized anode. This corresponds to an active area of about $2.4\,\mathrm{mm^2}$. The HVPE-grown epitaxial layer exhibits an effective donor concentration of about $9 \times 10^{15}\,\mathrm{cm^{-3}}$, as determined by capacitance–voltage measurements according to the procedures described in Section 3.3. The maximum current of $10\,\mathrm{A}$ corresponds to a current density of about $400\,\mathrm{A/cm^2}$, which means that the scaling is similar to that in Fig. 4.1a. With $11.5\,\mathrm{m\Omega\,cm^2}$, the specific on-resistance at $25\,^\circ\mathrm{C}$ is about twice as much as that of the trench diode, but the typical characteristics known from SiC Schottky diodes [202, 203] are observed. It should be noted that the parasitic resistance of the package is in the order of $0.3\,\mathrm{m\Omega}$ [31], which is $\ll 1\,\%$ of the differential on-resistance and does therefore not affect the measurements.

The results suggest that the changing temperature coefficient and curvature are not caused by the packaging or other assembly-induced issues. Instead, there seems to be a resistance-modulating effect in the Ga$_2$O$_3$ diode that counteracts the increase in electron mobility at lower temperatures and low forward currents under specific conditions. To clarify the origin, a further combined analysis of the impact of growth conditions and device processing techniques on the device characteristics must be performed by the device manufacturers. For an application in automotive power electronics, this issue can be of importance, e.g., regarding the paralleling of devices or the design of power modules as the lowest power loss and thus optimal operating point may be reached at a certain junction temperature at which the temperature coefficient



(a) Sample B1-XS. **(b)** Sample B3-ML. **(c)** Sample B3-ML (sim.).

Figure 4.2: Below the knee voltage and at junction temperatures between $-50\,°\mathrm{C}$ and $150\,°\mathrm{C}$, both the (a) B1-XS trench MOS and (b) B3-ML planar diode show a decrease of the forward voltage with rising temperature. Modeling with the thermionic emission (TE) model shows a good agreement in both cases. (c) By using the TE model with a constant differential on-resistance according to Eq. 4.1, the forward characteristics of the planar B3-ML diode from Fig. 4.1c can be modeled precisely, whereas large deviations above the knee voltage are obvious for the trench diode (not shown here). Parts adapted from [254].

changes directions. To gain further insight into the junction properties of both the trench and planar Ga_2O_3 diode type, the forward conduction at low currents is studied in the following.

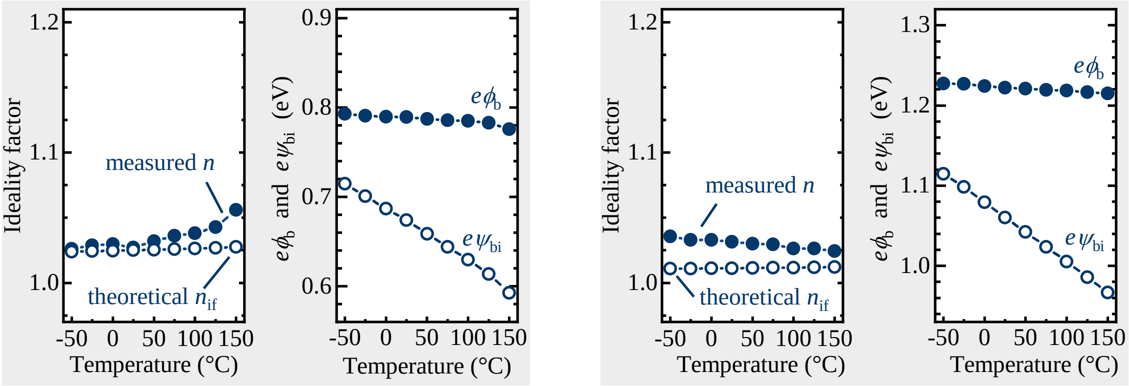
Junction properties at low and high temperatures

The forward characteristics of Schottky diodes can usually be described by the thermionic emission model [45], and it is often used to extract basic junction properties [135, 152, 159, 165, 166]. First, it will be examined in the following whether applying this model to the diodes under investigation is reasonable, considering the unusual forward characteristics above the knee voltage.

The solid lines in Fig. 4.2 show the measured temperature-dependent forward characteristics between $-50\,°\mathrm{C}$ and $150\,°\mathrm{C}$ below the knee voltage exemplarily for the trench-MOS diode B1-XS (Fig. 4.2a) and the planar diode B3-ML (Fig. 4.2b). The saturation current I_s can be determined from the intercept of a fit to the linear part of the low-current region, and the ideality coefficient n follows from the slope of the fit according to Eq. 3.2. The results are shown in Fig. 4.3a and will be discussed later in detail but used for the following consideration already. The ohmic voltage drop across the diode that is mostly caused by the lightly doped drift region dominates the current-voltage profile at high current densities above the knee voltage and leads to a transition from an exponential increase in current with rising voltage to a linear behavior. By including this additional ohmic voltage drop in the thermionic emission model, the forward characteristics can described by [34, 45]

$$I_\mathrm{D} = I_\mathrm{s}\left[\exp\left(\frac{e(V_\mathrm{D} - I_\mathrm{D}\,r_\mathrm{o})}{nkT_\mathrm{j}}\right) - 1\right]. \tag{4.1}$$

The resultant data are shown as dashed lines in Figs. 4.2a and 4.2b for the trench-MOS and the planar diode, respectively. The agreement between measurement and model below the knee



(a) Trench MOS diode (B1-XS). **(b)** Planar diode (B3-ML).

Figure 4.3: Measured (n) and calculated (n_{if}) ideality factors, Schottky barrier height $\phi_{\text{b,0}}$, and built-in potential ψ_{bi} at junction temperatures between $-50\,°\text{C}$ and $150\,°\text{C}$ for (a) a trench MOS diode with Mo as a Schottky metal and (b) a planar diode with a Ni Schottky contact. The barrier height and built-in potential differ in their absolute values but show the same temperature behavior. The ideality factors show opposite trends but are close to the ideal values, indicating a rather homogeneous junction and high temperature stability. Parts adapted from [254].

voltage, where the on-resistance is neglectable, confirms that the thermionic emission model can describe the current transport across the junction accurately for *both* diodes. Figure 4.2c shows the modeled forward current above the knee voltage for the planar diode when the differential on-resistance r_{o} is determined by a linear fit to the current–voltage profiles between $2\,\text{A}$ and $4\,\text{A}$. It agrees with the measured data in Fig. 4.1c at all temperatures and currents, suggesting that standard forward current models can be applied in common simulation tools such as LTspice. For diodes with non-constant differential on-resistance and change of temperature coefficient, the model is accurate at low currents (see Fig. 4.2a) but will evidently cause significant deviations above the knee voltage [254]. A simple method to improve the accuracy of the model is discussed in Section 4.4.

The previous considerations show that the thermionic emission model describes the basic junction properties despite deviations at high currents. Based on that, the Schottky barrier height $\phi_{\text{b,0}}$ and the built-in potential ψ_{bi} across the junction without image-force lowering are derived for different temperatures according to Eqs. 3.1 and 3.3.

Figures 4.3a and 4.3b show the corresponding results exemplarily for the trench MOS diode and the field-plated planar diode. The built-in potential decreases for both diodes with rising junction temperature, which is also apparent from the decrease of the knee voltage in the forward current–voltage profiles, as more charge carriers are thermally lifted into the conduction band. The Schottky barrier height remains almost constant with only a miniscule decrease of less than $0.02\,\text{eV}$ over the entire temperature range for both diodes.

The reason is that the density of states in the conduction band and with that also the energy difference between the conduction band and the Fermi energy $(E_{\text{C}} - E_{\text{F}})$ increases at higher temperatures (see Eq. 3.3) whereas the decreasing built-in potential counteracts this effect. As a result, and as also observed in [52] and [141] for Ga_2O_3 diodes with Pt as a Schottky metal, the Schottky barrier height $\phi_{\text{b,0}} = \psi_{\text{bi}} + (E_{\text{C}} - E_{\text{F}})$ remains approximately constant. For both diodes, the ideality factors are only slightly higher than the ideal value of $n = 1.00$, and they show only a weak temperature dependence. Interestingly, however, the direction of change with temperature is opposite. The temperature dependency and slight deviation from the ideal value can have several reasons known from other semiconductor devices [45, 204].

Tunneling currents can dominate the conduction mechanisms especially at high doping concentrations and low temperatures [45]. The characteristic tunneling energy E_{00} and accordingly expected ideality coefficient n_{tun} [45, 204]

$$E_{00} = (\hbar/2) \cdot \sqrt{N_{\text{D}}/(m_{\text{e}}^{*}\epsilon_0\epsilon_{\text{s}})} \quad \text{and} \tag{4.2}$$

$$n_{\text{tun}} = eE_{00}/(kT_{\text{j}}) \cdot \coth\left(eE_{00}/(kT_{\text{j}})\right) \tag{4.3}$$

can be calculated for both samples. When decreasing the temperature from $150\,°\text{C}$ to $-50\,°\text{C}$ the ideality factors should increase from 1.001 to 1.005 for the trench diode and 1.0002 to 1.0008 for the planar diode according to this theory. While it agrees with the basic trend of increasing ideality factor with decreasing temperature in case of the planar diode in Fig. 4.3b, the effect is too small to explain the measurement data and even within the measurement uncertainty.

The second commonly observed contribution is based on the image-force effect leading to an effective lowering of the Schottky barrier height. The barrier lowering at zero bias voltage $\Delta\phi_{\text{if,0}}$ and the corresponding ideality factors n_{if} can be derived from [205–207]

$$\Delta\phi_{\text{if,0}} = e \cdot \sqrt[4]{e^3 N_{\text{D}}\psi_{\text{bi}}/(8\pi^2\epsilon_{\text{s}}{\epsilon_0}^3{\epsilon_\infty}^2)} \quad \text{and} \tag{4.4}$$

$$n_{\text{if}} = \left[1 - \Delta\phi_{\text{if,0}}/(4e\psi_{\text{bi}})\right]^{-1} , \tag{4.5}$$

where ϵ_∞ is the high-frequency and ϵ_{s} is the low-frequency dielectric constant (approximately 3.6 [208, 209] and 11 [12, 209] for β–Ga_2O_3, respectively). The ideality factors considering the image-force lowering are higher than the ones expected from tunneling only, with about 1.011–1.012 for the planar diode and 1.024–1.027 for the trench diode for temperatures between $-50\,°\text{C}$ and $150\,°\text{C}$. In case of the trench diode (Fig. 4.3a), the calculated ideality factors almost coincide with the measured values for temperatures $\leq 25\,°\text{C}$, while there is a slight deviation at higher temperatures. In case of the planar diode (Fig. 4.3b), the deviations are slightly larger and increase at lower temperatures.

This indicates the commonly observed [165, 166, 210] influence of lateral inhomogeneities of the Schottky barrier caused by potential fluctuations around defects of not atomically flat interfaces [205]. For the Ga_2O_3 diode in [210], e.g., n increases from about 1.1 at about $75\,°\text{C}$ to about 1.4 at $-50\,°\text{C}$, while the Schottky barrier height decreases from about $1.0\,\text{eV}$ to $0.9\,\text{eV}$. In comparison, the barrier height of the diodes under test remains almost constant and the ideality factor changes by less than 0.01 in the same temperature range, showing that the effect is miniscule and the barrier is fairly homogeneous for both diodes under test. The slight increase in ideality factor from about 1.03 to 1.06 between $25\,°\text{C}$ and $150\,°\text{C}$ in case of the trench diode might, e.g., be caused by trap-assisted tunneling of thermally activated charge carriers across the Schottky barrier [165].

The findings illustrate that although Ga_2O_3 diodes can show different forward characteristics, the devices under investigation exhibit a high temperature stability with ideality coefficients close to the ideal values expected from the thermionic emission model. Whether similar statements can be made about the reverse blocking characteristics will be examined next.

4.2.2 Reverse blocking characteristics

The reverse blocking behavior of a diode is characterized in particular by two properties: the reverse current–voltage profiles and breakdown voltage, and the parasitic junction capacitance. Both aspects are covered in this section.

Varying reverse current–voltage profiles

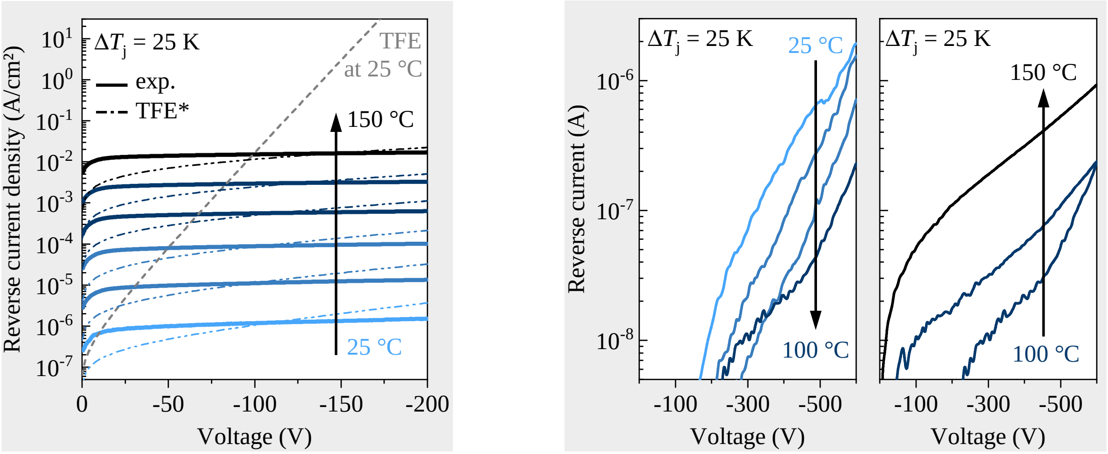
Figure 4.4 shows the reverse characteristics at junction temperatures between $25\,^{\circ}\mathrm{C}$ and $150\,^{\circ}\mathrm{C}$ exemplarily for the two previously discussed types of β–Ga_2O_3 diodes. In case of the trench-MOS diode (Fig. 4.4a), the reverse current increases with rising temperature over the entire voltage and current range, which is also typical for SiC Schottky diodes [235, 211]. The reverse current density $J_{\mathrm{r,TFE}}$ of the metal–semiconductor contact with wide-bandgap materials such as SiC or Ga_2O_3 can be described by the thermionic field emission (TFE) model [45, 50, 52]:

$$\begin{aligned} J_{\mathrm{r,TFE}} = \frac{A^{**} T_{\mathrm{j}} e\hbar E}{k} \cdot \sqrt{\frac{\pi}{2 m_{\mathrm{e}}^{*} k T_{\mathrm{j}}}} \\ \cdot \exp\left(-\frac{1}{kT_{\mathrm{j}}}\left[e\phi_{\mathrm{b,0}} + e\Delta\phi_{\mathrm{if,0}} - \frac{(e\hbar E)^2}{24 m_{\mathrm{e}}^{*}(kT_{\mathrm{j}})^2}\right]\right) \end{aligned} \tag{4.6}$$

All important diode parameters that are necessary for the calculation, such as the built-in potential, the Schottky barrier height, or the image-force lowering, are known already from Section 4.2.1. As explained in Section 2.3.4, the MOS junction is expected to decrease the electric field at the junction and reduce the reverse leakage current by decoupling it from the Schottky barrier height [160]. In comparison, the reverse leakage current should therefore be smaller than for a pure metal–semiconductor junction. Indeed, this behavior is observed in Fig. 4.4a: the reverse current calculated exemplarily for a temperature of $25\,^{\circ}\mathrm{C}$ is several orders of magnitude higher than the measured one. To further illustrate this, the electric field E in Eq. 4.6 is effectively reduced by multiplying it with the RESURF factor introduced in Section 2.3.4. With $\mathcal{R} = 0.3$, the resulting reverse current (marked as TFE* in Fig. 4.4a) reproduces the measurement much more accurately. This indicates that the intended function of the trench MOS structure is effective and that a simple empirical parameter can be used to adjust the profile, which can be helpful to improve corresponding simulation models (see also Section 4.4).

For many other Ga_2O_3 diodes, however, rather unusual reverse profiles are observed. Figure 4.4b shows this exemplarily for the field-plated planar diode B3-ML. Between $25\,^{\circ}\mathrm{C}$ and $100\,^{\circ}\mathrm{C}$, the reverse current decreases with rising junction temperature. At junction temperatures above $100\,^{\circ}\mathrm{C}$, the temperature coefficient changes its sign and the reverse current increases with rising temperature. As evident also from Fig. 4.4a, this is not expected from the thermionic field emission model. It is interesting to note that the trench diode exhibits an unexpected change of the sign of temperature coefficient in forward direction, but a typical reverse current–voltage profile. The opposite is true for the field-plated diode type. In general, all possible combinations were observed for different diodes.

The results indicate contributions to the reverse leakage current other than the typical thermionic field emission. Two possible conduction mechanisms also observed previously, e.g., in GaN [56] and $Al_x(Ga_{1\text{-}x})_2O_3$ [57] diodes, are the tunneling of electrons from the metal to the semiconductor through trap states at the interface (trap-assisted tunneling, TAT) [53, 55],



(a) Trench MOS diode (B1-XS). **(b)** Planar diode (B3-ML).

Figure 4.4: (a) The reverse leakage current of the trench MOS diode increases with rising junction temperature. While the classic thermionic field emission (TFE) model overestimates the reverse leakage current, including an empirical factor that reduces the electric field in the model (referred to as TFE*) results in a better match, showing that the trench MOS junction and field plates are highly effective. (b) For multiple other diodes the leakage current initially decreases and then increases with rising temperature, as exemplarily shown here for the field-plated planar diode type. This unusual behavior is not expected from the classic models such as TFE and suggests additional temperature-dependent contributions such as trap-assisted tunneling (TAT). Parts adapted from [254, 258].

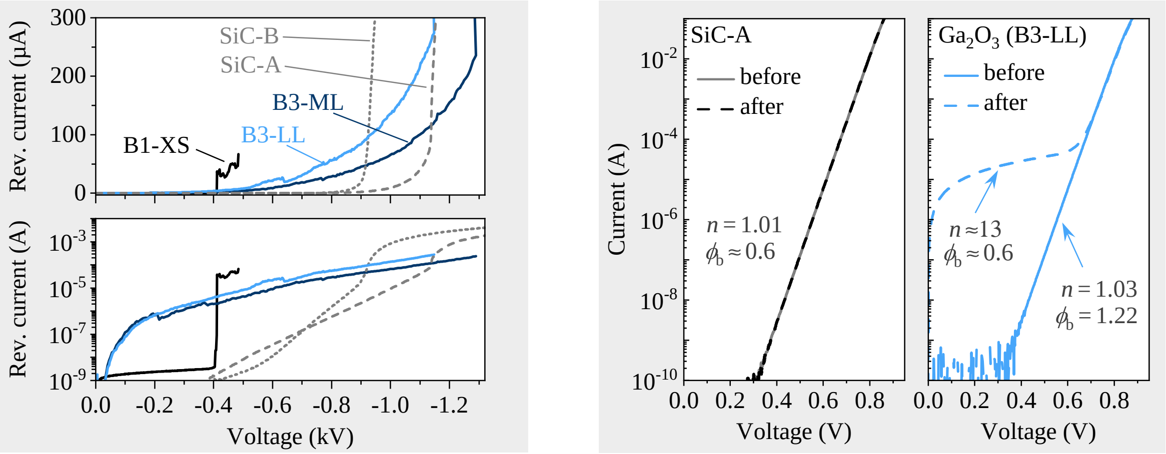
and the Poole–Frenkel emission (PFE) where trapped electrons are emitted into the conduction band through thermal excitation [53, 54].

Indeed, a linear relationship is observed at 25 °C when plotting the logarithmic reverse current density against the square root of the inverse reverse voltage, which is characteristic for a TAT process [56, 57]. At higher temperatures, however, the linear relationship vanishes. This suggests a change of the conduction mechanism with increasing temperature, possibly from dominating tunneling processes through interface states at low temperatures to TFE and/or PFE processes at high temperatures.

Since the unusual change of temperature coefficient is observed for multiple different types of diodes but not all devices under investigation, the effects do not seem to be intrinsic to Ga_2O_3 but rather depend on the device growth and processing parameters. Given the analysis of the Schottky junction properties in Section 4.2.1, which indicates a largely ideal TE behavior at low currents, the additional contribution to the reverse (and forward) current may, at least partly, result from issues with the ohmic contact at the cathode. A more detailed analysis allowing a definite conclusion would require knowledge of the exact growth conditions and material properties, which, however, are not known to the author. Nevertheless, this observation is important for the Spice models developed in Section 4.4.

Reverse breakdown and $V_{\mathrm{br}}{}^2/r_{\mathrm{o,sp}}$ figure-of-merit

Apart from the junction properties, one of the most important figures-of-merit is the tradeoff between on-resistance and breakdown voltage. In Fig. 4.5 the breakdown voltage at room temperature is measured for the two diodes discussed above, i.e., the early generation small-area trench diode (B1, XS size) and the newer planar diode (B3, ML size), as well as a second planar diode with the largest anode size (B3, LL size). The profiles are compared to two



(a)

(b)

Figure 4.5: (a) Reverse breakdown characteristics of three Ga_2O_3 (B1-XS, B3-ML, and B3-LL) and two commercial $650\,\mathrm{V}$ rated SiC diodes in a linear and semilogarithmic representation. Within the rated voltage, the Ga_2O_3 diodes exhibit a several orders of magnitude higher leakage current than the SiC reference diodes, showing the need for a further optimization of the diode structure. Nevertheless, breakdown voltages $> 1.1\,\mathrm{kV}$ can be achieved even for the largest diode. (b) Forward conduction profiles before and after breakdown, exemplarily for the SiC-A reference and the B3-LL Ga_2O_3 diode. The change at low forward voltages in case of the Ga_2O_3 diode reveals a partial destruction of the junction, resulting in an effective barrier lowering and degradation of the blocking capabilities.

commercial SiC diodes (see also Tab. 3.2): a $650\,\mathrm{V}/10\,\mathrm{A}$ rated SiC diode [235] assembled on custom AlN-DPC substrates referred to as SiC-A, and a $650\,\mathrm{V}/16\,\mathrm{A}$ rated SiC diode [236] referred to as SiC-B. Note that all Ga_2O_3 devices underwent multiple measurements at junction temperatures between $-50\,°\mathrm{C}$ and $150\,°\mathrm{C}$ prior to the determination of the breakdown voltage.

In case of the trench diode (B1-XS), the die was fully functional after multiple measurement cycles, but a disconnection of the bond wires at the package lead was revealed by removing parts of the mold mass via laser ablation (see [254] for details). A breakdown voltage of $V_{\mathrm{br}} = 484\,\mathrm{V}$ was determined by reestablishing an electrical connection to the bond wires. Using the previously determined specific on-resistance $r_{\mathrm{o,sp}}$ of $3.45\,\mathrm{m\Omega\,cm^2}$ at $25\,°\mathrm{C}$, this yields a ${V_{\mathrm{br}}}^2/r_{\mathrm{o,sp}}$ figure-of-merit of $68\,\mathrm{MW/cm^2}$. This value is significantly lower than the theoretical limit of about 10 to $40\,\mathrm{GW/cm^2}$ for β–Ga_2O_3 and $3\,\mathrm{GW/cm^2}$ for SiC, but exceeds the unipolar silicon limit by a factor seven (the exact value depends on the theoretical values used for the calculation, see Section 2.3.1).

From another perspective, the relatively high doping concentration of the epitaxial layer leads to a rather high electric field at the junction. Calculating the average breakdown field according to Eq. 3.4 yields 2.8 to $3.2\,\mathrm{MV/cm}$ for the device under test, depending on the exact values of ϵ_{s} and N_{D}. In [135] it was simulated for a β–Ga_2O_3 trench MOS diode of similar structure that the peak electric field in the epitaxial layer should be about $1\,\mathrm{MV/cm}$ lower than the one expected for a regular Schottky diode. Taking this difference into account, the achieved breakdown field is about seven times higher than the theoretical breakdown field of Si, and close to the theoretical SiC limit of $2.5\,\mathrm{MV/cm}$ [12].

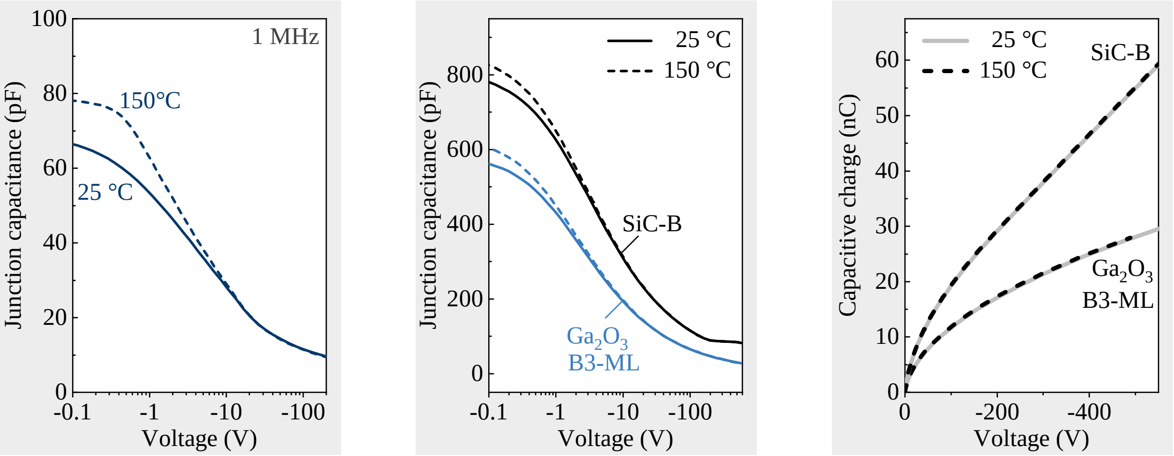
The batch 3 planar diode of size ML broke down at a reverse voltage of $1290\,\mathrm{V}$, corresponding to a breakdown field of about $2.0\,\mathrm{MV/cm}$, which is $80\,\%$ of the theoretical SiC limit and more than a factor 6 higher than the Si limit. The resulting ${V_{\mathrm{br}}}^2/r_{\mathrm{o,sp}}$ figure-of-merit of $145\,\mathrm{MW/cm^2}$ is about a factor of two higher than that of the early generation small-area trench diode. During the course of this thesis, similar and even higher breakdown fields exceeding $6\,\mathrm{MV/cm^2}$ (${V_{\mathrm{br}}}^2/r_{\mathrm{o,sp}}$ figure-of-merit $> 10\,\mathrm{GW/cm^2}$) have been achieved for small-area (anode diameter $< 200\,\mathrm{\mu m}$) Ga_2O_3 diodes [18, 22, 23], showing the promising features of gallium oxide for high-voltage power devices. However, such high values still need to be demonstrated for large-area devices.

Figure 4.5 also shows that the current–voltage profiles up to the breakdown voltage exhibit distinct differences. The trench diode shows an almost constant leakage current up to a voltage of $-410\,\mathrm{V}$, at which point the current rises steeply from $3\,\mathrm{nA}$ to $30\,\mathrm{\mu A}$. A second rather flat region then terminates in a hard and destructive breakdown at $-484\,\mathrm{V}$. The first step presumably indicates a non-reversible soft breakdown caused by an additional leakage path through the oxide layer, which was also observed in other Ga_2O_3 MOS capacitor and trench MOS structures [212]. On the other hand, the planar Ga_2O_3 diodes exhibit a rather uniform exponential growth, followed by a hard and non-reversible avalanche breakdown at $1145\,\mathrm{V}$ (LL) and $1290\,\mathrm{V}$ (ML). Within the specified reverse blocking voltage and up to breakdown voltages of about $1140\,\mathrm{V}$ (SiC-A) and $920\,\mathrm{V}$ (SiC-B), the leakage current of the SiC diodes is several orders of magnitude lower that that of the Ga_2O_3 diodes. In contrast to the Ga_2O_3 diodes, the SiC diodes remain fully functional even after significantly exceeding the onset of avalanche breakdown.

To further study this aspect, Fig. 4.5b compares the forward currents below the knee voltage before and after breakdown exemplarily for the $650\,\mathrm{V}/10\,\mathrm{A}$ rated SiC diode and the planar LL size Ga_2O_3 diode. While entering the breakdown region has no significant effect on the current–voltage characteristics of the SiC diode, a significant increase in current at forward voltages below $0.7\,\mathrm{V}$ can be seen in case of the Ga_2O_3 diode. The corresponding region is associated with a high ideality factor n of about 13 (compared to $n = 1.03$ before breakdown) and a low Schottky barrier height of $0.6\,\mathrm{eV}$ ($1.22\,\mathrm{eV}$ before breakdown). At the same time, a high leakage current of $1\,\mathrm{mA}$ at $-100\,\mathrm{V}$ that increases to the measurement limit of $8\,\mathrm{mA}$ at $-850\,\mathrm{V}$ is observed when repeating the breakdown measurement.

This suggests that the avalanche breakdown in the Ga_2O_3 diodes starts at the edge termination or junction region, leading to substantial damage to the junction structure and degradation of the blocking capabilities. On the other hand, the p-type areas in SiC MPS (Merged Pin Schottky) diodes shield the junction from high electric fields and move the location of the breakdown away from it, which leads to a high avalanche ruggedness [34–36]. Therefore, adopting similar structures, e.g., based on p-type NiO, might be a feasible option for Ga_2O_3 diodes. At this point, however, a more extensive investigation of the breakdown properties was not performed due to the small number of available samples and the associated degradation of the device properties.

With ${V_{\mathrm{br}}}^2/r_{\mathrm{o,sp}}$ figures-of-merit of about $870\,\mathrm{MW/cm^2}$ and $600\,\mathrm{MW/cm^2}$, both the $10\,\mathrm{A}$ and $16\,\mathrm{A}$ rated commercial SiC diodes outperform the Ga_2O_3 devices under test by at least a factor of four. Due to the early stage of development of large-area Ga_2O_3 diodes, it is therefore currently not possible to design power converters exceeding the efficiencies with SiC. However, the most recent progress allows to assess the device properties in first application-relevant high-voltage converter circuits, which is the foundation for Chapter 6.



(a) Sample B1-XS.

(b) Sample B3-ML and SiC-A.

(c) Sample B3-ML and SiC-A.

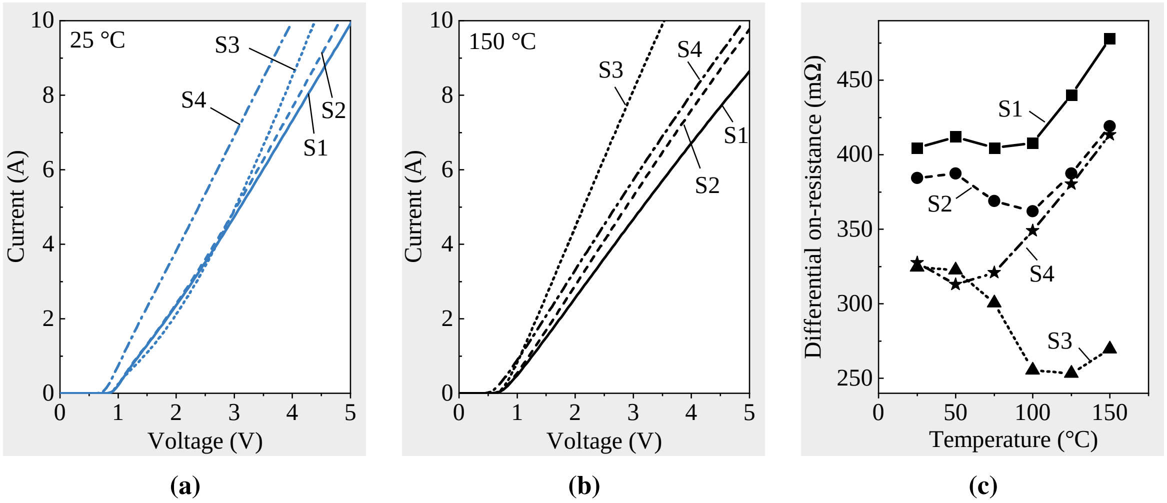
Figure 4.6: The capacitance–voltage profiles of (a) the small-area Ga_2O_3 trench MOS diode and (b) the large-area planar Ga_2O_3 as well as the SiC-B reference diode increase slightly when the junction temperature is raised from $25\,°\mathrm{C}$ to $150\,°\mathrm{C}$. As shown in (c) exemplarily for the SiC reference and ML-size Ga_2O_3 diode, the increase in junction capacitance has a negligible effect on the capacitive charge. Therefore, the switching behavior can be expected to be independent of temperature. Parts adapted from [254].

Stable capacitance–voltage characteristics

The preceding sections show that both the forward and reverse current–voltage profiles can deviate significantly from those of typical SiC diodes, and also between the different types of Ga_2O_3 diodes. This section examines the parasitic junction capacitance of the previously discussed diodes. It is one of the central properties that determines the switching behavior of the devices. Typical capacitance–voltage (C–V) profiles are shown for the B1-XS trench diode in Fig. 4.6a, and for the B3-ML type diode and the SiC-B reference diode in Fig. 4.6b, all at a measurement frequency of $1\,\mathrm{MHz}$ and at junction temperatures of $25\,°\mathrm{C}$ and $150\,°\mathrm{C}$. The basic profile is consistent with those typically observed for SiC diodes, where the capacitance decreases rapidly with increasing reverse bias as the space charge region extends further into the epitaxial layer and depletes it from charge carriers [183].

The junction capacitance at low reverse voltages (above $-10\,\mathrm{V}$) increases slightly at $150\,°\mathrm{C}$, i.e., by about $15\,\%$ for the XS-size Ga_2O_3 trench diode, $8\,\%$ the ML-size field-plated Ga_2O_3 diode, and $6\,\%$ for the SiC-B reference diode. Considering that at low reverse voltages the space charge region is only formed close to the Schottky junction, this may indicate a thermally activated release of charge carriers captured in defects at the metal–semiconductor (or metal–oxide–semiconductor) interface.

Fig. 4.6c shows the capacitive charge resulting from an integration of the C–V characteristics according to Eq. 3.5, exemplarily for the field-plated Ga_2O_3 diode and the SiC reference diode. The slight increase in capacitance at low reverse bias has a negligible effect on the stored charge. Therefore, the switching behavior of the device is not expected to change at high temperatures. The specific (i.e., related to the anode area) charge at voltage of $-400\,\mathrm{V}$ (typical DC link voltage of an automotive inverter) is similar for both diodes, with about $11.4\,\mathrm{nC/mm^2}$ in case of the SiC and $10.4\,\mathrm{nC/mm^2}$ in case of the Ga_2O_3 diode. This value is affected by the doping concentration of the epitaxial layer and determines the switching losses, as will be discussed in detail in Chapter 6 for different types of Ga_2O_3 diodes.



(a) (b) (c)

Figure 4.7: The forward current–voltage profiles of four identical types of Ga_2O_3 diodes of one of the early device generations (batch B2a) differ significantly. (a) At a junction temperature of 25 °C sample S3 shows a strong curvature, samples S1 and S2 show a slight curvature, and sample S4 shows a straight line above the knee voltage. (b) At 150 °C all samples show a constant differential on-resistance. (c) The temperature-dependent differential on-resistance varies by up to 80 % between the samples. The results reveal a strong in-plane variation of electrical properties across the wafer. Adapted from [255].

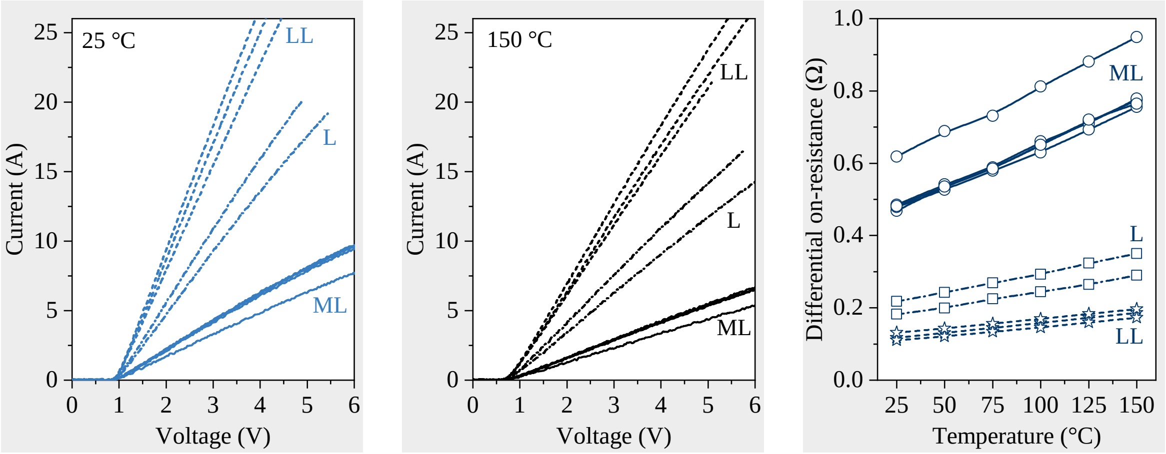
However, the following section shows that these basic properties can vary significantly between different devices, even when they stem from different positions of the same wafer.

4.2.3 In-plane variation of electric properties across the wafer

The fact that the characteristic features of different Ga_2O_3 diodes can differ substantially is also caused by the early stage of device processing technology. This section investigates how large these variations can be. The issue is discussed for an early batch of Ga_2O_3 diodes (B2a) in comparison to a second batch from one of the most recent wafers (B3).

To illustrate the problem, the forward characteristics of four TO247 packaged Ga_2O_3 diodes (B2a) with identical structure are examined. All devices stem from different positions of the same wafer and have a $1.6\,\mathrm{mm} \times 1.6\,\mathrm{mm}$ large Ni/Au anode while the cathode is formed by Ti/Ni/Au layers. Figure 4.7a shows the corresponding forward current–voltage profiles at a junction temperature of 25 °C. Samples S1, S2, and S3 show knee voltages of about 0.9 V while sample S4 shows a significantly lower knee voltage of about 0.7 V. In the case of sample S3, the profile is considerably curved, whereas the profiles of S1 and S2 are only slightly curved, and S4 exhibits a constant differential on-resistance above the knee voltage. At a junction temperature of 150 °C, all samples exhibit a constant differential on-resistance, but the actual values differ significantly.

This is shown in more detail in Fig. 4.7c, where the differential on-resistance is obtained for temperatures between 25 °C and 150 °C by fitting a straight line to the data between forward currents of 3 A and 6 A. For sample S3, a significant decrease in r_o is observed when increasing the temperature from 25 °C to 125 °C. After that, the differential on-resistance increases with rising junction temperature. For samples S1, S2, and S4, the on-resistances remain approximately constant up to about 75 to 100 °C and increase after that. The variation in differential on-resistance between the samples is as high as 80 % at 150 °C. When increasing



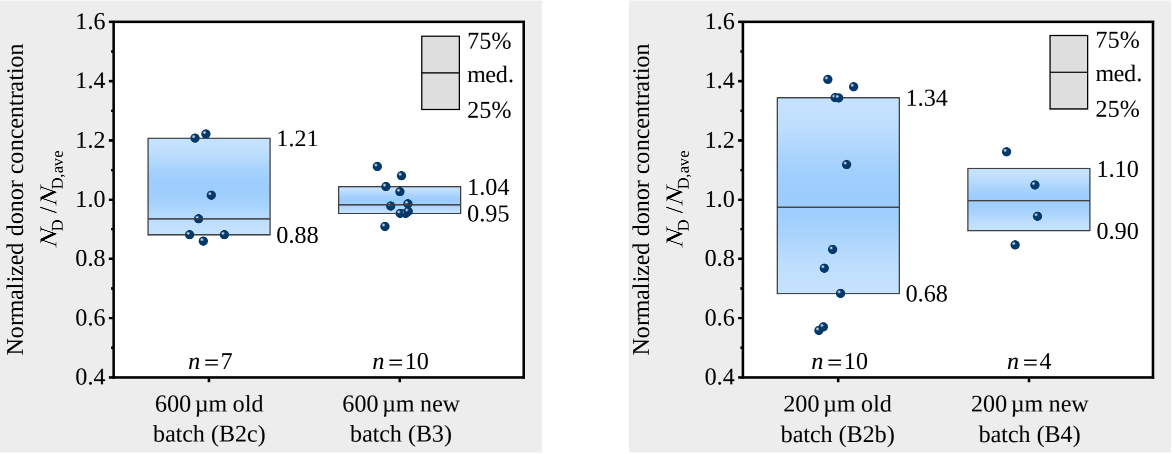
(a) **(b)** **(c)**

Figure 4.8: The forward current–voltage characteristics of a more recent generation of diodes (batch 3) with three different anode sizes (five of size ML, two of size L, and three of size LL) show a more consistent behavior than the early generation in Fig. 4.7. At a junction temperature of (a) 25 °C and (b) 150 °C, the knee voltage and shape of the profile are similar for each device type. (c) The differential on-resistance varies by up to about 30 % for type ML, and about 20 % for type L and LL. The data still show a variation of device electrical characteristics across the wafer, but suggest an improvement of the processing parameters.

the junction temperature from 25 °C to 150 °C the conduction losses at 10 A increase by 11 % for sample S1, but decrease by almost 20 % for sample S3.

This suggests a strong in-plane variation of material properties across the wafer which can include, e.g., the thickness of the epitaxial layer or its doping concentration. In this respect, it is important to note that the Ga_2O_3 wafer is exposed to oxygen during the growth of the epitaxial layer, which may at least partially reduce the effective donor concentration in the substrate and thus lead to a certain in-plane variation. For the devices under test, a reduction from $5.1 \times 10^{18}\,\mathrm{cm}^{-3}$ to about $1 \times 10^{18}\,\mathrm{cm}^{-3}$ is expected by the manufacturer [255]. Furthermore, the epitaxial layer of the samples under test was grown by halide-vapor phase deposition (HVPE, see Section 2.3.2). This method offers high deposition rates exceeding $20\,\mu\mathrm{m/h}$, but is indeed known for its difficulty in achieving a uniform doping concentration and film thickness, the incorporation of Si or Cl impurities during the growth process, and the potential diffusion of atoms between epitaxial layer and substrate caused by high deposition temperatures [18, 123, 125, 126]. Since Cl is also expected to be a shallow donor in Ga_2O_3 [127], it was previously speculated whether these impurities might affect the electrical properties [126]. From the measurements made here, it cannot be concluded which of these effects contribute to the observed variation in the current–voltage profiles. However, the process control during HVPE growth appears to be a central aspect.

Figure 4.8 shows the forward characteristics of a more recent batch (B3) of Ga_2O_3 Schottky diodes. Again, all diodes are of the identical type and only the anode size differs. Five samples of type ML (anode 1.6 mm × 1.6 mm), two samples of type L (anode 2.4 mm × 2.4 mm) and three samples of type LL (anode 3.2 mm × 3.2 mm) are compared. Again, a certain spreading of the forward characteristics at 25 °C (Fig. 4.8a) and 150 °C (Fig.4.8b) is visible. However, the profile is linear above the knee voltage for all devices, and the variation seems to be much less pronounced than that of the previous batch shown in Fig. 4.7. This becomes more evident when comparing the temperature dependent on-resistances in Fig. 4.8c. First, the



(a) **(b)**

Figure 4.9: Doping concentration of early and recent device generations fabricated on (a) 600 µm thick and (b) 200 µm thin wafers, normalized to the average doping concentration as determined from capacitance–voltage measurements. The spreading of the data, characterized by the difference between the 75th and 25th percentile, decreases significantly between the first and second batches. Although a significant variation of the doping concentration is still present in new generations, this indicates a substantial improvement in the growth and processing conditions of halide vapor phase grown epitaxial wafers.

on-resistance increases linearly between 25 °C and 150 °C for all devices under investigation, with a similar slope for all devices of the same size. Second, with about 31 % (type ML, one outlier diode causing the rather high value), 22 % (type L) and 19 % (type LL), the maximum deviation is significantly lower than that the of the previous batch of diodes. This suggests that, as claimed by the manufacturer [232, 246, 247], the process control was improved for the newer batches.

A more quantitative image can be obtained when comparing the variation in doping concentration of different device generations. As explained in Section 2.2.3, the inverse doping concentration ${N_D}^{-1}$ of a Schottky barrier diode is proportional to $A{\cdot}\mathrm{d}{C_j}^{-2}/\mathrm{d}V_D$, where A is the active area, C_j is the junction capacitance, and V_D is the diode voltage. Therefore, the doping concentration can directly be estimated from capacitance–voltage measurements. Figure 4.9a shows the doping concentration normalized to its average value for an early (batch B2c) and new generation (batch B3) of diodes grown on 600 µm thick wafers. The top and bottom of the box indicate the 75th and 25th percentiles with the respective absolute value as number next to it, and the middle line indicates the median. Figure 4.9b shows the same type of evaluation for diodes fabricated on early (B2b) and novel (B4) 200 µm thin wafers.

Taking the difference between the 75th and 25th percentiles as an indicator for the variation of the data, a reduction from 0.33 (old batch) to 0.09 (new batch) is observed for the 600 µm thick devices. In comparison, the absolute variation of the doping concentrations is higher for the 200 µm thin devices. However, a reduction from 0.66 (old batch) to 0.20 (new batch) is observed as well. As the number of devices available for this work is limited, a higher number of samples is needed for a more precise statistical evaluation. Nevertheless, the results suggest a decrease in the variation of electrical properties across the wafers as a result of an improved growth and process control, presumably associated with the epitaxial growth by HVPE. Although the device quality has been improved continuously over the course of this work, the variation of device properties that cannot be predicted precisely constitutes a challenge for the optimal design of application-relevant circuits. Therefore, it is key for all experiments conducted as part of this work to design setups that allow for an investigation of all necessary device properties for a wide range of different devices.

The data also show that the change in on-resistance with rising junction temperature can vary between different devices. Given its importance in power electronics, the following section examines in detail how the change in on-resistance of Ga_2O_3 devices compares to that of SiC diodes.

4.2.4 Low increase in on-resistance with rising temperature

The on-resistance of a diode is one of the most decisive properties as it directly determines the conduction losses and with that also the thermal management strategy and efficiency of a power converter. As the chip temperature increases during operation, the device properties at junction temperatures above $100\,°\mathrm{C}$ are of particular interest. Taking the previously discussed variation of device properties into account, this section assesses the change in on-resistance with rising junction temperature T_j. This can be done through the coefficient α_ref describing the increase in differential on-resistance r_o relative to its value at a certain reference temperature T_ref [203, 213, 214]:

$$r_\mathrm{o}\left(T_\mathrm{j}\right) = r_\mathrm{o}\left(T_\mathrm{ref}\right) \cdot \left(\frac{T_\mathrm{j}}{T_\mathrm{ref}}\right)^{\alpha_\mathrm{ref}} . \tag{4.7}$$

Usually, a reference temperature of $300\,\mathrm{K}$ is used for the calculation [213, 214]. The resulting coefficient will be referred to as α_{300} in the following. As outlined in Sections 4.2.1 and 4.2.3, however, the differential on-resistance above the knee voltage can be highly non-constant up to junction temperatures of usually about $50\,°\mathrm{C}$ to $75\,°\mathrm{C}$. A definition of a single temperature coefficient α_{300} is not meaningful for these diodes. To enable a further comparison for all types of diodes, Eq. 4.7 is adjusted so that the relative rise in on-resistance is referenced to a temperature T_ref of $100\,°\mathrm{C}$ or $373\,\mathrm{K}$, and only measurements above $75\,°\mathrm{C}$ are taken into account. The rise in differential on-resistance at high temperatures is then described by the corresponding parameter α_{373}.

Figure 4.10 shows the α_{373} coefficients for all types of Ga_2O_3 diodes studied in this thesis, except the ones that do not exhibit a steady increase in on-resistance with rising temperature even above $100\,°\mathrm{C}$ (the coefficients are < 1 for these devices). In addition, the α_{300} coefficients are shown for all Ga_2O_3 devices with a constant differential on-resistance that increases with temperature even at $25\,°\mathrm{C}$. The last column shows the corresponding coefficients of five commercial SiC reference diodes. The exact fitting interval when determining the on-resistance has a slight influence on the corresponding coefficient α_ref. However, the influence is minimized by using the same fitting intervals for all diodes as described in Section 3.3 (corresponding to a range from about $70\,\%$ to $130\,\%$ of the expected typical operating point) and it is negligible compared to the general trend of the data.

The corresponding α_{300} coefficients vary between 1.55 and 2.01 for the SiC diodes but only between 1.17 and 1.48 for the Ga_2O_3 diodes, showing that the Ga_2O_3 diodes exhibit a lower relative increase in differential on-resistance with rising temperature than their SiC counterparts. Interestingly, the α_{373} coefficients do not differ significantly from the α_{300} coefficients in case of Ga_2O_3. This means that the increase in on-resistance can be described well with Eq. 4.7 for all temperatures. Among all Ga_2O_3 diodes (i.e., also the ones with

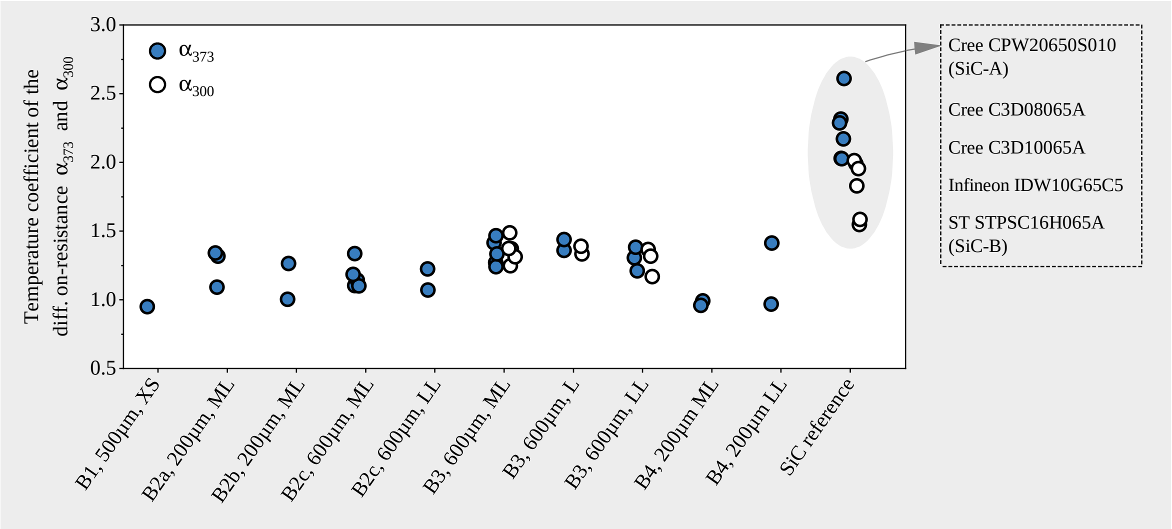


Figure 4.10: Increase in differential on-resistance with rising temperature as described by the coefficients α_{300} and α_{373} according to Eq. 4.7 for multiple Ga_2O_3 diodes from different batches (see Tab. 3.2) and SiC reference diodes. α_{300} values are only shown for diodes that exhibit a positive temperature coefficient of the forward voltage at all temperatures. The increase in on-resistance is significantly lower for Ga_2O_3 than for SiC, with an α_{373} average and standard deviation of 1.22±0.16 and 2.24±0.22, respectively. This difference is connected to the temperature-dependent electron mobility and makes Ga_2O_3 diodes appealing for high-temperature applications.

non-constant differential on-resistance at low temperatures), the α_{373} coefficients vary between about 0.95 and 1.47. For the SiC reference devices, however, they increase to values between 2.02 and 2.61, which indicates that the relative increase in differential on-resistance is stronger than described by Eq. 4.7. Averaging over all devices shown in Fig. 4.10 yields coefficients α_{373} of 1.22 with a standard deviation of 0.16 for Ga_2O_3, and 2.24 with a standard deviation of 0.22 for SiC. In the following, this difference will be connected to the basic material properties of Ga_2O_3 and SiC.

The series resistance of a Schottky diode is mainly caused by the lightly doped drift region in the epitaxial layer. Apart from structural parameters such as the active area A and thickness of the epitaxial layer z_{epi}, it is determined by the electron mobility μ_{e} and doping concentration N_{D} according to $r_{\mathrm{epi}} = z_{\mathrm{epi}}/(eAN_{\mathrm{D}}\mu_{\mathrm{e}})$ [34]. In a first approximation, all quantities except for the electron mobility are temperature independent. The relative increase in resistance of the epitaxial layer can therefore simply be calculated by $r_{\mathrm{epi}}\left(T_{\mathrm{epi}}\right)/r_{\mathrm{epi}}(T_{\mathrm{ref}}) = \mu_{\mathrm{e}}(T_{\mathrm{ref}})/\mu_{\mathrm{e}}(T_{\mathrm{epi}})$, i.e., the change of electron mobility with the temperature of the epitaxial layer T_{epi} related to a certain reference temperature T_{ref}. By combining this relationship with Eq. 4.7 (i.e., when assuming that the differential on-resistance is mainly caused by the epitaxial layer) the coefficient α_{ref} can be expressed by

$$\alpha_{\mathrm{ref}}\left(T_{\mathrm{epi}}\right) = \frac{\log\left(\dfrac{\mu_{\mathrm{e}}\left(T_{\mathrm{ref}}\right)}{\mu_{\mathrm{e}}\left(T_{\mathrm{epi}}\right)}\right)}{\log\left(\dfrac{T_{\mathrm{epi}}}{T_{\mathrm{ref}}}\right)} \tag{4.8}$$

A recent study [215] on the material properties of Ga_2O_3 and 4H-SiC showed that at $300\,\mathrm{K}$ the electron mobility of Ga_2O_3 is about four times lower than that of SiC, but the decrease of electron mobility with rising temperature is significantly less pronounced in Ga_2O_3. The electron mobilities of 4H-SiC ($\mu_{\text{e,SiC}}$) and β–Ga_2O_3 ($\mu_{\text{e,GaO}}$) at an effective donor concentration of $1 \times 10^{17}\,\text{cm}^{-3}$ were found to decrease exponentially with temperature T according to the following equations [215]:

$$\mu_{\text{e,GaO}}\,(T) = [1147 \cdot \exp(-T/131\,\text{K}) + 31]\ \text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1} \tag{4.9}$$

$$\mu_{\text{e,SiC}}\,(T) = [5422 \cdot \exp(-T/128\,\text{K}) + 95]\ \text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1} \tag{4.10}$$

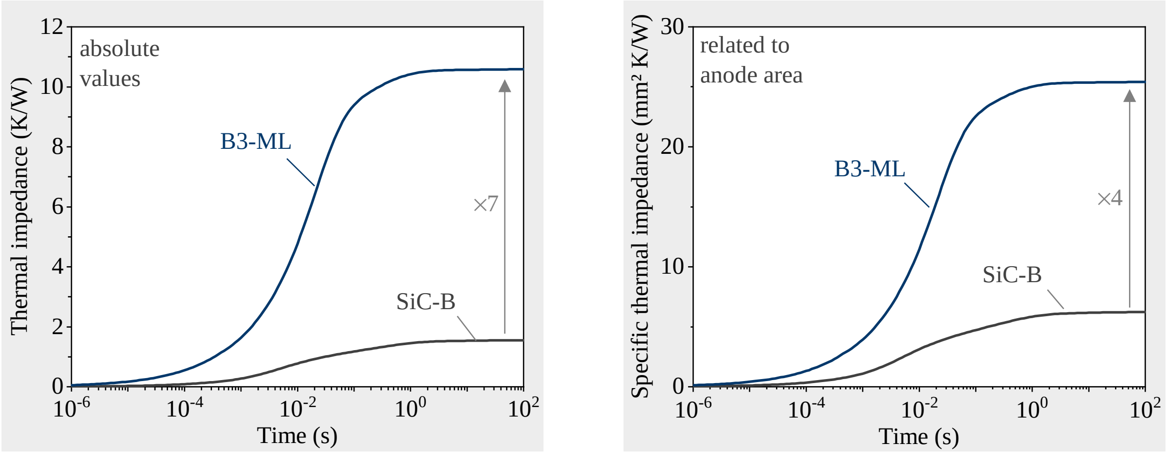
By inserting this dependency of the electron mobilities in Eq. 4.8, the coefficient α_{ref} of Ga_2O_3 and SiC can be estimated and compared also from a material point of view. Calculating the corresponding values exemplarily for $T = T_{\text{epi}} = 150\,^{\circ}\text{C}$ (i.e., the maximum measurement temperature in the experiments) results in coefficients α_{300} of 1.91 (Ga_2O_3) and 2.15 (SiC) as well as α_{373} of 1.94 (Ga_2O_3) and 2.23 (SiC). The value calculated for SiC is exactly within the range displayed in Fig. 4.10, which validates the calculation. However, the value for β–Ga_2O_3 is about 0.5 higher than the highest value observed in Fig. 4.10. First, it should be noted that the previously discussed unusual electrical characteristics indicate an additional influence on the current–voltage profiles that is not considered here. Also, note that the doping concentration of the studied diodes is about one order of magnitude lower than assumed in the calculations using the data from [61, 215] (the availability of reliable data to enable more detailed calculations is still limited for Ga_2O_3). As the doping concentration significantly affects the electron mobility [18, 61, 216], this is expected to affect the calculations. In addition, the influence of the heavily doped substrate that also contributes to the on-resistance is not considered here.

Despite the uncertainties accompanied by these simplifications, the data show that the low increase in on-resistance with rising junction temperature is not only caused by the specific structure of the Ga_2O_3 diodes under investigation in this thesis. Instead, it appears to be generalizable as a direct consequence of the material properties of β–Ga_2O_3. In recent studies, small-area $500\,\text{V}$ β–Ga_2O_3 diodes (anode diameter up to $250\,\mu\text{m}$) remained fully functional up to junction temperatures of $600\,\text{K}$ or $327\,^{\circ}\text{C}$ [143], and β–Ga_2O_3 transistor cells with a width of $50\,\mu\text{m}$ were operated successfully at $500\,^{\circ}\text{C}$ [217]. In combination with the results discussed here, this means that junction temperatures higher than the current typical limit of 150 to $175\,^{\circ}\text{C}$ may be feasible for Ga_2O_3 diodes. As a consequence, new packaging concepts with high-temperature materials (especially regarding the maximum temperature of the mold mass or die attach material) may become important for Ga_2O_3 devices. The actual device temperature is then determined by its thermal resistance, which will briefly be discussed in the next section.

4.3 Basic thermal considerations

To gain a basic insight into the thermal management of Ga_2O_3 power devices, the thermal impedance is measured for the previously discussed TO247 packaged Ga_2O_3 B3-ML type diode with a thickness of $600\,\mu\text{m}$ (currently, this is a standard value based on the available substrates [22, 231]) and the commercial TO247 packaged $650\,\text{V}/16\,\text{A}$ SiC-B reference diode according to the procedures described in Section 3.5. Here, thermal grease is used as thermal interface material between case and heatsink for both devices.

Figure 4.11b shows the resulting thermal impedance profiles and structure functions measured during the cooling phase after heating for $100\,\text{s}$ with a heating current of $3\,\text{A}$ (heating power



(a) **(b)**

Figure 4.11: (a) Absolute and (b) specific (related to anode area) thermal impedance profiles of a TO247 packaged $600\,\mu\mathrm{m}$ thick B3-ML type Ga_2O_3 diode and the TO247 packaged SiC-B reference diode. The low thermal conductivity of Ga_2O_3 leads to a significant increase of the thermal resistance. Even considering the differences in anode area, the junction-to-ambient thermal resistance is about four times higher than that of the SiC reference diode and limits the power rating substantially.

$9.0\,\mathrm{W}$) in case of the Ga_2O_3 diode and $16\,\mathrm{A}$ (heating power $25.5\,\mathrm{W}$) in case of the SiC diode. The conduction losses lead to a rise in junction temperature of about $99\,\mathrm{K}$ for the Ga_2O_3 and $39\,\mathrm{K}$ for the SiC diode. The thermal impedance profiles reach constant values of about $10.60\,\mathrm{K/W}$ and $1.55\,\mathrm{K/W}$, respectively. The fact that the two curves separate already after only microseconds indicates that the die is primarily responsible for the difference. Relating the values to the anode area of the devices yields $25.4\,\mathrm{mm}^2\,\mathrm{K/W}$ for the Ga_2O_3 diode, but only $6.2\,\mathrm{mm}^2\,\mathrm{K/W}$ for the SiC diode, which means that the specific junction-to-ambient thermal resistance of the Ga_2O_3 diode is more than four times higher than that of the SiC diode.

It should be noted that the different chip sizes affect the heat flow path also in the die-to-ambient thermal path. To get a clearer view on the influence of the die itself on the thermal resistance, the die and anode sizes should be similar, and they should be assembled exactly in the same way. In this respect, note that a $0.5\,\mathrm{mm}$ thick CuMo spacer is inserted between the die and lead frame in case of the Ga_2O_3 diode (see Section 3.2). However, assuming a thermal conductivity of 200 to $250\,\mathrm{W\,m^{-1}\,K^{-1}}$ for CuMo [218] and a heat flow area of $2.2\,\mathrm{mm} \times 2.2\,\mathrm{mm}$ based on the effective chip size, the thermal resistance should be around 0.4 to $0.5\,\mathrm{K/W}$ and thus make up less than $5\,\%$ of the junction-to-ambient thermal resistance.

Therefore, the low thermal conductivity of Ga_2O_3 clearly translates to a substantially reduced power rating, which is likely to cause thermal management issues if the die is supposed to be operated under the same conditions as the SiC reference diode. The results motivate the investigation of strategies to improve the power and current rating of Ga_2O_3 diodes discussed in detail in Section 5.

4.4 Modeling atypical current–voltage profiles in Spice

The preceding Sections 4.2 and 4.3 show that the classic models based on thermionic (field) emission can be applied to the investigated Ga_2O_3 devices only within certain operating

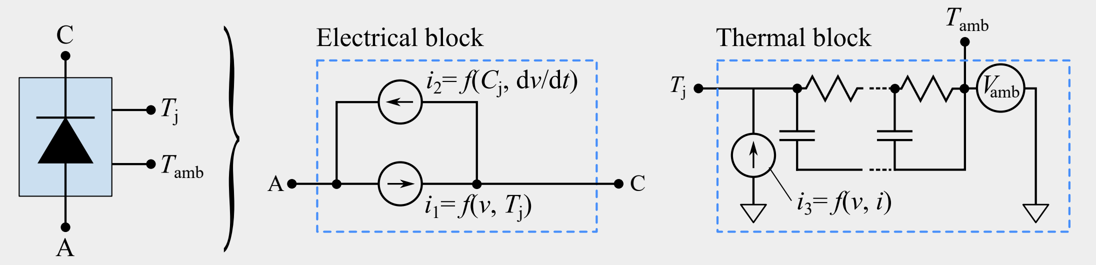


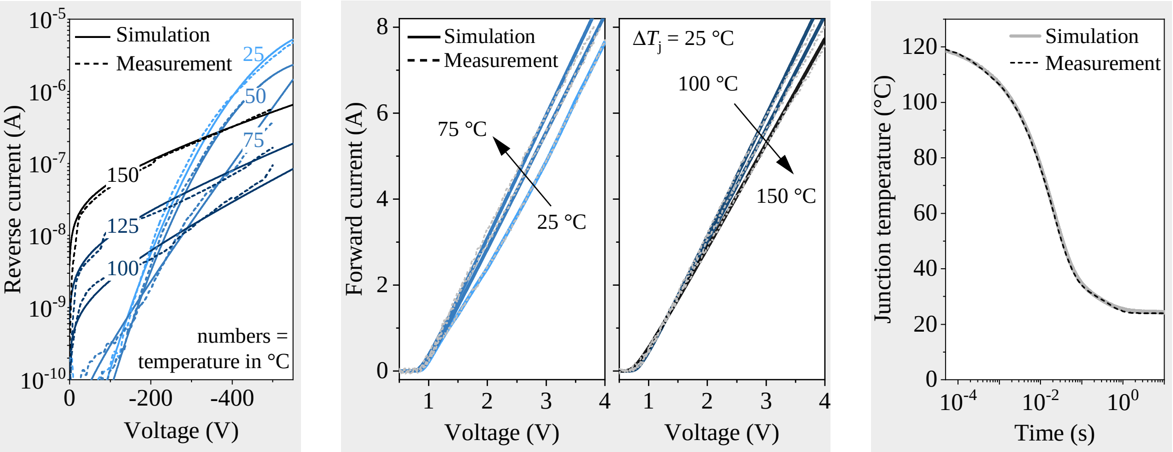
Figure 4.12: Basic principle of a diode simulation model in LTspice using behavioral current and voltage sources. The model can be divided into an electrical block modeling the forward and reverse current–voltage characteristics (i_1) as well as the current through the junction capacitance (i_2), and a thermal block modeling the junction temperature based on the heating power (i_3) that is fed into a thermal Cauer network. Adapted from [258].

ranges. Curved characteristics in the current–voltage profiles and a change in temperature coefficient lead to deviations from these models. Although the focus of this work is not the physical modeling of Ga_2O_3 diodes, accurate Spice models are essential for the development of power converters or simply for the design of experimental setups. Since models from manufacturers are not yet available, simple models that can reproduce the characteristics were created. Such models have been used throughout this work to estimate basic operating limits and thereby avoid the destruction of the limited number of devices.

Since the electrical properties of different diodes can differ significantly even when the diode structure and junction design are identical, a main requirement is that the model must offer enough degrees of freedom but also allow a simple adjustment to reproduce the varying characteristics. However, many physical properties of the gallium oxide diodes, such as the exact active area, the precise thickness of the epitaxial layer, or the accurate electron mobility of the substrate and epitaxial layer with their respective temperature dependence, are not known. Furthermore, without detailed knowledge of the growth process of the devices, the physical cause of the unusual behavior cannot be conclusively determined. Therefore, the model cannot be purely physical. Instead, it is based on semiconductor physics, but overlaid with purely mathematical terms.

The standard Spice model for Schottky diodes consists of a thermal block and an electrical block, as shown schematically in Fig. 4.12 and described in more detail in [219–221]. Behavioral current and voltage sources are used to implement formulas in LTspice. In the electrical block, i_1 models the forward and reverse current–voltage profiles, and i_2 is the current through the junction capacitance. The power dissipation leading to a rise in junction temperature is modeled by the current source i_3. The implementation of i_2 and i_3 follows standard methods also described, e.g., in [219–221]: The current through the junction capacitance is modeled by defining the capacitance values and calculating the current from $i_2(t) = C_\mathrm{j}(v)\mathrm{d}v/\mathrm{d}t$, and the thermal model consists of a Cauer network that can directly be extracted from measurements of the structure function (see Section 3.5). The more important part for this thesis is the implementation of the reverse leakage current and the forward current with changing temperature coefficients and curvatures.

First, the reverse blocking characteristics are considered. From Section 4.2.2 it can be seen that, starting from the simplified thermionic field emission model, the modeled curve can be shifted by several orders of magnitude, the slope in the logarithmic plot can be different, and there can be a temperature and voltage-dependent bending of the curve. To compensate for these shifts, a correction factor attributed to the diode structure (e.g., influence of trench structure or



(a) Sample B3-ML. **(b)** Sample B2a-ML. **(c)** Sample B3-ML.

Figure 4.13: Simulated and measured (a) reverse and (b) forward current–voltage characteristics of Ga_2O_3 diodes with unusual behavior at junction temperatures between 25 °C and 150 °C. (c) Simulated and measured temperature response of the Ga_2O_3 diode from Fig. 4.11b during the corresponding thermal measurement. The adjusted Spice models can reproduce the electrical and electrothermal properties accurately and can thus serve as an aid during further experiments.

edge termination) and the unknown source of additional leakage current is multiplied to the pure TFE term:

$$I_\mathrm{r} = I_\mathrm{r,TFE} \cdot 10^{\zeta_\mathrm{rs}(T_\mathrm{j}) + \frac{\zeta_\mathrm{ri}(T_\mathrm{j})}{V_\mathrm{ref}} \times (V_\mathrm{D} - V_\mathrm{ref}) + \frac{\zeta_\mathrm{rb}(T_\mathrm{j})}{{V_\mathrm{ref}}^2} \times (V_\mathrm{D} - V_\mathrm{ref})^2} \tag{4.11}$$

In a typical plot where the y-axis is logarithmic, the parameter ζ_rs shifts the curve by ζ_rs orders of magnitude upwards or downwards. The parameter ζ_ri changes the slope/inclination of the curve with respect to a reference voltage V_ref, e.g., $-600\,\mathrm{V}$ for the diode in Section 4.2.2. The parameter ζ_rb induces a parabolic bending of the current–voltage profile. The set of parameters (ζ_rs, ζ_ri, ζ_rb) are unique for each diode and can easily be determined for each temperature through a Matlab fitting tool after measuring the static reverse characteristics.

A similar procedure is performed in forward direction. Using the thermionic emission model as a starting point, the on-resistance $r_\mathrm{o}(V_\mathrm{D})$ is defined voltage-dependent using a look-up table, and a temperature-dependent shift parameter $\zeta_\mathrm{fs}(T_\mathrm{j})$ is added:

$$I_\mathrm{f} = I_\mathrm{s} \cdot \exp\left(\frac{e\,\zeta_\mathrm{fs}\left[V_\mathrm{D} - I_\mathrm{f} r_\mathrm{o}(V_\mathrm{D})\right]}{nkT_\mathrm{j}}\right) \tag{4.12}$$

Figure 4.13 compares the corresponding simulated and measured characteristics exemplarily for large-area β–Ga_2O_3 Schottky diodes with significantly varying temperature coefficients between junction temperatures of 25 °C and 150 °C. Clearly, the procedure is a simple but effective method to precisely reproduce the unusual reverse (Fig. 4.13a) and forward (Fig. 4.13b) current–voltage characteristics. Note that the parameters ζ_rs, ζ_ri, ζ_rb continuously approach zero at high temperatures for the previously discussed example of the field-plated batch 3 diodes with unusual temperature coefficient, which agrees with the previous presumption of a transition from trap assisted tunneling at low temperatures to TFE and/or PFE at higher temperatures.

Figure 4.13c shows the temperature response from a transient thermal measurement with a B3-ML diode according to the procedures described in Section 3.5. The thermal Cauer network model was extracted from the measurement by using the T3Ster Master software from Mentor. The measurement was then replicated in Spice with a full electrothermal model according to the previously described methods, showing that also the electrothermal properties can be reproduced accurately.

In summary, the unusual characteristics with unknown cause can be modeled in Spice by adding mathematical terms to physics-based equations. This helps with the planning and design of more advanced and application relevant circuits, or simply to lower the risk of harming the device before choosing certain measurement settings throughout the thesis.

4.5 Summary and questions arising

Chapter 4 investigates basic properties of β–Ga_2O_3 diodes. The key results can be summarized as follows:

1. Basic current–voltage profiles can show varying temperature coefficients of the forward voltage and thus differ significantly from standard SiC Schottky diodes. This seems to be caused by the device or wafer processing rather than the intrinsic properties of β–Ga_2O_3. A transition between different conduction mechanisms is also observed in reverse direction for multiple diodes. Spice models that can reproduce these varying characteristics have been created to simplify measurement planning.
2. A strong variation of material properties for early device generations is observed, but an improvement of the processing technology is discernible for newer device generations. However, experimental setups need to be flexible to allow an investigation of all types of diodes.
3. The increase in differential on-resistance with rising temperature is significantly smaller for Ga_2O_3 than for SiC diodes, which makes them attractive for high-temperature applications.
4. Reverse breakdown is hard and destructive (complete loss of blocking capability) and should thus be avoided.
5. The junction properties and temperature stability are found to be sufficient to proceed with the next step of research, where two main issues are identified regarding a potential application in power electronics:
    a) The low thermal conductivity of Ga_2O_3 was shown to translate to a substantial rise in junction temperature that limits the power rating. What are potential solutions to this problem, and how effective are they?
    b) Switching properties of power devices are key, but there is a lack of studies in the literature. Is a stable converter operation possible despite the high thermal resistance, and what must be done to improve the performance? How does the switching behavior compare to mature technologies?

These constitute the guiding questions that will be covered in the following Chapters 5 (thermal properties) and 6 (switching behavior).

Chapter 5

Thermal properties and methods to improve the heat dissipation

5.1 Chapter overview

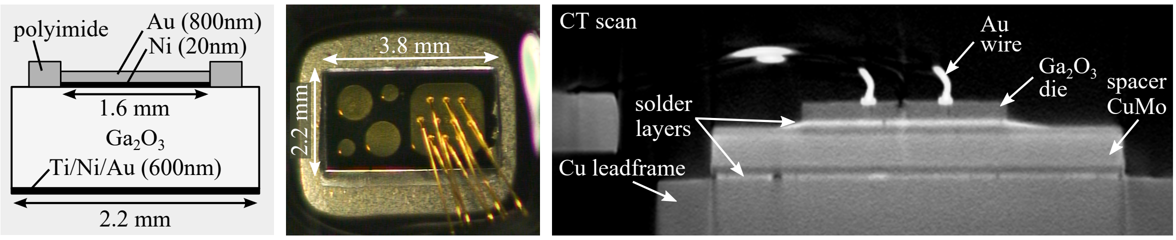
Section 4.3 showed that the low thermal conductivity of Ga_2O_3 causes a substantial thermal resistance when standard 600 µm thick Ga_2O_3 diodes are cooled from the cathode side, as common for Si or SiC. One way to alleviate this issue is to thin down the substrate. Motivated by this, Section 5.2 uses four 200 µm thin diodes to investigate the heat dissipation of thinned chips in TO247 standard packages, which are often used in applications. To this end, measurements of the structure functions are combined with parametric studies and X-ray analyses. Another potentially effective thermal management method is to cool the diodes directly from the junction side. In Section 5.3, it is comparatively examined how effective both substrate thinning and junction-side cooling are to improve the current and power rating of Ga_2O_3 diodes. To this end, 600 µm thick and new 200 µm thin Ga_2O_3 bare dice of identical lateral dimensions are assembled in cathode-side cooled (CSC) and junction-side cooled (JSC) configuration on custom-made ceramic substrates. A commercial SiC bare die of similar size is mounted in the same manner and serves as a benchmark. In addition, a 600 µm thick Ga_2O_3 with a larger chip size is briefly investigated to discuss the influence of increasing chip size on the junction temperature. This way, a direct and fair comparison is possible that is further supported by thermal simulations. Given the potentially low on-resistance of Ga_2O_3 diodes, it is discussed whether and how similar low chip temperatures as for SiC diodes can be achieved in the future. Section 5.4 summarizes the key results of this chapter. Parts of this chapter have been published by the author in [255, 256, 259] during the course of this thesis.

5.2 Heat dissipation in TO247 packaged diodes with thinned substrate

5.2.1 Setup and investigated samples

As outlined in Section 2.3, Ga_2O_3 devices are commonly fabricated on 500 to 700 µm thick substrates. By thinning the substrates, the heat flow path is effectively shortened. This is expected to reduce the thermal resistance and also the specific on-resistance of the devices. Thinning processes are generally known from silicon thin wafer technology, where thicknesses below 100 µm are common [222]. The mechanical properties of Ga_2O_3 wafers (see Section 2.3.2) allow thinning by similar methods such as mechanical grinding.

Here, four ML-size Schottky diodes (S1, S2, S3, S4, all from batch B2a according to Tab. 3.1) with a structure as shown in Fig. 5.1a were externally fabricated on a (001) β–Ga_2O_3 wafer



(a) **(b)** **(c)**

Figure 5.1: (a) Schematic structure of the $200\,\mu\mathrm{m}$ thin TO247-packaged diodes used to study the heat dissipation. (b) Photograph of a silicone-gel sealed sample. The chips are diced out in a rectangular shape, but only the ML-size anode is electrically connected with bond wires. (c) A computer tomography (CT) scan reveals the cross-sectional structure of the packaged dice with CuMo spacer between die and lead frame, and confirms the targeted die thickness. Adapted from [255].

that was thinned to a thickness of $200\,\mu\mathrm{m}$ by grinding and polishing. Detailed studies on essential wafer parameters, such as the resulting bow and yield after thinning, have not yet been performed. Currently the process is being adapted to enable thicknesses of $100\,\mu\mathrm{m}$ or below.

The substrate exhibits an initial effective donor concentration of $5.1\times10^{18}\,\mathrm{cm}^{-3}$. As explained in Section 2.3.3, the wafer is exposed to oxygen and high temperatures during the subsequent HVPE-growth of the epitaxial layer. This is expected to reduce the effective donor concentration of the substrate to between $1\times10^{18}\,\mathrm{cm}^{-3}$ and the initial value [255]. As specified by the manufacturer, the epitaxial layer is about 6.6 to $13\,\mu\mathrm{m}$ thick with an effective donor concentration of about 0.9 to $3\times10^{16}\,\mathrm{cm}^{-3}$ [255], which agrees with the capacitance–voltage measurements in Section 4.2.3. A Ti($50\,\mathrm{nm}$)/Ni($350\,\mathrm{nm}$)/Au($200\,\mathrm{nm}$) layered structure forms the ohmic cathode contact, and a Ni($20\,\mathrm{nm}$)/Au($800\,\mathrm{nm}$) layer forms the $1.6\,\mathrm{mm}\times1.6\,\mathrm{mm}$ large Schottky contact. Since the devices are fabricated purely for thermal testing, they do not contain any electric field management methods such as edge terminations or trench junctions. Note, however, that switching tests performed with the newest generation of $200\,\mu\mathrm{m}$ thin $650\,\mathrm{V}$ rated diodes with edge termination in Chapter 6 suggest that substrate thinning does not affect the breakdown voltage [260].

As described in Section 3.2, all diodes were assembled on TO247 lead frames by soldering (cathode) and wire bonding with ten $50\,\mu\mathrm{m}$ thin Au wires (anode). Samples S1, S2, and S3 are fully molded, while sample S4 is sealed with Si gel as shown in Fig. 5.1b. The figure also shows that the chips are diced out in a rectangular rather than square format because of additional test structures on the wafer. However, these test structures do not contribute to any current flow, as they are not contacted with bond wires. As will be shown later in this chapter, the heat spreading into these parts of the die is negligible. Therefore, an effective die size of $2.2\,\mathrm{mm}\times2.2\,\mathrm{mm}$ can be used for a more meaningful comparison to other devices. A computer tomography (CT) scan is performed to reveal the cross-sectional structure of the diode after assembly. The resulting image in Fig. 5.1c shows the Ga_2O_3 die soldered to a $0.5\,\mathrm{mm}$ thick CuMo spacer between lead frame and die, and confirms a die thickness of about $200\,\mu\mathrm{m}$.

As examined in Section 4.2.3, the variation of material properties across the wafer influences the electrical characteristics substantially. The forward I–V profiles of the samples S1–S4 studied here were already discussed exemplarily in Fig. 4.7. It was found that sample S3 shows a visibly curved I–V profile at $25\,°\mathrm{C}$ above the knee voltage, while samples S1, S2, and S4 show a constant specific differential on-resistance $r_{\text{o,sp}}$. All samples first exhibit a decrease in $r_{\text{o,sp}}$ with rising junction temperature that turns into an increase in $r_{\text{o,sp}}$ above $100\,°\mathrm{C}$ ($125\,°\mathrm{C}$ for S3). According to Eq. 2.3, thinning the heavily doped substrate from 600 to $200\,\mu\mathrm{m}$ should lower the $r_{\text{o,sp}}$ of the devices under investigation by about 5 to $30\,\%$. The actual reduction critically depends on the unknown exact doping concentration and associated electron mobility. Since the specific on-resistances of samples S1–S4 already differ by up to a factor of 1.8, a clear experimental comparison is not possible here, but will be performed in Section 5.3. Nevertheless, the diodes can carry a current of several amperes, which allows them to be subjected to transient thermal measurements.

5.2.2 Transient temperature response and potential measurement issues

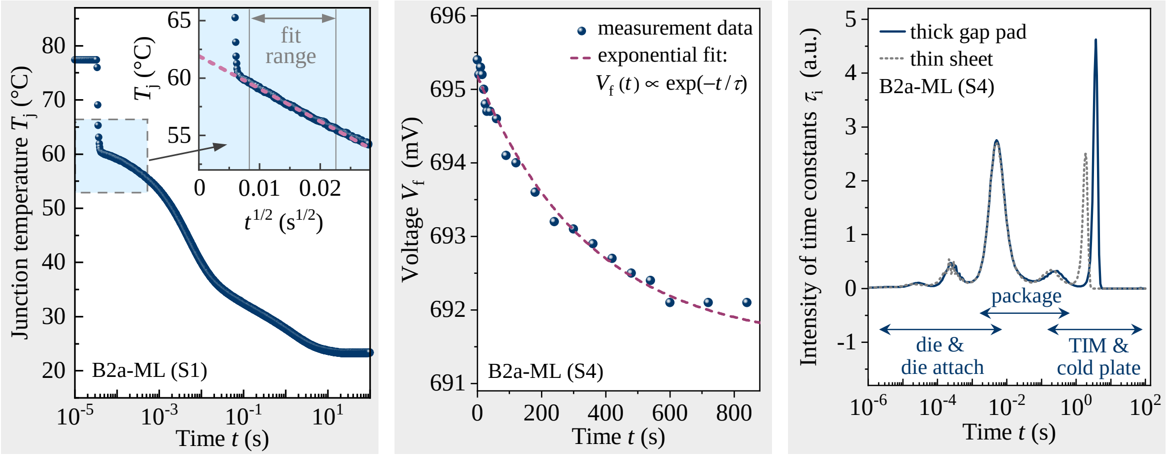
The general procedure to calibrate the temperature sensitive parameter (TSP) of Ga_2O_3 diodes and perform transient thermal measurements is described already in Section 3.5. A K-factor calibration is performed for the samples under investigation before the R_{th} measurements. All devices exhibit a linear relationship between the forward voltage at $10\,\mathrm{mA}$ ($V_{\text{f@10mA}}$) and the junction temperature T_{j} associated with a K-factor of about $1.7\,\mathrm{mV/K}$. To exclude an influence on the results caused by a potential change in junction properties of the rather experimental dice, K-factor calibrations were performed again after the transient thermal measurements. The differences are well below $1\,\%$ for all samples, which corresponds to an uncertainty in the determination of the junction temperature of well below $0.5\,\mathrm{K}$ when the average increase from 25 to $65\,°\mathrm{C}$ during the R_{th} measurements is considered.

Applying heating currents around $3\,\mathrm{A}$ causes an increase in junction temperature of about $40\,\mathrm{K}$ for all samples. Figure 5.2a shows the temperature response exemplarily for sample S1 during the cooling phase after heating for $100\,\mathrm{s}$. The shape of the profile is similar to the one obtained with the B3-L diode in Fig. 3.15. The inset in Figure 5.2a illustrates the determination of the initial junction temperature T_{j0} via the $\sqrt{t}$-method. The slope m_{T} of the fitted straight line is connected to the chip area $A_{\text{ch,eff}}$ and heating power ΔP_{H} via [94, 107, 197]

$$A_{\text{ch,eff}} = \frac{\Delta P_{\text{H}}}{m_{\text{T}}} \cdot \frac{2}{\sqrt{\pi \cdot c_{\text{th}} \cdot \lambda_{\text{th}} \cdot \rho}} \,. \tag{5.1}$$

When assuming standard values of $c_{\text{th}} = 560\,\mathrm{J\,kg^{-1}\,K^{-1}}$ [87] for the specific heat, $\lambda_{\text{th}} = 21\,\mathrm{W\,m^{-1}\,K^{-1}}$ [87] for the thermal conductivity, and $\rho = 5945\,\mathrm{kg/m^3}$ [102] for the mass density of Ga_2O_3, chip areas ranging from $3.1\,\mathrm{mm^2}$ (S4), $3.4\,\mathrm{mm^2}$ (S1), and $3.8\,\mathrm{mm^2}$ (S2) to $4.3\,\mathrm{mm^2}$ (S4) are obtained. For all samples, this is between the anode area of $2.4\,\mathrm{mm^2}$ and the previously presumed effective chip area of $4.8\,\mathrm{mm^2}$, but significantly lower than the entire chip area of $8.4\,\mathrm{mm^2}$. This is reasonable since the active area below the anode constitutes the major heat source of the die but a certain heat spreading is expected, and thus validates the measurements. Considering the difference between the calculated area and the entire chip area, it further indicates that the heat does not spread significantly into the additional part of the die that is not electrically connected with bond wires. This is also supported by thermal simulations in Section 5.2.4, and confirms that the additional part of the die should be neglected when comparing area-specific properties with other devices.

The fact that the temperature remains constant between about $20\,\mathrm{s}$ and the maximum measurement time of $100\,\mathrm{s}$ in Fig. 5.2a suggests that a thermal equilibrium is reached. However, the junction temperature appears lower than before the measurement. With a difference



(a) (b) (c)

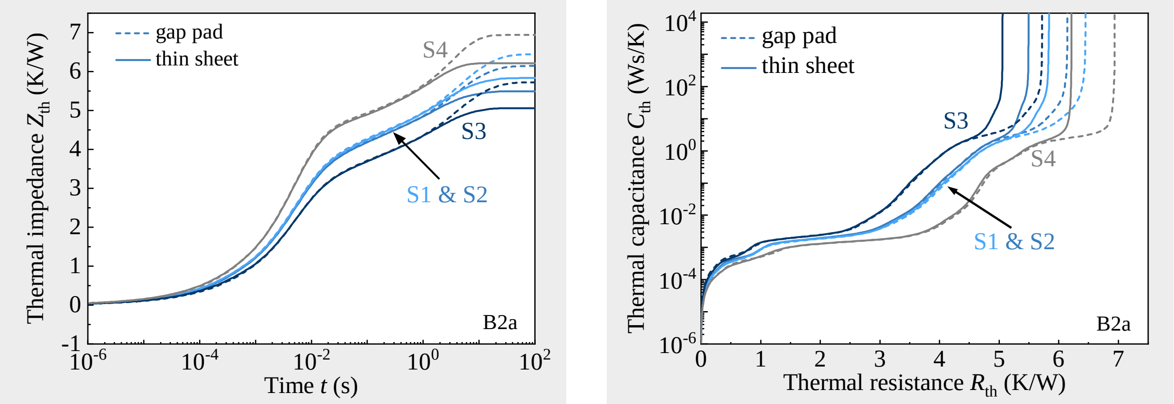
Figure 5.2: (a) Junction-temperature response and determination of the initial junction temperature exemplarily for sample S1. (b) After the cooling phase, an exponential decrease of $V_{f@10mA}$ back to the initial value with a time constant in the range of minutes is observed. (c) The time constant spectrum shows that the largest time constants associated with the R_{th} measurement are only in the range of seconds. The parasitic drift in (b) is therefore expected to be negligible for the evaluation of the R_{th} measurements. Adapted from [255].

of $-4\,\mathrm{K}$, the effect is the strongest in case of sample S4. The reason is a parasitic drift in $V_{f@10mA}$ of about $+6\,\mathrm{mV}$ in case of S4. In Fig. 5.2b, $V_{f@10mA}$ is recorded for a period of $60\,\mathrm{min}$ immediately after the R_{th} measurement. Fitting a function of the form $V_{f@10mA} \propto \exp(t/\tau)$ to the data suggests an exponential decrease of $V_{f@10mA}$ back to its initial value with a time constant of $(352 \pm 24)\,\mathrm{s}$. This may result from an accumulation or trapping of charge carriers at defects close to the MS junction during forward current flow, which increases the bending of the conduction band. The charge carriers are released when the external voltage and current flow are cut off. This thought in principle agrees with the findings in Section 4.2 that suggest the presence of some trap states at least in early generation devices.

To further study the influence of this effect on the R_{th} measurements, the continuous distribution of the time constants τ_i (see Section 3.5) is examined in Fig. 5.2c exemplarily for sample S4 for two measurements with different TIMs. Changing the TIM affects the time constant distribution on a scale of seconds. The distinct intensity peaks in the range from µs to s result mainly from the die, die attach, and package, indicating that heating and cooling of the die happens on a much shorter time scale. The time constant of the parasitic effect described above is in the range of several minutes (see Fig. 5.2b), and thus about one to two orders of magnitude larger than the largest time constant in Fig. 5.2c. Therefore, it is not expected to affect the R_{th} measurements significantly: Although the absolute junction temperature estimated from the K-factor calibration may be several Kelvin too low, the impact on the relative temperature increase as well as the cooling profile $T_j(t)$ in the early cooling phase should be negligible. This consideration provides the basis for the discussion of the transient thermal measurements in the following section.

5.2.3 Thermal structure functions, impedance profiles, and their variation

The thermal impedance profiles and structure functions of all samples are shown in Fig. 5.3. The thermal impedance profiles (Fig. 5.3a) all reach a constant value after $100\,\mathrm{s}$, from which junction-to-ambient thermal resistances $R_{th,ja}$ of $5.1\,\mathrm{K/W}$ (S3), $5.5\,\mathrm{K/W}$ (S1), $5.8\,\mathrm{K/W}$ (S2),



(a)

(b)

Figure 5.3: Results of transient thermal measurements for all TO247-packaged samples of batch B2a. (a) The thermal impedance profiles deviate already in the range of µs to ms, indicating that differences in the thermal resistance near the heat source might be responsible for the variations in $R_{\mathrm{th,ja}}$ and $R_{\mathrm{th,jc}}$. (b) The variation of the length of the plateau at about $0.001\,\mathrm{W\,s/K}$ in the structure functions supports this hypothesis. Adapted from [255].

$6.2\,\mathrm{K/W}$ (S4) can be extracted for the measurements with thin sheet as TIM. The splitting points of the curves with two different TIMs mark the transition from heat flow within the package to the TIM and heatsink. They indicate a variation of the associated junction-to-case thermal resistances $R_{\mathrm{th,jc}}$ between $4.3\,\mathrm{K/W}$ (S3) and $5.5\,\mathrm{K/W}$ (S4), i.e., a variation by a factor of 1.28. This is significantly higher than the maximum expected measurement uncertainty of up to $15\,\%$ (see Section 3.5) and therefore requires a closer investigation. The fact that the profiles start to deviate already in the range of µs to ms suggests that the difference may result from the die or die attach.

The structure functions in Fig. 5.3b allow a more detailed view. The initial plateau at a thermal capacitance of about $0.001\,\mathrm{W\,s/K}$ corresponds to the $\mathrm{Ga_2O_3}$ dice. The die attach, CuMo spacer, subsequent solder layer, and copper lead frame cause the following section with slightly varying slopes up to about $1\,\mathrm{W\,s/K}$. The $R_{\mathrm{th,jc}}$ determined from the respective splitting points varies between $4.2\,\mathrm{K/W}$ (S3) and $5.2\,\mathrm{K/W}$ (S4), i.e., by a factor of 1.23, which is consistent with the thermal impedance profiles as summarized in Tab. 5.1. For all samples, the slope resulting from spacer, solder layers, and lead frame spans over the same range of about $2\,\mathrm{K/W}$ and $1\,\mathrm{W\,s/K}$. This can be verified by assuming vertical heat flow in the $0.5\,\mathrm{mm}$ thick CuMo spacer ($\lambda_{\mathrm{th}} = 200\,\mathrm{W\,m^{-1}\,K^{-1}}$ [218]) and solder layers ($\lambda_{\mathrm{th}} = 60\,\mathrm{W\,m^{-1}\,K^{-1}}$ [176],

Table 5.1: Essential electrical and thermal parameters of the samples S1–S4 from batch B2a: differential on-resistance r_{o}, K-factor K_{f}, junction-to-case thermal resistance $R_{\mathrm{th,jc}}$ estimated from the thermal impedance profile and the structure function, and junction-to-ambient thermal resistance $R_{\mathrm{th,ja}}$, which is identical for both methods. Adapted from [255].

Parameter	Unit	S1	S2	S3	S4
r_{o} [at $100\,°\mathrm{C}$]	mΩ	408	362	256	349
K_{f} [at $10\,\mathrm{mA}$]	mV/K	1.73	1.74	1.77	1.68
$R_{\mathrm{th,jc}}$ [via $Z_{\mathrm{th}}(t)$]	K/W	4.7	4.9	4.3	5.5
$R_{\mathrm{th,jc}}$ [via str. fct.]	K/W	4.7	4.8	4.2	5.2
$R_{\mathrm{th,ja}}$ [both methods]	K/W	5.5	5.8	5.1	6.2

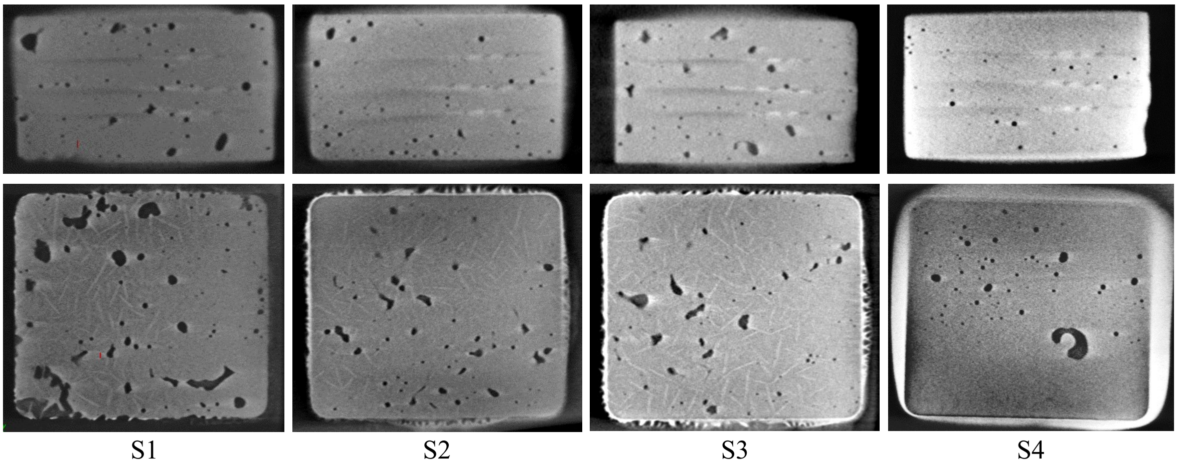


Figure 5.4: Top-view cross-sectional CT scans to investigate the quality of the solder layers between die and CuMo spacer (top row) and CuMo spacer and lead frame (bottom row) for all batch B2a samples. The similarity suggests negligible differences in the quality of the solder layers (especially the die attach layer) between the samples.

thickness $70\,\mu\mathrm{m}$) through an area that is equal to the effective chip size of $4.84\,\mathrm{mm}^2$, and a heat spreading in the $3\,\mathrm{mm}$ thick copper lead frame ($\lambda_{\mathrm{th}} = 394\,\mathrm{W\,m^{-1}\,K^{-1}}$) to twice this area, resulting in a thermal resistance of about $1.8\,\mathrm{K/W}$.

The plateau presumably resulting from the Ga_2O_3 die varies in length. Due to the flat rounded transition between two different materials in the structure function the length cannot be determined with a high precision, but is estimated to be about $2.3\,\mathrm{K/W}$ for S3, $2.6\,\mathrm{K/W}$ for S2, $2.7\,\mathrm{K/W}$ for S1, and 2.9 to $3.4\,\mathrm{K/W}$ for S4. Such differences can have multiple reasons such as variations in thickness or thermal conductivity of the die and the quality of the die attach layer. CT scans are performed for all samples to gain further insight. Side-view cross-sectional images such as in Fig. 5.1c indicate that the thickness of the dice varies by less than $20\,\mu\mathrm{m}$, which corresponds to differences in the $R_{\mathrm{th,die}}$ of below $0.2\,\mathrm{K/W}$ and is thus significantly less than the observed R_{th} variations. Although the resolution of such analyses is limited by the contrast of structures smaller than a few µm, this is consistent with the manufacturer's specifications of possible variations between $189\,\mu\mathrm{m}$ and $204\,\mu\mathrm{m}$. Top-view cross-sectional CT scans in Fig. 5.4 are performed to investigate the quality of the solder layers. The top row images show the solder layer between die and CuMo spacer, and the bottom row images show the solder layer between CuMo spacer and lead frame. For all samples, a rather normal and similar amount of voids in the solder layers is visible. This suggests that differences in the quality of the solder layers should be negligible here. The detailed analysis of the sample structures allows the design of an accurate diode model that is used to gain further insight into the heat dissipation by static and transient thermal simulations conducted in the next section.

5.2.4 Parametric studies to identify critical parameters

The previous section revealed differences in the thermal structure functions and impedance profiles of the four samples under investigation. To better understand this behavior, the transient thermal response of the diodes is simulated and compared to the experimental data. Based on this, the steady state heat distribution is simulated and discussed.

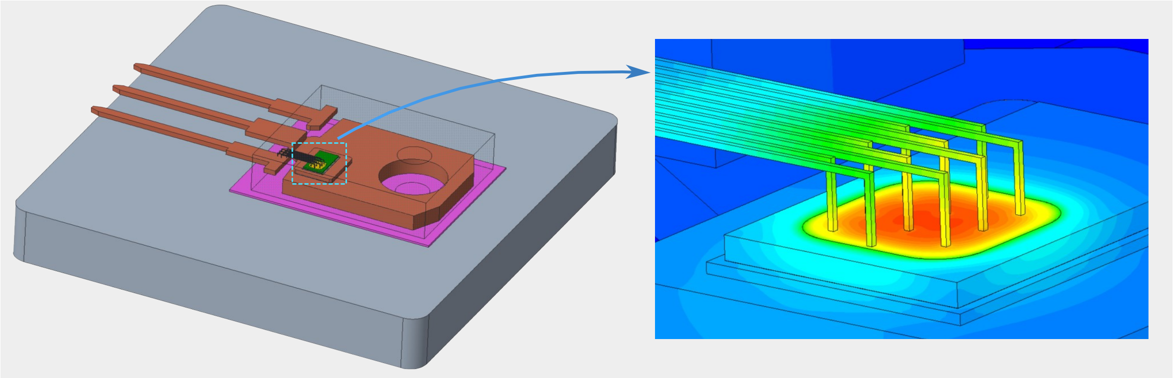


Figure 5.5: Model used to simulate the transient and steady state thermal properties of the TO247-packaged Ga_2O_3 devices of batch B2b. The bottom of the cold plate is defined as 25 °C and a 10 µm thick volume at the chip surface serves as the heat source. For components with unknown thermal conductivity and heat capacity, the values are allowed to vary in a defined range when performing parametric studies.

Model properties and simulation procedure

The CT images of the devices serve as a basis for a precise model shown in Fig. 5.5. The die is 200 µm thick and exhibits the same rectangular shape and anode location as shown in Fig. 5.1b. Since the major part of the heat is created at the Schottky junction and the drift layer [94, 107], a 10 µm thick volume with the same lateral dimensions as the anode is defined as the heat source. A heating power equal to the respective experimental value (about 7 W) is assigned to this volume. The heat sink is implemented by defining the bottom of the cold plate as 25 °C as suggested in [248]. The ambient temperature is set to 25 °C and surface radiation (e.g., from the surface of the mold mass) is taken into account, but is negligible.

The goal of parametric studies is to find material parameters that best describe the measured impedance profiles and structure functions. As visible from Fig. 5.5, the large number of different materials in the heat flow path complicates the calculations. Therefore, the thermal properties of well-known components (e.g., the Al heatsink and Cu lead frame) are defined as a constant value. Subsequent thermal simulations of the steady state heat distribution will show that a major part of the heat is transferred through the substrate rather than the bond wires or the mold mass. Variations in the thermal properties of these components can therefore

Table 5.2: Overview of model parameters used to study the transient thermal properties of the TO247-packaged samples. The allowed ranges of the thermal conductivity λ_{th} and the thermal capacitance C_{th} specified for parametric studies are based on [29, 31, 87, 88, 231, 176, 218]. Adapted from [255].

Layer	**Type**	λ_{th} **(W m^{-1}K^{-1})**	C_{th} **(J kg^{-1}K^{-1})**
die	Ga_2O_3	10–35	400–750
die attach layers	SAC solder	20–905	150–290
spacer	CuMo	150–300	200–400
lead frame	Cu	∼394	∼385
TIM	sheet	∼1.5	∼800
cold plate	Al	∼237	∼900
bond wire	Au	∼300	∼130
encapsulant	mold	∼1	∼1000

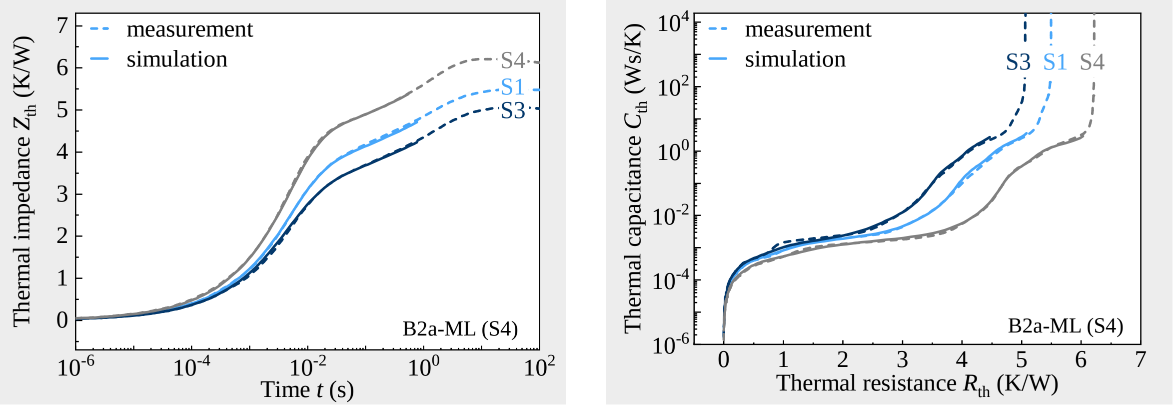
be neglected in comparison with the materials in the main heat flow path. For all other components, most importantly the Ga_2O_3 die, solder layers, and CuMo spacer, the thermal conductivity and heat capacity are allowed to vary within a defined range. The corresponding simulation parameters summarized in Tab. 5.2. The parametric study is performed with the T3Ster autocalibration feature in FloEFD. For each free parameter, at least five scenarios are generated in which the respective parameter is varied within the specified ranges according to a Latin hypercube method. By simulating the transient thermal response for all scenarios and iteratively reducing the parameter ranges, the respective best-fit values are calculated.

Parametric studies and steady state thermal simulations

Parametric studies are conducted for the three samples S1, S3, and S4. By performing the previously mentioned steps, the model parameters of all components within the junction-to-case heat flow path are optimized. The resulting simulated and measured thermal impedance profiles (Fig. 5.6a) and thermal structure functions (Fig. 5.6b) agree well when certain parameters in the model are slightly varied. In this respect, it was explained in Section 5.2.3 that the length of the plateau that corresponds to the $R_{\text{th,die}}$ seems to vary, but it is difficult to distinguish from the die attach layer. Although a variation in thermal conductivity and heat capacity of the die attach is allowed in the parametric study, the best fit is obtained when the thermal conductivity and specific heat capacity of the Ga_2O_3 die are varied between $24\,\mathrm{W\,m^{-1}\,K^{-1}}$ and $500\,\mathrm{J\,kg^{-1}\,K^{-1}}$ for S4, $28\,\mathrm{W\,m^{-1}\,K^{-1}}$ and $615\,\mathrm{J\,kg^{-1}\,K^{-1}}$ for S1, and $31\,\mathrm{W\,m^{-1}\,K^{-1}}$ and $660\,\mathrm{J\,kg^{-1}\,K^{-1}}$ for S3. The specific heat capacities agree with typical literature values of 490 to $600\,\mathrm{J\,kg^{-1}\,K^{-1}}$ [87, 231]. Furthermore, the results suggest a variation of the thermal conductivity within the upper third of the known range of about 10 to $30\,\mathrm{W\,m^{-1}\,K^{-1}}$ [12, 88]. Previously experimentally determined values in the [001] direction (which is about $14°$ off of the [001]* direction of the devices investigated here, see Fig. 2.6) vary between about $15\,\mathrm{W\,m^{-1}\,K^{-1}}$ [29] and $(21 \pm 2)\,\mathrm{W\,m^{-1}\,K^{-1}}$ [89].

When interpreting these results, it must be considered that experimental data are used as input for the calibration, which in turn are associated with measurement uncertainties. In addition, previously mentioned differences in chip thickness could affect the results. However, a smaller die thickness and volume should not only reduce the thermal resistance but also the thermal capacitance, provided that the thermal conductivity and specific heat capacity remain unchanged. In contrast to this, the die with the lowest thermal resistance (S3) also exhibits the highest thermal capacitance, and the die with the highest thermal resistance (S4) also exhibits the lowest thermal capacitance. Note that, as outlined in Section 2.3.2, several studies find that defects in the crystal structure, such as oxygen or gallium vacancies and line defects, significantly affect the thermal conductivity of Ga_2O_3 thin films [90–92]. Furthermore, such defects are known to affect the effective doping concentration and electrical properties [87, 102]. Considering that the samples S1–S4 also vary in their forward current–voltage profiles, this could indeed hint at a certain variation in the thermal conductivity of the die caused by a variation of material properties across the wafer — even though potentially to a lesser extent than suggested by the simulation and measurement due to the above-discussed influences. To obtain a more definite answer, it is suggested to combine, e.g., energy dispersive X-ray spectroscopy (EDX) to map different elements in the die with thermoreflectance or laser pulsed methods to determine the precise thermal conductivity. These experimental methods are, however, not available in this work.

The calibrated model enables the study of the steady state heat distribution in the Ga_2O_3 dice in more detail. A thermal conductivity of $28\,\mathrm{W\,m^{-1}\,K^{-1}}$ is defined for the Ga_2O_3



(a) **(b)**

Figure 5.6: Measured and simulated (a) thermal impedance profiles and (b) structure functions of the 200 µm thin TO247-packaged Ga_2O_3 samples when all parts within the junction-to-case heat flow path are fully calibrated. The best match between measurement and simulation is observed when the thermal conductivity and heat capacity of the Ga_2O_3 dice are varied within the typically observed ranges. Adapted from [255].

die based on the best-fit parameter for sample S1, and the heating power is set to $7\,\mathrm{W}$. Other material parameters correspond the average values summarized in Tab. 5.2. Steady state thermal simulations are performed for both the $2.2\,\mathrm{mm} \times 3.8\,\mathrm{mm}$ rectangular and the $2.2\,\mathrm{mm} \times 2.2\,\mathrm{mm}$ square die. Figure 5.7 displays the corresponding temperature distribution and heat flux through a cross section in the center of the dice. Regarding the rectangular die (top), the heat does not spread significantly into the additional volume of the die that is not electrically connected with bond wires. Therefore, the heat distribution and heat flux remain similar when reducing the die size to the effective square size with an only $300\,\mathrm{\mu m}$ wide rim around the anode. Consequently, an average junction temperature of about $62\,^{\circ}\mathrm{C}$ and $R_{\mathrm{th,die}}$ of $2.8\,\mathrm{K/W}$ is obtained in both scenarios. These values also agree with the experimental data in Fig. 5.2a and Fig. 5.3. Next, the chip thickness is increased to the standard value of $500\,\mathrm{\mu m}$ such as in [97]. This increases the $T_{\mathrm{j,ave}}$ and $R_{\mathrm{th,die}}$ to about $81\,\mathrm{K}$ and $6.3\,\mathrm{K/W}$. This means that, according to the simulation, the thermal resistance of the die is reduced by about $55\,\%$ and the average junction temperature is reduced by about $23\,\%$ by substrate thinning to $200\,\mathrm{\mu m}$ in this setup.

Comparison and further steps

In a recent study [97], a $1\,\mathrm{mm}$ thick silver plate was bonded to both sides of a $500\,\mathrm{\mu m}$ thick and $4.6\,\mathrm{mm} \times 4.6\,\mathrm{mm}$ large die with an anode size of $3\,\mathrm{mm} \times 3\,\mathrm{mm}$ by pressureless silver sintering. Subsequent transient thermal measurements indicated an $R_{\mathrm{th,die}}$ ($R_{\mathrm{th,jc}}$) of $0.8\,\mathrm{K/W}$ ($1.43\,\mathrm{K/W}$) when cooling the assembly from the cathode side. This corresponds to an area-specific $R_{\mathrm{th,die}}$ of $17\,\mathrm{mm^2\,K/W}$, and an area-specific $R_{\mathrm{th,jc}}$ of $30\,\mathrm{mm^2\,K/W}$. Taking sample S3 with an estimated $R_{\mathrm{th,die}}$ of $2.3\,\mathrm{K/W}$ as a reference, this suggests that an up to $34\,\%$ lower specific $R_{\mathrm{th,die}}$ of $11\,\mathrm{mm^2\,K/W}$ and an up to $33\,\%$ lower specific $R_{\mathrm{th,jc}}$ of $20\,\mathrm{mm^2\,K/W}$ is achieved here. Thus, substrate thinning seems to be more effective than sintering metal plates to both sides of the die and cooling it from the cathode side, but possibly still less effective than cooling the die from the junction side [94, 97]. Also, the effect of substrate thinning seems to be smaller than expected from the thermal simulations.

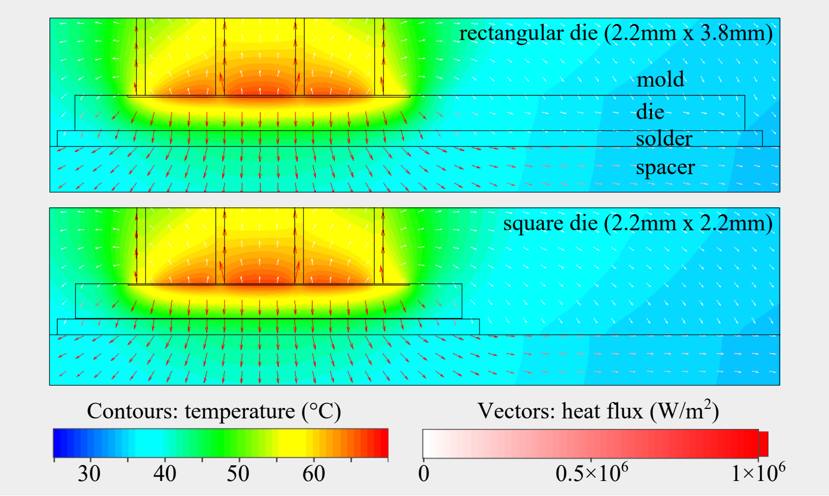


Figure 5.7: Simulated steady state temperature and heat flux profiles through a cross section of the actual rectangular die (top) and the hypothetical effective square die (bottom) of the 200 µm thin TO247-packaged sample. The heat does not spread significantly into the part of the die that is not electrically connected with bond wires, and the major part of the heat is dissipated vertically through the substrate. Consequently, the difference in junction temperature is negligible. Adapted from [255].

The main reason for this is that the comparison is inevitably limited by certain factors: First, the package structures vary considerably (sintering to a Ag plate in [97] versus soldering to a CuMo spacer on a TO247 lead frame here).

Second, also the anode and chip sizes differ substantially and, as discussed, the thermal properties of the substrate may vary to a certain degree. Both effects decisively influence the heat flow in the chip and package. Thus, while this section reveals the details of the heat dissipation in thinned Ga_2O_3 chips, a more comparable setup is required to judge the effectiveness of different cooling methods and compare the heat dissipation to mature technologies such as SiC.

5.3 Direct comparison of substrate thinning and junction-side cooling

5.3.1 Overview and investigated samples

In the previous section, new TO247-packaged 200 µm thin Ga_2O_3 diodes were introduced. The combination of parametric studies and experimental data indicates a certain variation of material properties, but ultimately suggests that substrate thinning seems to be effective in reducing the junction temperature. Based on this, this section directly compares the heat dissipation in 600 µm thick cathode-side cooled (CSC), 200 µm thin CSC, and also 200 µm thin junction-side cooled (JSC) Ga_2O_3 bare dice with identical lateral dimensions (ML-type) more precisely. Furthermore, a commercial SiC bare die (sample SiC-A) with a similar die and anode size is used as a benchmark. As shown in Fig. 5.8, all samples are assembled in the same way on custom AlN-DPC substrates via pressureless silver sintering and wire bonding according to the methods described in Section 3.2. This setup allows a fair and comparable investigation of the thermal properties, which is missing in literature. In addition, a 600 µm thick LL-type diode is assembled in the same manner to briefly discuss the effect of increasing chip size on thermal resistance, although this will not be the focus for reasons explained below.

Table 5.3: Overview of Ga_2O_3 and SiC diodes with die thickness z_{die} mounted on DPC substrates in cathode-side cooled (CSC) and junction-side cooled (JSC) configuration. As shown in Section 5.2, the rectangular die shape of sample J200* does not affect the thermal properties significantly. The pressureless silver sintering process and determination of the die-attach thickness z_{att} after sintering was performed externally by a contractor. Adapted from [259].

Die material	Batch no.	Anode (mm^2)	Die (mm^2)	z_{die} (µm)	Cooling method	Sample abbrev.	Print area (mm^2)	z_{att} (µm)
β–Ga_2O_3	B2c	1.6 × 1.6	2.2 × 2.2	600	CSC	C600	2.5 × 2.5	114
β–Ga_2O_3	B2b	1.6 × 1.6	2.2 × 2.2	200	CSC	C200	2.5 × 2.5	133
β–Ga_2O_3	B2b	1.6 × 1.6	2.2 × 2.2	200	JSC	J200	1.5 × 1.5	108
β–Ga_2O_3	B2b	1.6 × 1.6	2.2 × 3.8	200	JSC	J200*	1.5 × 1.5	121
β–Ga_2O_3	B2c	3.2 × 3.2	3.8 × 3.8	600	CSC	C600LL	4.3 × 4.3	114
SiC	SiC-A	1.65 × 1.65	1.92 × 1.92	377	CSC	S377	2.0 × 2.0	123

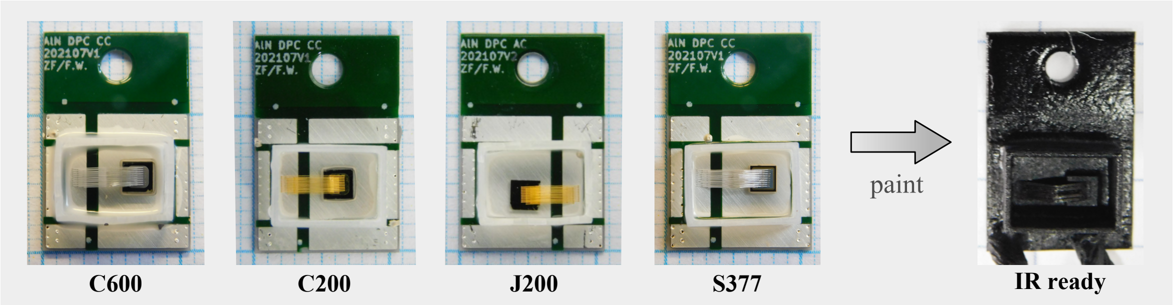


Figure 5.8: Photograph of the CSC and JSC ML-size Ga_2O_3 samples and the CSC SiC reference diode after assembly on AlN-DPC substrates. The devices are covered in black paint for temperature measurements with an infrared (IR) camera. Adapted from [259].

Table 5.3 provides an overview of the corresponding devices under investigation. Samples J200 and J200* are identical regarding their junction structure, but sample J200* is diced out in a rectangular shape such as the one shown in Fig. 5.1b, whereas sample J200 is diced out in a standard square shape with a 300 µm wide rim around the anode. As discussed in Section 5.2.4, the difference in shape does not influence the thermal resistance significantly. Nevertheless, the rectangular sample J200* will not primarily be used to study the heat dissipation. It will, however, be used to assess the influence of varying differential on-resistances resulting from a variation of material properties across the wafer on the current and power rating. For CSC samples, the aperture opening of the sintering stencil can be larger than the actual chip size which ensures a proper thermal coupling to the substrate and heatsink. For JSC samples however, the aperture opening leaves a gap of 50 µm between sinter paste and edge of the anode. This is to ensure full electrical functionality by avoiding an overflow of the sinter paste to the outer parts of the diode when the die is placed, causing undesired electric fields close to the edge termination region or even damage to the die.

Samples C600 and S377 are gold metallized on the cathode side and aluminum metallized on the anode side of the dice, whereas samples C200, J200, and J200* are gold metallized on both sides of the die. Therefore, to ensure a reliable bond and achieve a similar current capability, samples C600 and S377 are electrically contacted with 30 Al wires with a diameter of 40 µm, whereas 30 gold wires with a diameter of 30 µm are used for samples C200, J200, and J200*. The effect of these slight differences in the assembly on the results derived in this chapter is negligible, especially considering that the major part of the heat is dissipated through the substrate to the cold plate (see Section 5.2.4) [255]. The aluminum metallized sample C600LL was contacted with 30 pieces of $100\,\mu\mathrm{m}$ thick aluminum bond wires.

The devices were subjected to JEDEC JESD51-15 compliant measurements of the thermal impedance profiles and structure functions with two different TIMs (either thermal grease or a thin thermal sheet) according to the procedures explained in Section 3.5. In addition, the junction temperature is measured after heating for $50\,\mathrm{s}$ with different heating currents and corresponding heating powers applied to the diode. From this, conclusions about the power and current rating of the devices can be derived. The junction temperature is determined via the $\sqrt{t}$-method and also with an Optris PI 640i high-resolution infrared (IR) camera (system accuracy $2\,\mathrm{K}$ or $2\,\%$, the higher value applies) placed directly above the respective die. For IR measurements the devices were covered in a thin layer of black paint as shown in Fig. 5.8 to raise the emissivity close to unity and enhance the measurement accuracy.

5.3.2 Differences in the thermal structure

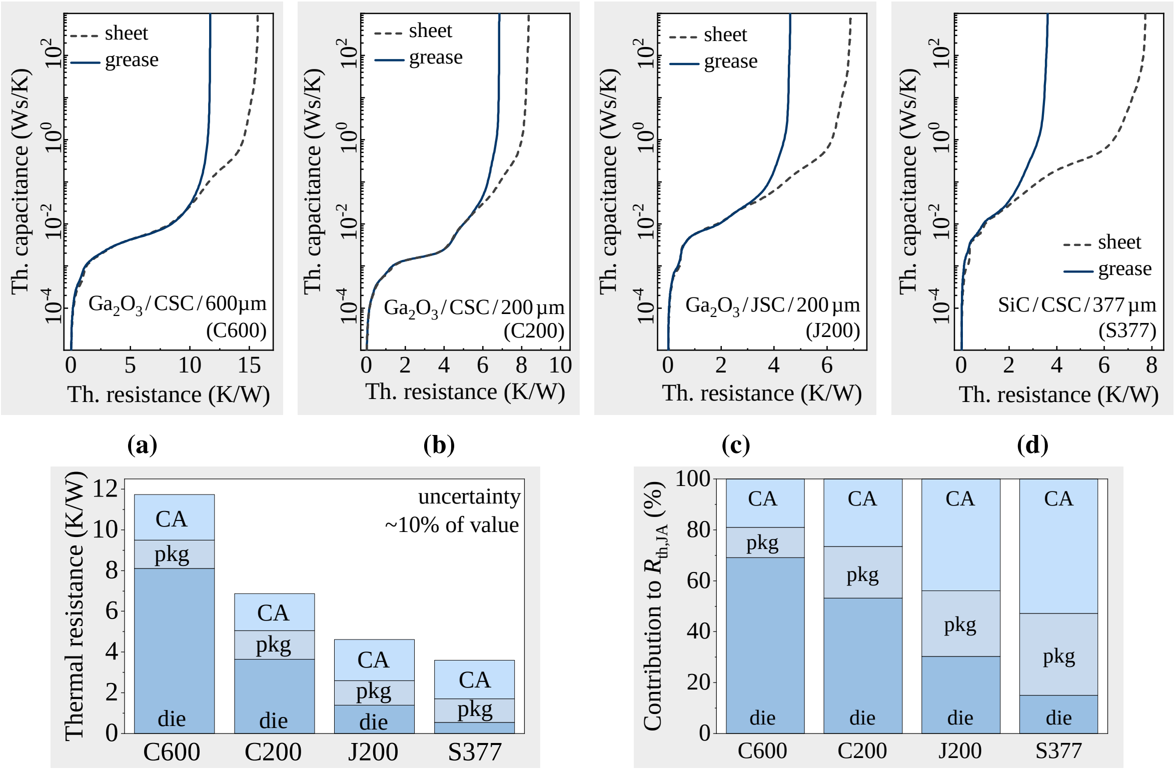
Transient thermal measurements

For all samples, both the thermal impedance profiles and structure functions are measured and show consistent results. For the setup with grease as TIM, the junction-to-ambient thermal resistance $R_{\text{th,ja}}$ reduces from $11.7\,\mathrm{K/W}$ for C600 over $6.9\,\mathrm{K/W}$ for C200 to $4.6\,\mathrm{K/W}$ for J200. The lowest $R_{\text{th,ja}}$ of $3.6\,\mathrm{K/W}$ is achieved with the reference SiC diode S377. Due to the identical assembly method and experimental setup, the differences must be caused predominantly by the dice. Since the structure functions are more suitable to distinguish the different parts in the entire heat flow path, they are analyzed in more detail in the following.

As shown in Fig. 5.9 the curves with two different TIMs coincide up to a certain point as they result from the heat flow within the package, which helps to identify different parts of the structure functions. The regions from the respective separation points to about $1.3\,\mathrm{K/W}$ left of them originate from the AlN-DPC and the sintered silver layer. The rather flat plateau-like regions with varying length extending from there down to $0\,\mathrm{K/W}$ are associated with the thermal resistance and capacitance of the respective dies.

From this, the contribution of the various parts within the heat flow path to the total $R_{\text{th,ja}}$ can be divided into those coming from the chip, the package (i.e., the die-attach layer and the AlN substrate, abbreviated as pkg), and the cooling apparatus (i.e., the remaining path from the case to ambient, abbreviated as CA). Considering the results obtained from the measurements with thermal grease as TIM, the contribution of the cooling apparatus is similar for all samples (1.8 to $2.2\,\mathrm{K/W}$), and the same applies for the contribution of the package (1.2 to $1.4\,\mathrm{K/W}$). This is plausible since all devices are mounted in the same way and thus validates the measurements.

Furthermore, the thermal resistance of the die ($R_{\text{th,die}}$) is about $3.6\,\mathrm{K/W}$ in case of C200, which is similar to the value observed for the $200\,\mu\mathrm{m}$ thin sample S4 in Section 5.2.3. Compared to a value of $8.1\,\mathrm{K/W}$ for C600, this corresponds to a reduction of the $R_{\text{th,die}}$ of about $55\,\%$ by substrate thinning from 600 to $200\,\mu\mathrm{m}$, which is in agreement with the considerations in Section 5.2.4. An additional $60\,\%$ reduction down to an $R_{\text{th,die}}$ of $1.4\,\mathrm{K/W}$ is achieved for J200, i.e., by cooling the diode from the junction side. However, this is still more than twice the $R_{\text{th,die}}$ of the commercial and nearly twice as thick SiC-A reference diode, which exhibits the lowest $R_{\text{th,die}}$ of about 0.5 to $0.6\,\mathrm{K/W}$. Even in JSC assembly, the low thermal conductivity of Ga_2O_3 seems to limit the heat dissipation. The underlying reasons and methods to improve the effective thermal resistance down to the level of SiC will be studied in Section 5.3.4.



(a) (b) (c) (d)

(e) (f)

Figure 5.9: (a)–(d) The thermal structure functions with two TIMs show a decrease of the junction-to-ambient ($R_{\text{th,ja}}$) and junction-to-case ($R_{\text{th,jc}}$) thermal resistance in the order (a) C600, (b) C200, (c) J200, (b) S377. (e) The thermal resistance can be divided into the (e) absolute and (f) relative contributions of the die, the package (pkg) and the remaining thermal path from case to ambient (CA) to the total $R_{\text{th,ja}}$. Substrate thinning is highly effective in reducing the $R_{\text{th,ja}}$ and $R_{\text{th,jc}}$, but even in case of the $200\,\mu\text{m}$ thin sample C200 the die still dominates the $R_{\text{th,ja}}$ with more than $50\,\%$. Junction-side cooling is most effective, but $R_{\text{th,jc}}$ and $R_{\text{th,ja}}$ are still higher than for the CSC SiC sample S377. Adapted from [259].

The relative contributions of the different parts to the total $R_{\text{th,ja}}$ are displayed in Figs. 5.9e and 5.9f. For the C600 sample, the packaging and cooling apparatus together account for only about $30\,\%$ of the $R_{\text{th,ja}}$. For the thinned device C200, about half of the $R_{\text{th,ja}}$ is caused by package and cooling apparatus, and for the JSC device J200 the share increases to about $70\,\%$. Thus, for thick Ga_2O_3 chips, improving the TIM or cold plate has comparatively little effect because the chip dominates the thermal resistance. For JSC assemblies, however, this issue is highly relevant. In case of the SiC-A sample, the die contributes with only about $15\,\%$ to the $R_{\text{th,ja}}$ and the heat dissipation is mostly limited by the package, TIM, and cold plate. In the following, the effect of these different thermal structures on the surface temperature of the devices is studied in more detail.

Thermal imaging of the steady state surface temperature

To study the surface temperatures of the devices, all samples are heated with a power of about $10\,\text{W}$ by applying forward currents of $3.7\,\text{A}$ (C600), $4.2\,\text{A}$ (C200), $4.6\,\text{A}$ (J200), and $7.2\,\text{A}$ (S377). The resulting infrared images after heating for $50\,\text{s}$ are shown in Fig. 5.10.

For CSC samples, the maximum temperature is located approximately in the middle of the anode, as it constitutes the major heat source. However, the high number of bond wires

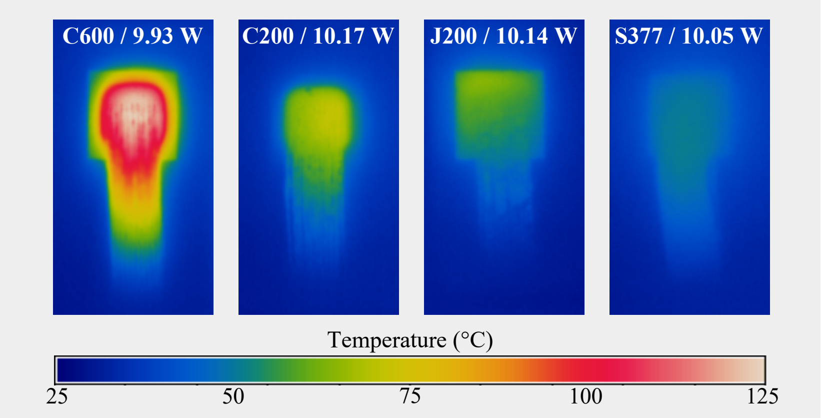


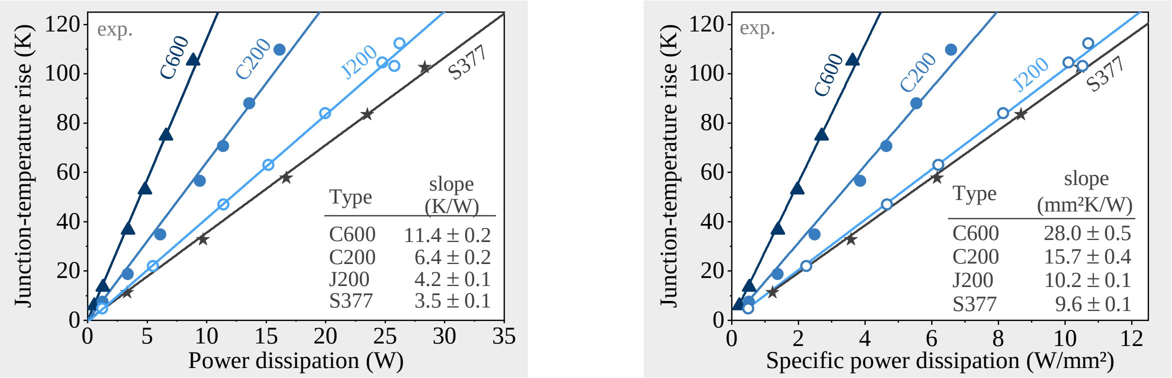
Figure 5.10: Steady state surface temperature after heating with about 10 W. For CSC assemblies, the peak temperature is located approximately in the center of the die as the anode constitutes the main heat source, but it is underestimated due to shading by the bond wires. Among the Ga_2O_3 samples, the lowest peak temperature is achieved with JSC sample J200, although it is still higher than that of the CSC SiC sample S377. Furthermore, it occurs on the side of the chip instead of the center, which presumably results from a non-ideal coverage of the anode surface with die-attach material. Adapted from [259].

results in a shading of the anode area. Therefore, the surface temperature appears somewhat inhomogeneous and the measured maximum surface temperature is expected to be lower than the actual one. In addition, note that the junction temperature and anode surface temperature usually differ by up to a few Kelvin. For the JSC sample J200, the peak surface temperature (i.e., cathode temperature) is located at the side of the chip instead of the center, and there is a pronounced lateral temperature gradient from the upper left corner to the lower right corner. This suggests that an area along the outer edge of the anode is not properly coupled to the heatsink – presumably caused by the printing area leaving a 50 µm edge between sinter paste and edge of the anode area and potential misalignments of anode and paste area. Thus, while the inner part is effectively cooled, the non-connected outer edge of the die can heat up. This hypothesis will be confirmed by simulations in Section 5.3.4.

Substrate thinning from 600 µm to 200 µm results in a decrease of the apparent maximum surface temperature from 125 °C (C600) to 72 °C (C200). For the JSC sample, the maximum surface temperatuere further decreases to 64 °C despite the previously discussed effect. With that it is closest to the commercial SiC chip, which heats up to only 52 °C. The surface temperature thus decreases in the same order as expected from the thermal resistance measurements. Note that the limited heat dissipation in the thick C600 Ga_2O_3 die also causes the bond wires to heat up more than in case of C200 or J200, although the same power is dissipated in the diode and an even lower current is conducted through them. Therefore, substrate thinning might also be advantageous from a bond reliability point of view, as the temperature swing and temperature drop per current unit across them is decreased. However, a larger number of samples would be required for sound reliability studies.

5.3.3 Impact on power and current rating

To examine the impact of the different assembly methods on the power and current rating, different heating currents and corresponding heating powers are applied to the diodes. The average junction temperature is determined with the $\sqrt{t}$-method after heating for 50 s. This way, the influence of differences between surface and junction temperature and of parasitic



(a) **(b)**

Figure 5.11: Junction temperature measured with the $\sqrt{t}$-method when different heating powers are applied. (a) The $R_{\mathrm{th,ja}}$ extracted from the slope of the linear fit agrees with the structure functions. The JSC Ga_2O_3 device J200 exhibits the highest power rating, although slightly lower than that of the CSC SiC reference diode S377. (b) The difference between J200 and S377 decreases slightly, when the results are related to the anode area. Adapted from [259].

shading effects due to the bonding wires is circumvented. Note that no safe operating area or maximum possible current is defined by the manufacturer of the diodes. To avoid potential harm to the dice, a maximum average junction temperature of about $140\,°\mathrm{C}$ at the maximum DC forward current is not exceeded. Generally, the low increase in on-resistance (see Section 4.2.4 [253, 260]) in combination with recent reports of Ga_2O_3 transistor cells being operated successfully at $500\,°\mathrm{C}$ [217] indicates that junction temperatures exceeding the chosen maximum are feasible in general.

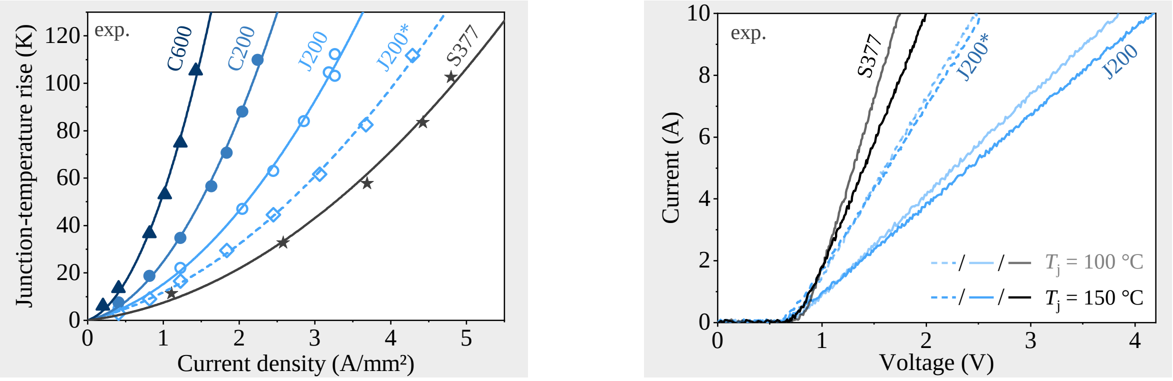
Power Rating

In the following, the term “power rating” describes the maximum possible heating power that leads to a defined maximum allowed rise in average junction temperature. Figure 5.11a shows how the average junction temperature rises when the heating power P_{H} is increased.

For CSC assemblies, the junction temperatures are significantly higher than suggested by the IR images because, as discussed, the temperature maximum is located in the center of anode, which is shaded by bond wires. For the JSC assembly, the junction temperatures are only slightly higher because the peak temperatures occur at side of the chip resulting from a gap between anode edge and die attach. This agrees with the considerations in Section 5.3.2.

As expected from $\Delta T_{\mathrm{j}} = R_{\mathrm{th,ja}} \cdot P_{\mathrm{H}}$, a linear relationship is observed and the $R_{\mathrm{th,ja}}$ can be calculated from the corresponding linear fit. For the sake of clarity, the data for J200* are not shown here. However, its fitted $R_{\mathrm{th,ja}}$ of $(4.20 \pm 0.03)\,\mathrm{K/W}$ agrees with a value of $(4.20 \pm 0.09)\,\mathrm{K/W}$ obtained for J200. This confirms that the additional inactive part of the die (see Section 5.2.1) has a negligible effect on the heat dissipation also in JSC assemblies.

For all samples, the $R_{\mathrm{th,ja}}$ agrees with the respective value obtained from the transient thermal measurements (Fig. 5.9), although systematically being a few percent lower. The reason is that in transient thermal measurements only one value resulting from a temperature swing of about 90 to $110\,\mathrm{K}$ is determined. At high temperatures, the thermal conductivity of the materials in the heat flow path is reduced, which translates to an increased $R_{\mathrm{th,ja}}$. In Fig. 5.11a, however, an average value also over lower temperatures is obtained.



(a) **(b)**

Figure 5.12: (a) Junction temperature versus heating current density related to the anode area. Substrate thinning increases the power rating, but the highest current rating is achieved with junction-side cooling. (b) Forward current–voltage profiles at junction temperatures of $100\,°\mathrm{C}$ and $150\,°\mathrm{C}$ show that the difference between J200 and J200* in (a) results from a variation of the differential on-resistance. Adapted from [259].

Since the lateral dimensions of SiC and the $\mathrm{Ga_2O_3}$ samples are similar but not identical, the power dissipation is related to the respective anode area in Fig. 5.11b. From this, an increase in power rating by $78\,\%$ through substrate thinning from $600\,\mu\mathrm{m}$ to $200\,\mu\mathrm{m}$ is obtained. For the JSC assembly, the power rating increases by another $53\,\%$ which, however, is still about $6\,\%$ below the SiC-A reference power rating.

Current rating

The previous considerations only reflect the pure thermal properties of the devices as they take into account only the power loss. In order for the electrical properties (i.e., in particular the differential on-resistance) to be taken into account as well, the rise in junction temperature is plotted as a function of the applied current density in Fig. 5.12a. In the following, the term “current rating” describes the maximum possible heating current that leads to a defined maximum allowed rise in average junction temperature.

In contrast to the previous measurements, a significant difference is now visible between samples J200 and J200*. Since the $R_{\mathrm{th,ja}}$ of these samples is almost identical, the reason can only lie in their electrical properties. Figure 5.12b shows the forward characteristics of samples J200, J200* and S377 at junction temperatures of $100\,°\mathrm{C}$ and $150\,°\mathrm{C}$. All samples exhibit a similar knee voltage V_0 of about $0.7\,\mathrm{V}$. Due to a variation of the drift layer regarding its effective donor concentration and potentially also its thickness (see Section 4.2.3 [255]), the differential on-resistance of sample J200* is almost half that of sample J200. The S377 reference diode shows the lowest differential on-resistance. Although the $R_{\mathrm{th,ja}}$ is similar for these samples, this translates to substantial differences in the junction temperature. For example, at a current density of $3.7\,\mathrm{A/mm^2}$, a temperature rise of $58\,\mathrm{K}$ and $83\,\mathrm{K}$ is achieved for S377 and J200*, respectively, while this current density cannot be applied to sample J200 because the maximum junction temperature would be exceeded. To obtain a more quantitative comparison, the rise in junction temperature can be expressed as

$$\Delta T_{\mathrm{j}} = R_{\mathrm{th,ja}} \cdot P_{\mathrm{cond}} = R_{\mathrm{th,ja}} \cdot \left(V_0\, I_{\mathrm{f}} + r_{\mathrm{o}}\, I_{\mathrm{f}}^{\,2}\right). \tag{5.2}$$

Table 5.4: The effective knee voltage V_0' and specific differential on-resistance $r_{\mathrm{o,sp}}'$ obtained by fitting the data in Fig. 5.12a with Eq. 5.2 agree well with respective curve-tracer measurements at $125\,^\circ\mathrm{C}$. The ratios γ_T, calculated from Eq. 5.3 and the $R_\mathrm{th,ja}$ in Fig. 5.11b, show that for the JSC assembly the conduction losses would need to drop to only $6\,\%$ below the SiC level to reach the same junction temperature as the SiC reference. Adapted from [259].

Sample name	Fitted V_0' (V)	Fitted $r_{\mathrm{o,sp}}'$ ($\mathrm{m\Omega cm^2}$)	$r_{\mathrm{o,sp}}$ at $125\,^\circ\mathrm{C}$ ($\mathrm{m\Omega cm^2}$)	Needed ratio γ_T	Needed P_cond drop below SiC ref.
C600	0.43 ± 0.16	14.9 ± 1.4	11.7	0.34	$66\,\%$
C200	0.44 ± 0.17	11.4 ± 4.0	8.5	0.61	$39\,\%$
J200	0.74 ± 0.20	7.5 ± 0.7	7.8	0.94	$6\,\%$
J200*	0.75 ± 0.07	4.1 ± 0.2	4.3	0.94	$6\,\%$
S377	0.42 ± 0.25	3.6 ± 0.1	2.8	–	–

The data in Fig. 5.12a can be fitted with this relationship when setting $R_\mathrm{th,ja}$ to the respective value determined in Fig. 5.11 and defining V_0 and r_o as free variables. Both parameters depend highly on the junction temperature. Therefore, this approach results in effective values V_0' and $r_{\mathrm{o,sp}}'$ averaged over the entire temperature and current range.

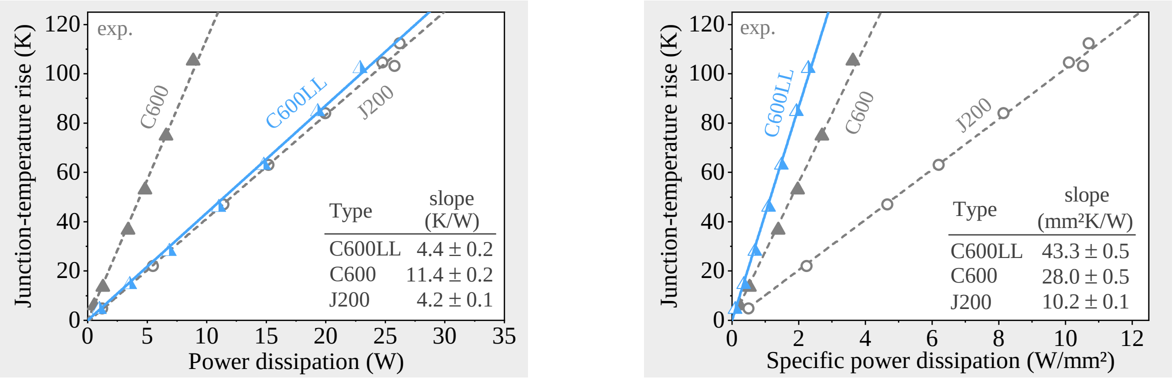
The results are summarized in Tab. 5.4. Taking into account the associated uncertainties, the knee voltages are similar for all samples. Furthermore, the averaged specific differential on-resistances increase in the order S377, J200*, J200, C200, and C600. These values agree with the differential on-resistances measured with a curve tracer at a junction temperature of $125\,^\circ\mathrm{C}$, which are also summarized in Tab. 5.4. The $r_{\mathrm{o,sp}}$ of C200 and J200 are similar but almost twice as high as that of the also $200\,\mu\mathrm{m}$ thin sample J200* because of the previously discussed influences. Sample C600 exhibits the largest $r_{\mathrm{o,sp}}'$ and $r_{\mathrm{o,sp}}$. This is reasonable because a thicker substrate should exhibit a larger electrical resistance and demonstrates the benefits of substrate thinning also in terms of on-resistance. With the fitted lines in Fig. 5.12a as a reference, and when assuming a maximum permitted rise in junction temperature of $100\,\mathrm{K}$, the current rating can be quantified: Starting from $1.41\,\mathrm{A/mm^2}$ for C600 it increases by $54\,\%$ to $2.17\,\mathrm{A/mm^2}$ for C200. With $3.13\,\mathrm{A/mm^2}$ ($4.05\,\mathrm{A/mm^2}$) an additional $44\,\%$ ($87\,\%$) increase is observed with junction-side cooling for sample J200 (J200*). The highest value of $4.83\,\mathrm{A/mm^2}$ is obtained for the SiC-A reference sample S377.

Lowering the junction temperature by increasing the chip size

It was suggested in [223] that simply increasing the chip and corresponding die attach area may be effective in reducing the junction temperature of $\mathrm{Ga_2O_3}$ diodes. Here, a short experimental examination of this hypothesis is given.

To this end, a $600\,\mu\mathrm{m}$ thick LL-type $\mathrm{Ga_2O_3}$ diode was assembled in CSC configuration on AlN-DPC substrates in the same way as the previous diodes. The sample will be referred to as C600LL in the following. It exhibits an about four times larger anode area of $3.2\,\mathrm{mm} \times 3.2\,\mathrm{mm}$ and an about 3 times larger chip size of $3.8\,\mathrm{mm} \times 3.8\,\mathrm{mm}$ than the ML-type diodes. Accordingly, a significant reduction in the thermal resistance is expected.

Figure 5.13a shows the rise in average junction temperature of the sample as determined by the $\sqrt{t}$-method. In addition, the previous results obtained with ML-size diodes C600 and J200 are shown. By increasing the die size, the average junction temperature is reduced significantly. Thus, the junction-to-ambient thermal resistance $R_\mathrm{th,ja}$, calculated from a linear fit to the data, is reduced to $4.4\,\mathrm{K/W}$, making the method almost as effective as junction-side cooling. Compared to sample C600, the power rating increases by a factor of about 2.6.



(a) **(b)**

Figure 5.13: Rise in junction temperature T_j for a $600\,\mu\mathrm{m}$ thick LL-size diode compared to previous assemblies with ML-size diodes. (a) Increasing the die size of a $600\,\mu\mathrm{m}$ thick Ga_2O_3 diode by about a factor of three increases the absolute power rating by a factor of about 2.6. (b) Relating the increase in T_j to the actual anode size reveals a decrease in the maximum possible power density compared to the smaller C600 sample. Adapted from [259].

However, it must be taken into account that an increase in the size of the chip also means a reduction in the specific power dissipation. Figure 5.13b therefore compares the junction temperature in relation to the specific (i.e., with respect to the anode area) power dissipation. With a specific $R_\mathrm{th,ja}$ of about $43.3\,\mathrm{mm}^2\,\mathrm{K/W}$, the area-related cooling performance of sample C600LL is actually worse than that of the smaller ML-size diode. Therefore, increasing the die size is not in line with the general goal of enhancing the power density. In addition, increasing the die size will also increase the chip cost and inherently contradicts the potential cost advantage of Ga_2O_3. Therefore, the following discussion only focuses on methods that allow a reduction of the junction temperature without changing the chip size.

Discussion of experimental results

To be competitive, Ga_2O_3 diodes should exhibit an equivalent or lower rise in junction temperature than their SiC counterparts under the same operating conditions, i.e., the same forward current and die size. To investigate the implications for Ga_2O_3 diodes, the following discussion assumes an application in which conduction losses dominate. Accordingly, $\Delta T_\mathrm{j,GaO}/\Delta T_\mathrm{j,SiC} \leq 1$ should be satisfied at the same forward current. Using Eq. 5.2 and assuming the limit where the quotient is equal to one, this requirement can be expressed as

$$\frac{P_\mathrm{cond,GaO}}{P_\mathrm{cond,SiC}} \overset{!}{=} \frac{R_\mathrm{thJA,SiC}}{R_\mathrm{thJA,GaO}} := \gamma_\mathrm{T}, \tag{5.3}$$

where γ_T basically describes the maximum allowed conduction loss in Ga_2O_3 diodes with a given junction-to-ambient thermal resistance $R_\mathrm{th,ja}$ that will lead to the same rise in junction temperature as in a SiC counterpart of identical chip size at the same forward current. The junction-to-ambient thermal resistance are already known for all devices from Fig. 5.11. Therefore, γ_T can directly be calculated for each sample. Since the active area constitutes the main heat source, and the on-resistance and thermal resistance depend heavily on it, specific values related to the respective anode area are used for the evaluation.

The results are summarized in Tab. 5.4. Due to the high thermal resistance of the $600\,\mu\mathrm{m}$ thick substrate, the conduction losses of the C600 sample would have to drop to one-third of the conduction losses of the SiC diode in order to achieve the same junction temperature. For the thinned sample C200, conduction losses $39\,\%$ below the SiC level would be required, and for the JSC samples J200 and J200* the difference reduces to only $6\,\%$ below the SiC reference. Therefore, JSC assemblies appear to be the most effective and require the least progress in lowering the on-resistance. Note that the results may be influenced to a certain extent by a variation in thermal properties, as discussed in Section 5.2. To validate the data and gain a deeper understanding of the differences in heat dissipation, the results are backed up with thermal simulations in the next section.

5.3.4 Simulative validation and methods to improve junction-side cooling

The previous section showed that even a slight difference in die size and thickness or a variation of the material properties can affect the results of the thermal measurements. Therefore, the experimental setup is replicated in FloEFD and thermal simulation data are compared to the measurements. This will also allow to study how the cooling methods can be improved.

Simulation model

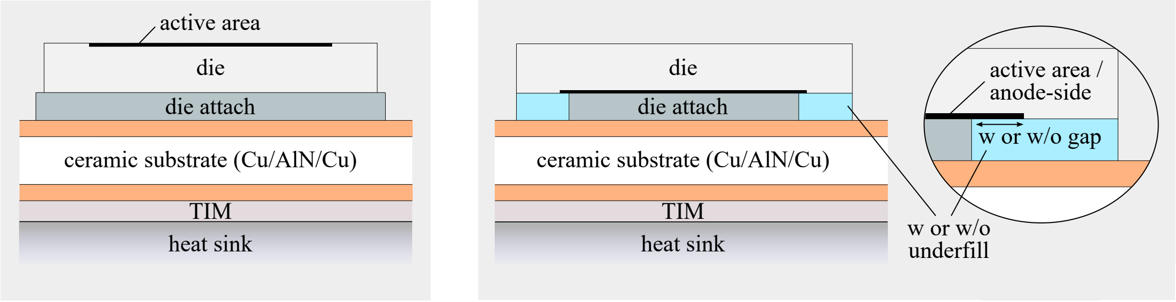
The results in Section 5.2.4 indicate that only a minor part of the heat is dissipated through the bond wires. Therefore, they are omitted in the following. Fig. 5.14 shows the model for CSC and JSC assemblies, and Tab. 5.5 summarizes the corresponding simulation parameters. For CSC assemblies, the entire cathode is thermally coupled with the ceramic substrate and the cold plate via the die attach. For JSC assemblies, either the entire anode is covered with die attach, or a $50\,\mu\mathrm{m}$ gap between anode edge and die attach is inserted. This value corresponds to the experimental aperture size of $1.5\,\mathrm{mm} \times 1.5\,\mathrm{mm}$ for the $1.6\,\mathrm{mm} \times 1.6\,\mathrm{mm}$ ML-type diode (see Tab. 5.3).

All devices (i.e., both the Ga_2O_3 and SiC model) are $2.2\,\mathrm{mm} \times 2.2\,\mathrm{mm}$ large and have a $1.6\,\mathrm{mm} \times 1.6\,\mathrm{mm}$ large anode. This means that the SiC model is slightly larger than the actual die which, however, makes the simulation more comparable. Based on the dimensions of the actual drift layer, the anode area is thickened to $10\,\mu\mathrm{m}$ and defined as a volume heat source. Even in the scenario with gap, the entire active area is considered to have a diode function. Therefore, the definition of the heat source is not changed, but the heat flow into the die-attach material and ceramic substrate is affected. The heat sink is implemented by defining the bottom of the cold plate as $25\,^{\circ}\mathrm{C}$.

The thickness of the sintered silver layer is set to $120\,\mu\mathrm{m}$, which is equal to the average experimental die-attach thickness (see Tab. 5.3). Given this rather high value, the effect of a reduced thickness of the die-attach material will also be studied.

Table 5.5: Simulation parameters used to study the heat dissipation in Ga_2O_3 and SiC diodes sintered to AlN-DPC substrates as shown in Fig. 5.14. Adapted from [259].

Part	Material	Th. Conductivity (W/mK)	Thickness (µm)
Die	β–Ga_2O_3	20	50, 200, 600
	SiC	270	377
Die attach	sintered Ag	130	120
Underfill material	unspecified	0 – 100	40, 120
Substrate top/bottom	Cu	393	70
Substrate ceramic	AlN	170	300
Thermal interface material	grease	2	100
Heat sink with channels	Al	237	7000



(a) **(b)**

Figure 5.14: Model of Ga_2O_3 and SiC diodes mounted on AlN-DPC substrates based on the actual experimental setup used to simulate the heat dissipation in (a) cathode-side cooled (CSC) and (b) junction-side cooled (JSC) assemblies. In case of JSC assemblies, either the whole anode area is covered with die-attach material, or a $50\,\mu\mathrm{m}$ large gap is inserted between anode edge and die attach. The effect of underfill materials on the junction temperature is studied for both scenarios. Adapted from [259].

JSC and CSC assemblies: key differences in heat dissipation

The first step in evaluating the effectiveness of the various cooling methods and exploring potential ways to improve them is to understand the difference in heat dissipation between CSC and JSC setups. To this end, $200\,\mu\mathrm{m}$ thin Ga_2O_3 dice in CSC assembly, ideal JSC assembly, and JSC assembly with $50\,\mu\mathrm{m}$ wide gap between anode edge and die attach area are modeled, all at heating power of $30\,\mathrm{W}$. Figure 5.15 shows temperature distribution through a cross section in the center of the dice, as well as a view on the anode side of the die when hiding all other components. Parameters of interest are the average ($T_{\mathrm{j,ave}}$) and local maximum ($T_{\mathrm{j,max}}$) temperature of the junction area.

In the case of sample C200, the heat is created near the top surface and can be dissipated symmetrically over the whole area of the die, but it has to flow through the entire substrate with low thermal conductivity. Therefore, $T_{\mathrm{j,max}}$ is located in the center at the top side of the anode surface, which causes a high temperature drop through the substrate, i.e., a high thermal resistance. Consequently, with $246\,^{\circ}\mathrm{C}$ it exhibits the highest $T_{\mathrm{j,ave}}$ and $28\,\mathrm{K}$ higher $T_{\mathrm{j,max}}$ of all samples.

For the ideal JSC assembly without gap, the entire active area is thermally coupled to the die attach. Therefore, $T_{\mathrm{j,max}}$ is again located in the center of the anode. Compared to sample C200, $T_{\mathrm{j,ave}}$ decreases by about $97\,\mathrm{K}$. With an only $9\,\mathrm{K}$ higher $T_{\mathrm{j,max}}$ also the temperature difference across the active area is reduced. The peak temperature shifts slightly away from the anode surface and into the volume of the chip, which translates to a certain remaining thermal resistance of the die. Note that the exact simulation conditions such as the definition of the heat source will influence the exact location of the peak temperature, but not change this trend. Furthermore, the reduced cooling area results in a primarily lateral temperature gradient through the entire die, in contrast to the rather vertical gradient in case of C200.

When a gap is introduced in JSC configuration, a part of the anode that acts as the heat source is not directly cooled. This results in the maximum temperature shifting away from the center of the anode area towards its edge. Consequently, $T_{\mathrm{j,ave}}$ increases by $16\,\mathrm{K}$. With a plus of $35\,\mathrm{K}$, the increase in $T_{\mathrm{j,max}}$ is even more pronounced. The temperature difference across anode is now similar to C200, but $T_{\mathrm{j,max}}$ is still $81\,\mathrm{K}$ lower than in case of sample C200.

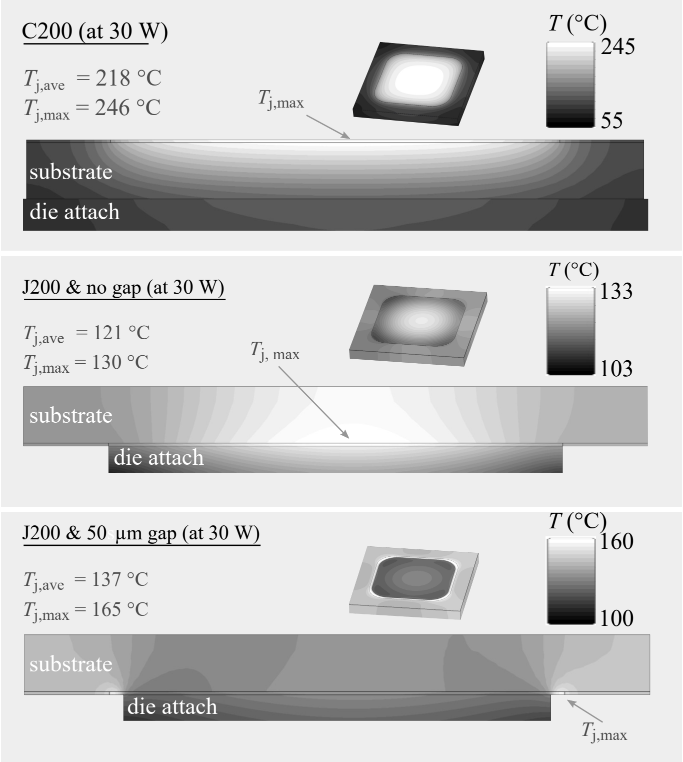


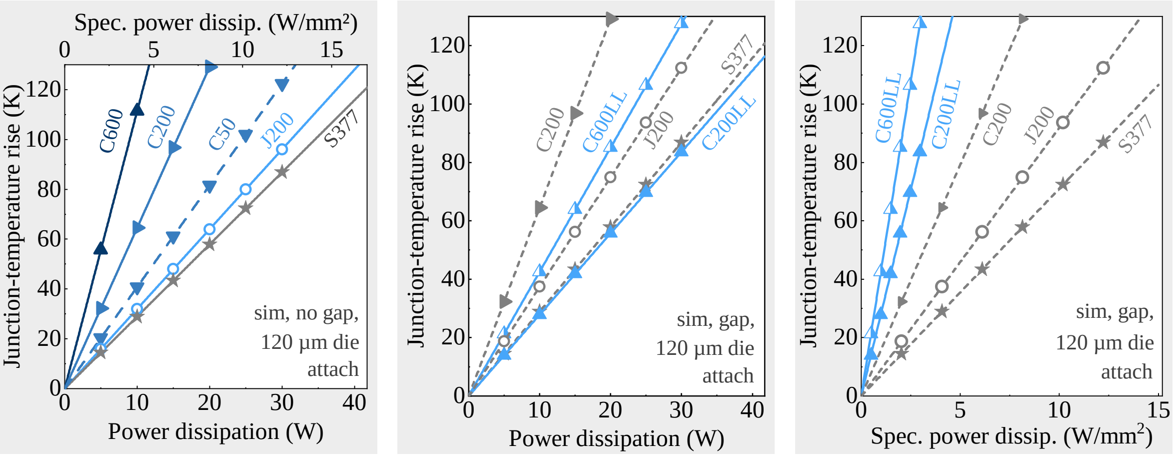
Figure 5.15: Simulated cross-sectional surface temperature (view on the anode when hiding all other parts) of the $200\,\mu\mathrm{m}$ thin Ga_2O_3 diode at a heating power of $30\,\mathrm{W}$. Assembling the die in CSC configuration (C200) leads to the highest average ($T_{\text{j,max}}$) and maximum ($T_{\text{j,ave}}$) junction temperature. In JSC assembly, the heat dissipation is enhanced by shifting $T_{\text{j,max}}$ closer to the die attach, although it moves slightly towards the volume of the chip. A gap in JSC assembly shifts the $T_{\text{j,max}}$ to the edge of the anode and increases $T_{\text{j,ave}}$ and $T_{\text{j,max}}$ significantly. Adapted from [259].

In summary, junction-side cooling shifts the main heat source and $T_{\text{j,max}}$ closer to the die attach layer through which the heat is dissipated, which reduces the thermal resistance of the die significantly and makes JSC highly effective for Ga_2O_3. The fact that even small gaps in JSC setups lead to an enhanced temperature gradient across the die and a significant rise in $T_{\text{j,max}}$ but a less severe increase in $T_{\text{j,ave}}$ has consequences also for the measurement procedures: Using the forward voltage as a sensor yields the junction temperature averaged over the entire active area [198]. Therefore, the high local peak temperatures may not be detected, posing a potential risk to the chip. For this reason, average junction temperatures of about $140\,°\mathrm{C}$ as determined with the $\sqrt{t}$-method were not exceeded in the measurements presented here.

Simulated power rating

With the improved understanding of the heat dissipation, the simulation is repeated for different heating powers, and the average junction temperature $T_{\text{j,ave}}$ is determined. As shown in Fig. 5.16a, the $R_{\text{th,ja}}$ is again calculated from a linear fit to the data and summarized in Tab. 5.6 for each setup.

Bearing in mind that some deviations even between the experimental setups are expected (such as variations in thickness and thermal conductivity of dice, the sintered silver layer, or the thickness of the thermal grease), the simulated rise in average junction temperature $\Delta T_{\text{j,ave}}$ and the $R_{\text{th,ja}}$ are in agreement with the measurements in Fig. 5.11 in case of the cathode-side cooled samples C600 and C200. This verifies the experimental and simulative procedures.



(a) **(b)** **(c)**

Figure 5.16: The simulated rise in average junction temperature when different heating powers are applied agrees with the experimental results. (a) The 200 µm thin ML-size JSC diode (J200) still shows a higher thermal resistance than its CSC SiC counterpart (S377), but a further decrease in T_j can be achieved by optimizing the die-attach thickness. Even a hypothetical 50 µm thin CSC diode (C50) cannot achieve the JSC limit. (b) Increasing the lateral dimensions of the die to LL-size reduces T_j significantly for a 600 µm thick diode (C600LL). When the substrate is additionally thinned to 200 µm (C200LL), T_j is similar to the SiC diode S377. (b) However, increasing the chip size reduces the maximum possible power density. Parts adapted from [259].

In the case of sample J200, the simulated $\Delta T_{j,ave}$ is significantly lower than the measured one, with about 86 K compared to 112 K in Fig. 5.11, both at a heating power of 27 W. This difference is mainly caused by the impact of the gap between die attach and anode edge, as examined in Fig. 5.15.

In case of the CSC assembled SiC reference sample S377, the simulated $\Delta T_{j,ave}$ is also lower than the measured one (about 68 K and 83 K, respectively, both at a heating power of 23.4 W). A major reason is that the anode sizes of the SiC and Ga_2O_3 dice are similar, but the lateral size of the modeled SiC die is larger than that of the actual one (see Tab. 5.3). As shown in Fig. 5.17a, this enables an effective heat spreading as a result of the high thermal conductivity of SiC and reduces the average and maximum junction temperature. Besides, variations in the die thickness of ±10 % according to the datasheet [235] can affect its thermal resistance.

When the SiC die is cooled ideally from the junction side (see also Fig. 5.17a), the temperature difference across the active area is reduced from 18.5 K to 7.5 K, similar to the setup with Ga_2O_3. However, $T_{j,ave}$ increases by about 7.5 K. In this setup, the effective heat spreading

Table 5.6: Simulation results for various Ga_2O_3 samples: The thermal resistances and drop of the conduction losses below the SiC level required to achieve the same T_j as an identical SiC counterpart according to Eq. 5.3 agree with the experimental results. Adapted from [259].

Sample name	Sim. $R_{th,ja}$ (K/W)	Sim. spec. $R_{th,ja}$ (mm^{2}K/W)	Sim. needed ratio γ_T	Sim. needed drop of P_{cond} below SiC level
C600	11.14	27.35	0.26	74 %
C200	6.46	15.85	0.45	55 %
C50	3.20	7.86	0.71	29 %
J200	2.90	7.11	0.91	9 %

in SiC and the associated large cooling area seem to outweigh the advantage of a shortened thermal path when cooling directly from the junction side.

This is a decisive difference to Ga_2O_3, where both the experimental and simulated data confirm that due to the low thermal conductivity of Ga_2O_3, JSC assemblies can yield lower junction temperatures despite the smaller cooling area — if a sufficiently large portion of the anode area is thermally coupled with the die-attach material. This is further illustrated by simulating the heat dissipation in a hypothetical $50\,\mu m$ thin CSC die. As shown in Fig. 5.16a, even this device exhibits a higher $T_{\mathrm{j,ave}}$ than its $200\,\mu m$ thick JSC counterpart (both without and with $50\,\mu m$ gap). This shows that different packaging methods for Ga_2O_3 and SiC devices will be required in order to achieve the maximum possible device performance.

The γ_{T} factors, i.e., the necessary reduction in P_{cond} below the SiC level to achieve the same T_{j} at the same forward current, can be calculated from the simulated $R_{\mathrm{th,ja}}$ by using Eq. 5.3. The results are summarized in Tab. 5.6. Due to the previously discussed influences, minor differences between the simulated and the experimentally determined γ_{T} factors are present, but they show the same trend. While even for the $50\,\mu m$ thin CSC die the conduction losses would have to drop to $29\,\%$ below the SiC level, a difference of only $9\,\%$ is necessary for the $200\,\mu m$ thick JSC device.

Figures 5.16b and 5.16c show the influence of increasing die size on the junction temperature. The simulations confirm the experimentally observed decrease in junction temperature for the $600\,\mu m$ thick LL-size diode close to that of the JSC ML-size sample J200, although at the cost of a significantly reduced specific power handling capability. If the LL-size sample is additionally thinned to $200\,\mu m$, the junction temperatures are similar to the CSC SiC sample S377. For the reasons already mentioned, the effect of increasing chip size is not examined in more detail. Nevertheless, the considerations are helpful in interpreting the results of the buck converter tests in Chapter 6.

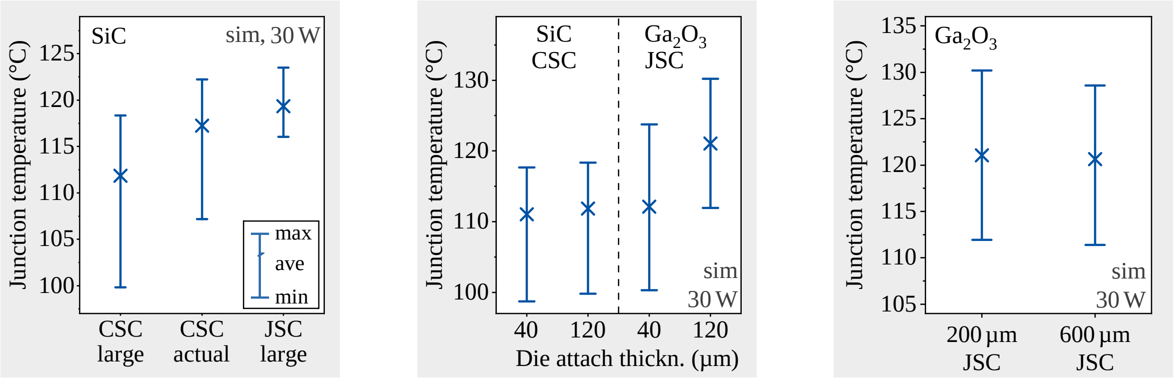
Influence of die attach and substrate thickness in JSC

At the first glace, the simulative and experimental results suggest that even with JSC assemblies, Ga_2O_3 devices can still not achieve junction temperatures as low as those of CSC assembled SiC counterparts. However, as shown in Fig. 5.17b, the thickness of the die attach layer affects the results.

In case of the Ga_2O_3 sample J200, a decrease of the die-attach thickness from the experimental value of $120\,\mu m$ to a hypothetical value of $40\,\mu m$ decreases $T_{\mathrm{j,ave}}$ by about $9\,\mathrm{K}$. In case of the CSC diode S377, however, an identical decrease in die-attach thickness does not affect the junction temperature substantially. Thus, by optimizing the thickness of the sintered silver layer, the Ga_2O_3 sample can achieve the approximately same $T_{\mathrm{j,ave}}$, yet while still exhibiting an about $6\,\mathrm{K}$ higher local $T_{\mathrm{j,max}}$ than the SiC reference.

In Fig. 5.17c, the influence of the thickness of the die on the thermal resistance in JSC configuration is studied. Increasing the thickness from $200\,\mu m$ to $600\,\mu m$ does not affect the junction temperature significantly. From a purely thermal point of view, time-consuming substrate thinning processes do therefore not seem necessary if a JSC assembly is chosen. However, considering the electrical properties, substrate thinning is still recommended to lower the on-resistance and reduce the conduction losses and associated heating power. This aspect will be studied in more detail in Section 5.3.5.

So far, it has been found that optimizing the die-attach thickness in JSC assemblies can reduce the junction temperature, but also that gaps between anode edge and die attach increase the



(a) **(b)** **(c)**

Figure 5.17: Simulated junction temperature T_j of different samples at a heating power of 30 W. (a) When the lateral dimensions of SiC diode model are reduced to the actual chip size, the limited heat spreading results in an increase in T_j. Cooling the die from the junction side leads to a further increase in T_j for the same reason. This contrasts with the heat dissipation in Ga_2O_3 dies. (b) The average T_j of JSC assembled Ga_2O_3 dice can be reduced to the CSC SiC level by decreasing the thickness of the sintered silver layer. (c) When JSC assembled, the thickness of the Ga_2O_3 substrate has a negligible effect on T_j. Adapted from [259].

peak temperature and shift it towards the edge of the anode that is not covered with die-attach material. Hereinafter, it is therefore studied if underfill materials can alleviate this issue.

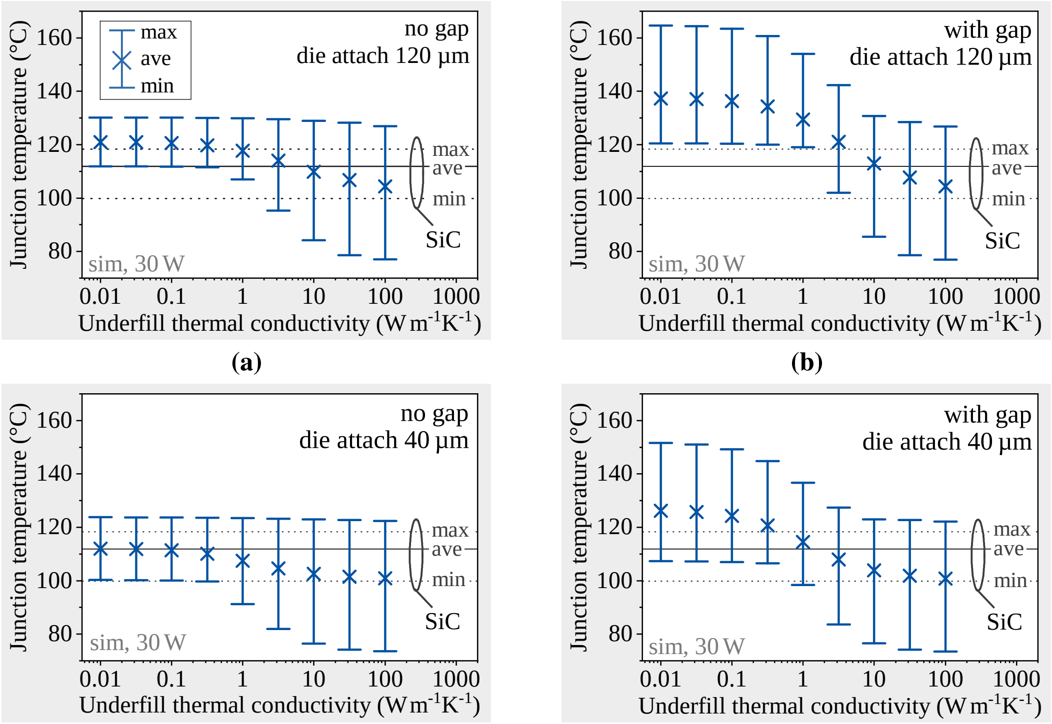
Improving JSC with underfill materials

The effect of underfill materials on the junction temperatures is examined by inserting a part with a thickness identical to that of the die attach layer and filling the entire volume between the ceramic substrate and the surface of the die, as shown in Fig. 5.14b. The thermal conductivity of the underfill material is increased from $0.01\,\mathrm{W\,m^{-1}\,K^{-1}}$ to $100\,\mathrm{W\,m^{-1}\,K^{-1}}$ and a heating power of 30 W is applied. The analysis is performed for four different JSC setups: without and with gap as well as with $120\,\mathrm{\mu m}$ thick and $40\,\mathrm{\mu m}$ thin underfill. The results are shown in Fig. 5.18.

In the scenario with $120\,\mathrm{\mu m}$ thick underfill and ideal JSC assembly (Fig. 5.18a), no effect on T_j is observed for thermal conductivities below $1\,\mathrm{W\,m^{-1}\,K^{-1}}$. To increase $T_\mathrm{j,ave}$ below the SiC level, a minimum thermal conductivity of $5\,\mathrm{W\,m^{-1}\,K^{-1}}$ is required. The change in $T_\mathrm{j,ave}$ is caused by a decrease of the minimum junction temperature $T_\mathrm{j,min}$ while $T_\mathrm{j,max}$ remains almost the same. The reason is that $T_\mathrm{j,max}$ is located in the center of the anode area (see Fig. 5.15) far away from the underfill, which limits its influence.

When the gap is introduced (Fig. 5.18b), both $T_\mathrm{j,ave}$ and $T_\mathrm{j,max}$ increase significantly. An increase in the thermal conductivity of the underfill now reduces both $T_\mathrm{j,max}$ and $T_\mathrm{j,min}$. This is because $T_\mathrm{j,max}$ now occurs at the anode edge (see Fig. 5.15) and thus the underfill has a direct effect on it. However, a thermal conductivity of the underfill of $10\,\mathrm{W\,m^{-1}\,K^{-1}}$ is required to decrease $T_\mathrm{j,ave}$ down to the SiC level. Note that underfill materials usually achieve a thermal conductivity below $3\,\mathrm{W\,m^{-1}\,K^{-1}}$. Intensive research into suitable underfills is therefore critical in this scenario. Yet, even a material with a thermal conductivity $3\,\mathrm{W\,m^{-1}\,K^{-1}}$ can reduce $T_\mathrm{j,ave}$ by 16 K and $T_\mathrm{j,max}$ even more significantly by 22 K.

Next, the thickness of the die-attach material and underfill is reduced to $40\,\mathrm{\mu m}$ (Fig. 5.18d). This enhances the influence of the underfill material. A thermal conductivity of about



(a) (b) (c) (d)

Figure 5.18: The junction temperature T_j of JSC assembled Ga_2O_3 diodes can be decreased with underfill materials. The minimum thermal conductivity of the underfill material required to reach the same $T_\mathrm{j,ave}$ as the SiC counterpart depends on the die-attach thickness, as shown exemplarily in (a) and (b) for the $120\,\mu\mathrm{m}$ die attach layer without and with gap between anode edge and die attach. In (c) and (d) the impact of the underfill material is further increased by reducing the die-attach thickness to $40\,\mu\mathrm{m}$, both without and with gap. Adapted from [259].

$1.6\,\mathrm{W\,m^{-1}\,K^{-1}}$ is now sufficient to reduce $T_\mathrm{j,ave}$ to the SiC level, demonstrating that also standard underfills can be advantageous in JSC assemblies with Ga_2O_3.

When the gap is removed (ideal JSC assembly, Fig. 5.18c), the $T_\mathrm{j,ave}$ is already on SiC level even without underfill. Similar to the case in Fig. 5.18a only $T_\mathrm{j,min}$ decreases with increasing thermal conductivity of the underfill, while the $T_\mathrm{j,max}$ remains unchanged for the above-discussed reasons. With a thermal conductivity of only $0.3\,\mathrm{W\,m^{-1}\,K^{-1}}$, $T_\mathrm{j,ave}$ can be reduced to below the SiC level. In summary, thinner die attach layers not only increase the direct heat dissipation through it, but also make underfill materials more effective. They are thus recommended especially if gaps between anode edge and die attach area cannot be avoided when assembling the dice.

5.3.5 How conduction losses can affect the assembly strategy

Apart from the pure thermal resistance, the junction temperature and safe operating range of a power semiconductor device are also determined by its actual power loss at the respective operating point. If the power loss of the device is low enough, a higher thermal resistance can be accepted. To further discuss this aspect for Ga_2O_3 diodes, an application where conduction losses are dominant is assumed, and a simplified calculative approach that will be justified in the following is pursued.

Table 5.7: Material parameters used to calculate the theoretical on-resistance of Ga_2O_3 diodes in a realistic-optimistic, a moderate, and a pessimistic scenario by using Eq. 5.5. A breakdown voltage of 1200 V is assumed. Adapted from [259].

		optimistic	**moderate**	**pessimistic**
Substrate	$\mu_{\text{e,sub}}$ (cm^2/Vs)	60	30	30
	$N_{\text{D,sub}}$ (cm^{-3})	1×10^{19}	1×10^{19}	1×10^{19}
	⇒ Resistivity (mΩcm)	10.4	20.8	20.8
Epitaxial layer	$\mu_{\text{e,epi}}$ (cm^2/Vs)	200	100	100
	E_{br} (MV/cm)	8	5	4
	⇒ Specific resistance (mΩcm^2)	0.06	0.52	1.02

According to Eq. 5.2, the forward conduction losses P_{cond}, and with that also the rise in junction temperature ΔT_{j} are determined by the knee voltage V_0 and the differential on-resistance r_{o}. In this equation, the contributions of auxiliary parts such as the bond wires but also the Schottky and ohmic contact to the on-resistance are neglected as they accout for less than $1\,\%$, i.e., substrate and drift layer strongly dominate the resistance (see also Section 4.2), and as they do not primarily result from the pure semiconductor material. To facilitate the comparison of different semiconductor technologies regarding their performance limits, it is furthermore common to consider only the differential on-resistance. Before adopting this method, a brief discussion will be given on whether this simplification is reasonable here and what impact it may have on the results. To this end, the conduction losses P_{cond} in Eq. 5.2 are expressed with Eq. 4.7 as

$$P_{\text{cond}} = V_0(T_{\text{j}}) \cdot I_{\text{f}} + \left[r_{\text{o}}(T_{\text{ref}}) \cdot \left(\frac{T_{\text{j}}}{T_{\text{ref}}} \right)^{\alpha_{\text{ref}}} \right] \cdot I_{\text{f}}^2, \tag{5.4}$$

where α_{ref} describes the increase in differential on-resistance r_{o} with rising junction temperature T_{j} related to a reference temperature T_{ref}. The first simplification is to neglect the term $V_0 I_{\text{f}}$ in Eq. 5.4. This is reasonable for the following reasons: First, the profiles in Fig. 5.12b and the indications in Tab. 5.4 (bearing in mind their uncertainties) show that the knee voltage is similar for all SiC and Ga_2O_3 diodes under investigation. Second, the term $V_0 I_{\text{f}}$ increases linearly with I_{f} and V_0 decreases with rising junction temperature, whereas the second summand is proportional to I_{f}^2 and increases with rising junction temperature. Thus, the second summand dominates the conduction losses for sufficiently high forward currents. Third, as summarized in Sections 2.3.3 and 2.3.4, V_0 is largely determined by the Schottky metal, the quality and type of junction (e.g., pure MS- versus hetero-junction), and the substrate orientation, and can vary almost by a factor of three. This influence is neglected by omitting the term $V_0 I_{\text{f}}$. The second simplification is to assume that the rise in on-resistance with rising junction temperature is identical for Ga_2O_3 and SiC, i.e., $\alpha_{\text{GaO}} = \alpha_{\text{SiC}}$. As shown in Section 4.2.4, however, α_{GaO} is significantly lower than α_{SiC}, which means that this assumption is rather pessimistic for Ga_2O_3.

With these simplifications, the quotient $P_{\text{cond,GaO}}/P_{\text{cond,SiC}}$ in Eq. 5.3 can be replaced with $r_{\text{o,sp,GaO}}/r_{\text{o,sp,SiC}}$. The remaining theoretical specific differential on-resistance $r_{\text{o,sp}}$ can be calculated from the sum of the resistance of the substrate and the epitaxial layer by combining Eqs. 2.3 and 2.5, which gives

$$r_{\text{o,sp}} = r_{\text{sub,sp}} + r_{\text{epi,sp}} = \frac{z_{\text{sub}}}{e \mu_{\text{e,sub}} N_{\text{D,sub}}} + \frac{4 V_{\text{br}}^2}{\epsilon_0 \epsilon_{\text{s}} \mu_{\text{e,epi}} E_{\text{br}}^3}, \tag{5.5}$$

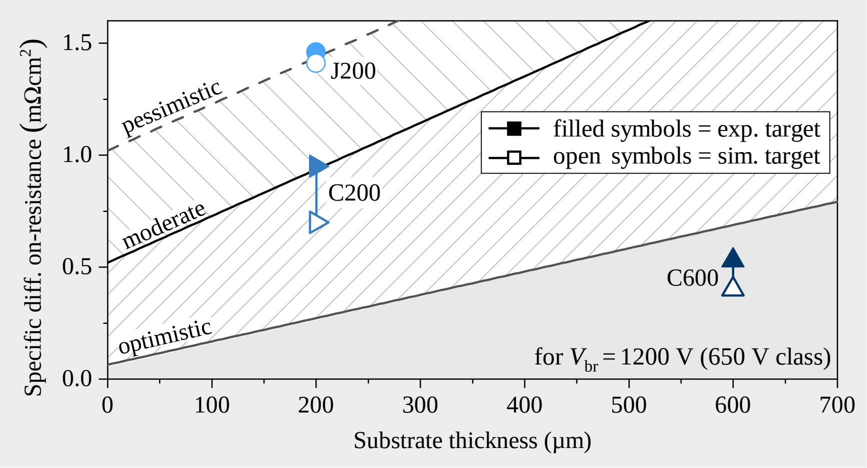


Figure 5.19: Specific differential on-resistance $r_{o,sp}$ versus substrate thickness for a Ga_2O_3 Schottky diode in the optimistic, moderate, and pessimistic scenarios defined in Tab. 5.7. The symbols indicate the previously experimentally and simulatively determined target $r_{o,sp}$ required to reach a rise in junction temperature identical to that of the SiC reference diode at the same forward current. With a 600 µm thick CSC diode, the required $r_{o,sp}$ cannot be achieved even in the optimistic case. With a 200 µm thin JSC diode, however, it can be achieved even in the pessimistic case. Adapted from [259].

with z_{sub}, $\mu_{e,sub}$, and $N_{D,sub}$ the thickness, electron mobility and effective donor concentration of the substrate, $\mu_{e,epi}$ the electron mobility of the drift layer, ϵ_0 and ϵ_s the vacuum permittivity and relative dielectric constant, and V_{br} and E_{br} the breakdown voltage and field. The corresponding specific differential on-resistance is calculated for Ga_2O_3 diodes assuming a V_{br} of $1200\,V$ for a $650\,V$ rated diode based on the measurements with batch B3 samples in Fig. 4.5. Electron mobilities and breakdown fields for β–Ga_2O_3 are taken from the experimentally achieved and theoretically derived ones summarized in [216] and [18].

Based on this, three scenarios summarized in Tab. 5.7 with their corresponding $r_{o,sp}(z_{sub})$ shown in Fig. 5.19 are considered: The optimistic but still realistic scenario exhibits the highest electron mobilities and the maximum theoretical breakdown field, leading to the lowest substrate resistivity and specific resistance of the drift layer. In the moderate scenario, the electron mobilities and the breakdown field are reduced to values that have been achieved and even exceeded in different experiments with small-area diodes already [18, 216]. The pessimistic scenario differs from the moderate one only in the fact that the breakdown field is reduced by $1\,MV/cm$, i.e., to half of the theoretical value. In addition to these theoretical on-resistance limits, Fig. 5.19 also shows the maximum allowed on-resistance for the investigated Ga_2O_3 diodes, which leads to the same rise in junction temperature as for the SiC reference sample S377 at the same forward current. Following the above-discussed simplifications, it is approximated by

$$r_{o,sp,GaO} \overset{!}{=} r_{o,sp,SiC} \cdot \gamma_T\,, \tag{5.6}$$

where both the simulated (Tab. 5.6) and experimentally determined (Tab. 5.4) ratios γ_T are considered. Based on curve tracer measurements at $25\,°C$, an $r_{o,sp,SiC}$ of $1.55\,m\Omega\,cm^2$ is used for the calculation.

Figure 5.19 shows that in case of the CSC and $600\,\mu m$ thick sample C600, the required $r_{o,sp}$ cannot be achieved even in the optimistic scenario. It can be achieved in the optimistic case, however, when the CSC substrate is thinned to $200\,\mu\mathrm{m}$ (sample C200). In the moderate scenario, sample C200 can achieve the required $r_{\text{o,sp}}$ according to the measurements, but not according to the simulation data. When the $200\,\mu\mathrm{m}$ thin substrate is cooled from the junction-side without gap (sample J200), the required $r_{\text{o,sp}}$ can be achieved in the optimistic as well as the moderate scenario, and by a very narrow margin also in the pessimistic one. Note that Fig. 5.17c suggests that substrate thickness does not affect the junction temperature significantly in JSC assemblies, provided that the same power is dissipated. However, Fig. 5.19 demonstrates that thinning JSC samples to at least $400\,\mu\mathrm{m}$ is recommended to ensure a sufficiently low $r_{\text{o,sp}}$ in the moderate scenario, and further thinning to at least $200\,\mu\mathrm{m}$ is recommended in the pessimistic scenario.

The fact that the only difference between the moderate and pessimistic scenario is a difference of $1\,\mathrm{MV/cm}$ in E_{br} illustrates that it is crucial to fully exploit this parameter in Ga_2O_3 devices, especially with respect to the medium electron mobility. Therefore, field management methods such as edge terminations or trench junctions and, with regard to potential commercial devices, the safety margin between rated reverse voltage and actual breakdown voltage will affect the mounting method. Here, a fairly large, i.e., rather pessimistic safety margin was chosen.

As summarized in Section 2.3.4 first small-area β–Ga_2O_3 diodes recently achieved record $V_{\text{br}}^2/r_{\text{o,sp}}$ figures of merit of $6.4\,\mathrm{kV}/3.4\,\mathrm{m\Omega\,cm^2}$ for a diode with deep SiO_2 trenches [22], and $8.3\,\mathrm{kV}/5.2\,\mathrm{m\Omega\,cm^2}$ for a n-Ga_2O_3/p-NiO heterojunction diode [23]. Both on-resistances fall below the 1D unipolar on-resistance limit of SiC and translate to a ratio γ_{T} of about 0.3. Note that these results were achieved with test structures with lateral dimensions in the range of some hundreds of µm and thus still need to be demonstrated for chips scaled up to sizes of some mm^2.

Nevertheless, when comparing these results to the γ_{T} values in Tabs. 5.4 and 5.6 it thus seems realistic that the on-resistances required to achieve a rise in junction temperature similar to that of commercial SiC diodes may be achieved also for large-area devices that are more relevant for power electronics applications, such as $650\,\mathrm{V}$ or $1200\,\mathrm{V}$ class Ga_2O_3 diodes. Therefore, from a purely technological point of view (i.e., not considering development effort and cost), it may be preferred to pursue JSC assemblies in the early Ga_2O_3 development phase, while for future generation diodes with thinned substrate and improved on-resistance simple CSC assemblies may be sufficient depending on the application — especially considering that Ga_2O_3 devices could potentially be operated at much higher temperatures than their SiC or GaN counterparts (see Section 4.2.4).

5.4 Chapter conclusion

Chapter 5 deals with the thermal properties of Ga_2O_3 diodes. The main results can be summarized as follows:

1. Large-area (001) oriented β–Ga_2O_3 Schottky diodes with $200\,\mu\mathrm{m}$ thin native substrates have been introduced for the first time and shown to reduce the junction temperature significantly compared to previous standard Ga_2O_3 diodes.

2. Not only the electrical properties but also the thermal properties have been found to vary between TO247 packaged devices of the same type. Combined X-ray analysis and parametric studies suggest that this may partly be due to a variation in the material properties of the Ga_2O_3 wafer.

3. To analyze strategies to reduce the junction temperature, a direct experimental and simulative comparison of the heat dissipation in Ga_2O_3 and SiC bare dice assembled in different ways is performed:
    a) The heat dissipation in Ga_2O_3 differs significantly from that in SiC. For Ga_2O_3, junction-side cooling is found to be more effective than substrate thinning.
    b) Even small gaps between die attach layer and edge of the anode in junction-side cooled assemblies increase the peak and average junction temperature significantly. Underfill materials can alleviate this issue effectively.
    c) Increasing the die size reduces the junction temperature, but also limits the maximum possible power density.
    d) The potentially low on-resistances of Ga_2O_3 devices can enable a rise in junction temperature similar to that of SiC counterparts despite the low thermal conductivity, if a suitable assembly method is chosen.

The insight gained into the heat dissipation, including recommendations for different mounting techniques, is essential to design first power converters with Ga_2O_3 devices such as in the following Chapter 6.

Chapter 6

Application of gallium oxide power diodes in a buck converter

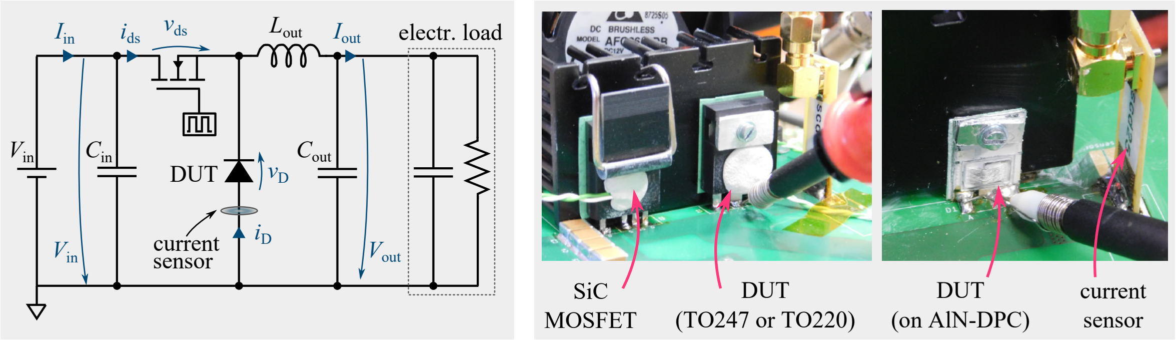
6.1 Chapter overview

The previous investigations of the basic current–voltage profiles and thermal properties of Ga_2O_3 diodes in Chapters 4 and 5 as well as novel current sensors in Section 3.4 lay the groundwork to examine the newest Ga_2O_3 Schottky diodes regarding their switching properties in an application-oriented manner. As such, this chapter addresses the lack of studies on the switching application of Ga_2O_3 diodes in the literature, which is pointed out in Section 2.3.4. This is particularly interesting because several diodes already exhibited atypical forward and reverse current-voltage profiles or signs of electron trapping (see Chapters 4 and 5). Novel large-area Ga_2O_3 power diodes and a low-inductive PCB layout enable voltage and current slew rates significantly exceeding those in first reports and allow new insights into the current development status, including the first-ever demonstration of Ga_2O_3 diodes in a $400\,\mathrm{V}$ buck converter.

Section 6.2 first introduces the experimental setup in more detail. Section 6.3 studies TO247 packaged $600\,\mu\mathrm{m}$ thick batch B3 diodes of sizes ML, L, and LL. First, the static electric properties that are relevant for buck converter application are briefly discussed. Based on this, the switching properties are examined by means of double pulse tests under varying conditions. This enables the final interpretation of efficiency measurements during buck converter application. Section 6.4 studies new $200\,\mu\mathrm{m}$ thin batch B4 diodes of sizes ML and LL assembled on ceramic substrates but mounted on the same buck converter PCB. Relevant static and dynamic electric properties are first briefly discussed. Then, efficiency and temperature measurements during buck converter operation are analyzed and also compared to the previous results in Chapter 5. Section 6.5 summarizes the main results. Parts of this chapter have been published in [260] by the author during the course of this thesis.

6.2 Experimental setup and investigated samples

A buck converter topology, the basics of which are explained in Section 2.2.1, is chosen to study the switching behavior of Ga_2O_3 diodes. Figure 6.1a shows the detailed measurement circuit schematics and Fig. 6.1b shows a photograph of the corresponding setup. Since the diode is placed on the side of low potential, non-isolated high-bandwidth probes can be used to capture the waveforms. Here, a $400\,\mathrm{MHz}$ passive probe (PMK PHV1000) is used to measure the diode voltage. The IPM sensor is used to resolve single fast switching transients with high precision and the M-shunt is used to capture the diode current during buck converter



(a) **(b)**

Figure 6.1: Experimental setup used for double pulse tests and buck converter operation: (a) Circuit schematics and (b) photograph with TO-packaged devices (left) and diode mounted on an AlN-DPC substrate (right). During buck converter operation, the M-shunt is used to measure the diode current. For double pulse tests, the inductive load is connected in parallel to the diode, C_{out} and the electronic load are removed, and the IPM sensor is used to capture single switching transients. Adapted from [260].

operation as it offers enhanced heat dissipation, DC capability and lower insertion inductance than coaxial shunt, as thoroughly investigated in Section 3.4. The drain–source voltage of the high-side transistor is measured with a $120\,\mathrm{MHz}$ differential probe (LeCroy HVD3106A) and the drain current is measured with a $30\,\mathrm{MHz}$ Rogowski probe (CWTUM 015/B from PEM). Note that the low bandwidth of the Rogowski probe leads to underestimated current slopes and a distorted representation of the oscillations as discussed in Section 3.4.

The circuit is PCB-based with $70\,\mathrm{\mu m}$ thick copper tracks forming a vertical commutation loop. A $650\,\mathrm{V}/107\,\mathrm{m\Omega}$ TO274-4 packaged SiC MOSFET (Infineon IMZA65R107-M1HXKSA1 with an output charge of about $53\,\mathrm{nC}$ at $400\,\mathrm{V}$) is used as active switch. The additional Kelvin source pin decreases switching losses and ringing by reducing the coupling between the gate and power loop [224]. By using an isolated Skylabs SI8271 gate driver and varying external gate resistors, the transistor is switched between gate–source voltages of $0\,\mathrm{V}$ (off-state) and $18\,\mathrm{V}$ (on-state).

For buck converter operation, the diode and transistor are mounted on the same heat sink (Ohmite PV-T22-38E) with an identical electrically insulating thermally conductive pad, and cooled with air using a fan (Delta Electronics AFC0612DB). Note that a certain mutual thermal influence is possible due to the common heat sink. An electronic load (EA ELR 9750-66) controls the output current while the output LC filter is formed by a $580\,\mathrm{\mu H}$ air coil and a $7.5\,\mathrm{\mu F}$ foil capacitor. However, the input capacitance of the electronic load ($>100\,\mathrm{\mu F}$) dominates the capacitive part of the output LC filter. To avoid associated high inrush currents, the start-up is performed by steadily increasing the DC link voltage from $0\,\mathrm{V}$ to its final value, thus charging the output capacitance in a controlled manner. The use of an air coil circumvents saturation effects and keeps the thermal mass low, thus reducing the time to reach a steady state during efficiency measurements with a Zimmer LMG500 power analyzer.

During double pulse tests, a single heating resistor is attached to the diode lead frame instead of using the common heat sink. This allows to heat only the diode without affecting the MOSFET temperature. Furthermore, a $111\,\mathrm{\mu H}$ coil is connected in parallel to the diode instead of the output LC filter and electronic load. As explained in Section 3.4.6, the point of interest is the second turn-on of the MOSFET when the freewheeling current flowing through the diode is abruptly disrupted and the diode turns off.

Note that the buck converter is not designed to achieve maximum efficiency, but to effectively study how the various diodes affect the buck converter switching waveforms and performance. This is achieved by keeping the same MOSFET but swapping the diodes. Diodes under investigation here are the $600\,\mu m$ thick TO247 packaged Ga_2O_3 batch B3 samples with field plates and N-ion implanted guard rings of size ML, L, and LL. The TO247-3 packaged SiC-B and state-of-the-art TO220-3 packaged Si-A diode [238] are used as a benchmark as they exhibit similar lateral dimensions. Furthermore, novel $200\,\mu m$ thin batch B4 Ga_2O_3 diodes of size ML and LL mounted on AlN-DPC substrates are investigated. The SiC-A diode, which is assembled in the same way and exhibits lateral dimensions similar to the ML type diode, is used as a benchmark for these measurements.

The TO packages cause a rather high stray inductance, which causes ringing and slows down the commutation speed. However, they are still widely used due to their low cost and easy handling, making the results application-relevant. Furthermore, the stray inductance is similar for all samples. Therefore, as will be evident later, differences in waveforms and efficiencies can be clearly attributed to the semiconductor despite the influence of the package.

6.3 Investigating 600 µm thick TO247 packaged diodes with different chip sizes

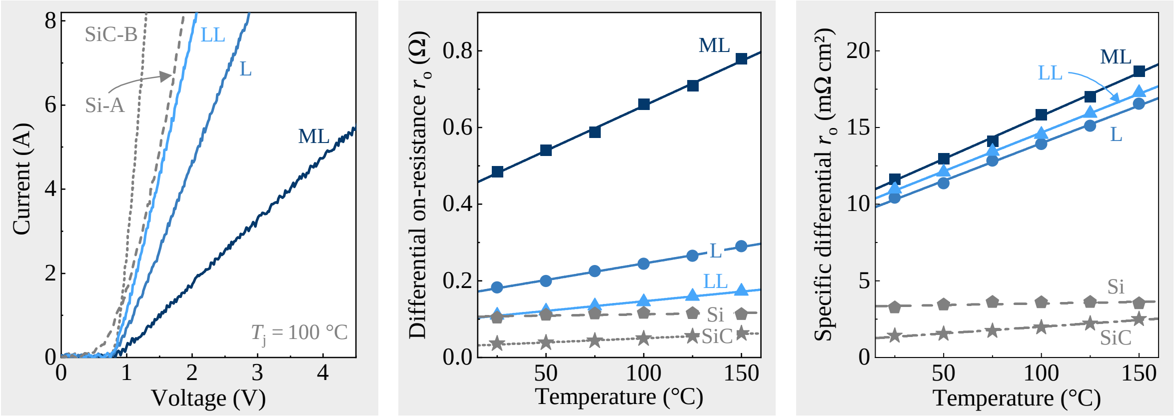
6.3.1 Static electrical properties relevant for switching operation

Differential on-resistances

The conduction losses caused by the on-resistances dominate the efficiency especially at low switching frequencies and high output currents [225, 226]. The forward characteristics of the three $600\,\mu m$ thick Ga_2O_3 diodes and the SiC-B and Si-A reference diodes selected for buck converter operation are shown in Fig. 6.2a at a junction temperature of $100\,°C$. The SiC and Ga_2O_3 diodes have a similar knee voltage of about 0.8 to $0.9\,V$ but the knee voltage of the Si-A diode is only about $0.5\,V$. Furthermore, the Si-A diode exhibits a curved forward current–voltage profile as typical for bipolar diodes. The on-resistances of Ga_2O_3 sample B3-LL and reference sample Si-A are similar, which is important for the later comparison of the buck converter efficiencies. Fig. 6.2b.

In Figs. 6.2b and 6.2c the temperature-dependent absolute and specific differential on-resistances of the Ga_2O_3 diodes are directly compared to those of the SiC-B and Si-A reference diodes. The values for the Si-A diode with non-constant differential on-resistance are averaged from a fit between $5\,A$ and $8\,A$, which corresponds to the typical operating range in Section 6.3.3. Since the junction structure of all Ga_2O_3 diodes is identical, the on-resistance increases with decreasing active area in the order r_o(LL)$<r_o$(L)$<r_o$(ML), but their specific on-resistances are similar. The SiC-B reference diode reaches the lowest absolute and specific on-resistances. Although the Ga_2O_3 diodes L and LL have the largest active areas, the SiC-B diode is therefore expected to enable higher efficiencies under heavy load conditions.

The increase in on-resistance with rising temperature is discussed in more detail in Section 4.2.4. By using Eq. 4.7, α_{300} and α_{373} are 1.3 to 1.4 for all Ga_2O_3 diodes almost independent of the reference temperature, but 1.6 and 1.9 for the SiC-A diode, respectively. Thus, at high temperatures and under heavy load conditions, Ga_2O_3 is expected to continuously approach the efficiencies with the SiC-B sample – provided the rise in junction temperature of the Ga_2O_3 diode does not reach a level that would compensate the advantage in α_{300} and α_{373}.



(a) **(b)** **(c)**

Figure 6.2: (a) Forward current–voltage characteristics of the three 600 µm thick TO247 packaged Ga_2O_3 samples of sizes ML, L, and LL from batch B3 and the SiC-B and Si-A reference diodes at a junction temperature T_j of $100\,^\circ\mathrm{C}$. (b) The extracted temperature-dependent differential on-resistances increase with decreasing chip size in case of Ga_2O_3, while SiC-B exhibits the lowest values. (c) The specific (related to anode size) differential on-resistance is similar for all Ga_2O_3 diodes and significantly smaller in case of SiC-B. Parts adapted from [260].

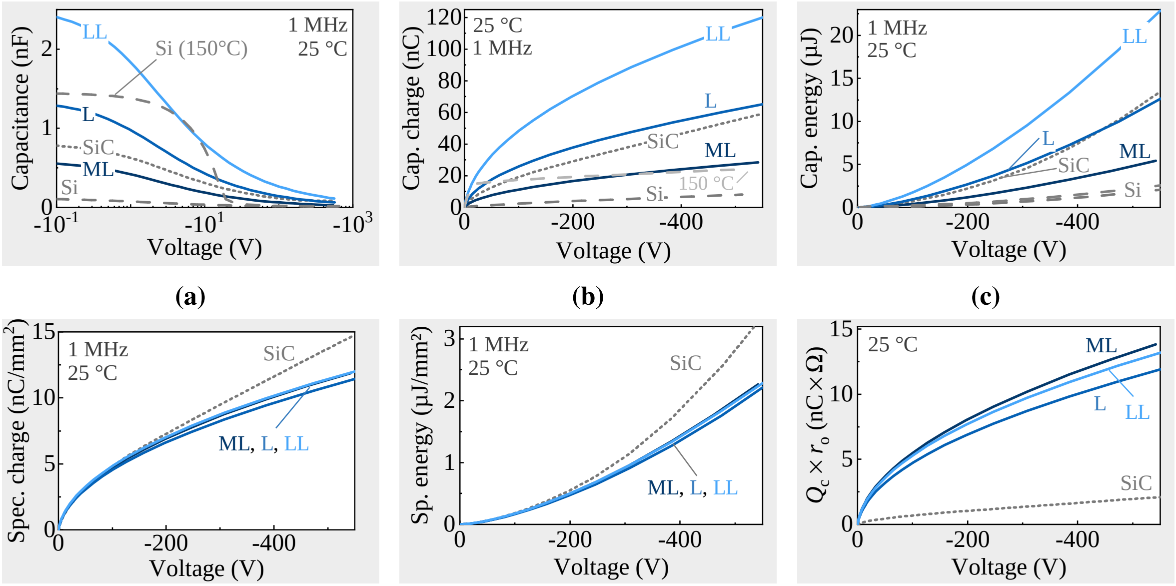
Capacitance, capacitive charge, and capacitance stored energy

The junction capacitances C_j shown in Fig. 6.3a for all diodes dominate the efficiency especially at high switching frequencies and low output currents [225, 226]. The capacitive charge Q_c and capacitance stored energy E_c are calculated from the C–V profiles using Eqs. 3.5 and 3.6, and shown in Figs. 6.3b and 6.3c, respectively. Since there is no significant change in junction capacitance with temperature for the unipolar samples (see also Section 4.2.2), only the room temperature profiles are shown for clarity.

The small bandgap and bipolar nature of the Si-A diode, however, cause a significant rise of the junction capacitance at zero bias voltage (C_j0) when the temperature is increased to $150\,^\circ\mathrm{C}$. Yet, C_j drops sharply at a voltage of about $-10\,\mathrm{V}$, resulting in a minuscule increase in the stored charge and a negligible change of the capacitance energy. Both C_j0 and Q_c decrease with decreasing anode area in the order $C_\mathrm{j0}(\mathrm{LL}) > C_\mathrm{j0}(\mathrm{L}) > C_\mathrm{j0}(\mathrm{SiC}) > C_\mathrm{j0}(\mathrm{ML})$. At room temperature, the bipolar Si diode exhibits the lowest C_j0 and Q_c.

For the Ga_2O_3 diodes, the capacitance energy also decreases with decreasing anode area in the order $E_\mathrm{c}(\mathrm{LL}) > E_\mathrm{c}(\mathrm{L}) > E_\mathrm{c}(\mathrm{ML})$. Although C_j0 is lower for SiC-A than for Ga_2O_3 sample L, both samples exhibit a similar E_c at $-400\,\mathrm{V}$, and the E_c of Ga_2O_3 sample L even drops below that of sample SiC-B as the reverse voltage increases. This results from differences in the doping profile of the epitaxial layer of the SiC-B and Ga_2O_3 diodes, causing the junction capacitance of sample L to fall beneath that of SiC-A at voltages below $-300\,\mathrm{V}$.

The specific (related to the anode area) capacitive charge and energy are shown in Figs. 6.3d and 6.3e, respectively. They are similar for all Ga_2O_3 diodes because of the identical junction design. Below about $-200\,\mathrm{V}$ the SiC-B diode exhibits a higher specific capacitive charge and energy than the Ga_2O_3 diodes. At the planned operating point of $-400\,\mathrm{V}$, the specific Q_c (specific E_c) is about $10\,\mathrm{nC/mm^2}$ ($1.4\,\mathrm{\mu J/mm^2}$) for the Ga_2O_3 diodes and about $11.6\,\mathrm{nC/mm^2}$ ($1.9\,\mathrm{\mu J/mm^2}$) for the SiC-B diode. Note that the given values are associated



(a) (b) (c)

(d) (e) (f)

Figure 6.3: For the Ga_2O_3 samples, the absolute (a) junction capacitance C_j (b) capacitive charge Q_c and (c) capacitance stored energy E_c are temperature-independent and increase with increasing chip size. Although Q_c of SiC-B is lower than the Q_c of diode L, the C_j of sample L drops below that of sample SiC-B below about $-300\,\mathrm{V}$, leading to similar E_c profiles. The specific (related to anode size) capacitive (d) charge and (e) energy of the Ga_2O_3 diodes are slightly lower than those of the SiC-B reference at voltages below $-200\,\mathrm{V}$. (f) However, the high on-resistance leads to a substantially higher charge × resistance figure of merit. Adapted from [260].

with uncertainties of up to $10\,\%$ based on the determination of the anode size via optical microscopy after removing the mold mass with a laser (see Section 3.2).

Figure 6.3f shows that despite this difference, the high on-resistance of the Ga_2O_3 diodes causes the $r_o \times Q_c$ figure of merit to be almost seven times higher than that of the SiC-B reference. From Eq. 3.4 an average breakdown field of $2.0\,\mathrm{MV/cm}$ is estimated, which corresponds to about $80\,\%$ of the theoretical SiC limit, and $60\,\%$ of GaN limit, but only $25\,\%$ of Ga_2O_3 limit (see Section 2.3.1) [12]. It is thus vital for future applications to increase the breakdown field. This concerns especially an improved edge termination and process control to enhance the breakdown voltage and allow a reduction of the epitaxial layer thickness to the minimum required value. Also note that with about $1.2\,\mathrm{kV}$ for the $650\,\mathrm{V}$ rated samples, the safety margin between actual breakdown and rated reverse voltage is rather large here, which should be avoided from an electrothermal point of view according to Section 5.3.5. These basic considerations help to analyze the basic switching properties studied in the following section.

6.3.2 Analysis of the basic switching waveforms

General waveforms

As a first step to study the switching properties, Fig. 6.4 shows the current and voltage waveforms during turn-off for all diode samples at a load current of $15\,\mathrm{A}$ and a DC link voltage of $400\,\mathrm{V}$.

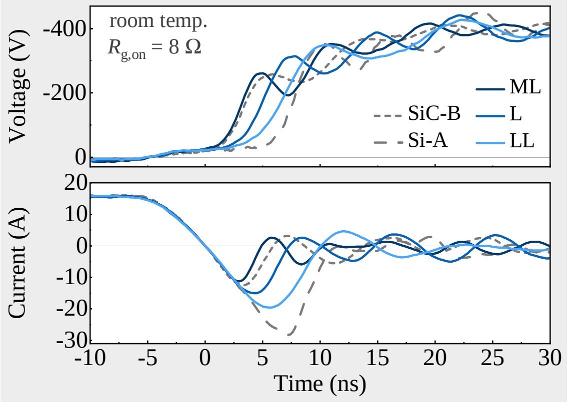


Figure 6.4: Current and voltage waveforms during diode turn-off for the three Ga_2O_3 batch B3 samples ML, L, and LL, and the SiC-B and Si-A references at $400\,\text{V}$ and $15\,\text{A}$. The current undershoot increases with increasing Ga_2O_3 chip size due to the higher capacitive charge. Even for the largest Ga_2O_3 diode, however, it is still lower than the reverse recovery peak of the bipolar Si-A diode. Adapted from [260].

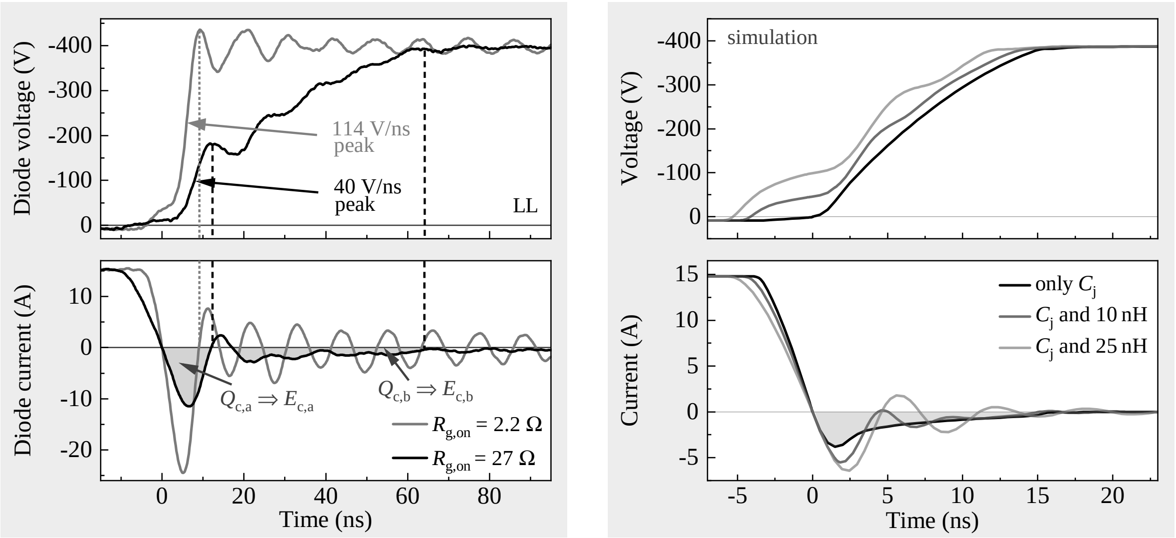
The current slew rate is mainly controlled by the turn-on of the transistor and is therefore similar for all diodes. The negative current undershoot (sinusoidal half-wave) is caused by the charging of the junction capacitance of the diode. The associated maximum reverse current and undershoot time increase with increasing chip area and junction capacitance (see also Fig. 6.3). More detailed explanations of the waveforms will follow below. In the case of the Si-A diode, the recombination of charge carriers adds to the charging of the comparatively small junction capacitance, resulting in the highest reverse current and longest undershoot time.

Varying gate resistance and distinct charging phases

In the following, the gate turn-on resistance $R_{\text{g,on}}$ is varied to study the influence of the MOSFET turn-on speed on the turn-off behavior of the different diodes. The diode current and voltage waveforms at an $R_{\text{g,on}}$ of $2.2\,\Omega$ and $27\,\Omega$ are shown in Fig. 6.5a exemplarily for the Ga_2O_3 LL type diode. Decreasing the turn-on gate resistance increases both the voltage slew rate $\mathrm{d}v_\text{D}/\mathrm{d}t$ and the current slew rate $\mathrm{d}i_\text{D}/\mathrm{d}t$. The current undershoot, often referred to as “reverse recovery” following the nomenclature for bipolar diodes, has previously been used to assess and compare the switching properties of first Ga_2O_3 diodes from different publications with different experimental setups [133, 156–158]. However, even small changes such as a different gate resistance clearly affect the magnitude and shape of the current undershoot substantially. As will be discussed in the following in more detail, such comparisons can therefore be highly misleading.

At low switching speeds (high $R_{\text{g,on}}$) the turn-on speed of the transistor, during whose Miller plateau the junction capacitance of the diode is charged, limits voltage slew rate. At high switching speeds (low $R_{\text{g,on}}$), however, the parasitic commutation-loop inductance and associated LC circuit increasingly limit the voltage slew rate. This gives rise to the following phenomenon visible in Fig. 6.5a.

A low $R_{\text{g,on}}$ (high $\mathrm{d}v_\text{D}/\mathrm{d}t$ and $\mathrm{d}i_\text{D}/\mathrm{d}t$) triggers a high peak reverse current $i_{\text{D,rm}}$ of $-25\,\text{A}$ and an undershoot time of $9\,\text{ns}$. With a correspondingly steep maximum slew rate of $114\,\text{V/ns}$, this current undershoot is already sufficient to charge the junction capacitance to the DC link voltage of about $-400\,\text{V}$. A high $R_{\text{g,on}}$ lowers the current slew rate $\mathrm{d}i_\text{D}/\mathrm{d}t$ and increases



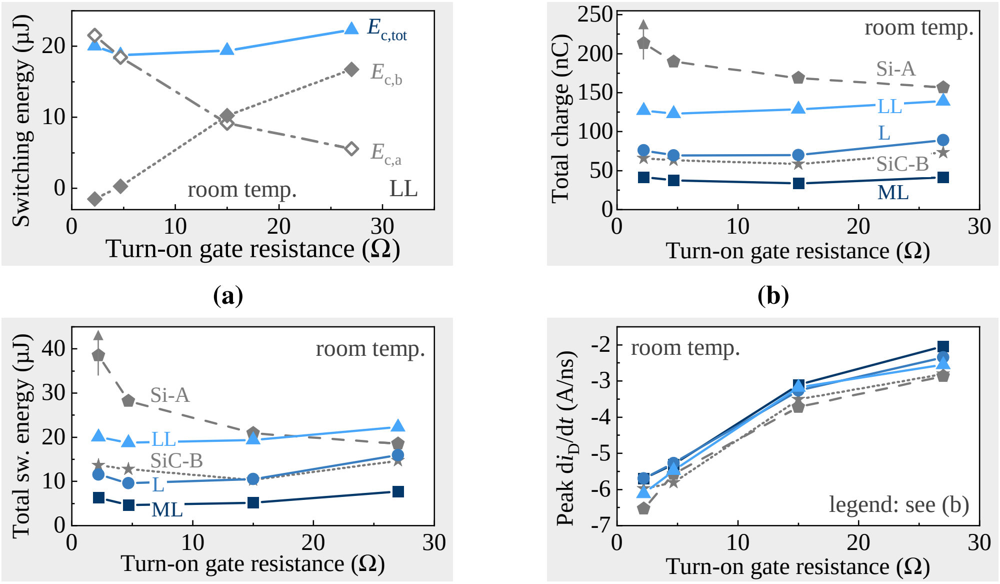
(a) **(b)**

Figure 6.5: (a) The current and voltage slew rate of the Ga_2O_3 diode (here: B3-LL type) during turn-off is reduced by increasing the turn-on gate resistance. This also affects the current undershoot: During the first undershoot associated with the charge $Q_{c,a}$ and energy $E_{c,a}$ the junction capacitance is only partially charged. A second current undershoot supplies the remaining required charge $Q_{c,b}$ and energy $E_{c,b}$ required to reach the DC link voltage. The previous literature comparing the basic properties of different Ga_2O_3 diodes does not take this effect into account. (b) The simulated charging of a voltage-dependent capacitance further illustrates that only the addition of a sufficiently large stray inductance makes the undershoot appear as a sinusoidal half-wave. During this half-wave, however, the charging phase does not necessarily have to be completed. Adapted from [260].

the duration of the first current undershoot to $12\,\mathrm{ns}$ but reduces the peak reverse current to $-11.5\,\mathrm{A}$. With a correspondingly low peak voltage slew rate $\mathrm{d}v_\mathrm{D}/\mathrm{d}t$ of $40\,\mathrm{V/ns}$, the junction capacitance is only charged to a voltage of about $-180\,\mathrm{V}$ during the first current undershoot. The charge associated with this process is marked as $Q_{c,a}$ in Fig. 6.5a and must be smaller than in the previous setup with low gate resistance. Therefore, a second charging phase associated with a second current undershoot of longer duration but lower amplitude supplies the remaining charge $Q_{c,b}$ required to charge the junction capacitance to its final value of $-400\,\mathrm{V}$.

The occurrence of these two charging phases can be explained using the simulations shown in Fig. 6.5b (diode model created on the basis of the explanations in Section 4.4). The fact that the junction capacitance of the diode and the output capacitance of the MOSFET are voltage-dependent causes the charging profile to intrinsically (i.e., without parasitic inductances in the commutation loop) exhibit a peak current followed by a flattened tail rather than resembling a sinusoidal half-wave. Adding a parasitic inductance slows down $\mathrm{d}i_\mathrm{D}/\mathrm{d}t$ and increases the undershoot peak and duration but also induces ringing. A sufficiently high inductance causes the undershoot to appear as a sine half-wave. In agreement with the experimental data, however, the junction capacitance is not yet fully charged after the initial current undershoot.

To get further insight, the gate resistance is varied exemplarily for diode LL at a DC link voltage of $400\,\mathrm{V}$ and a load current of $15\,\mathrm{A}$. The initial charge $Q_{c,a}$ and corresponding energy $E_{c,a}$ are calculated by integrating over the duration of the first undershoot, i.e., from $t = 0\,\mathrm{ns}$ to the first zero-crossing point with positive $\mathrm{d}i_\mathrm{D}/\mathrm{d}t$. The total charge $Q_{c,tot}$ and corresponding



(a) **(b)**

(c) **(d)**

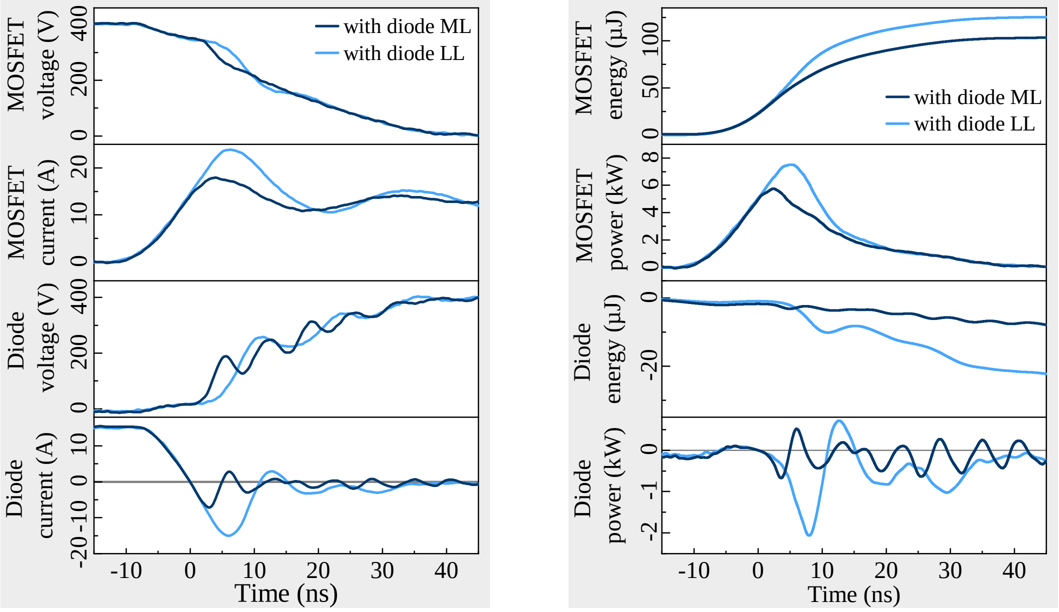
Figure 6.6: Switching measurements at 400 V and 15 A. (a) At low switching speeds (high gate resistance $R_{\text{g,on}}$), the major part of the energy necessary to charge the junction capacitance is supplied in the second charging phase (see Fig. 6.5a). When $R_{\text{g,on}}$ is reduced, $E_{\text{c,b}}$ decreases and $E_{\text{c,a}}$ increases but the total switching energy $E_{\text{c,tot}}$ remains constant. The total (b) charge and (c) energy are independent of $R_{\text{g,on}}$ in case of Ga_2O_3 and SiC, but increase significantly for the Si-A diode. Due to a saturation of the IPM sensor, the values for Si-A at 2.2 Ω are higher than shown. (d) The absolute peak current slew rate increases with decreasing $R_{\text{g,on}}$ but is similar for all diodes. Adapted from [260].

energy $E_{\text{c,tot}}$ are obtained by integrating from $t = 0\,\text{ns}$ up to the time when the diode voltage reaches the DC link voltage of $-400\,\text{V}$. The charge $Q_{\text{c,b}}$ and energy $E_{\text{c,b}}$ associated with the second charging phase are then estimated from the difference of the respective parameters.

The results are shown in Fig. 6.6a. As $R_{\text{g,on}}$ increases, both $\mathrm{d}v_{\text{D}}/\mathrm{d}t$ and $|\mathrm{d}i_{\text{D}}/\mathrm{d}t|$ decrease, reducing the oscillations but increasing the charging time. Therefore, in agreement with the previous considerations in Fig. 6.5, $E_{\text{c,a}}$ decreases and $E_{\text{c,b}}$ increases, but the total energy $E_{\text{c,tot}}$ remains constant. When $R_{\text{g,on}}$ is reduced to $2.2\,\Omega$, the junction capacitance is initially charged to even below $-400\,\text{V}$ because of the voltage overshoot associated with the parasitic loop inductance. Therefore, $E_{\text{c,a}}$ is slightly larger than $E_{\text{c,tot}}$, which is then compensated by a negative $E_{\text{c,b}}$.

Previous statements about the undershoot time, peak current, or charge often only consider the first charging phase [133, 156–158]. This is only meaningful if critical circuit parameters such as loop inductance and switching speed are similar and if the full DC link voltage is reached during the first charging phase. Comparing characteristics of Ga_2O_3 Schottky diodes using these procedures, as often found in literature, is thus not necessarily the most appropriate way. Based on these considerations, only the total charge $Q_{\text{c,tot}}$ and total switching energy $E_{\text{c,tot}}$ is used to compare the devices under investigation in the following.

Figs. 6.6b and 6.6c show the corresponding results at 400 V and 15 A for different turn-on resistances. When increasing the switching speed by lowering the turn-on gate resistance, both $Q_{\text{c,tot}}$ and $E_{\text{c,tot}}$ increase significantly for the Si diode due to its bipolar structure. At an $R_{\text{g,on}}$ of $2.2\,\Omega$, the built-in integrator of the IPM sensor saturates because of the magnitude of the reverse recovery current (see Section 3.4.2). The associated charge and energy are



(a) **(b)**

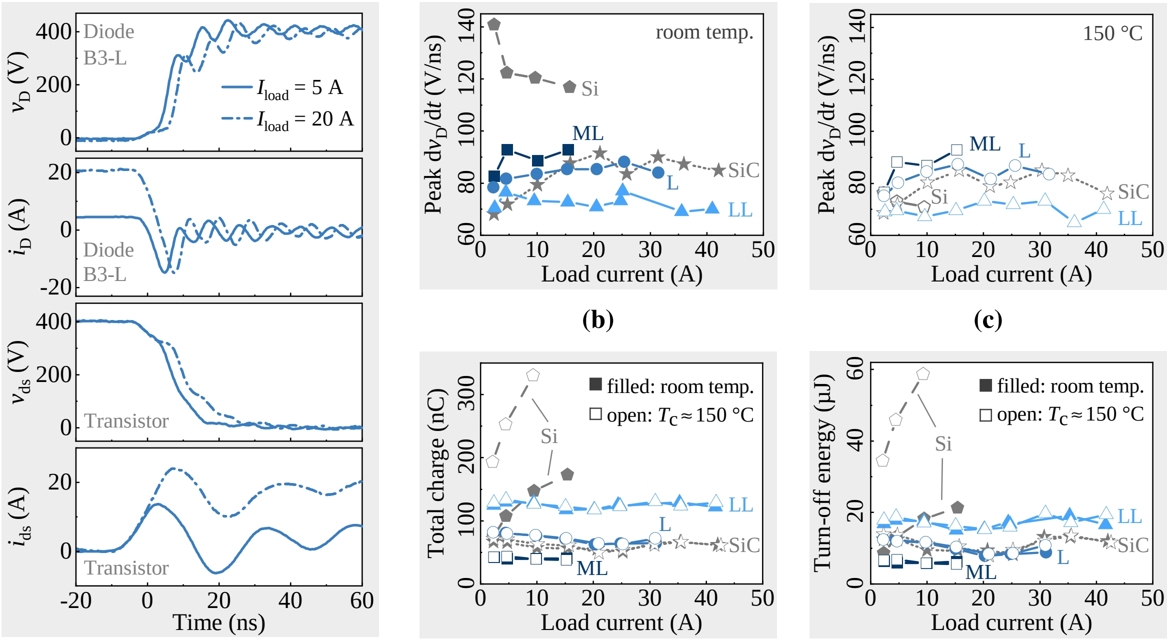
Figure 6.7: (a) Current and voltage waveforms and (b) associated switching power and energy of MOSFET and diode during diode turn-off for the smallest (ML) and the largest (LL) Ga_2O_3 diode. The purely capacitive charging creates negligible losses in the Schottky diode. However, the higher capacitance charge of sample B3-LL results in a larger reverse current peak. This increases the turn-on peak current in the transistor and with that also its turn-on switching loss significantly. Adapted from [260].

therefore higher than shown in Figs. 6.6b and 6.6c, which is indicated by the respective arrows. On the contrary, $Q_{\text{c,tot}}$ and $E_{\text{c,tot}}$ remain constant for both the Ga_2O_3 diodes and the SiC-B diode when the load current is increased.

Among the Ga_2O_3 diodes, both $Q_{\text{c,tot}}$ and $E_{\text{c,tot}}$ increase in the order as expected from the C–V measurements in Fig. 6.3, i.e., they increase with rising anode area. The different doping profile in the epitaxial layer of Ga_2O_3 sample L and the SiC-B sample results in a lower $Q_{\text{c,tot}}$ of the SiC diode, but a similar $E_{\text{c,tot}}$ at the selected DC link voltage, which is also in agreement with the previous considerations. Figure 6.6d shows that the absolute value of the maximum current slope increases with decreasing gate resistance. However, it is similar for all diodes because it is mainly controlled by the turn-on speed of the MOSFET and the commutation-loop inductance rather than the diode properties.

While the bipolar recombination in the Si diode comes with a substantial switching energy loss, the purely capacitive charging and discharging of the junction capacitance in case of the Ga_2O_3 samples only causes minimal energy losses related to a hysteresis between the two processes [227]. However, the corresponding charging and discharging current also affects the switching waveforms in the SiC MOSFET.

Figure 6.7 shows the current and voltage waveforms of the MOSFET and the Ga_2O_3 diode ML an LL (Fig. 6.7a), as well as the associated respective power and switching energy (Fig. 6.7b) when the MOSFET turns on. The higher capacitive charge of diode sample LL in comparison to sample ML enhances the current undershoot. This leads to an increased peak in the transistor current and increases its turn-on power loss, which is expected to increase the MOSFET temperature and limit the high-frequency capability.



(a) **(b)** **(c)** **(d)** **(e)**

Figure 6.8: (a) Diode turn-off and MOSFET turn-on switching waveforms exemplarily for Ga_2O_3 sample B3-L at 400 V and load currents of 5 A and 20 A. Increasing the load current increases the time required to commutate the current and charge the junction capacitance. (b) The room-temperature peak voltage slew rate increases with decreasing Ga_2O_3 anode size, is independent of the load current, and (c) does not change when the case temperature is increased to 150 °C. The (d) charge and (e) energy is independent of the load current and the temperature in case of the unipolar diodes but increases with increasing Ga_2O_3 anode size. Parts adapted from [260].

Influence of load current and junction temperature

Next, the load current is varied between 2.5 A and 40 A at a DC link voltage of 400 V and a turn-on gate resistance $R_{\mathrm{g,on}}$ of 8.2 Ω by changing the length of the first pulse. Measurements are performed at lead frame temperatures of about 30 °C (room temperature) and 150 °C.

Figure 6.8a shows the room-temperature switching waveforms of the diode and the MOSFET exemplarily with sample B3-L at load currents of 5 A and 20 A. Note that the drain current of the MOSFET was measured with a 30 MHz Rogowski probe, which leads to the problems of underestimated current slope and a distorted representation of the oscillations examined in Section 3.4. Similar to the discussion in Section 3.4.5, the absolute current slew rate $\mathrm{d}i_{\mathrm{D}}/\mathrm{d}t$ increases slightly when the load current is increased, but it is still largely affected by the turn-on speed of the MOSFET, i.e., the continuous opening of its channel while the transistor is in saturation mode. Correspondingly, the time required to commutate higher load currents I_{L} increases. Taking the interval between $0.9 \cdot I_{\mathrm{L}}$ and 0 A as the basis, it increases from 1.7 ns at $I_{\mathrm{L}} = 2.5$ A to 7.3 ns at $I_{\mathrm{L}} = 30$ A in the exemplary case of sample B3-L.

The peak $\mathrm{d}v_{\mathrm{D}}/\mathrm{d}t$ depicted in Fig. 6.8b occurs during the initial stage of the charging of the junction capacitance after the current commutation when the reverse current undershoot reaches its maximum. Since the output capacitance of the MOSFET is fairly constant and low when it is still sufficiently charged (about 60 pF for $V_{\mathrm{ds}} > 250$ V), the junction capacitance of the diode strongly influences the peak voltage slew rate. Consequently, the peak $\mathrm{d}v_{\mathrm{D}}/\mathrm{d}t$ decreases with increasing anode size for the Ga_2O_3 diodes as, for the same voltage difference, the duration of the halfwave-like charging current increases, and so does the associated voltage rise time. However, it does not change significantly with varying load current.

On the other hand, the average voltage slew rate (determined between $10\,\%$ to $90\,\%$ of the DC link voltage) decreases significantly, e.g., from about $32\,\mathrm{V/ns}$ at $I_\mathrm{L} = 2.5\,\mathrm{A}$ to $17\,\mathrm{V/ns}$ at $I_\mathrm{L} = 30\,\mathrm{A}$ in the example case of diode B3-L. The reason is that due to the higher load current, the Miller plateau shifts to higher voltages and its duration (during which the output capacitance is discharged) increases. As a consequence, the duration of the second charging phase as defined in Fig. 6.5a increases significantly (e.g., from about $5\,\mathrm{ns}$ at $I_\mathrm{L} = 2.5\,\mathrm{A}$ to about $13\,\mathrm{ns}$ at $I_\mathrm{L} = 30\,\mathrm{A}$), which decreases the overall voltage slew rate.

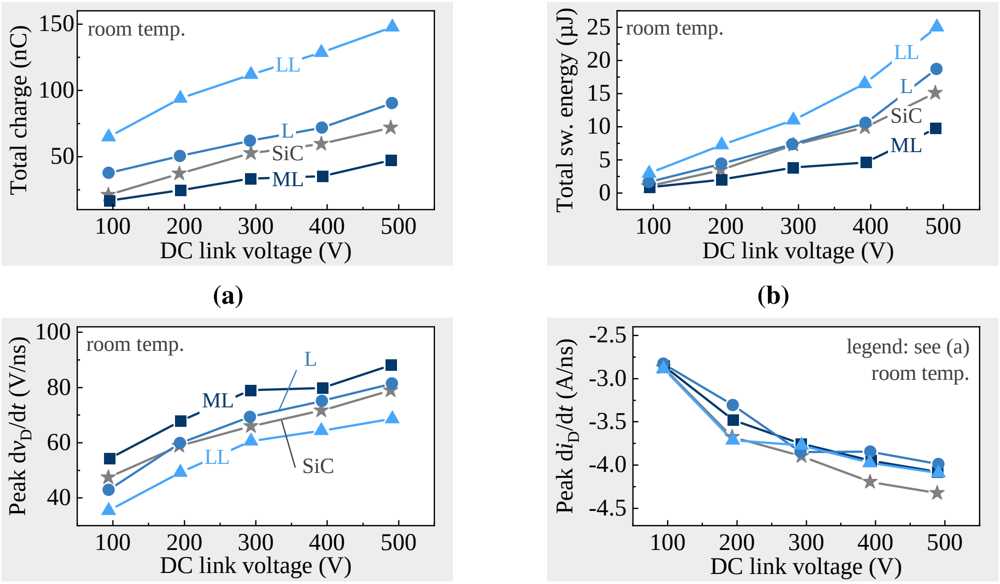
Comparing the results at room temperature and $150\,^\circ\mathrm{C}$ in Figs. 6.8b and 6.8c shows that it is independent of the junction temperature in case of the $\mathrm{Ga_2O_3}$ and SiC samples, but it decreases significantly with rising temperature for the bipolar Si-A diode.

For the $\mathrm{Ga_2O_3}$ samples, the capacitive charge (Fig. 6.8d) decreases in the same sequence as expected from the C–V measurements, i.e., with decreasing anode area in the order $Q_\mathrm{c,tot}(\mathrm{LL}) > Q_\mathrm{c,tot}(\mathrm{L}) > Q_\mathrm{c,tot}(\mathrm{SiC}) > Q_\mathrm{c,tot}(\mathrm{ML})$. In agreement with the previously discussed difference in the doping profile of the epitaxial layers, the total capacitance stored energies $E_\mathrm{c,tot}$ of samples SiC-B and B3-L are similar despite the difference in $Q_\mathrm{c,tot}$ (see Fig. 6.8e) . Apart from that, $E_\mathrm{c,tot}$ and $Q_\mathrm{c,tot}$ show the same trend. For both the SiC and the $\mathrm{Ga_2O_3}$ diodes, $E_\mathrm{c,tot}$ and $Q_\mathrm{c,tot}$ are independent of the junction temperature and load current, proving their purely unipolar character. In case of the Si-A diode, however, the reverse recovery charge and energy increase with both the junction temperature and the load current.

Influence of DC-link voltage

Next, a load current of $10\,\mathrm{A}$ is set with an unchanged turn-on gate resistance of $8.2\,\Omega$, and the DC link voltage is increased from 100 to $500\,\mathrm{V}$ for the SiC and $\mathrm{Ga_2O_3}$ diodes. Measurements are performed only at room temperature, since the preceding experiments confirm the temperature independence of the switching waveforms. Both the capacitive charge $Q_\mathrm{c,tot}$ (Fig. 6.9a) and energy $E_\mathrm{c,tot}$ (Fig. 6.9b) increase with rising DC link voltage and with rising anode size as expected from the C–V measurements, while samples SiC-B and $\mathrm{Ga_2O_3}$ sample B3-L again exhibit similar energies.

Both parameters are, however, some $10\,\%$ higher than the C–V data suggest. As discussed in Section 3.4.1, note that even slight differences in the deskew between current and voltage signal can lead to deviations up to $20\,\%$ in the calculated switching energy. The current signal itself is not affected by this measurement error but two effects lead to additional deviations: First, although the captured current slopes should be accurate within some percent, peak currents might be somewhat overestimated (see also Section 3.4.1) and especially after the transient a slight offset to lower currents is sometimes observed, which increases both $Q_\mathrm{c,tot}$ and $E_\mathrm{c,tot}$. Second, the parasitic commutation-loop inductance increases the maximum reverse current and causes oscillations [31, 180, 228], which also means that the junction capacitance is repeatedly slightly discharged during the charging process. The consequences are two-fold: For one, this results in a purely mathematically higher total charging $Q_\mathrm{c,tot}$ calculated by the analysis algorithm. Furthermore, the (dis-)charging processes can cause additional losses, which should, however, be in the range of well below $1\,\mu\mathrm{J}$ [227] and thus negligible here. Although low-inductive package designs could further reduce ringing and with that some of the discussed effects, note that the influence of the semiconductor itself is still evident here.



(a) (b)

(c) (d)

Figure 6.9: Increasing the DC link voltage at a load current of 10 A leads to an increase in (a) capacitive charge (b) capacitance stored energy (c) peak voltage slew rate and (d) absolute peak current slew rate. The parasitic loop inductance and associated distortion of the switching waveforms lead to a slight deviation from the values expected from the capacitance–voltage measurements. Adapted from [260].

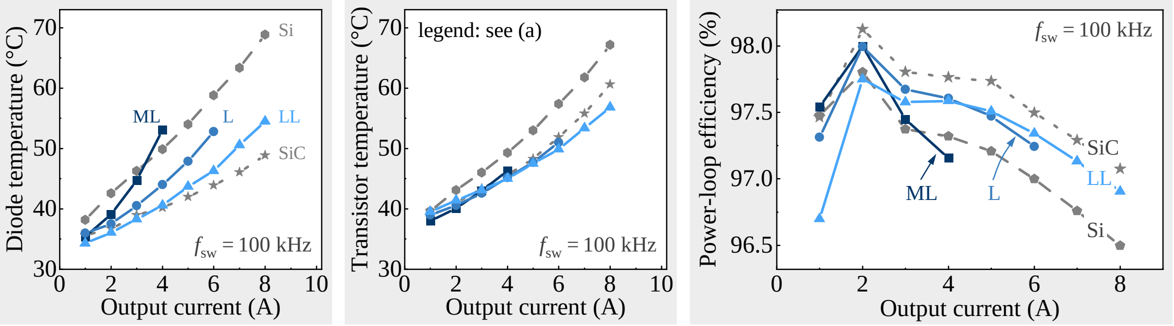
The current slew rate $\mathrm{d}i_\mathrm{D}/\mathrm{d}t$ (Fig. 6.9d) increases directly with rising DC link voltage according to Eq. 3.9 but is similar for all samples since the loop inductance is comparable for all diodes and the switching speed is determined mainly by the turn-on of the MOSFET. The higher capacitive charge associated with higher DC link voltages increases the initial inrush current into the junction capacitance. Although the voltage transient time increases with rising DC link voltage (e.g., from $6.4\,\mathrm{ns}$ at $100\,\mathrm{V}$ to $17.2\,\mathrm{ns}$ at $500\,\mathrm{V}$ for the ML type diode), this leads to a rise in peak $\mathrm{d}v_\mathrm{D}/\mathrm{d}t$ as shown in Fig. 6.9c. In agreement with the previous considerations, the peak $\mathrm{d}v_\mathrm{D}/\mathrm{d}t$ increases with decreasing anode size.

6.3.3 Buck converter operation under varying conditions

The double pulse tests performed in the previous sections provide insight into the switching behavior of $\mathrm{Ga_2O_3}$ diodes and confirm that fast and clean switching is possible with the PCB layout even at voltages exceeding the planned system voltage of $400\,\mathrm{V}$. This provides the necessary basis to proceed with continuous operation tests in a $400\,\mathrm{V}$ to $200\,\mathrm{V}$ buck converter topology. To this end, first the output current is varied at a constant switching frequency of $100\,\mathrm{kHz}$. Then, a constant output current is set, and the switching frequency is increased up to $350\,\mathrm{kHz}$. It is worth emphasizing that a stable operation of the buck converter at $100\,\mathrm{kHz}$ and above for several hours is achieved with the still experimental $\mathrm{Ga_2O_3}$ chips.

Variation of the output current at constant switching frequency

The temperature of the diodes during buck converter operation after reaching a steady state is shown in Fig. 6.11b. It is measured on the lead frame next to the die in case of the $\mathrm{Ga_2O_3}$ diodes, and on the mold mass in case of SiC-B and Si-A. As the output current is increased, the diode temperature rises because of the growing conduction losses. By increasing the chip



(a) **(b)** **(c)**

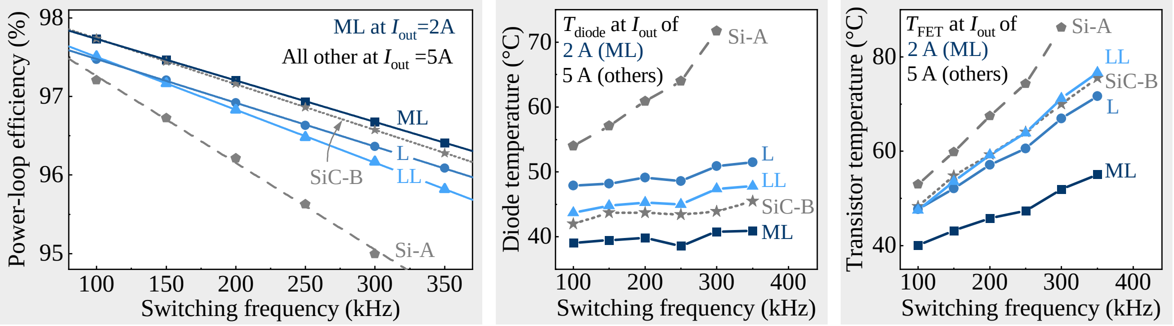
Figure 6.10: 400 V to 200 V buck converter operation at a switching frequency of 100 kHz with TO-packaged Ga_2O_3 batch B3 and the Si-A and SiC-B reference diodes. (a) Increasing the output current leads to a significant increase in the lead frame temperature of the Ga_2O_3 diodes due to growing conduction losses. A thermal relief is achieved by increasing the anode area. (b) The transistor temperature increases more with the bipolar Si-A diode than with the unipolar diodes. (c) Under light load conditions, the efficiency decreases with increasing Ga_2O_3 anode size and capacitive charge. The opposite is the case under heavy load conditions, where the on-resistances dominate. Despite the higher on-resistance, a higher efficiency is achieved with the Ga_2O_3 diodes than with the state-of-the-art Si diode. Adapted from [260].

size, a substantial thermal relief can be achieved: At an output current of 4 A it decreases from 53 °C for ML, over 44 °C for L to 41 °C for LL in agreement with Sections 5.3.3 and 5.3.4.

As shown in Fig. 6.10b, increasing the output current also increases the transistor temperature. The temperature rise is similar for the unipolar Ga_2O_3 and SiC diodes, but slightly higher for the Si-A diode due to the additional reverse recovery current that increases at higher output currents and leads to additional switching losses in the MOSFET in agreement with Fig. 6.7. To avoid possible damage to the devices caused by high junction temperatures related to the high thermal resistance of the 600 µm thick and cathode-side cooled Ga_2O_3 devices (see Chapter 5 and [255, 256, 259]), the maximum output current was limited to 4 A for B3-ML, 6 A for B3-L and 8 A for B3-LL, SiC-B and Si-A. This corresponds to case temperatures of about 50 to 60 °C for the Ga_2O_3 diodes.

Figure 6.10c shows the power loop efficiencies for different output currents. Swapping the freewheeling diode significantly affects the efficiency profiles, which is the basis for the targeted studies.

Under light load conditions, the efficiency is predominantly affected by the parasitic capacitances of the devices. Therefore, the efficiency at 1 A decreases in the order $\eta_p(\text{ML}) > \eta_p(\text{SiC, Si}) > \eta_p(\text{L}) > \eta_p(\text{LL})$, i.e., it decreases with increasing junction capacitance and capacitive charge (increasing anode area) in agreement with the static and dynamic electric characterization in Sections 6.3.1 and 6.3.2. The previously observed thermal relief associated with larger chip sizes is therefore also accompanied by increased switching losses, underscoring the importance of the thermal management strategies explored in Chapter 5. In this respect, the 600 µm thick ML Ga_2O_3 diode broke instantly when the output current was increased from 4 A to 5 A, presumably due to a temperature-induced failure of the blocking capability. However, operating the buck converter with the new 200 µm thin ML type diode was possible at 5 A/100 kHz despite the higher thermal resistance of the AlN-DPC substrate compared to the copper-based TO247 lead frame (see Section 6.4.2).



(a) **(b)** **(c)**

Figure 6.11: When increasing the switching frequency during buck converter operation, even the largest Ga_2O_3 diode (LL) exhibits a lower efficiency drop than the Si-A diode. Thus, the Ga_2O_3 diodes exceed the efficiencies with Si-A despite their high on-resistance. (b) The lead frame temperature of the Ga_2O_3 diodes increases only slightly with rising switching frequency, while the reverse recovery losses in Si-A lead to a significant rise of the mold temperature. (c) Despite the high capacitive charge of Ga_2O_3 sample LL, the increase in MOSFET temperature is lower than with the Si-A reference diode. Adapted from [260].

Under heavy load conditions, the efficiency is increasingly dominated by the on-resistance of the devices. Although the on-resistances of samples Si-A and Ga_2O_3 LL are similar in the range between 2 A and 8 A (see Fig. 6.2a) and Si-A exhibits an even slightly lower on-resistance at higher temperatures (see Fig. 6.2b), the increasing reverse recovery losses in case of Si-A lead to lower efficiencies. Above about 4 A, the efficiencies therefore decrease in the order $\eta_p(\text{SiC}) > \eta_p(\text{LL}) > \eta_p(\text{L}) > \eta_p(\text{Si}) > \eta_p(\text{ML})$. The high on-resistance is clearly a drawback at present, but the fact that small-area diodes have been developed that outperform the theoretical unipolar PFOM of SiC [22, 23] (see also Section 2.3.4) suggests that the efficiencies can be increased in the future. At an output current of 2 A, there appears to be an optimum between the influences of parasitic on-state resistances and capacitances, which is determined largely by the transistor, and leads to a peak efficiency of 97.80 % with Si, 97.75 % with LL, 98.00 % with ML and L, and 98.13 % with SiC.

Variation of the switching frequency at constant output current

Next, a constant output current of 2 A for the ML type Ga_2O_3 diode and 5 A for all other diodes is set during the 400 V to 200 V step-down operation. Then, the switching frequency is increased from 100 to 350 kHz in steps of 50 kHz to assess the high-frequency switching capability of Ga_2O_3 Schottky diodes.

As shown in Fig. 6.11a, a linear decrease in the buck converter efficiency with rising switching frequency is observed for the Ga_2O_3 and SiC Schottky diodes. The efficiency drop increases in the order −0.53 % (ML), −0.56 % (L), −0.58 % (SiC), and −0.67 % (LL) per 100 kHz, as estimated from a linear fit to the data with an uncertainty of about 0.01 %. This agrees with the results in Sections 6.3.1 and 6.3.3 as the parasitic capacitances dominate the efficiency at high switching frequencies. In the case of the Si-A diode, the absolute slope increases disproportionately with increasing switching frequency. If a linear fit is performed nevertheless, the highest average efficiency drop of −1.11 % per 100 kHz is obtained. Compared to the Ga_2O_3 sample B3-L, the efficiency of the converter with Si-A diode is 0.27 % lower at 100 kHz and 1.4 % lower at 300 kHz.

The temperatures measured on the lead frame for the Ga_2O_3 diodes and on the mold mass in case of the Si and SiC diode are shown in Fig. 6.11b. An exact comparison of the absolute temperatures is difficult because of the different positions of the sensors. Nevertheless, significant differences are evident: In case of the unipolar Ga_2O_3 and SiC Schottky diodes, only a slight rise in temperature of about 3 to $4\,\mathrm{K}$ over the entire frequency range is observed. In contrast, the switching losses in the bipolar Si-A diode increase significantly, resulting in a temperature rise of $18\,\mathrm{K}$ when the switching frequency is increased from $100\,\mathrm{kHz}$ to $300\,\mathrm{kHz}$.

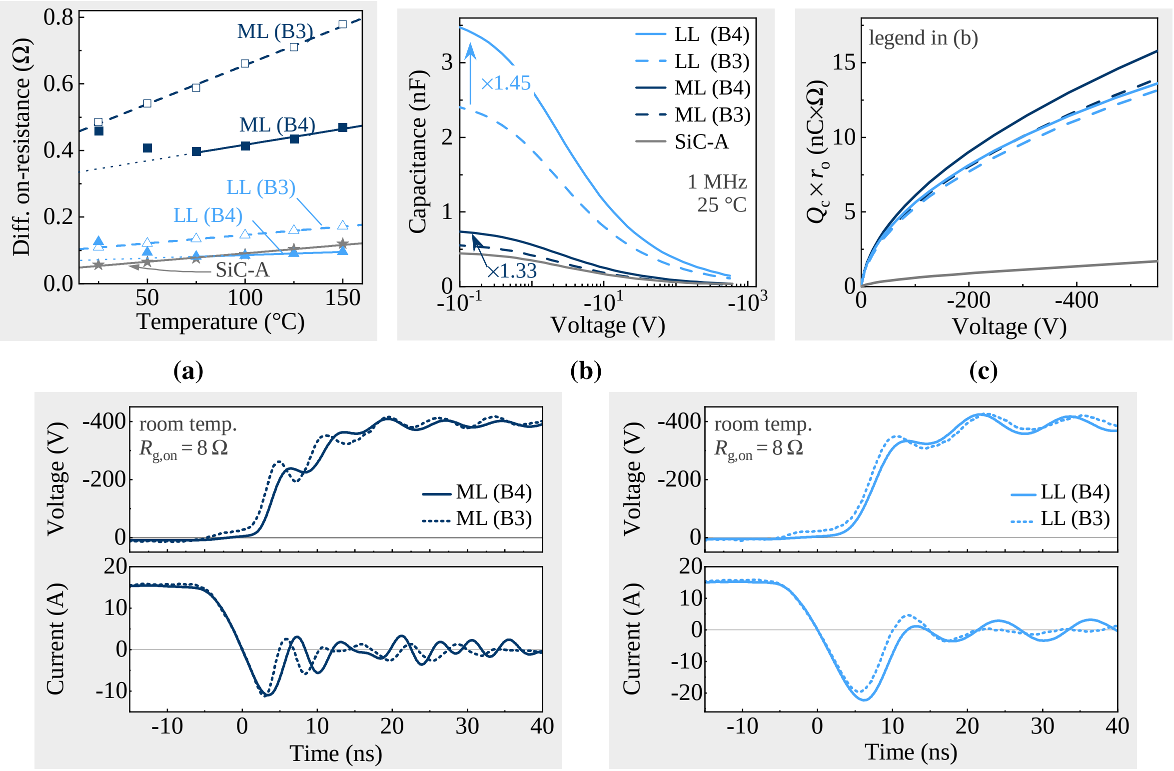
Based on the data in [227], a purely capacitive (dis-)charging of the junction capacitance of the SiC-B diode should lead to an energy dissipation of $< 0.2\,\mu\mathrm{J}$ per cycle. Assuming a worst-case $R_{\mathrm{th,ja}}$ of $10\,\mathrm{K/W}$ (see also discussion in Section 6.4.2) the increase in junction temperature should thus be less than $0.5\,\mathrm{K}$ when the switching frequency is increased from 100 to $350\,\mathrm{kHz}$. As shown in Fig. 6.11c, the transistor temperature measured on its mold mass increases significantly with increasing switching frequency for all samples due to its growing switching losses. Measurements with a thermal camera in the setup with $200\,\mu\mathrm{m}$ thin diodes discussed later (see Fig. 6.11c) show that this increases the temperature of the heat sink by a few Kelvin. The latter effect is therefore (bearing in mind the above estimate) mainly responsible for the slight increase in the temperature of the unipolar diodes.

Since the negative current undershoot during diode turn-off adds to the intrinsic switching losses in the transistor (see Fig. 6.7), the temperature rise is largest when the Si-A diode is used ($+33\,\mathrm{K}$), and decreases for the unipolar diodes in the order Ga_2O_3-LL ($+24\,\mathrm{K}$), SiC-B ($+22\,\mathrm{K}$) and Ga_2O_3-L ($+19\,\mathrm{K}$). This further illustrates that despite the negligible switching losses in the Ga_2O_3 diodes and the temperature relief that can be achieved by increasing their chip size, other thermal management strategies such as those discussed in Chapter 5 should be preferred. Nevertheless, it is noteworthy that even with $600\,\mu\mathrm{m}$ thick Ga_2O_3 diodes and cathode-side cooling, the efficiencies with a state-of-the-art Si diode of similar chip size (which itself shows a comparatively high efficiency) can be surpassed, coupled with a substantial reduction in the junction temperature of the active high-side switch. Although the devices are still at an early stage of development and have a high on-resistance, the advantages of pure unipolar switching seem to outweigh the problems associated with the high thermal resistances when compared to bipolar Si technology in terms of high-frequency switching operation.

6.4 Investigating 200 µm thin diodes with different chip sizes assembled on ceramic substrates

In this section, the newest available generation of $600\,\mathrm{V}$ rated Ga_2O_3 diodes with $200\,\mu\mathrm{m}$ thin substrate from batch B4, soldered to AlN-DPC substrate, is examined in a buck converter application and compared to the $600\,\mu\mathrm{m}$ thick TO-packaged batch B3 devices in the previous section. In addition, the SiC-A diode sintered to an AlN-DPC substrate is used as a commercial reference. Since the dice are not sealed with mold mass or silicone gel, an infrared camera can be used to measure chip surface temperature.

The same measurement settings and PCB layout as in the preceding section are used. To fit the AlN-DPC substrate onto the PCB, only the corresponding footprint has been slightly adjusted. Fundamental switching properties of Ga_2O_3 diodes (such as basic waveforms, temperature-independence, or influence of chip size or gate resistance) are already known from Section 6.3. Therefore, only the data that are important for understanding potential changes in buck converter performance are discussed in the following.



(a) **(b)** **(c)**

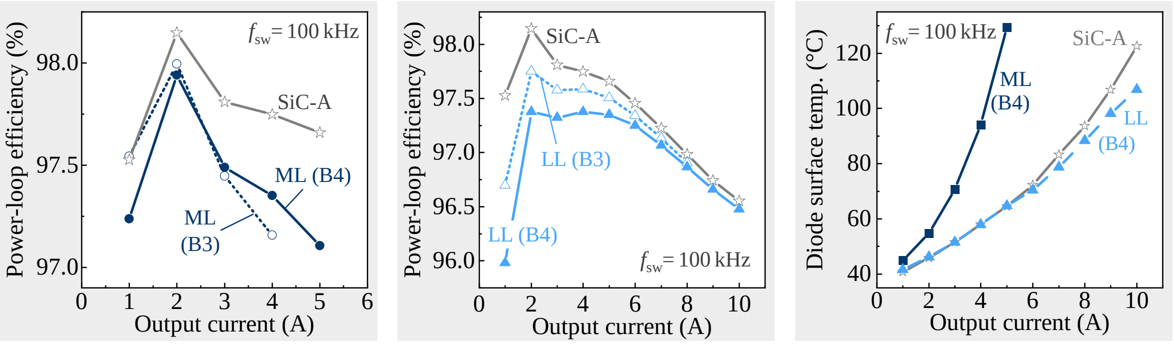
(d) **(e)**

Figure 6.12: Preliminary studies for buck converter tests with 200 µm thin batch B4 Ga_2O_3 diodes of sizes ML and LL in comparison to their batch B3 predecessors: (a) differential on-resistance, (b) capacitive charge, (c) charge × resistance FOM, and double pulse tests with (d) ML and (e) LL diodes. The significant decrease in on-resistance is found to stem from an increase in the doping concentration of the epitaxial layer, which increases the capacitive charge. Therefore, the $Q_c \times r_o$ FOM is not improved, but the higher charge increases the current undershoot during diode turn-off. Adapted from [260].

6.4.1 Electrical properties relevant for converter operation

The forward current–voltage profiles exhibit a change in the temperature-coefficient of the forward voltage at about 75 °C as discussed in Section 4.2.1, i.e., the conduction losses decrease with rising junction temperature until 75 °C but increase for higher temperatures. The coefficient α_{373} describing the increase in differential on-resistance with rising temperature related to a junction temperature of 100 °C is calculated by using Eq. 4.7. With a value of about 1.0 it is lower than the α_{373} values of 1.3 to 1.4 determined for the previous batch B3 diodes. Furthermore, as shown in Fig. 6.12a, the differential on-resistance is reduced significantly compared to batch B3 diodes. Figure 6.12b shows that at the same time the junction capacitance is a factor 1.3 to 1.5 higher than for the batch B3 diodes.

According to Eqs. 2.3 and 3.7 the differential on-resistance is proportional to the inverse effective doping concentration N_D^{-1} while the junction capacitance is proportional $\sqrt{N_D}$. This suggests that the reduction in on-resistance is not only achieved by substrate thinning but mainly by increasing the donor concentration of the epitaxial layer. Indeed, the evaluation of capacitance–voltage profiles according to Section 3.3 yields effective donor concentrations of about $0.8 \times 10^{16}\,\text{cm}^{-3}$ and $0.9 \times 10^{16}\,\text{cm}^{-3}$ for the B3-ML and B3-LL Ga_2O_3 diodes, but about $1.5 \times 10^{16}\,\text{cm}^{-3}$ for the B4-ML and $1.8 \times 10^{16}\,\text{cm}^{-3}$ for the B4-LL diode. This



(a) **(b)** **(c)**

Figure 6.13: The power-loop efficiencies with the (a) ML and (b) LL type diodes of batch B4 are lower under light load conditions but the difference decreases under heavy load conditions and is even reversed in case of the ML diode due to the previously revealed increased doping concentration of the epitaxial layer. (c) The surface temperatures of B4-LL and SiC-A are similar, whereas B4-ML shows a much stronger increase with rising output current. Adapted from [260].

corresponds to an increase of N_D by a factor of 2 and thus constitutes the reason for the rise in junction capacitance by a factor of $\sqrt{2} \approx 1.4$.

Both the substrate and the epitaxial layer contribute to the differential on-resistance, although to a different degree. Assuming an electron mobility of $20\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ in the substrate at an effective donor concentration of $1 \times 10^{19}\,\mathrm{cm^{-2}}$, which is even lower than the pessimistic scenario in Tab. 5.7, this results in a high resistivity of about $31\,\mathrm{m\Omega\,cm}$. In the example case of the ML diode, the substrate should then contribute to the total differential on-resistance with a maximum of $78\,\mathrm{m\Omega}$ for a $600\,\mathrm{\mu m}$ thick diode and $26\,\mathrm{m\Omega}$ in case of the $200\,\mathrm{\mu m}$ thick diode. A comparison to the actual differential on-resistance of about 400 to $450\,\mathrm{m\Omega}$ shows that the diode resistance is dominated by the drift layer despite the increase in doping concentration.

The higher doping concentration of the epitaxial layer translates to a higher capacitive charge and capacitance stored energy. Therefore, as shown in Fig. 6.12c the charge $\times$ resistance figure of merit is not improved with the batch B4 diodes and significantly higher than that of the SiC-A reference diode. The double pulse tests in Figs. 6.12d and 6.12e compare the switching waveforms of the $600\,\mathrm{\mu m}$ thick batch B3 and the $200\,\mathrm{\mu m}$ thin batch B4 diodes at a DC link voltage of $400\,\mathrm{V}$ and a load current of $15\,\mathrm{A}$. The higher doping concentration causes the area and duration of the current undershoot to increase. The additional charge released during diode turn-off adds to the turn-on current peak in the transistor and increases its switching losses as shown in Fig. 6.7. This is expected to ultimately impact the efficiency of the buck converters. Signs of atypical behavior, as seen in the forward and reverse current–voltage profiles, are not evident here.

6.4.2 Buck converter operation under varying conditions

Based on the preliminary considerations, the power-loop efficiencies with varying output currents during $400\,\mathrm{V}$ to $200\,\mathrm{V}$ step-down operation at a switching frequency of $100\,\mathrm{kHz}$ are discussed. The results with the $200\,\mathrm{\mu m}$ thin B4-ML diode, the SiC-A reference diode, and the previous efficiencies with the B3-ML diode are shown in Fig. 6.13a.

Under light load conditions (at $1\,\mathrm{A}$), the efficiency with the B4-ML diode is about $0.3\,\%$ lower than with the B3-ML diode. Under heavy load conditions (at $4\,\mathrm{A}$), however, the efficiency the with B4-ML diode is $0.2\,\%$ higher. Similarly, the B4-LL diode exhibits a $0.7\,\%$ lower efficiency than its batch B3 counterpart under light load conditions but a flatter decrease towards higher output currents, resulting in the same efficiency at $8\,\mathrm{A}$. At an output current of $10\,\mathrm{A}$ the efficiency with diode B4-LL is less than $0.1\,\%$ below the SiC-A reference.

The maximum surface temperatures of the B4-ML, B4-LL, and SiC-A diode are shown in Fig. 6.13c. The temperatures were measured with an infrared camera from the perspective shown in Fig. 6.15b, which is similar to the angle in the photograph in Fig. 6.1b. Although the SiC and ML diode have similar chip size, the increase in surface temperature is significantly higher in case of ML. As expected from the larger chip size and lower on-resistance of the LL size diode, the surface temperatures are significantly lower. Up to $5\,\mathrm{A}$ they are similar to the SiC-A sample, and even lower at higher output currents. A direct comparison of the temperatures of the B3 and B4 samples is not possible due to the different package structures and the fact that only the lead frame temperature was measured for the sealed batch B3 chips. However, the following consideration provides further details.

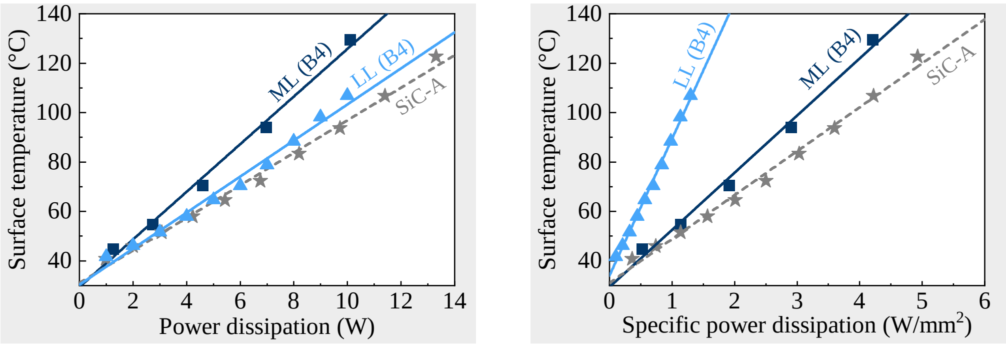
The junction temperature is determined by the junction-to-ambient thermal resistance $R_{\text{th,ja}}$ and the actual power loss. To gain further insight, the temperature dependent knee voltages V_0 and the temperature dependent differential on-resistances r_{o} are fitted with polynomial curves. By approximating the junction temperature as the measured chip surface temperature, this allows to estimate the conduction losses during buck converter operation according to

$$P_{\text{cond}}\left(T_{\text{j}}\right) = V_0\left(T_{\text{j}}\right) \cdot I_{\text{D,ave}} + r_{\text{o}}\left(T_{\text{j}}\right) \cdot I_{\text{D,rms}}^2, \tag{6.1}$$

where $I_{\text{D,ave}}$ is the average and $I_{\text{D,rms}}$ is the RMS (root-mean-square) current. The respective measured current ripples (about $1.7\,\mathrm{A}$ at $100\,\mathrm{kHz}$ for all diodes) and duty cycles (about $50\,\%$ for all diodes) are used to calculate the RMS current. As shown in Section 6.3.2, the switching losses in the Schottky diodes are negligible. Furthermore, the power loss during blocking operation is roughly two to three orders of magnitude lower than the forward conduction losses. The diode power loss is therefore dominated by the conduction losses and can, in a simplified view, be approximated by them.

On this basis, Figs. 6.14a and 6.14b display the chip surface temperature as a function of the absolute and area-related (with respect to anode area) conduction losses, i.e., the absolute and the specific heating power. Clearly, the same trend as predicted in Sections 5.3.3 and 5.3.4 is observed: The B4-LL size diode shows a similar increase in junction temperature as the SiC-A reference diode, and a significantly lower temperature rise than the ML-size counterpart. Relating the power dissipation to the anode area, however, reveals a significant decrease in the power density capability of the LL-size diode. These considerations directly validate the results in Chapter 5.

To further quantify this aspect, the γ_{T} value (see Eq. 5.3) is roughly estimated for the actively operated buck converter. Note that the setup differs from the one in Section 5.3 in several respects. Amongst others, these are the less effective air cooling implemented here, the use of a different thermal interface material than in the previous measurements, and the fact that not the entire DPC substrate is coupled to the heatsink because of the required solder connection to the PCB (see Fig. 6.1b). Furthermore, as discussed in Section 6.3.3, the additional power loss in the transistor also affects the heat sink temperature close to the diode. The apparent $R_{\text{th,ja}}$ determined from a linear fit to the data in Fig. 6.14 are therefore expected to be higher than the ones determined with grease in Figs. 5.9b and 5.9d. Indeed, the fit yields about



(a) **(b)**

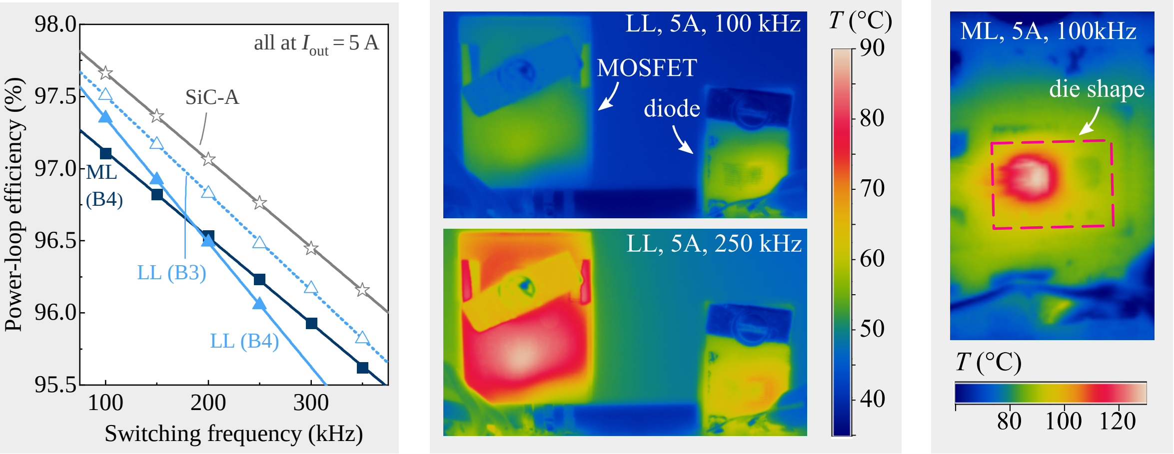
Figure 6.14: The power dissipation during buck converter operation with different output currents is estimated from the measured surface temperature, the ripple current, and the temperature dependent forward current–voltage profiles. This allows the extraction of the junction-to-ambient thermal resistance. Although increasing the chip size is (a) effective in decreasing the junction temperature, it (b) decreases the maximum possible power density significantly. This validates the result in Section 5.3.

$9.6\,\mathrm{K/W}$ for Ga_2O_3 sample B4-ML and $6.5\,\mathrm{K/W}$ for SiC-A, which is about $3\,\mathrm{K/W}$ larger than the previously determined values. Using the apparent $R_{\mathrm{th,ja}}$ values and Eq. 5.3, γ_{T} values of 0.68 and 0.76 are obtained for the B4-ML diode from Figs. 6.14a and 6.14b, respectively, which is slightly higher than the experimentally determined one of 0.61 in Section 5.3.5. This is reasonable since the $R_{\mathrm{th,ja}}$ is larger in the buck converter setup, therefore decreasing the influence of the chip.

In Fig. 6.15a, an output current of $5\,\mathrm{A}$ is set for all diodes and the switching frequency is increased in steps of $50\,\mathrm{kHz}$. The B4-ML Ga_2O_3 diode and the SiC-A reference diode exhibit a similar efficiency drop of about $-0.6\,\%$ per $100\,\mathrm{kHz}$ due to their similar junction capacitance and capacitive charge. The B4-ML failed after $4\,\mathrm{min}$ at $350\,\mathrm{kHz}$ and a maximum surface temperature of about $131\,°\mathrm{C}$, which is the last data point shown in Fig. 6.15a. When the failure occurred, the diode had already been in operation for $3\,\mathrm{h}$ without interruption, at $400\,\mathrm{V}$ and between $100\,\mathrm{kHz}$ and $350\,\mathrm{kHz}$.

Since the current undershoot during turn-off of diode B4-LL is enhanced as a result of the higher capacitive charge compared to sample B3-LL (see Fig. 6.12e), the corresponding turn-on switching losses in the MOSFET increase. This leads to the highest efficiency drop of about $0.86\,\%$ per $100\,\mathrm{kHz}$ for sample B4-LL. The effect of the additional charge on the MOSFET temperature is so pronounced that the switching frequency has been limited to $250\,\mathrm{kHz}$: As shown in Fig. 6.15b, increasing the switching frequency from $100\,\mathrm{kHz}$ to $250\,\mathrm{kHz}$ leads to a rise of $7\,\mathrm{K}$ in the maximum chip surface temperature of the B4-LL Ga_2O_3 diode, while a $32\,\mathrm{K}$ increase in the maximum mold temperature of the MOSFET is observed — twice as much as with the B3-LL diode in the same frequency range. Figure 6.15c shows a thermal image of the rectangular ML-size diode during buck converter operation at $5\,\mathrm{A}$ and $100\,\mathrm{kHz}$. The anode clearly constitutes the major heat source and the heat does not spread significantly into the non-active part of the die due to the low thermal conductivity of Ga_2O_3. This further validates the thermal simulations in Section 5.2.4.

The data demonstrate the successful introduction of $200\,\mathrm{\mu m}$ thin $600\,\mathrm{V}$ class Ga_2O_3 diodes and validate the thermal considerations in Section 5.3, but also show that the tradeoff between on-resistance and capacitive charge needs to be further improved. It should be noted that as a next step, reliability studies with a larger sample size should also be conducted once available.



(a) **(b)** **(c)**

Figure 6.15: Buck converter operation at an output current of 5 A with different switching frequencies. (a) When increasing the switching frequency, the drop in efficiency is higher for the batch B4 LL-type diode than for its batch B3 predecessor, due to the higher doping concentration in the epitaxial layer. (b) While the chip surface temperature of the LL-type diode increases by only 7 K for an increase from 100 kHz (top) to 250 kHz (bottom), the mold temperature of the MOSFET increases by 32 K. (c) In agreement with the simulations in Chapter 5, the heat does not spread significantly into the non-active part of rectangular ML-size Ga_2O_3 diodes. Parts adapted from [260].

6.5 Chapter conclusion

This chapter analyzes the switching properties of 600 µm thick TO247 packaged and new 200 µm thin Ga_2O_3 diodes mounted on ceramic substrates in a first 400 V to 200 V buck converter application. The main results can be summarized as follows:

1. The new chips enable load currents, DC link voltages and associated current and voltage slew rates significantly exceeding those in previous literature.
2. A stable buck converter operation for several hours at switching frequencies up to 350 kHz is observed, demonstrating the successful introduction of 200 µm thin wafer Ga_2O_3 technology despite the atypical current–voltage characteristics.
3. The failure of ML size diodes at high power densities provides a first insight into operating limits and shows the need for further studies with a larger sample size once available.
4. Despite the early stage of development and high on-resistance, power-loop efficiencies with a state-of-the-art Si diode can be exceeded.
5. Measurements of the chip temperature validate the considerations in Chapter 5 and show that increasing the chip size reduces the junction temperature but also limits the switching frequency and the power density. Therefore, it is not recommended as the main method of circumventing the low thermal conductivity of Ga_2O_3.
6. It is vital for future device generations to reduce the on-resistance without increasing the capacitive charge. This will especially concern the optimization of electric field management methods, the thickness of the epitaxial layer, and its doping profile.

Chapter 7

Summary and outlook

β–Ga_2O_3 is a semiconductor material that combines a wider bandgap than that of SiC or GaN with the availability of wafers fabricated by standard melt-growth techniques. Based on these material properties, it could help meet the growing demand for low-cost, high-efficiency power electronics. Motivated by this, the basic electrical, thermal, and switching properties of first non-commercial β–Ga_2O_3 diodes from a planned manufacturing line are studied in this work with the goal of building a bridge from fundamental device-level research to first applications with Ga_2O_3 devices in power electronics. The corresponding guiding questions formulated in Chapter 1 concern characteristic similarities and differences between Ga_2O_3 and SiC diodes, the assessment of the device quality in view of a potential application in power electronics, the feasibility of an implementation in fast-switching power converters despite the low thermal conductivity, and the identification of associated problems but also potential solutions.

First, a low-inductive discrete package based on an AlN ceramic substrate was designed. Bare Ga_2O_3 diode chips with unknown characteristics and SiC reference samples were assembled on these substrates in various ways to enable the required variety of different experiments. Studying the nanosecond short switching transients is an especially challenging task. Therefore, new current sensors are comparatively evaluated. A new magnetic sensor, referred to as IPM sensor, was selected to capture single switching transients. The resistive M-shunt was used for continuous measurements with longer DC periods. This preliminary work allows for a gradual answering of the initial guiding questions through combined experimental and simulative studies.

Several β–Ga_2O_3 diodes exhibit temperature-dependent forward and reverse current–voltage profiles similar to those of commercial SiC diodes. For multiple diodes, however, a transition between different conduction mechanisms is observed: both in forward and reverse direction, the conduction losses first decrease and then increase with rising junction temperature. This seems to be related to the manufacturing process of the dice and a possibly linked influence of trap states rather than intrinsic properties of Ga_2O_3 or packaging issues. The differences are intensified by a variation of material properties, such as the effective donor concentration of the epitaxial layer between different devices of the same type. Spice models that can replicate these varying characteristics in a simple but effective way are created to help design future power converters.

For all Ga_2O_3 diodes, the relative increase in differential on-resistance with rising temperature is lower than that of commercial SiC diodes, which can be traced back to the lower temperature-dependence of the electron mobility in Ga_2O_3. In combination with a fairly homogeneous junction as indicated by the low change of ideality factor and Schottky barrier height with rising temperature, the Ga_2O_3 samples could, in principle, be suitable for high-temperature applications and allow for the conduct of more application-oriented tests. However, they still suffer from significantly higher specific on-resistances than their SiC counterparts, and the low thermal conductivity of Ga_2O_3 limits the power and current rating with the current $600\,\mu m$ thick and cathode-side cooled standard devices significantly.

Driven by this concern, methods to increase the current and power rating of Ga_2O_3 diodes were studied. The combination of thermal measurements and simulations shows that the heat dissipation in Ga_2O_3 differs significantly from that in SiC. Although substrate thinning to $200\,\mu m$ can reduce the junction temperature of Ga_2O_3 diodes effectively, cooling from the junction side is found to be substantially more effective despite the smaller cooling area. However, if not the entire anode area is precisely covered with die attach material, the resulting gaps can lead to a severe increase in the local peak temperature and must be avoided. Underfill materials can alleviate this issue. The results are combined with different scenarios regarding potential improvements of the growth conditions and material properties. This way it is shown that, despite the low thermal conductivity, thinned or junction-side cooled Ga_2O_3 diodes could achieve junction temperatures similar to those of commercial SiC counterparts at the same forward current as a result of their potentially lower conduction losses.

The newest generation of $600\,\mu m$ thick and $200\,\mu m$ thin Ga_2O_3 cathode-side cooled diodes was tested for the first time in a $400\,V$ to $200\,V$ buck converter with switching frequencies between $100\,kHz$ and $350\,kHz$. Even $600\,\mu m$ thick cathode-side cooled samples can be implemented successfully despite the early stage of development and high thermal resistance. In agreement with the previous considerations, the rise in junction temperature is significantly stronger than that of a commercial SiC reference diode of similar size. Increasing the die size is effective in reducing the junction temperature only to a certain extent, as it also reduces the maximum specific power density and limits the switching frequency. However, despite the currently still high on-resistances, higher power-loop efficiencies than with a state-of-the-art bipolar Si diode can be achieved thanks to the purely unipolar device structure and the associated absence of recombination losses.

Further device-level research must focus on improving the tradeoff between on-resistance and capacitive charge. This especially concerns electric field management strategies to fully exploit the high theoretical breakdown field of Ga_2O_3 also in large-area devices. Although an improvement in the device quality is observed for the newest generation diodes, the variation in the basic device characteristics must be further reduced. Once a larger sample size is available, this is also the basis for reliability studies whose importance is underlined by the presumably temperature-induced failure of two Ga_2O_3 diodes during buck converter application. Apart from Ga_2O_3 as a material in itself, the packaging procedures may need to be reconsidered. This could also entail the development of new underfill materials with high thermal conductivity for junction-side cooled assemblies.

In summary, a device quality sufficient to enable application-oriented research has been achieved. The experimental and simulative results reveal certain limitations, but also point to possible solutions that can help pave the way to Ga_2O_3 power electronics.

Appendix

A Overview of material properties of different semiconductors

Table A.1: Summary of important material properties of Si, 4H-SiC, wurzite GaN, and β–Ga_2O_3 at room temperature. Note that the given values vary slighlty in literature. In case of Ga_2O_3, the properties additionally depend on the crystal direction due to its strong anisotropy. Electrical and thermal properties are taken from [12, 28, 71, 85], Vickers hardness H_v and Young's moduli E_young are taken from [105, 107, 108, 229, 230] for Si, 4H-SiC and GaN, and from [102, 231, 104] for β–Ga_2O_3.

	Si	**4H-SiC**	**Bulk GaN**	**β–Ga_2O_3**
E_G (eV)	1.1	3.3	3.4	4.6–4.9
E_br (MV / cm)	0.3	2.5	3.3	~8
ϵ_s	11.8	9.7	9.0	10–12
μ_e (cm^2 (Vs)$^{-1}$)	1400	1000	1200	200
v_sat (10^7 cm / s)	1.0	2.0	2.5	1.5
λ_th (W (mK)$^{-1}$)	150	270	210	10–30
melt-grown wafers?	yes	no	no	yes
H_v (GPa)	9–12	30	10-11	6–13
E_young (GPa)	160	500	290	230

B List of measurement equipment

Table B.2: The following measurement equipment and tools have been used throughout the entire thesis in various chapters for temperature-dependent electrical characterization, transient thermal characterization, thermal imaging, computer tomography investigations, and laser ablation.

Type	**Device Name**	**Purpose**
power device analyzer	Keysight B1505A	static electrical characterization
air heater	ATS-545 Thermostream	temperature control during electrical characterization
transient thermal tester	Mentor T3Ster	impedance profiles and structure functions
infrared camera	Optris PI640i	thermal imaging of chip temperature
computer tomography	GE Sensing v|tome|x microfocus CT	cross-sectional inspection of dice and packages
laser	Trumpf TruMark Station 5000	laser ablation/ removal of mould mass

Table B.3: The following measurement equipment was used for the dynamic electrical characterization in Sections 3.4.2, 3.4.3 and 3.4.5. More details about the current sensors under investigation in this chapter are listed in Tab. 3.3.

Type	Device Name	Comment
oscilloscope	LeCroy Waverunner 104Xi	display waveforms of active switch
oscilloscope	LeCroy Waverunner 44Xi	display waveforms of passive switch and load current
voltage probe	LeCroy PP006-WR	drain–source voltage
voltage probe	LeCroy ADP033	gate–source voltage
current probe	LeCroy CP031	load current
high-voltage source	TopCon Quadro Power Supply	DC link voltage
low-voltage source	Toellner TOE 8952-60	PCB power supply
pulse generator	Aim-TTi TGP3152	gate driver PWM signal

Table B.4: The following measurement equipment was used for the dynamic electrical characterization in Section 3.4.6.

Type	Device Name	Comment
oscilloscope	Tektronix MSO58	display waveforms
voltage probe	Tektronix TIVP05	diode voltage
current probe	Tektronix TCP0030A	load current
high-voltage source	EA PSI 91000-30	DC link voltage
low-voltage source	Toellner TOE 8952-60	PCB power supply
pulse generator	Aim-TTi TGP3152	gate driver PWM signal

Table B.5: The following measurement equipment was used for the dynamic electrical characterization in Chapter 6, i.e., for double pulse tests and buck converter application.

Type	Device Name	Comment
oscilloscope	LeCroy Waverunner 104Xi	display diode waveforms
oscilloscope	LeCroy Waverunner 44Xi	display transistor waveforms
voltage probe	PMK PHV1000	diode voltage
current probe	IPM sensor	diode current (double pulse test)
current probe	M-shunt	diode current (continuous operation)
voltage probe	LeCroy HVD3106A	transistor drain–source voltage
voltage probe	LeCroy HVD3106A	transistor gate–source
current probe	PEM CWTUM 015/B	transistor drain current
current probe	PEM CWTUM 6/B	transistor drain current
current probe	LeCroy CP031	load current
data logger	Graphtec GL220E	log temperature with k-type thermocouple
high-voltage source	EA PSI 91000-30	DC link voltage
electronic load	EA ELR 9750-66	control converter output current
power analyzer	ZES Zimmer LMG 500-4	efficiency measurements
low-voltage source	GW-Instek PSP-603	PCB power supply
low-voltage source	Delta Elektronika ES 030-5	fan power supply
pulse generator	Aim-TTi TGP3152	gate driver PWM signal

C List of used software

Table C.6: Overview of the most important software used for simulation and data analysis throughout this thesis.

Software	**Purpose**
KiCad 5.1.6	design of PCBs and discrete packages
PTC Creo 4	construction of device models
Simcenter FloEFD 2020.2	static and transient thermal simulation
Ansys Q3D 2020-R1	simulation of parasitic loop inductance
LTSpice XVII	circuit simulation & device modelling
Mentor T3Ster-Master V.3.0.0.7109	post processing of thermal transient results
Volume Graphics myVGL 34	analysis of X-ray images
Matlab R2019a, Matlab R2022b	data analysis
OriginPro 2020 SR1	data analysis

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References

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