

**Influence of domain walls on transport properties of  
LaAlO<sub>3</sub> / SrTiO<sub>3</sub> nanostructures**

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*Dedicated to my parents and dear family members*

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# Abstract

This thesis primarily focuses on the influence of domain walls on the transport properties of LAO/STO nanostructure. Since the discovery of the conducting interface between LAO and STO, numerous studies have been conducted to understand the underlying mechanism behind interfacial conductivity and the multitude of properties exhibited by this interface. However, it took almost a decade to discover the importance of domain walls, which are formed as a result of the cubic-tetragonal phase transition occurring at around 105 K in the STO substrate, on the interfacial conductivity.

Nanopatterning of the interface poses a challenge for quite some time since etching with high-energy radiation induces conductivity on the STO substrate. This conductivity of the interface limited the application of this interface. But recently several reliable nanopatterning techniques have been successfully implemented. Studies on nanoscale devices reveal that the influence of domain walls on transport properties is more significant than in large area structures. We have implemented a series of experiments to investigate the role of domain walls on the transport properties of the nanopatterned LAO/STO interface.

By using a special sample geometry we have investigated how the orientation angles of the nanopatterned hall bars alters the magnetoresistance properties of the interface. We observed a significant difference in MR with orientation angles which can be attributed to different orientations and the number of domain walls present in the nanostripes. Additional experiments reveal that the warming of the samples through the phase transition temperature significantly alters the MR behaviour. This is a clear indication that the reconfiguration of domain walls pattern after a temperature sweep through 105 K alters the MR. All such anisotropy in MR vanishes when the size of the structure is increased above a certain limit.

For the future practical application of the oxide-based heterostructures, it is very important to understand how the interfacial properties are influenced by the application of gate voltages. We have implemented side gated devices to investigate the significance of gate voltages. Side gating configuration modulates the carrier concentration at the interface much stronger for smaller gate voltage compared to back gate configuration. Side gating significantly differs from top gating since the electric field is applied through

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the STO substrate in the side gate configuration while in the latter the field is applied typically through a top dielectric with a lower dielectric constant. Studies conducted on the side gated nanostructures reveal that the gate voltage, independent of its polarity, induces persistent changes in the transport properties of the interface such as the increase in base resistance, change in MR behaviour and pronounced resistance anomaly at 80 K. Former studies showed persistent changes that were attributed to charge carrier trapping and oxygen vacancies. This was supported by the fact that the modifications were only observed at positive gate voltages. Our side gating techniques allow us to observe these changes also at negative gate voltages. This fact is new and at the same time shows that trapping cannot be the origin. We can now link these modifications to the expansion of domains which up to now was only observed by optical studies and that was not linked to changes in transport properties.

Another aspect, which also can only be demonstrated by the side gating technique is the observed scaling of the structure size in which domain related transport effects are observed. As shown in the past, transport through domain walls can dominate the conductivity in structures smaller than a few hundred nm. In larger structures parallel conduction through parallel domain walls makes the effects small or even undetectable. In our experiments we increase the average domain size and reduce the number of parallel domain walls. This way, we increase the size limit observed before to at least 2  $\mu\text{m}$ .

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# Abbreviations

<b>STO</b>	Strontium titanate
<b>LAO</b>	Lanthanum aluminate
<b>2DEG</b>	Two Dimensional Electron Gas
<b>uc</b>	unit cell
<b>AFM</b>	Atomic Force Microscope
<b>MBE</b>	Molecular Beam Epitaxy
<b>BHF</b>	Buffered fluoric acid
<b>AlO<sub>x</sub></b>	Alumina (aluminium oxide)
<b>SHE</b>	spin Hall effect
<b>ISHE</b>	Inverse spin Hall effect
<b>IEE</b>	Inverse Rashba-Edelstein effect
<b>FM</b>	Ferromagnet
<b>FE</b>	Ferroelectric
<b>WL</b>	Weak localisation
<b>WAL</b>	Weak anti-localisation
<b>SOI</b>	spin-orbit interaction
<b>SOC</b>	spin-orbit coupling
<b>EY</b>	Elliott-Yafet
<b>DP</b>	D'yakonov-Perel
<b>MR</b>	Magnetoresistance
<b>STM</b>	scanning tunnelling microscopy
<b>SQUID</b>	superconducting quantum interference device
<b>SET</b>	single electron transistor
<b>AFD</b>	antiferrodistortive
<b>LTSEM</b>	low-temperature scanning electron microscop
<b>PLD</b>	Pulsed Laser Deposition

<b>pO<sub>2</sub></b>	Oxygen partial pressure
<b>RHEED</b>	Reflection High Energy Electron Diffraction
<b>RIE</b>	Reactive Ion Etching
<b>ICP</b>	Inductively Coupled Plasma
<b>UV</b>	Ultraviolet
<b>e-beam</b>	electron beam
<b>SEM</b>	Scanning electron microscope
<b>NEP</b>	N-Ethylpyrrolidone
<b>DAC</b>	Digital-Analog-Converters
<b>FET</b>	Field-Effect-Transistor
<b>QW</b>	Quantum well

# Symbols

$\square$	Square area
$n$	carrier density
$\mu$	carrier mobility
$B$	Magnetic field
$T_{PT}$	Phase transition temperature (105 K)
$T_{PT_1}$	Lower phase transition temperature (65 K)
$T_{PT_2}$	Upper phase transition temperature (105 K)
$V_G$	Back gate voltage
$V_{SG}$	Side gate voltage
$V_{SG_{max}}$	Maximum side gate voltage
$T_{min}$	Minimum temperature
$T_{max}$	Maximum temperature
$I_G$	Gate current
$\lambda$	Wavelength
$R_{ref}$	Reference resistor
$R_s$	Sample resistor
$\sigma$	sheet conductance
$\tau_i$	inelastic scattering time
$\tau_{so}$	spin relaxation time
$\tau_e$	elastic scattering time



# Introduction

The demand for powerful and portable electronic devices is increasing at an enormous pace. In order to fulfil the growing demands, physicists and engineers are designing novel architectures, with a prime focus on increasing the power efficiency of the device while at the same time shrinking the size as far as possible. For the past several decades, the semiconductor industry has relied on the prediction of Gordon Moore that the number of components per integrated circuit doubles every two years [1, 2]. This was possible because of the constant scaling down of transistors and their cost of production, along with the increasing complexity of novel architecture. But unfortunately, the constant speed of scaling is approaching its limit. Graphene and transition metal oxides are two alternative materials that can be used to create devices that are versatile, more intelligent, and faster [3–5] even though the modern electronics industry is still primarily silicon-based. These oxide-based materials have a wide range of properties that are extremely sensitive to crystal chemistry, electronic correlations, and structural distortions.

A family of transition metal oxides that have attracted a huge amount of attention is  $ABO_3$  perovskite compounds. Oxide materials exhibit numerous electronic properties of semiconductors. They also exhibit other fascinating properties like high-temperature superconductivity [6], colossal magnetoresistance [7], strain-driven ferroelectricity [8], interfacial conductivity and ferromagnetism [9, 10] and quantum Hall effect [11], to name a few. All of these unique features made the oxide materials a promising choice for future multifunctional oxide electronics in memory, logic, and sensing applications [12]. One of the most intensively studied complex oxides is the interface between band gap insulators  $LaAlO_3$  (LAO) and  $SrTiO_3$  (STO).

In 2004, Ohtomo and Hwang discovered a highly mobile conducting two-dimensional electron gas (2DEG) at the interface between LAO and STO [9]. Studies following the discovery of the 2DEG reveal many other fascinating properties of the LAO/STO interface, such as induced ferromagnetism, superconductivity, gate tunable metal-insulator transition and many more [10, 13–15]. All these fascinating properties of the  $LaAlO_3/SrTiO_3$

interface make it an ideal system to study the fundamental properties of strongly correlated electron systems and also a viable candidate for future electronic applications.

When complementary metal-oxide-semiconductor (CMOS) technology reaches characteristic sizes of 7 nm [16–18], transistor functionality begins to be affected by electron tunnelling effects. On top of that, Dennard’s scaling [19] asserts that as transistors get smaller, the power density stays nearly the same, deviated over the past 15 years. In order to tackle this problem, Intel recently came up with a new generation of transistors, MESO (Magneto-Electric Spin-Orbit) transistor [20, 21]. MESO transistors rely on writing of magnetic information through magneto-electric coupling [21–24], and reading it by spin-charge conversion [25–27]. Oxide 2DEGs are promising candidates for the spin-charge conversion mechanism as their spin-charge conversion efficiency is large. Recently highly efficient and gate voltage tunable spin-to-charge conversion through Rashba coupling has been reported at LAO/STO heterostructures [28, 29] and other STO-based heterostructures [30], which further enhances the importance of these interfaces.

These recent developments with LAO/STO heterostructures and other STO-based heterostructures demand further investigation of the properties of these interfaces, especially in nanoscale dimensions. We have developed an industrial-compatible nanopatterning technique in our group and used it to fabricate structures down to 100 nm. The main goal of this work is to understand the fundamental difference in transport properties of LAO/STO nanostructures compared to large area structures and the significance of domain walls on their transport properties. We conducted magnetoresistance (MR) measurements on the nanostructures and revealed a striking impact of the orientation of domain walls on MR behaviour, especially true for nanostructures. We also conducted side and back gating experiments, which are crucial for implementing this interface in practical applications, observed persistent changes induced by gate voltages and provided a simple model to explain the observation.

## Thesis Organisation

This thesis is comprised of five chapters. In the first chapter, we present the general overview of the  $LaAlO_3/SrTiO_3$  (LAO/STO) interface and the background theoretical knowledge necessary to explain the experimental observations. We start by discussing the important bulk properties of both LAO and STO, followed by discussing the formation of a highly mobile conducting interfacial 2DEG and some of the intriguing properties of this 2DEG. We also discuss the main mechanisms that explain the formation of the 2DEG,

including polar discontinuity at the interface, formation of oxygen vacancies in the STO substrate, and cation intermixing. In the last section, we discuss in detail the localisation effects and how they affect the transport properties of the LAO/STO interface.

Chapter two introduces the phase transition in STO and how it affects the charge conduction of the interface. This is very crucial background information required to understand the result of the experimental work carried out throughout this thesis. A cubic to tetragonal phase transition occurring around 105 K in STO leads to the formation of domains and domain walls in STO, which becomes the major charge conduction path at the interface. The significance of domain wall conduction becomes more dominant when the lateral size of the structure becomes smaller.

In the third chapter, we explain the steps involved in the fabrication of large-area structures as well as nanostructures. Starting with the preparation of STO substrates, followed by using Pulsed laser deposition (PLD) and in-situ monitoring of the layer thickness up to unit cell level and using photo-lithography and electron beam lithography techniques for patterning and finishing off by using reactive ion etching (RIE) process for successful fabrication of micron and nanoscale devices. Some nanostructures are patterned using the Aluminium oxide ( $Al_2O_3$ ) mask method. In the final section of this chapter, the electronic transport measurement set-up that is used during the course of this work is explained and the electrical characterisation of the interface is presented.

The fourth chapter deals with the investigations of magnetoresistance (MR) in LAO/STO. We have designed a series of experiments to systematically study the role of domain walls in MR measurement in both nanostructures and large-area structures. MR measurements were carried out in out-of-plane magnetic field configuration with the current carrying segments oriented at different respective angles to the edge of the STO substrate. We have observed clear anisotropy in MR with orientation for nanostructures, whereas large-area structures show no deviation. The role of transition temperature on the MR behaviour was also studied, and results are presented, which reveal how the phase transition alters the property of the interface. Back-gating experiments were also carried out to confirm the role of domain walls.

In the final chapter, the results from the side and back-gating experiments are discussed. Side gating act as a local back gate where the field lines reach the interface from below through the STO substrate. The advantage of the side gate over the back gate is that only a few volts are required to significantly modulate the carrier density of the LAO/STO interface. Domain walls are not only mobile under the application of an electric field, but also ferroelectricity is induced in the domain walls when an electric

field above the threshold value is applied. As a result, the domain wall distribution and properties change significantly with the application of gate voltage. These changes are persistent even after the gate voltage is swept back to zero volts, as we demonstrate from our experiments. We have proposed a simple model to explain our observation with side gating experiments.

In the final section of this thesis, we summarise all the important results and outcomes of all the work carried out throughout the course of this thesis. We also stated some questions that need to be answered before the practical implementation of these complex oxides, which can be considered as the scope for future study.

# 1

## Overview of the $\text{LaAlO}_3/\text{SrTiO}_3$ interface and background theory

When Nobel laureate Herbert Kroemer quoted "the interface is the device" [31], he was referring to the remarkable potential of thin film semiconductor-based devices. But this can be true for complex oxide-based devices also which exhibit remarkable properties such as magnetism, superconductivity, ionic conduction, ferroelectricity and so on. Owing to these multitudes of properties, complex oxides are finding applications in many areas like batteries, fuel cells, information storage and more.

The highly mobile conducting two-dimensional electron gas (2DEG) at the interface between the two band gap insulators lanthanum aluminate ( $\text{LaAlO}_3$ ) and strontium titanate ( $\text{SrTiO}_3$ ), which is commonly referred to as LAO/STO interface is the heart of this thesis. Before the exploration of this interface, it is important to understand the bulk properties of the constituent materials, how the 2DEG is formed and the properties exhibited by this interface. This introductory chapter deals with the bulk properties of the perovskite materials  $\text{LaAlO}_3$  and  $\text{SrTiO}_3$  and additional key information which is relevant to this thesis including models for explaining the origin of the conducting interface.

### 1.1 $\text{ABO}_3$ Perovskites

Perovskite is a calcium titanium oxide mineral composed of  $\text{CaTiO}_3$  which was discovered by Gustav Rose in 1839. Later the name is transferred to the class of compounds having the same crystal structure as  $\text{CaTiO}_3$  ( $\text{ABX}_3$ ), where A is a large cation, B is a

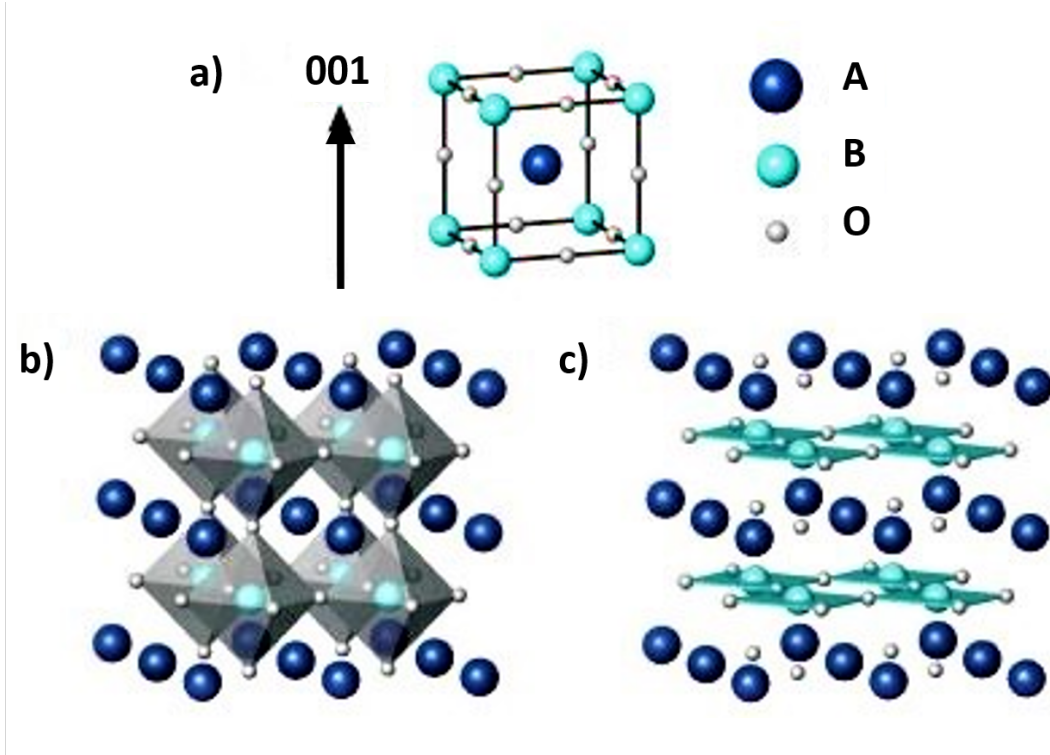


FIGURE 1.1: Schematic illustration of the perovskite  $ABO_3$  structure. (a) The cubic unit cell with an A ion occupying the centre, B ions at the corners and O ions in the middle of the edges. (b)  $BO_6$  octahedra network of the perovskite structure is highlighted. (c)  $ABO_3$  structure of the perovskite can also be viewed as an alternating stacking of AO and  $BO_2$  layers. Adapted from [35]

small cation and X is an anion usually halogen or oxygen. The term “perovskite” was assigned in honour of the name of Russian mineralogist Court Lev Aleksevich von Perovski (1792–1856).  $ABX_3$  compounds exist in diverse crystal structures like cubic, orthorhombic, tetragonal, rhombohedral, and monoclinic due to lattice distortion [32]. Structural phase transitions are also observed in these classes of compounds as a function of external parameters like temperature, pressure etc. Depending on the choice of A and B ions, the physical and chemical properties of the perovskites can be significantly different [33]. Perovskites exhibit many diverse behaviours like insulating, semiconducting, metallic, superconducting, magnetic, piezoelectric, ferroelectric, and multiferroic [34], which makes them a very interesting class of compounds for research.

The ideal cubic unit cell of perovskite  $ABO_3$  is as shown in the Figure 1.1 a. The A cation occupies the body centre position which is caged in  $BO_6$  octahedra. B cations are at the corner of the cube and the oxygen atoms are located in the middle of the edge of the cube. Generally, the A cation can be a transition metal or a third group element, while

B is an alkaline, alkaline-earth metal or rare earth. The stability of the  $\text{BO}_6$  octahedra is guaranteed by covalent bonding between the B atom and the oxygen atom. For this work, the most instructive description of the perovskite structure is the one shown in [Figure 1.1 c](#), where along the (001) direction a perovskite can be visualised as stacking of alternating  $\text{AO}$  and  $\text{BO}_2$  layers. This layer-by-layer structuring of perovskites will be utilised later in this chapter to provide a better understanding of the formation of 2DEG at the interface.

Both the constituting compounds of the heterostructure investigated in this thesis,  $\text{SrTiO}_3$  and  $\text{LaAlO}_3$  which are presented next, belong to the class of perovskites.

## 1.2 $\text{SrTiO}_3$

STO is a complex oxide with a perovskite structure and one of the most versatile material complex oxide family [\[36\]](#). Due to its similarities in structure and lattice parameters, STO is used as a substrate material for the growth of many different materials. Additionally, STO is chemically inert and does not react with the materials deposited on it which further favours its use as a universal substrate. At room temperature, STO has a cubic perovskite structure with a lattice constant of 0.3905 nm [\[37\]](#). The cubic lattice structure consists of a titanium atom at the centre of the cube and an oxygen atom present at every wall of the cube forming a cage around the Ti atom, and small strontium atoms occupying the corners of the cube [\[38\]](#) as shown in [Figure 1.2 a](#). The three most studied crystallographic orientations of STO are (001) (non-polar and most stable), (110) and (111) (both polar). In the (001) crystallographic direction STO can be viewed as an alternating stack of  $\text{SrO}$  and  $\text{TiO}_2$  layers. This means that two different types of surface termination are possible. The surface termination of STO can be controlled by different chemical methods. Single  $\text{TiO}_2$  termination can be achieved by treatment with buffered Hydrofluoric acid (BHF) [\[39\]](#) followed by annealing in an oxygen atmosphere at a high temperature. This is very crucial for the formation of 2DEG at the LAO/STO interface as we discuss later.

In its stoichiometric form, STO has a relatively large, indirect band gap of 3.25 eV [\[37\]](#). So it can be viewed either as a band-gap insulator or semiconductor. The cubic crystal field lifts the degeneracy of empty Ti 3d orbital (conduction band), resulting in splitting them into  $t_{2g}$  triplets and  $e_g$  doublets [\[40\]](#) ([Figure 1.2 b](#)). The  $t_{2g}$  triplets lies approximately 2eV below  $e_g$  doublets, which results in a conduction band minimum consisting of  $t_{2g}$  states. STO can be made conducting by doping. Bulk conductivity in STO is reported at carrier densities as low as  $\sim 8.5 \times 10^{15} \text{ cm}^{-3}$  [\[41\]](#). Electron doping can be achieved by the

substitution of Sr with La or Ti with Nb [42, 43] or by oxygen removal which can induce even a metallic state. At higher carrier densities in the range of  $10^{19} - 10^{21} \text{ cm}^{-3}$ , even superconductivity has been reported with critical temperatures  $< 300 \text{ mK}$  [44–46].

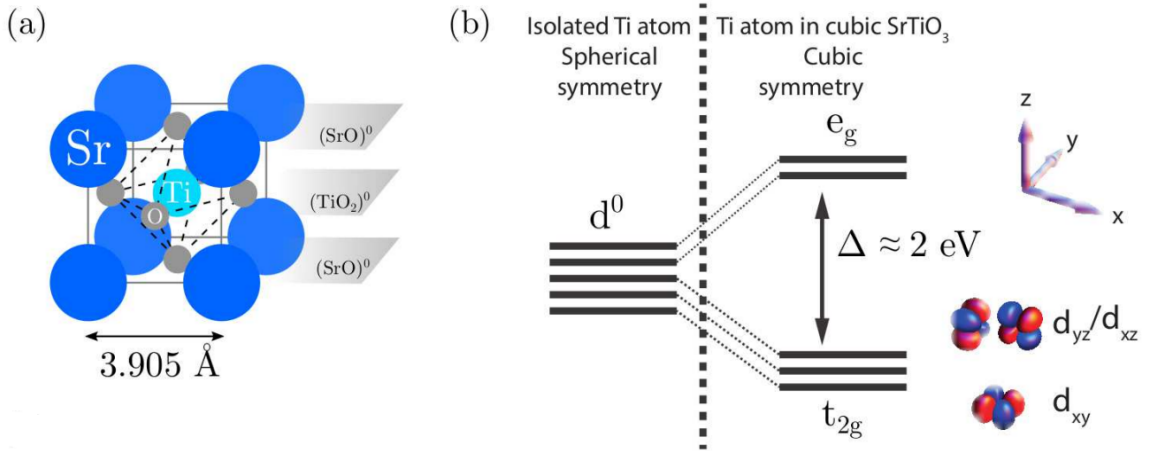


FIGURE 1.2: This figure represents the lattice structure of  $\text{SrTiO}_3$  and the band diagram. (a) STO has a cubic lattice structure with a Ti atom at the centre of the cube with oxygen atoms forming a cage around Ti. Sr atoms are present at the corner of the cube. an alternating layer of SrO and TiO<sub>2</sub> is formed in the 001 direction. (b) Energy levels of 3d orbitals of Ti atom. Band splitting of the degenerate  $e_g$  doublets and  $t_{2g}$  triplets states. Adapted from [47]

STO possesses two types of structural distortions which are driven by stress or temperature changes, ferroelectric type (FE) displacement or antiferrodistortive (AFD) rotation. At around 105 K, STO undergoes an antiferrodistortive phase transition from cubic to tetragonal crystal structure [48]. This phase transition is characterised by the rotation of oxygen octahedra and elongation of the  $c$  parameter. As a result of the phase transition, new domains and domain walls are formed which play a key role in the transport as we discuss in later chapters.

STO is non-magnetic and its magnetic susceptibility is partly diamagnetic and partly (Van Vleck) paramagnetic. Both parts are approximately temperature-independent [49, 50].

STO exhibits exceptional dielectric properties. STO is one of the few materials that exhibit quantum paraelectricity and remains paraelectric down to 0.3K [51]. The presence of quantum fluctuations prevents the formation of ferroelectric ordering at low temperatures. The dielectric constant of STO increases with decreasing temperature and its value ranges from several hundred at room temperature to up to 25000 at 4 K in bulk samples [52–54] and up to 4000 in thin films [55, 56] has been reported. Regardless of this high



dielectric constant, its practical applications such as for energy storage in high- $\kappa$  capacitors are limited since the dielectric constant is considerably reduced by the application of electric field [55]. Ferroelectricity can be induced in STO by slight alterations of the crystal lattice which could be due to epitaxial strain [57], non-stoichiometry [58], doping [59], large electric fields [60] or even by an oxygen isotope <sup>18</sup>O [61].

The high dielectric constant makes STO a good candidate for use as a gate dielectric in field effect experiments. This property has been completely utilised in designing back and side gating experiments in this work (see [chapter 5](#))

### **1.3 LaAlO<sub>3</sub>**

LaAlO<sub>3</sub> (LAO) is a perovskite which is the second building block of the LAO/STO interface with a rhombohedral structure. The lattice parameter of LAO is 0.379 nm [62] and it is composed of polar AlO<sub>2</sub><sup>-</sup> and LaO<sup>+</sup> stacked layers. Similar to STO, LAO also has a good lattice match with many oxide materials and has been thoroughly investigated as a substrate material [63].

Structurally LAO undergoes a phase transition from rhombohedral to a cubic structure at a high temperature around  $T \approx 813$  K [64]. In the lower temperature range, the crystal structure differs from the cubic structure only by a small antiphase rotation of AlO<sub>6</sub> octahedra, which can be described as pseudocubic. This similarity in lattice parameter and comparable thermal expansion coefficient facilitates the epitaxial growth of LAO on STO.

LAO is a band insulator with a band gap of 5.6 eV [65], separating filled O 2*p* valence bands and empty Al 3*s* – 3*p* and La 5*d* conduction bands. Unlike in STO, none of the cations can access the mixed valence state in LAO, making it an extremely robust insulator. Like STO, LAO belongs to the class of high- $\kappa$  oxide materials with a dielectric constant of about 25 for temperatures between 300 K and 4 K and finds its application as a gate dielectric in silicon-based [66] and LAO/STO field effect devices [67–70].

### **1.4 The LaAlO<sub>3</sub>/SrTiO<sub>3</sub> interface**

Following their discovery of charge transfer in unit cell precise LaTiO<sub>3</sub>/SrTiO<sub>3</sub> heterostructures [71, 72], in 2004 Akira Ohtomo and Harold Y. Hwang conducted an experiment to form a field effect configuration with an undoped STO channel and epitaxially

grown LAO as a gate dielectric. To their surprise, Ohtomo and Hwang discovered that they did not need to apply any voltage or even need a gate electrode to turn their LAO-STO field effect device conducting. It occurs as if the electric field is somehow built into the LAO thin film. So a conducting interface was discovered at the interface between two band insulators,  $\text{LaAlO}_3$  and  $\text{TiO}_2$ -terminated  $\text{SrTiO}_3$  [9].

They analysed the interface between LAO and STO in great detail. Two different terminations of STO ( $\text{TiO}_2$  and  $\text{SrO}$ ) were used for the epitaxial growth of LAO thin film using pulsed layer deposition (PLD) at  $800^\circ\text{C}$ . At first, LAO is grown epitaxially on 001 oriented STO substrate with  $\text{TiO}_2$  termination. Later, an additional monolayer of  $\text{SrO}$  was inserted into  $\text{TiO}_2$ -terminated STO before the growth of LAO. These two configuration result in the formation of  $\text{TiO}_2/\text{LaO}$  (Figure 1.3a) and  $\text{SrO}/\text{AlO}_2$  (Figure 1.3b) stacking. Surprisingly, the highly conducting interface was formed only with  $\text{TiO}_2/\text{LaO}$  stacking while  $\text{SrO}/\text{AlO}_2$  was insulating. This observation was quite shocking and demands further in-depth investigation of the interface to understand the underlying mechanism behind the conduction of the interface. The conductivity of the interface depends on the stacking sequence and the electronic properties differ from conducting to insulating.

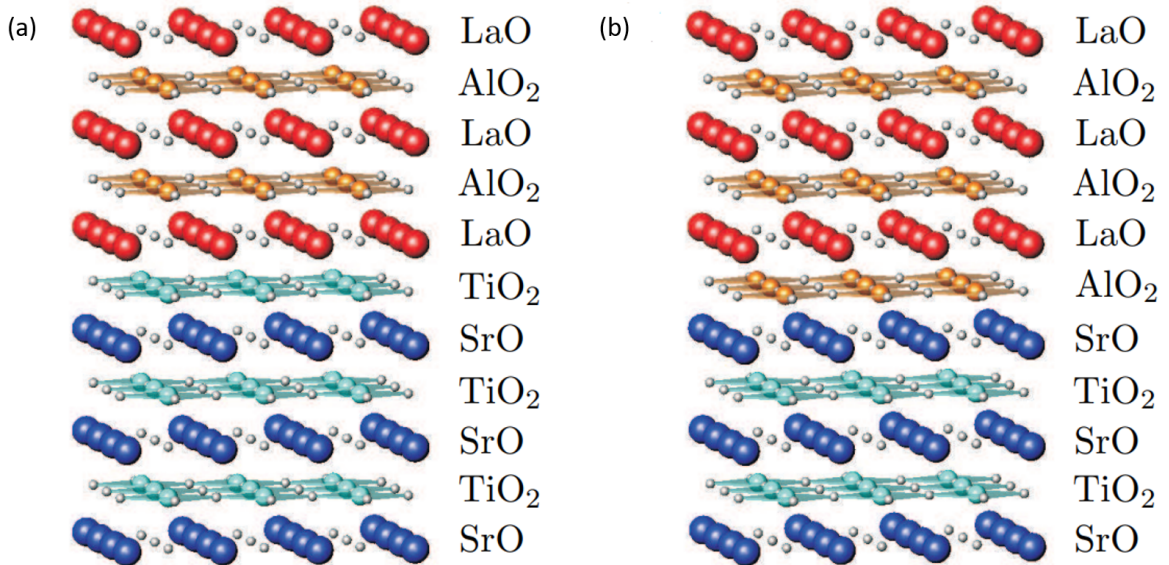


FIGURE 1.3: Schematic representation of the two possible stackings of the  $\text{LaAlO}_3/\text{SrTiO}_3$  interface. In (a), at the interface we have  $\text{LaO}$  layer on top of  $\text{TiO}_2$  terminated  $\text{SrTiO}_3$  surface and in (b) we have  $\text{AlO}_2$  on top of  $\text{SrO}$  terminated  $\text{SrTiO}_3$  surface. It has been experimentally verified that only the stacking of layer as in (a) yields a conducting interface. Adapted from [35]

In order to provide an explanation of this special situation at the interface, we must understand the difference in the stacking layers and their valence states ( $\text{Sr}^{2+}$ ,  $\text{Ti}^{4+}$ ,  $\text{La}^{3+}$ ,

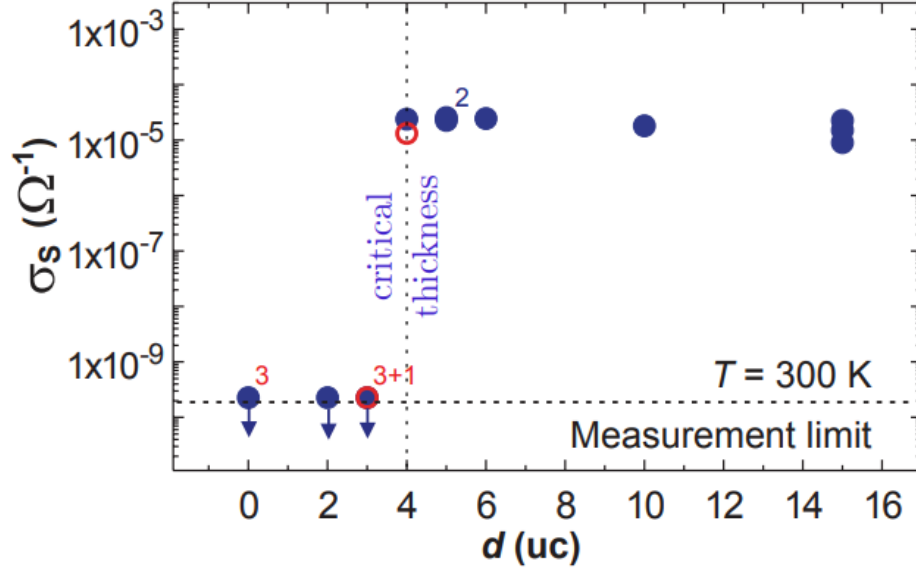


FIGURE 1.4: This graph shows the conductivity of the LAO/STO interface w.r.t the thickness of the LAO layer. LAO layer thickness up to 3 u.c did not induce conductivity at the interface. Finite conductivity is exhibited only at a critical thickness of 4 u.c of LAO layers. However, the interface with 3 u.c of the LAO layer can be made conducting with the application of gate voltage or by the conducting AFM method of Levy [75]. Adapted from [15]

$\text{Al}^{3+}, \text{O}^{2-}$ ). The stacking layers of STO,  $(\text{SrO})^0$  and  $(\text{TiO}_2)^0$  are charged neutral layers whereas LAO consists of  $(\text{LaO})^+$  and  $(\text{AlO}_2)^-$  charged layers. This makes the interface between LAO and STO special since there are adjoining charge-neutral and charged layers. The consequences of such an alternate sequence of layers were first discussed by Baraff et al. [73] and Harrison et al. [74] for Ge/GaAs semiconductor heterojunctions. In 2006, an important experimental observation was made by Stefan Thiel [15] and others that the critical thickness of LAO is very crucial for interface conductivity. They observed interfacial conductivity in samples with LAO thickness  $>4$  unit cells, otherwise, the interface remains insulating (Figure 1.4). However, with 3 u.c LAO thickness, the interface conductivity can be induced with the application of gate voltage. To understand the origin of the interfacial conductivity, various models have been proposed such as the polar discontinuity at the interface, formation of oxygen vacancies in the STO substrate and cation intermixing at the interface.

## 1.5 Interfacial q2DEG formation mechanisms

The underlying mechanism behind the formation of a highly conducting electron gas at the interface between LAO and STO is still under debate. Different models have been proposed to understand the origin of interfacial conductivity and other intriguing properties of the interface (which will be discussed later). In this section, we will discuss some of the existing models.

### 1.5.1 Polar catastrophe

The polar catastrophe model was initially proposed by Ohtomo and Hwang [9]. In the (001) plane STO consists of alternating stacks of  $(\text{SrO})^0$  and  $(\text{TiO}_2)^0$  which are both electrically neutral but LAO consists of alternating stacks of charged  $(\text{LaO})^+$  and  $(\text{AlO}_2)^-$  layers as shown in Figure 1.5 a, c. As a result, when LAO is grown on top of STO, an abrupt polar discontinuity occurs at the interface and electric potential builds up in LAO which increases with an increasing thickness (Figure 1.5 a). In order to avoid the so-called polar catastrophe (or polar discontinuity) and to eliminate the divergence in electrostatic potential, the redistribution of electrons happens within the layers. The mixed valence state available for the atoms facilitates the charge distribution at the LAO/STO [76] interface by transferring electrons as shown in Figure 1.5 b. Half an electron per unit cell is transferred from the  $\text{LaO}$  layer towards the STO surface. During this charge redistribution, the net polarity of the system remains neutral, and only the Ti atoms at the interface become  $\text{Ti}^{3.5+}$ . This charge distribution eliminates the diverging electrostatic potential. This charge transfer results in the addition of electrons at the  $\text{LaO}/\text{TiO}_2$  interface resulting in n-type conductivity. Likewise, electrons will be removed from  $\text{SrO}/\text{AlO}_2$  interface resulting in p-type conductivity (Figure 1.5 d). However such p-type interfaces are found to be insulating [9, 77].

Several experimental findings have validated the polar catastrophe model. An explanation of the significance of the critical thickness of the LAO layer has been provided as a result of electrostatic buildup and band tilting in LAO. [78–80] At a critical thickness of 4 u.c LAO valence band maximum reaches the conduction band minimum of STO allowing the transfer of electrons from LAO to the quantum well. On the other hand, many studies raised inconsistencies regarding the polar catastrophe scenario [81–84]. [81] showed that no tilting of bands happens in the LAO film. The energy offsets found below and above the critical thickness were much smaller than what was initially predicted [82]. The presence

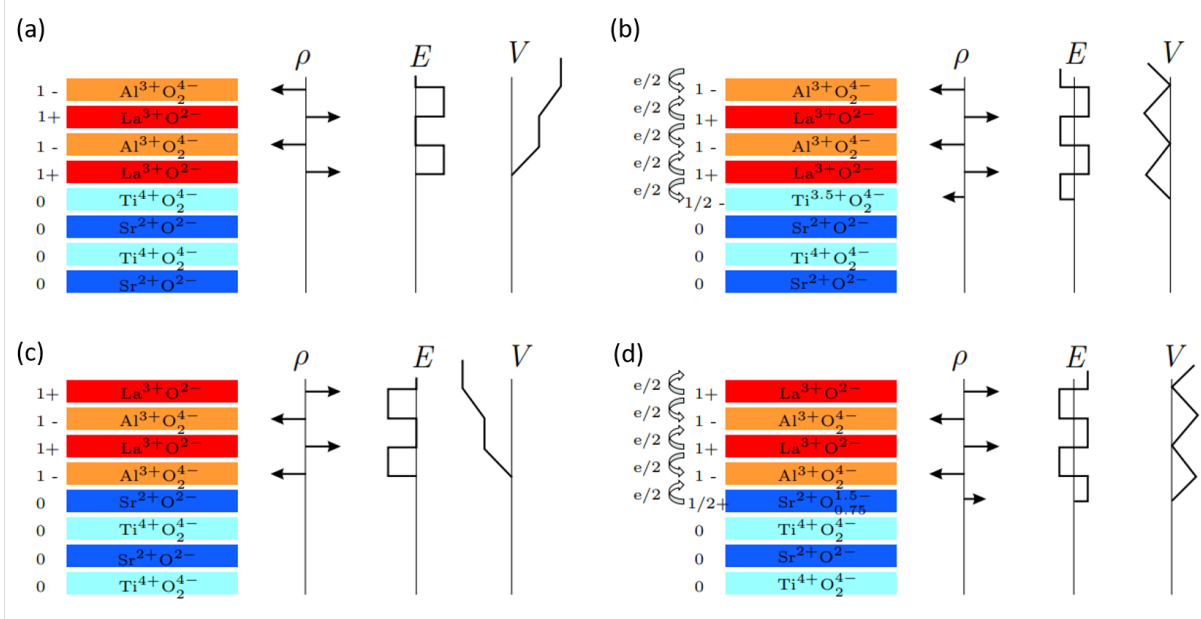


FIGURE 1.5: Schematic illustration of electronic reconstruction happening at the LAO/STO interface. Here  $\rho$  indicates the net charge of the layers,  $E$  is the electric field and  $V$  is the potential generated by the electric field. (a) In the absence of electronic reconstruction, the n-type interface ( $\text{LaO}/\text{TiO}_2$ ) leads to a diverging potential  $V$  due to polar discontinuity. (b) When half an electron is transferred from the LAO layers to the  $\text{TiO}_2$  layer, the potential stays finite. (c) and (d) shows a similar mechanism happening at the p-type interface ( $\text{SrO}/\text{AlO}_2$ ) which suppresses the diverging potential. In this case, half an electron is removed from the SrO layer. Adapted from [76]

of  $\text{Ti}^{3+}$  was observed below the critical thickness and has also been reported signalling the charge transfer below critical thickness [81, 83].

Even though the polar catastrophe model provides a good explanation for how the conductivity is generated at the n-type interface, it fails to explain why the p-type interface is insulating.

## 1.5.2 Formation of oxygen vacancies

Oxygen vacancies are intrinsic electron donors in STO that can be generated by annealing in a vacuum or hydrogen atmosphere at high-temperature [85]. Higher carrier concentrations and mobility have been reported in conductive LAO/STO interfaces. Oxygen vacancies that are generated during the high-temperature deposition of LAO are one of the sources of conductivity at the interface [10, 86, 87]. Use of conductive AFM tip at 3 u.c of insulating LAO/STO heterostructure generates oxygen vacancies and adds electrons to the STO conduction band resulting in interfacial conductivity [75].

The role of background oxygen pressure during the pulsed laser deposition of LAO on STO plays a vital role in determining the properties of the interface [10, 86–89]. Depending on the background pressure, certain concentration of oxygen vacancies can be generated which alters the substrate conductivity. In the case of LAO/STO, the oxygen affinity of LAO is higher than that of STO [90]. This results in the STO oxygen diffusing to LAO and a reduction of STO substrate is attained. Thus semiconducting or even metallic behaviour is induced in STO.

The role of background oxygen pressure on the properties of the LAO/STO interface has been extensively studied by Brinkman et al. [10]. For the sample deposited at lower oxygen pressure ( $< 10^{-3}$  mbar), transport properties are mainly governed by reduced STO substrate. This issue was resolved, either by depositing the LAO film in high oxygen pressure or through post-deposition annealing to overcome these oxygen vacancies. Wang et al. [91] showed that the interface grown at oxygen background pressure lower than  $10^{-3}$  mbar exhibits 3-D conductivity and magnetoresistance of an order of magnitude larger was observed in low  $P_{O_2}$  samples compared to those of high  $P_{O_2}$  samples. However, high deposition pressure does not automatically rule out the presence of oxygen vacancies, but their influence on transport properties can be minimised. In our case, they are not dominating the transport properties of the LAO/STO interface.

### 1.5.3 Cation interdiffusion

Another possible mechanism to explain the formation of the conductivity at the interface can be chemical reconstruction, i.e. creation of an inter-diffused interface. In GaAs/Ge(001) heterostructure, at the polar/non-polar interface, atomic reconstruction has been observed in which the intermixing species compensated for the build-up of electric field [74]. Such effect has been observed in  $\text{LaNiO}_3/\text{LaAlO}_3$  superlattices [92].

The reduction of dipole energy is the driving force for cation intermixing. Interdiffusion of La, Sr, Al and Ti (Figure 1.6 a) was observed in the vicinity of the interface through x-ray diffraction (SXRD) [93], medium-energy ion spectroscopy (MEIS) [94] and electron energy loss spectroscopy (EELS) [76]. A metallic layer of  $\text{La}_{1-x}\text{Sr}_x\text{TiO}_3$  was formed at the interface, on the STO side, which could possibly be the origin of interface conductivity. Structural analysis of LAO/STO interface by coherent Bragg rod analysis [93] revealed the existence of graded intermixing over 3 unit cells. Nagakawa et al. [76] using EELS reported that the n-type interface is rougher than the p-type interface. Chen et al. [95]

presented in their theoretical work that La/Sr intermixing is favourable only for the n-type interface, which could be a contributing factor to the absence of conductivity at the p-type interface.

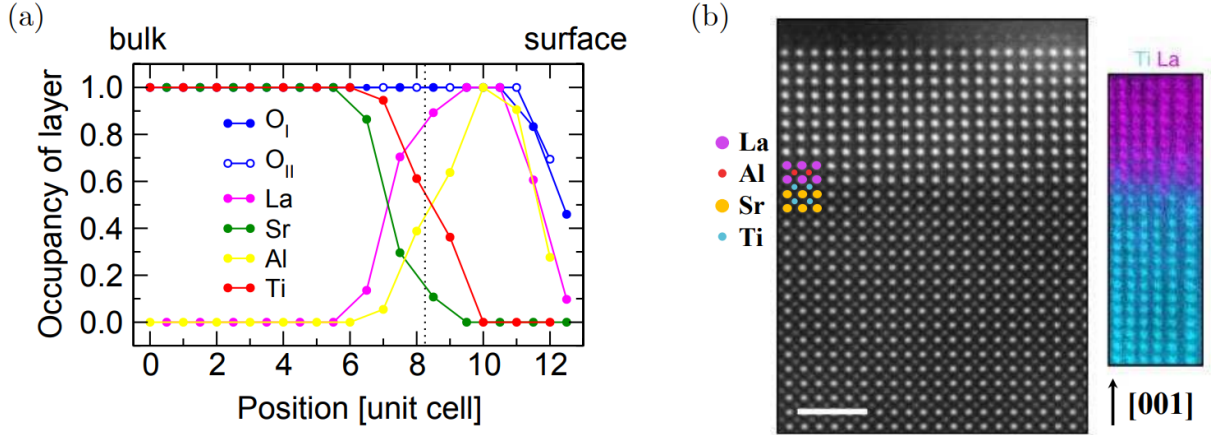


FIGURE 1.6: (a) Shows the expected layer occupancy of Ti, Al, Sr, La and O atoms as a function of their position within  $\text{LaAlO}_3/\text{SrTiO}_3$  interface. Adapted from [93]. (b) STEM and EELS of conducting MBE grown  $\text{LaAlO}_3/\text{SrTiO}_3$  samples. The left-hand side shows the high-angle annular dark-field STEM image which indicates the crystalline epitaxial growth. The right-hand side image shows the Ti and La concentration map which reveals only a small trace of interdiffusion. Adapted from [96]

But on the contrary, Warusawithana et al. [96] grew LAO/STO samples using molecular beam epitaxy (MBE) and found no evidence of interdiffusion at the interface after analysis with scanning tunnelling electron microscopy (STEM) and EELS (Figure 1.6 b). The samples were still conducting even though no cation interdiffusion occurs which raises the question about the credibility of the cation intermixing scenario. As we discussed at the beginning, in the case of GaAs/Ge heterostructure, atomic reconstruction is the most favourable mechanism due to the fixed charge of each ion. However, the mixed valence state of Ti atoms allows electronic reconstruction, which could nullify the effect of interdiffusion in the case of LAO/STO heterostructure compared to other fixed valence systems.

In summary, a lot of studies have been conducted to understand the origin of conductivity at the LAO/STO interface and many possible mechanisms have been proposed. Despite all these proposed mechanisms, the origin of conductivity is not clearly understood. The mechanism behind the origin of conductivity could be more complex and may require more than one mechanisms to explain the properties of the interface. Growth parameters during the deposition of LAO thin films also alter the property of the interface to a great extent.

## **1.6 Other properties of 2DEG**

In this following section, we will discuss some intriguing properties of the 2DEG which make it very unique and interesting for investigation.

### **1.6.1 Electronic properties**

The confinement of the electron gas at the (001) interface has important implications for the electronic structure of the 2DEG: on the one hand, it creates a subband structure and determines the orbital order of the various subbands, and on the other hand, it is believed that it underlies the strong spin-orbit interaction observed in the system. Transport properties of the interface at low temperatures are predominantly dominated by Weak localisation (WL) effects, to which every 2-D system is susceptible. The Rashba spin-orbit interaction in the LAO/STO system can be dramatically tuned by the application of gate voltage. Several interpretations have been proposed to explain the gate voltage-dependent increase in spin-orbit interaction which include the field-induced change in confinement potential and variation of carrier density and the enhanced spin-orbit interaction since the Fermi level is close to the crossing point between electronic bands of a different character.

### **1.6.2 Spin-charge interconversion**

It has been demonstrated that it is possible to inject electrical spin from a ferromagnet (FM) into the LAO/STO interface by measuring the Hanle effect with the magnetic field applied perpendicular or parallel to the sample plane [29]. This discovery paves the way toward a new era in oxide spintronics, beyond perpendicular devices such as tunnel junctions or spin filters. Traditionally, polarized electrons from a ferromagnetic (FM) electrode are injected into the 2DEG channel through a tunnel contact in a spin injection device. The resulting imbalance of spin population at the channel side, referred to as spin accumulation, generates a finite extra voltage at the FM/2-DEG contact (Figure 1.7 a). In a three-point measurement technique, it may be possible to determine the contribution of this spin accumulation-generated voltage to the overall voltage measured between the top electrode and an Ohmic reference contact by measuring the electrical Hanle effect. Traditionally, the effect is detected by applying an external magnetic field perpendicular to the magnetization of the FM injector in order to generate an incoherent precession of the injected electronic spins, which suppresses spin accumulation and results in negative MR. Conversely, by introducing a magnetic field parallel to the FM magnetization, it



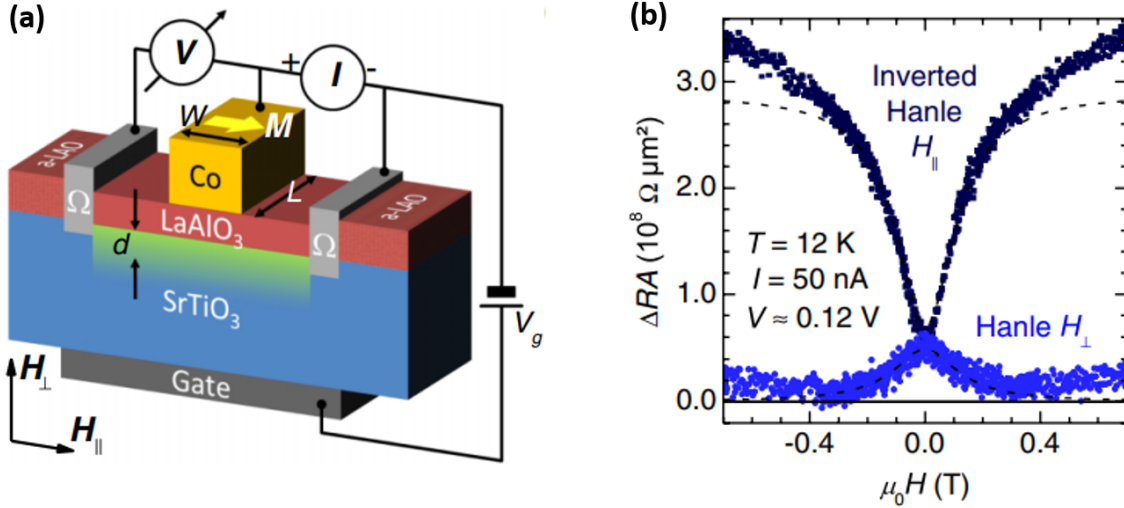


FIGURE 1.7: (a) Co/LAO/STO junction used for the Hanle measurements with in-plane and out-of-plane magnetic fields. Co is used as a ferromagnetic material to inject spin-polarised electrons into the 2DEG channel. (b) Shows the MR as a function of out-of-plane magnetic field (Hanle effect) and in-plane field (inverse Hanle effect) at 12 K. The solid lines represent the fits with a Lorentzian plus a parabolic background while the dashed lines correspond to the Lorentzian contribution due to the Hanle effect without parabolic background. Adapted from [29]

is possible to probe the existence of a local random magnetic field that exists within the 2-DEG or close to the FM/2-DEG contact which is responsible for the partial spin depolarization at zero external fields. As the applied magnetic field increases, the spin depolarization caused by the random field is gradually inhibited, restoring maximum spin accumulation. This results in a positive magnetoresistance or inverted Hanle effect, with a width corresponding to the random field's amplitude (Figure 1.7 b).

Another experiment carried out by Lesne and group [28] found that the LAO/STO interface possesses very highly efficient and tunable spin-to-charge conversion through Rashba spin-orbit coupling. The spin-orbit interaction couples the electrons' motion to their spin. Due to the presence of spin-orbit interaction, charge current flowing through a material can be converted to spin current via spin-orbit coupling, which is known as spin Hall effect (SHE) and vice versa (spin to charge current) known as inverse spin hall effect (ISHE). The spin hall effect and Inverse spin hall effect are both bulk properties and their interconversion efficiency does not account for the interfacial and low dimensional effects. Rashba-Edelstein Effect is an intrinsic charge-to-spin conversion mechanism, which is an interface-driven spin-orbit mechanism predicted in 1990 by V.M. Edelstein [97]. In a

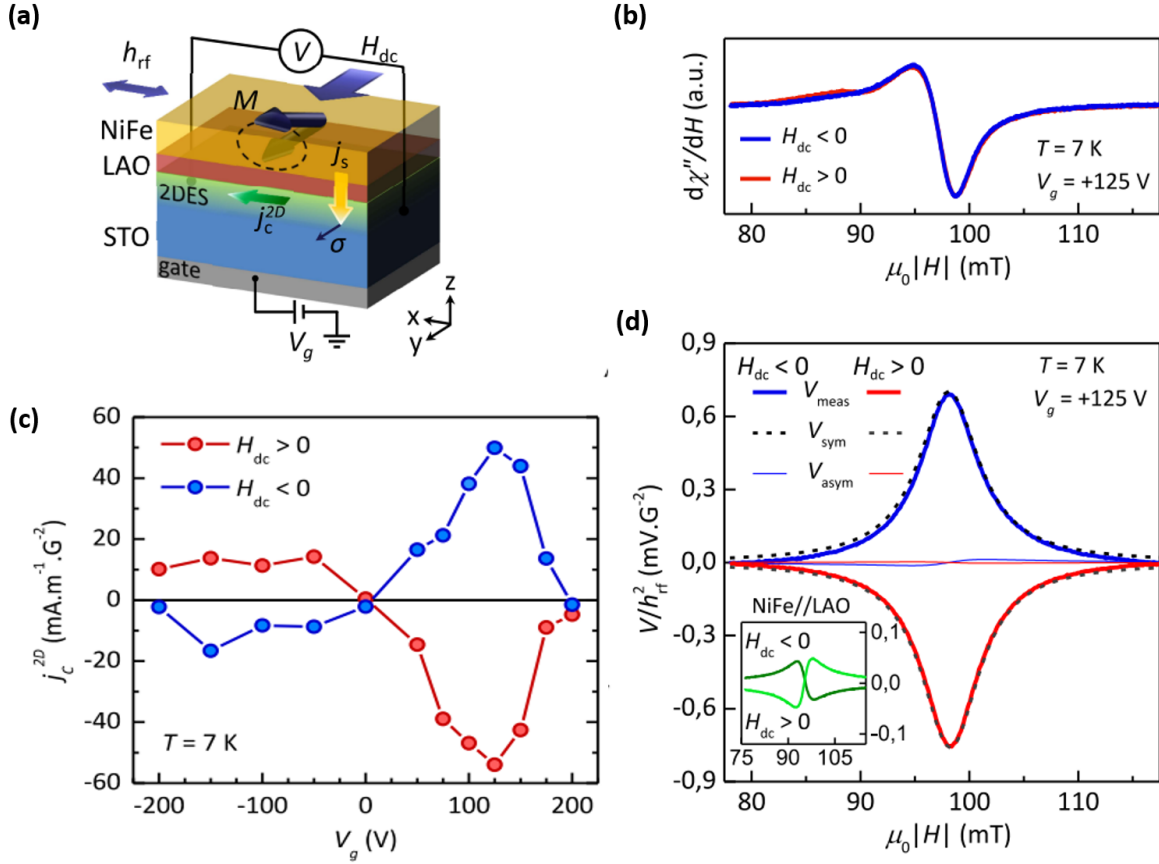


FIGURE 1.8: (a) Representation of spin pumping experimental configuration of NiFe/LAO/STO. (b) FMR signal at negative and positive external magnetic fields, at a gate voltage of  $+125$  V. (c) shows the influence of back gate voltage on the spin-to-charge conversion efficiency. The detected charge current shows maximum amplitude at  $+125$  V gate voltage. (d) Detected voltage normalized to the square of the amplitude of the rf field (thick solid lines) at negative and positive external magnetic fields at  $V_g = +125$  V. Symmetric (dotted lines) and asymmetric (thin solid lines) are also plotted. Inset: detected voltage for a NiFe//LAO reference. Adapted from [28]

Rashba 2DEG, the flow of a charge current results in the creation of a nonzero spin accumulation. This type of conversion between a 2D charge current and a spin accumulation is termed the direct Rashba-Edelstein effect. Similar to the inverse Spin Hall effect (ISHE), the inverse Rashba-Edelstein effect (IEE) describes the conversion of a spin accumulation into a 2D charge current. Using spin pumping, the spin current has been injected into the interface from NiFe ferromagnet (Figure 1.8a). Rashba spin-orbit coupling of the interface can be utilised to convert this spin current into charge current which can be measured. They observed that the spin-to-charge interconversion efficiency is much higher. Not only the spin-charge conversion efficiency is excellent, but also its amplitude and sign can be strongly modulated by gate voltage (Figure 1.8c). The emergence of the

Inverse Rashba-Edelstein effect, which is due to the presence of Rashba coupling at the LAO/STO interface, as charge-to-spin interconversion mechanisms offer a variety of novel spintronic functionalities and devices. This high spin-to-charge conversion has opened up the possibility to integrate the LAO/STO interface into MESO transistors.

### **1.6.3 Magnetism and superconductivity**

The quest for signatures of spin-polarized states has been conducted using a variety of techniques which include magnetotransport [10], torque [14] and superconducting quantum interference device (SQUID) magnetometry [98], X-ray magnetic circular dichroism (XMCD) [99], polarized neutron reflectometry [100] and magnetic force microscopy [101]. Ferromagnetic alignment of magnetic moments is found to occur at ordering temperatures in the range of 300 K for low carrier concentration samples and at around 100 K for superconducting samples. In 2007, Brinkman et al. [10] observed hysteresis in the magneto-transport measurements in LaAlO<sub>3</sub> and SrTiO<sub>3</sub> prepared under certain growth conditions. It has been generally accepted that not only the electronic properties but also the magnetic properties of the LAO/STO interface are significantly influenced by the growth parameters. In the same year, Reyren et al. [13] reported the presence of superconducting ground states below the critical temperature of 250 mK. Shortly after this discovery, Back gating experiments [102] were conducted to modulate the carrier density and also the critical temperature ( $T_c$ ). The temperature at which the resistance is reduced to 50% of its normal state value is considered an estimate of  $T_c$ .

Later the coexistence of ferromagnetism and superconductivity at the LAO/STO interface has been reported by several independent studies [14, 98, 103]. This is very unusual since ferromagnetism is considered to counteract the formation of superconducting ground states as it destroys the singlet correlations responsible for the pairing interaction. The co-existence of ferromagnetism and superconductivity can be explained by the presence of two types of carriers with different transport behaviour at the LAO/STO interface. One type of carrier which is more confined near the surface and have low mobility is associated with the polar catastrophe mechanism while the other type of carrier with higher mobility lies deep in the STO substrate which is associated with the formation of oxygen vacancies at the LAO/STO interface.

Before diving deep into the fabrication techniques and the experimental section, background theory is necessary to understand the observations.

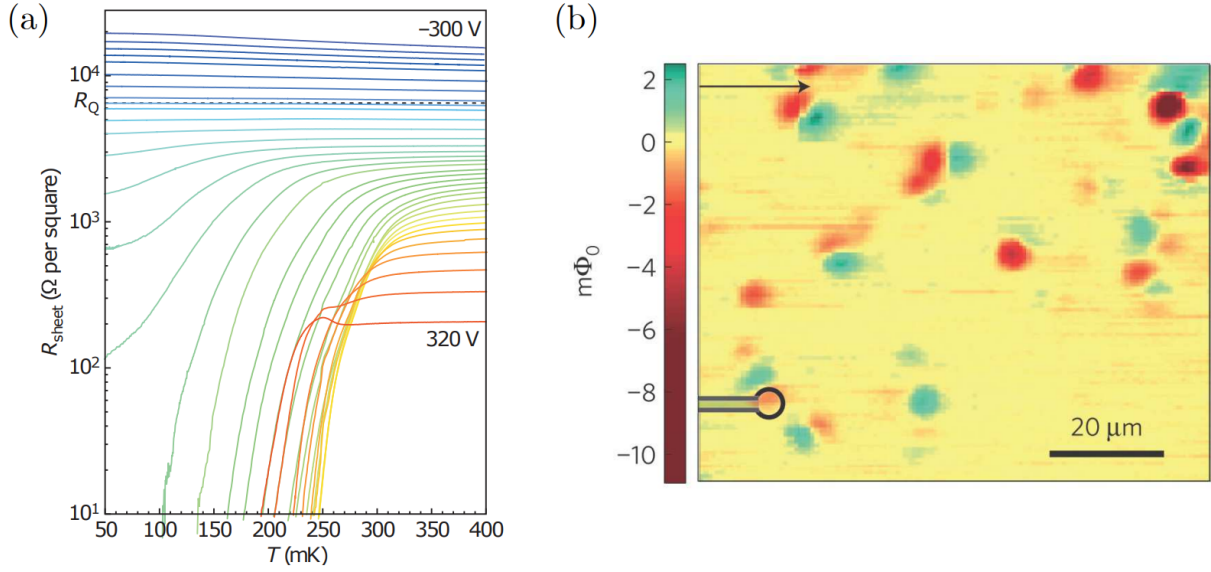


FIGURE 1.9: (a) Shows the modulation of sheet resistance ( $R_{\text{sheet}}$ ) as a function of temperature in the LAO/STO interface. With the application of negative gate voltage, the superconducting transition is suppressed ( $T_c \sim 250 \text{ mK}$ ). Adapted from [102]. Scanning SQUID microscopy image mapping the magnetic dipoles in LAO/STO samples at 20 mK. Adapted from [98].

## 1.7 Localisation effects

In order to understand the magnetoresistance behaviour of the LAO/STO system, theoretical background information on the presence of quantum interference effects like Weak localisation (WL) and weak anti-localisation (WAL) (which is due to Rashba spin-orbit coupling) is necessary. The low electron density implies a large Fermi wavelength (typically 40 nm), which is comparable to the dimensions of some nanostructures that can be fabricated today. Because the electron mean free path can be quite large (greater than  $10 \mu\text{m}$ ) [104], quantum transport is easily studied in a 2DEG due to the combination of a large Fermi wavelength and a large mean free path.

Electron transport in solids can be classified by several characteristic lengths : (i) The mean free path  $l$ , which is the average distance travelled by an electron before its momentum is altered by elastic scattering from static scattering centres. (ii) The phase coherence length  $l_\phi$ , which is the average distance over which an electron can maintain phase coherence. Inelastic scattering from electron-phonon coupling and interactions with other electrons is used to determine  $l_\phi$ . (iii) The length of the sample,  $L$ .

If  $l \gg L$  is true, electrons will be able to travel unimpeded through the sample without being scattered. This is how ballistic transport works. The diffusive transport

regime occurs when electrons suffer from scattering and diffuse through the sample in the opposite limit  $l \ll L$  [105, 106] which is referred to as semi-classical diffusion in the diffusive regime, and this part gives the Drude conductivity. Electrons will retain their phase coherence even after being scattered many times when  $l \ll l_\phi$ , which is referred to as the quantum diffusive regime. The quantum interference between time-reversed scattering loops will cause a conductivity correction in this regime. The effect of this correction in conductivity in the quantum diffusive regime can be either weak localization or weak anti-localization, which we will discuss in the following section.

## 1.8 Weak Localisation

Quantum diffusion correlations can last up to several times the phase coherence time ( $\tau_\phi$ ), whereas classical diffusion correlations vanish on the time scale of the scattering time ( $\tau$ ). At low temperatures, the phase coherence time is associated with inelastic scattering ( $\tau_i$ ) and can be much longer than the time associated with elastic scattering. The conductivity correction from quantum interference in two dimensions takes the form of a logarithmic function [107], with  $l$  and  $l_\phi$  serving as two cutoffs and can be represented by the following equation:

$$\sigma^{qi} \propto \pm \frac{e^2}{\pi h} \ln \frac{l_\phi}{l} \quad (1.1)$$

where  $e^2/\pi h$  is the conductance quantum, - corresponds to weak localisation and + corresponds to weak anti-localisation. We should note that  $l$  is determined by the elastic scattering and is independent of temperature, while  $l_\phi$  which is determined by the inelastic scattering, is a function of temperature.

The electron trajectory between two points is uniquely determined in classical treatment by minimizing the action [108]. All possible paths between the two points are feasible in the quantum case. As a result, the square of the total amplitude, which is the sum of the complex amplitudes  $A_i$  relative to each path, gives the total probability of reaching point  $r$  starting from point  $r_o$  [109, 110].

$$P = |\sum A_i|^2 = \sum |A_i|^2 + \sum_{i \neq j} (A_i * A_j) \quad (1.2)$$

The first term denotes the classical diffusion probability due to sum over the classical Feynman paths [108], whereas the second denotes quantum interference that Drude - Boltzmann's theory ignores. Because different trajectories have uncorrelated phases, this quantum effect is generally averaged to zero. Instead, the same path can be travelled in both directions when the starting and ending points are the same (backscattered trajectories) [111–113]. This closed path can be followed in two time-reversed directions (clockwise and anticlockwise): the electron waves in the two paths eventually interfere, and we can group these trajectories in the second contributions of the sum of equation 1.2. If the system is invariant for temporal inversion, the travel direction of the electrons has no effect on the probability to travel in a loop and the two loops will constructively interfere. Because the quantum probability of returning to the starting point is twice that of the classical probability, time-reversal invariance ensures that propagation around the closed loop is identical, ie  $A^+ = A^- = A$  and the coherent back-scattering probability will be  $4 |A|^2$ . This quantum correction to the probability leads to a correction in conductance as well. The magnitude of the weak localization correction to the Drude conductivity is proportional to the probability that the electron returns to the point of departure [110].

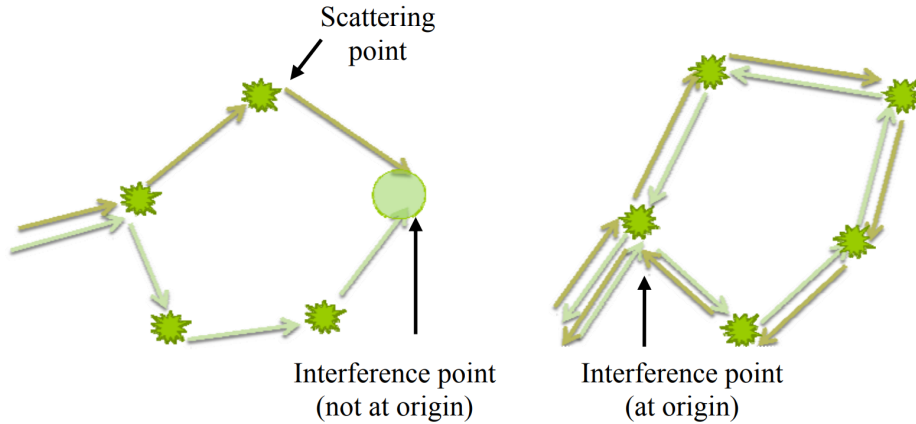


FIGURE 1.10: Schematic representation of the trajectory of an electron in a disordered system at low temperature. (a) Shows the interference of non-time reversed paths. (b) Shows the interference of time-reversed paths. In the presence of time-reversal symmetry, interference between the two time-reversed paths leads to the localisation of the electron in the loop. Adapted from [114]

Using a magnetic field to explore the weak localization correction is a very elegant method [115]. Indeed, in the presence of a magnetic field  $B$  perpendicular to the 2DEG, the two electron waves propagating in opposite directions along the same closed trajectory acquire a phase difference. Hence, the magnetic field breaks the time-reversal symmetry and destroys the constructive interference and introduces a time scale into the system.

This variation in conductivity as a function of the magnetic field, which is measured experimentally as a negative magnetoresistance, is unquestionably one of the most striking indications of weak localization.

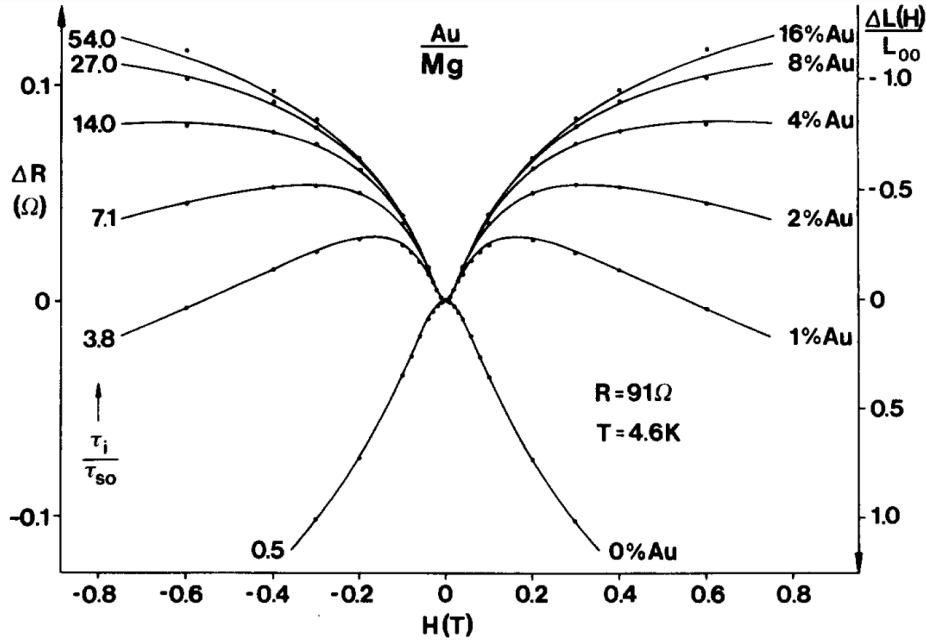


FIGURE 1.11: Magnetoresistance measurements of an Mg/Au bilayer with different thicknesses of Au. Pure Mg thin film shows negative MR due to weak localisation effects. As the thickness of the Au film is increased, the influence of spin-orbit scattering on the MR also increases and the MR changes from negative (WL) to positive (WAL). Adapted from [116]

## 1.9 Weak anti-localisation

The interfacial electrons in the LAO/STO heterostructure reside in the d-orbital. Due to the strongly anisotropic nature of the d-orbitals as well as the quantum confinement contributing to the d-subbands, complicated spin-orbit interactions (SOI) may develop within inter-d-subbands which is more complicated than s-p electron gas SOI behaviour.

The Dresselhaus SOI and the Rashba SOI are two well-known existing spin-orbit interactions. The bulk inversion asymmetry in the crystal structure results in the Dresselhaus SOI and the spatial inversion asymmetry gives the Rashba SOI. The Rashba SOI becomes more significant in low-dimensional systems due to its enhanced strength at the hetero-interface [117] and its tunability by an external electric field. Now, we will discuss the Rashba spin-orbit interaction in detail in order to understand the weak anti-localisation effect.

### 1.9.1 Rashba Spin-Orbit Interaction

Spin-orbit coupling (SOC) splits electronic energy bands in crystals without an inversion centre. For non-centrosymmetric wurtzite semiconductors, the Rashba SOC, a spin-orbit coupling linear in momentum  $\vec{p}$ , was first proposed in 1960 [118]. Bychkov and Rashba [119, 120] employed modulation-doped semiconductor heterostructures for the study of SOC in a two-dimensional electron gas (2DEG) with structural inversion asymmetry. SOC becomes odd in momentum  $\vec{p}$  in systems with inversion symmetry breaking, which simplifies to a linear dependence in the simplest two-dimensional free electron approximation. In a wide range of materials without spatial inversion, odd-in- $\vec{p}$  SOC has been confirmed. The most important aspect of any SOC is that electrons travelling in an electric field experience an effective magnetic field in their frame of motion, called the spin-orbit field, which couples to the magnetic moment of the electron even in the absence of an external magnetic field. When inversion symmetry is broken in a system, the spin-orbit field becomes odd in the electron's momentum  $\vec{p}$ , allowing for a wide range of intriguing occurrences [121].

An electron with momentum  $\vec{p}$  travelling in a magnetic field  $\vec{B}$  experiences a Lorentz force, which is perpendicular to the direction of its motion and can be represented as

$$\vec{F} = \frac{-e\vec{p} \times \vec{B}}{m} \quad (1.3)$$

and has Zeeman energy which is of the form

$$\hat{H} = \mu_B \vec{\sigma} \cdot \vec{B} \quad (1.4)$$

where  $\vec{\sigma}$  is the Pauli spin matrices vector,  $m$  and  $e$  are the mass and charge of the electron, respectively, that travels in an electric field  $\vec{E}$ ,  $\mu_B = 9.27 \times 10^{-24} \text{J/T}$  is the Bohr magnetron.

By analogy to the above situation, an electron travelling in an electric field  $\vec{E}$  experiences an effective magnetic field  $\vec{B}_{eff}$  in the rest frame of the electron and can be represented as

$$\vec{B}_{eff} = \frac{\vec{E} \times \vec{p}}{mc^2} \quad (1.5)$$

where  $c$  is the speed of light.



This effective magnetic field ( $\vec{B}_{eff}$ ) will in turn induce a momentum-dependent Zeeman energy which is referred to as spin-orbit coupling and represented as

$$\hat{H}_{so} \sim \mu_B \vec{\sigma} \cdot \vec{B}_{eff} \quad (1.6)$$

$$\hat{H}_{so} \sim \frac{\mu_B (\vec{E} \times \vec{p}) \cdot \vec{\sigma}}{mc^2} \quad (1.7)$$

The spin subbands are separated in energy in quantum wells whose structural inversion symmetry is broken along the growth direction  $\vec{z}$ . Bychkov and Rashba proposed an explanation for this band splitting that takes into account an electric field  $\vec{E} = E_z \vec{z}$  that produces an effective SO coupling of the form [120]:

$$\hat{H}_R = \frac{\alpha_R}{\hbar} (\vec{z} \times \vec{p}) \cdot \vec{\sigma} \quad (1.8)$$

where  $\alpha_R$  is called the Rashba parameter. However, this simplistic form which is derived from 2-D plane waves does not apply to realistic systems. This is due to the fact that in the absence of inversion symmetry, in addition to the electric field  $\vec{E}_z$ , distortion to the wave function of an electron in the vicinity of nuclei happens where the plane wave approximation is no longer valid [122]. Furthermore, the SO coupling is only required to be odd in electron momentum  $\vec{p}$  due to the violation of inversion symmetry, ie,  $\hat{H}_{so} = \vec{w}(-\vec{p}) \cdot \hat{\sigma}$ , where  $\vec{w}(-\vec{p}) = -\vec{w}(\vec{p})$ . It only turns linear in  $\vec{p}$  under specific circumstances (e.g. when the free electron approximation is valid or under strain). Therefore, it is important to keep in mind that the p-linear Rashba SO coupling is a helpful phenomenological approximation that does not exactly capture the true form of the SO coupling in inversion asymmetric systems. The investigation of Rashba physics is currently at the heart of the rapidly emerging area of spin-orbitronics, a spintronics branch devoted to the regulation of non-equilibrium material properties via spin-orbit coupling [123].

The weak localization (WL) correction changes sign in the presence of spin-orbit interaction, and the magnetoresistance values are positive. Weak anti-localization is a phenomenon discovered by Hikami, Larkin, and Nagaoka in 1980 [124]. The obvious question is why, in the presence of spin-orbit scattering, weak localization becomes weak antilocalization which we will discuss now.

During a sequence of electron scattering in diffusive transport in the presence of spin-orbit scattering, the spin orientation diffuses into a final state that is rotated compared to

the original spin state. The interference of the two partial waves is constructive without the spin rotation, hence there is WL (in the absence of an external field). The interference becomes destructive in the presence of spin-orbit scattering. In reality, when a system has spin-orbit interaction, the spin component of the electron states contributes to the amplitude of the interference. The spins in two time-reversed paths rotate in opposite directions. Then, when the waves recombine, their orientation will differ by a finite amount, reducing the interference amplitude compared to the state without spin interactions. Antilocalisation occurs as a result of this reduction, and back-scattering is reduced below the statistical level. This causes an echo in the forward direction and a decrease in resistance (an increase of conductance) [116]. RSO is also affected by the presence of a magnetic field. In conclusion, Rashba SOC causes negative magnetoconductance (positive magnetoresistance), whereas WL causes positive magnetoconductance (negative magnetoresistance).

## 1.9.2 WAL in LAO/STO

Because of the polar/non-polar character of interfaces, an effective electric field is formed in LAO/STO systems with a quantum well along the (001) growth direction, and thus a Rashba spin-orbit effect impacts the electrons trapped in the 2DEG.

According to certain studies [125–128], the Ti 3d subbands define the lowest order of Rashba splitting at the LAO/STO interface, with the SOI strength maximized at the  $d_{xy} - d_{xz/yz}$  crossings due to the band hybridization effect. This causes a spin splitting in the surface bands around the zone centre,  $\Gamma$  point ( $k = 0$ ). The lowest energy states in this region create fourfold degenerate bands, which correspond to atoms with total angular momentum  $J=3/2$  ( $m_j = 3/2$  and  $m_j = 1/2$ ). At the  $\Gamma$  point, ie at  $k = (0, 0, 0)$ , the separation in energy between  $J = 3/2$  and  $J = 1/2$  states measures the intensity of the spin-orbit interaction in a material. As a result, the spin-orbit Hamiltonian's dominant term is k-cubic Rashba, which provides exceptionally high spin-orbital interaction and is heavily reliant on the external field generated by the broken inversion symmetry.

Caviglia et al. [129] showed that there is a tunable transition from WL to WAL in the LAO/STO Rashba SOI, which has been investigated since 2010. Figure 1.12 a depicts the relative magnetoconductance response to various gate voltage field effects. Figure 1.12 a indicates that for large negative gate voltages, the magnetoconductance is positive, but for positive gate voltages, the response is negative. A contribution of the WAL is detected at positive gate voltages in a low magnetic field, indicating spin-orbit coupling.

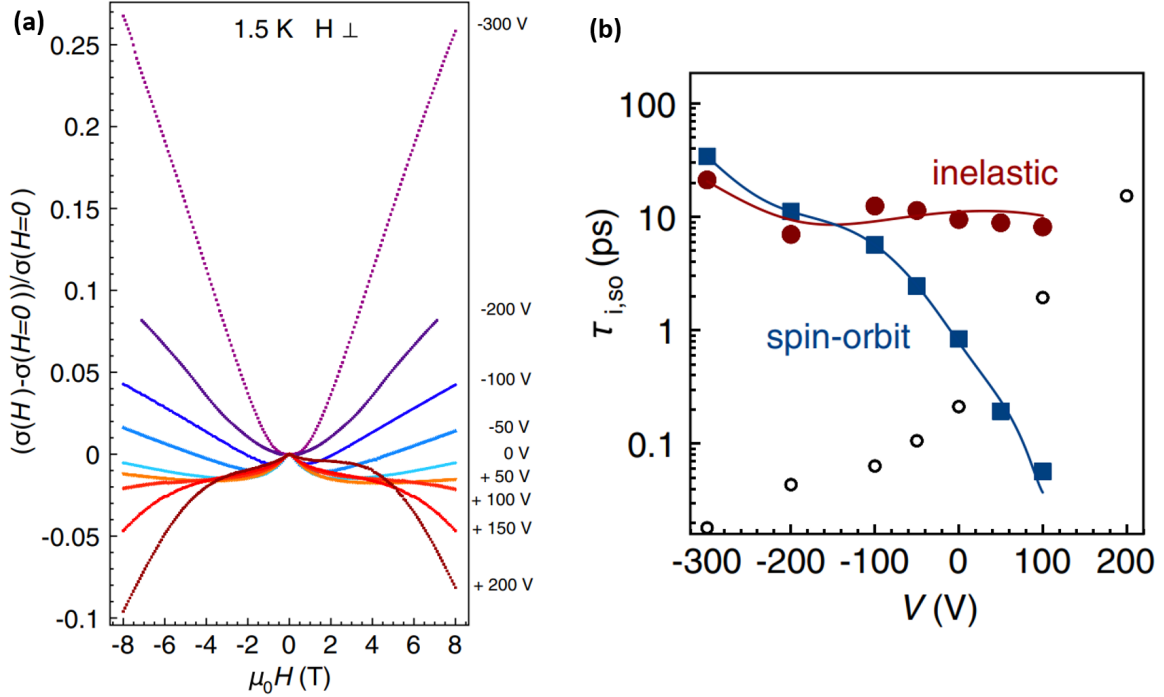


FIGURE 1.12: (a) The modulation of magnetoconductance of the LAO/STO interface at 1.5 K under the influence of the electric field. Positive magnetoconductance is enhanced by negative gate voltage while with positive gate voltage, negative magnetoconductance starts to dominate. (b) Dependence of inelastic scattering times  $\tau_i$  and spin relaxation time  $\tau_{so}$  as a function of gate voltage. Open circle denotes the predicted behaviour of  $\tau_{so}$  based on Elliot relation. Adapted from [129]

The relaxation times ( $\tau_{i,so}$ ) are plotted against gate voltage in the Figure 1.12 b. The inelastic scattering time  $\tau_i$  is less than the spin relaxation time  $\tau$  for large negative gate voltages, showing that the spin-orbit interaction is low relative to the orbital effect due to the magnetic field. Weak localization can be attributed to the quantum correction to conductivity in this regime. The spin relaxation time becomes shorter than the inelastic scattering time above a certain gate voltage and declines sharply, by three orders of magnitude, as the voltage is increased. The inelastic scattering time, on the other hand, remains relatively constant as the voltage rises. A weak anti-localization regime with a strong spin-orbit interaction arises here. The Rashba SO mechanism can also be identified based on the behaviour of these scattering times. The SO coupling does not conserve spin in general, but it does provide a mechanism for non-equilibrium spin concentrations to relax. The spin-orbit relaxation time ( $\tau_{so}$ ) is defined by spin-relaxation mechanisms due to spin-orbit coupling, which is a central aspect to characterize transport in a two-dimensional electron gas in the presence of a strong homogeneous electric field.

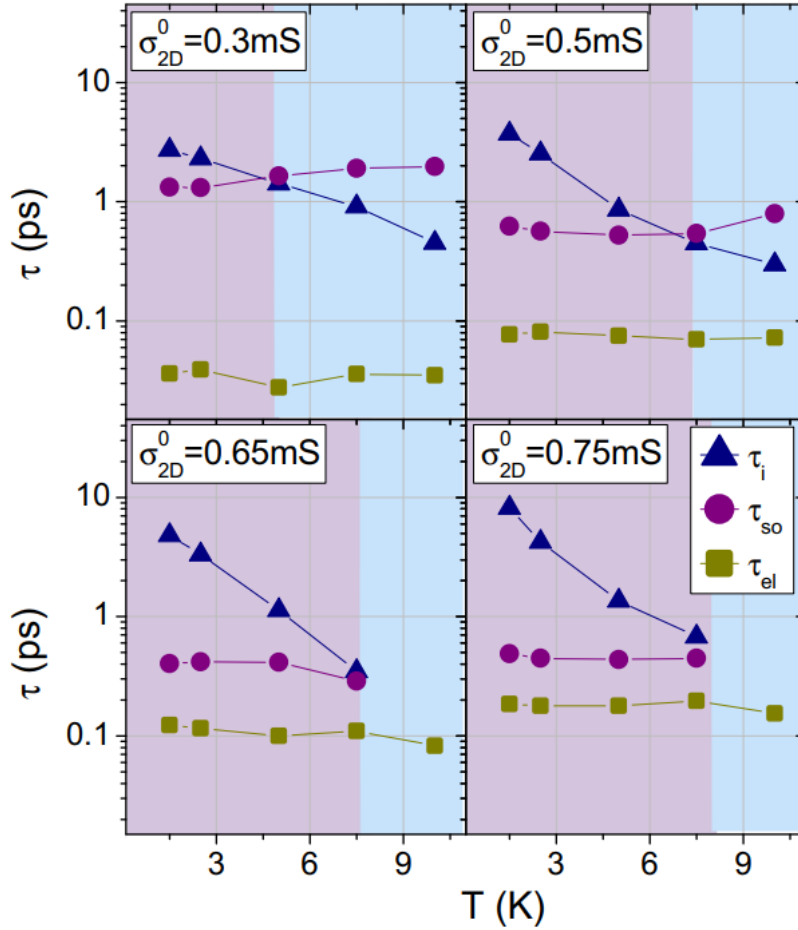


FIGURE 1.13: Temperature dependent variation of inelastic scattering times  $\tau_i$ , spin relaxation time  $\tau_{so}$  and elastic scattering times ( $\tau_e$ ) for different values of sheet conductance for  $0.75 \mu\text{m}$  wide channel. The pink shaded area represents the region where the spin-orbit interaction is the most dominant scattering mechanism ( $\tau_i > \tau_{so}$ ). Crossover temperature ( $T_{cross}$ ) is the determined from the crossing point between  $\tau_i$  and  $\tau_{so}$ . Adapted from [130]

There are two types of spin relaxation mechanisms, the D'yakonov-Perel' (DP) [131] mechanism and the Elliott-Yafet (EY) [132] mechanism. The D'yakonov-Perel' (DP) mechanism is present in materials with no symmetry by inversion; in these circumstances, spin-orbital interaction prevents degeneration between spin-ups and spin-downs. Elliott-Yafet can be caused by a variety of factors such as scattering with impurities, interaction with lattice ions, and, at high enough temperatures, scattering with phonons, where the Hamiltonian functions are no longer the eigenfunction of the spin. There is a direct connection between the spin relaxation time  $\tau_{so}$  and the elastic scattering time  $\tau_e$  in the EY mechanism (ionic spin-orbit interaction). The spin relaxation time is inversely related to the elastic scattering duration in a DP situation (Rashba spin-orbit interaction). Caviglia et al.[129] discovered a distinct signature of the DP mechanism in the Rashba spin-orbit

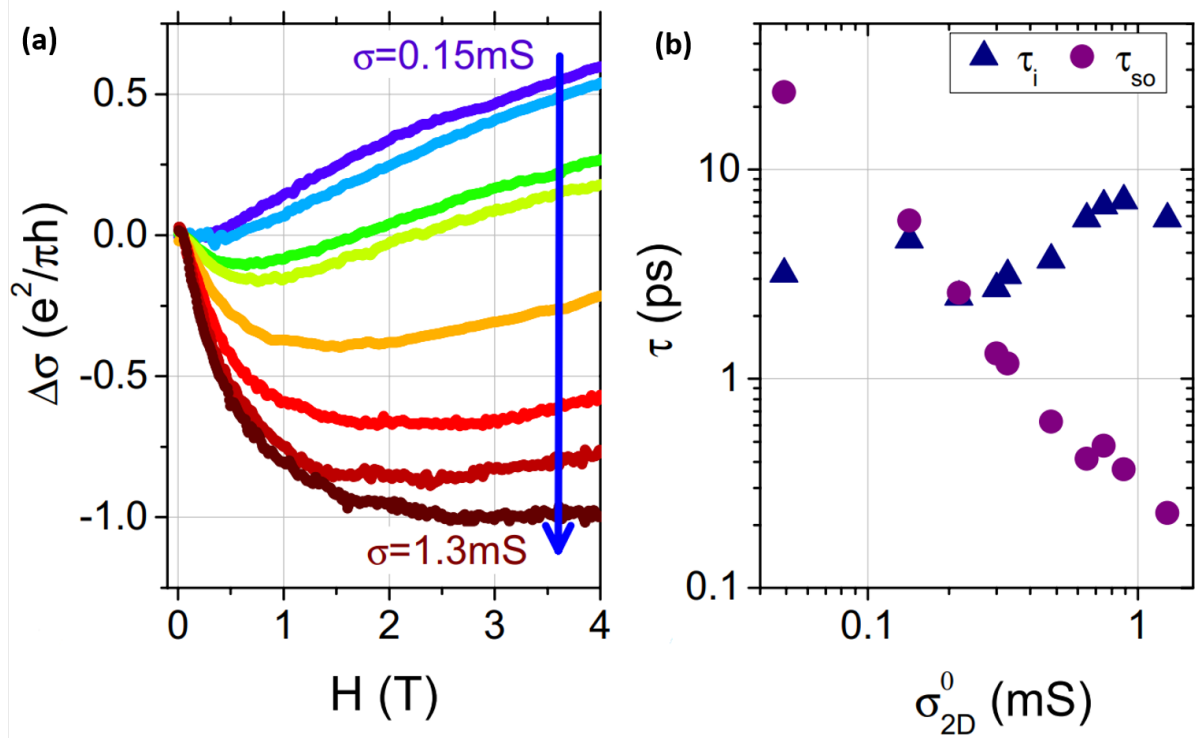


FIGURE 1.14: (a) Modulation of magnetoconductance as a function of sheet conductance at  $T = 1.5 \text{ K}$  for a magnetic field applied perpendicular to the interface. (b) Shows the variation of inelastic scattering times  $\tau_i$  and spin relaxation time  $\tau_{so}$  as a function of sheet conductance. Crossover between WL and WAL occurs at  $\sigma_{2D}^0 \approx 1.2 \text{ mS}$ . Adapted from [130]

interaction in their work. Ben Shalom and colleagues [133, 134] investigated the evolution of the in-plane superconducting critical field as the gate voltage is adjusted, implying a significant SO coupling in LAO/STO systems.

Another important aspect to consider is the temperature and carrier density-dependent crossover between WL and WAL regimes. Temperature-dependent magnetoconductance studies reveal that the  $\tau_i$  exhibits a power law increase with decreasing temperature as shown in Figure 1.13. At this same temperature range, on the other hand,  $\tau_{so}$  is unaffected (Figure 1.13). As a result, WL and WAL have a temperature-dependent crossover, signalling a change in the dominant scattering mechanism. Figure 1.14a depicts the evolution of magnetoconductance curves as a function of sheet conductance ( $\sigma$ ). The temperature at which  $\tau_i = \tau_{so}$  (as shown in Figure 1.15) is referred to as the crossover temperature ( $T_{cross}$ ) which signals the change of the dominant scattering mechanism from WL to WAL or vice versa. However,  $T_{cross}$  can be modified by changing the carrier density at the interface, as previously reported. In other words, changing the carrier density

at a given temperature can change the dominant scattering mechanism at the LAO/STO interface.

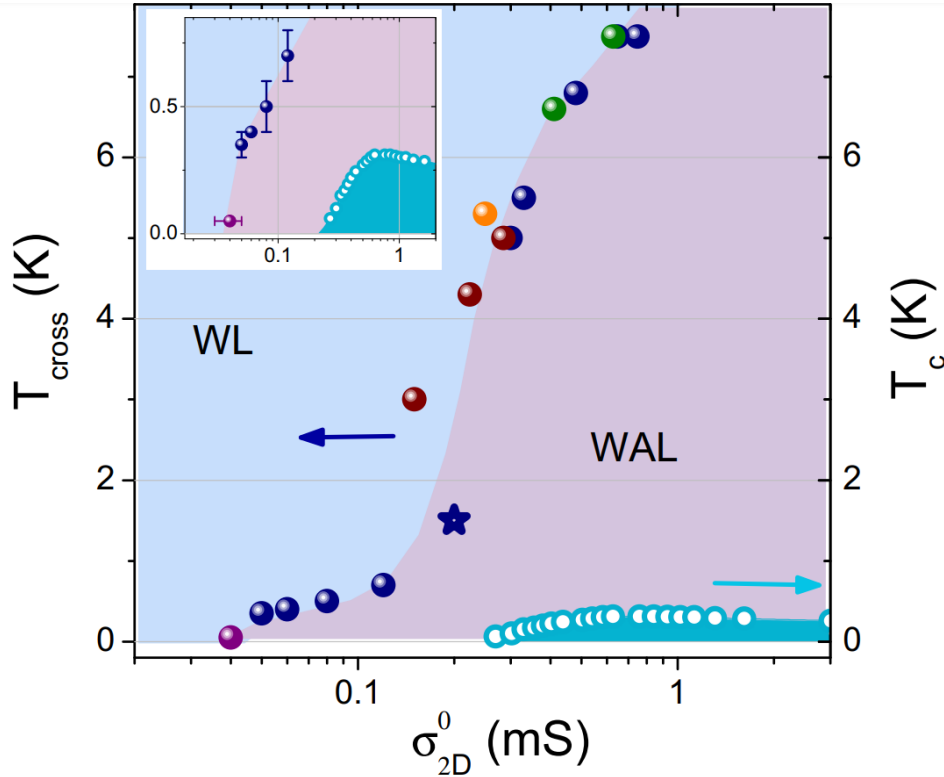


FIGURE 1.15: Phase diagram representing the temperature and conductivity ranges for which the magnetotransport in LAO/STO interface is characterised by WL or WAL. Different colours of the points represent the different sizes of the structures under investigation. The blue area at the bottom indicates the superconducting dome. The inset is the zoom of the low conductance regime where the crossover temperature is very small. Adapted from [130]

## 1.10 Summary

The discovery of highly conducting two-dimension electron gas at the interface between two band gap insulators  $\text{LaAlO}_3$  and  $\text{SrTiO}_3$  sparked extensive research in the field of complex oxides and their functionalities. We have discussed the structural and electronic properties of the bulk LAO and STO, followed by the discussion of the formation of 2DEG. Multiple mechanisms have been proposed to explain the origin of interfacial conductivity. However, a single model is not sufficient since the nature of interfacial conductivity is quite complex. Still, research has been carried out to understand the properties of the interface. Some of the fascinating properties of the interface have also been discussed in the final section. This interface's multitude of properties makes it unique and a potential

candidate for future electronics. Electronic transport properties of the interface are governed to an extent by the localisation effects. Depending on their nature and correction to conductivity, it can be either weak localisation or weak antilocalisation effects. The latter is due to the presence of strong spin-orbit coupling. In the presence of a magnetic field, WL and WAL behave in a completely different way and yields negative and positive MR, respectively. It has been reported in the LAO/STO interface that the crossover between WL and WAL regimes happens depending on temperature and conductance. Localisation effects play a key role in the transport properties of nanostructures, as we will see in the later chapters ([chapter 4](#) and [chapter 5](#))

# 2

## Influence of domain walls on the transport properties of the interface

Since the discovery of 2DEG at the interface between LAO/STO, a lot of studies have been conducted to explore the electrical and magnetic properties of the interface. STO is one of the most celebrated substrates used as the building block of numerous complex oxides with very interesting properties. Until 2013 the interface was considered to exhibit homogeneous conductivity. But some studies conducted later show that the conductivity of the interface is not homogeneous but greatly influenced by the structural changes in STO. Before this discovery, not a lot of attention was given to studying the influence of structural changes in STO on the transport properties of the LAO/STO interface. One of the main difficulties in conducting such studies is due to the limitation of standard surface probing methods such as scanning tunnelling microscopy (STM), which are incapable of studying the buried interface, which has left their effect largely unexplored. Scanning nanoscale probes were used to tackle this problem and used to map the spatial distribution of charge carriers at the interface with great sensitivity [135]. These studies reveal the significance of microscopic structural domains on the transport properties of the interface [136, 137]. Nanoscale probes are also used to realise unique nanoscale devices at the interface [138, 139]. The influence of these structural domains is more pronounced when the interface is patterned into nanoscale dimensions. In this chapter, we will discuss the structural phase transition in STO and how it affects the properties of the LAO/STO interface.



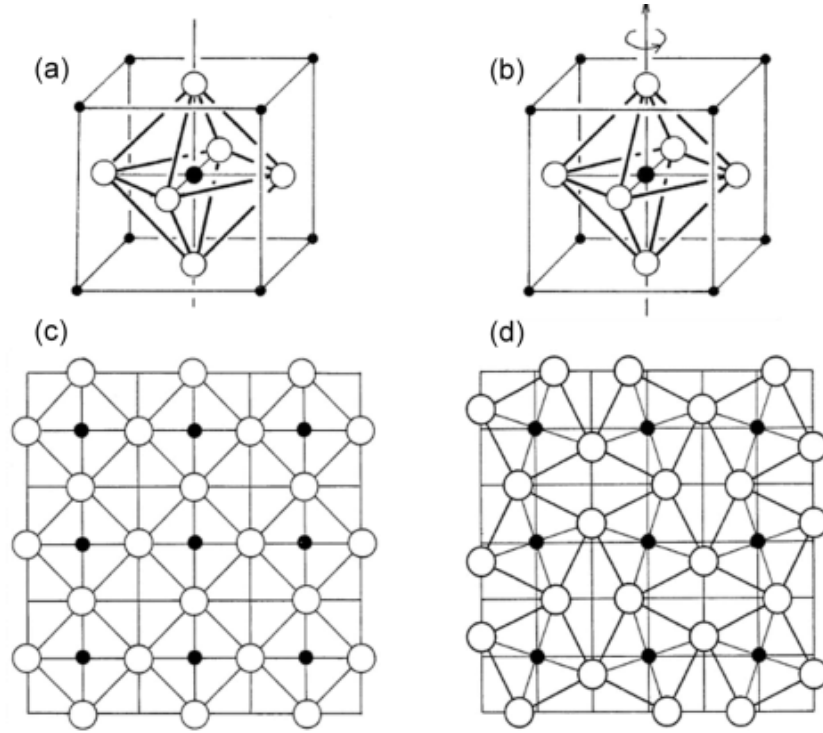


FIGURE 2.1: The crystal structure of  $SrTiO_3$  perovskite with a titanium atom at the centre, an oxygen atom in each of the six cube walls creating a cage around the titanium atom, strontium atoms are located at the cube's corners. (a) The normal phase, (b) the  $TiO_6$  octahedra rotating around the C4 axis in the STO crystal, (c) the organization of the atoms during the normal phase, and (d) the arrangement of the atoms following the  $TiO_6$  octahedra rotation. Adapted from [140].

## 2.1 Phase transition in STO

At room temperature, STO has a cubic crystal structure with a titanium atom at the centre and oxygen atoms in each of the six cube walls forming a cage around a titanium atom, and strontium atoms at the corners of the cube. At around  $T = 105$  K, a ferroelastic phase transition from cubic to tetragonal structure occurs. This phase transition is a result of the rotation of  $TiO_6$  octahedra which results in the breaking of cubic symmetry. The rotation of octahedra happens in such a way that every neighbouring octahedron rotates in opposite directions to one another in all three directions. As a result of this phase transition, elongation of one of the axes (c-axis) occurs along with two short axes (a-axes). The long axis can be oriented along any of the crystal axes resulting in the formation of domains within STO characterised by the orientation of their unit cells.

In order to minimize dislocation, the domains follow a simple tiling rule: share the short axes (a-axes). So the tetragonal unit cells along X (100), Y (010) or Z (001) crystal

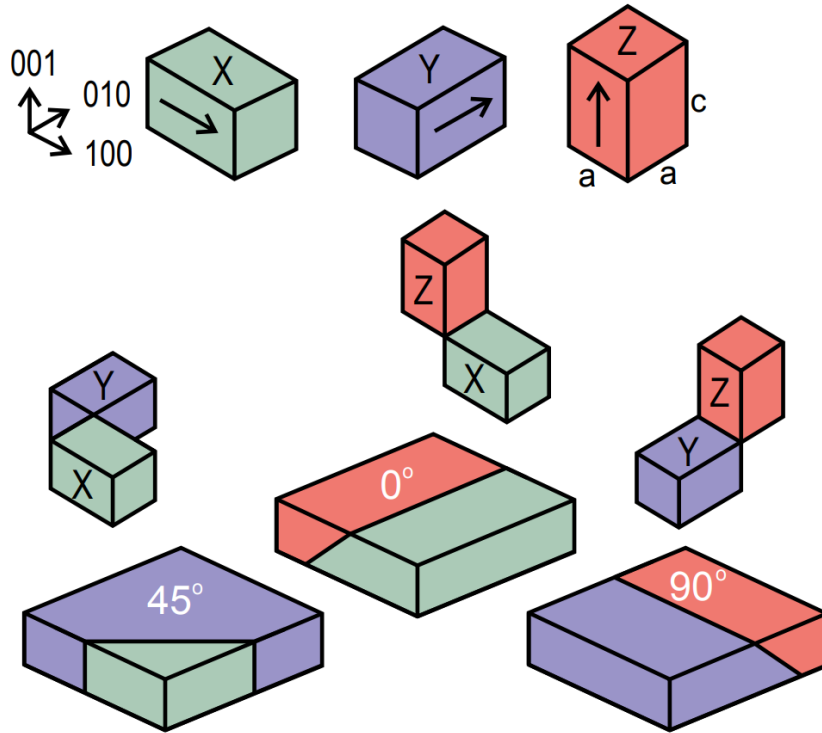


FIGURE 2.2: Due to the rotation of  $TiO_6$  during the phase transition at around 105 K, elongation of the cubic unit cells along one of the three crystalline directions (c-axis) take place which will result in the formation of tetragonal unit cells. Depending on the orientation of the c-axis which could be along 100 (green), 010 (blue) or 001 (red) direction as shown in the top image, different domains are formed (X, Y or Z). The domains share their short axis (a-axis) in order to minimize dislocations which results in the formation of different domain boundaries having angles of either  $0^\circ$ ,  $45^\circ$ ,  $90^\circ$  or  $135^\circ$  with respect to the crystallographic axes as viewed from the top. Adapted from [136].

directions share their short axes (a-axes) at domain walls (twin boundaries). The domain walls between X and Y domains must lie at  $45^\circ$  or  $135^\circ$ , between Z and X at  $0^\circ$ , and between Z and Y at  $90^\circ$  at the top surface. This kind of domain wall pattern has been reported 50 years ago using polarized optical microscopy [48]. These domain walls play a key role in charge conduction and other transport properties of the LAO/STO interface.

## 2.2 Charge conduction through domain walls

The major focus of the study of the LAO/STO interface has been devoted to the exploration of its conducting 2DEG and its unique properties. The effect of the diverse array of physical phenomena of hosting STO material on the interfacial properties has not been explored in great detail at the beginning. The limitations in using classical surface probes

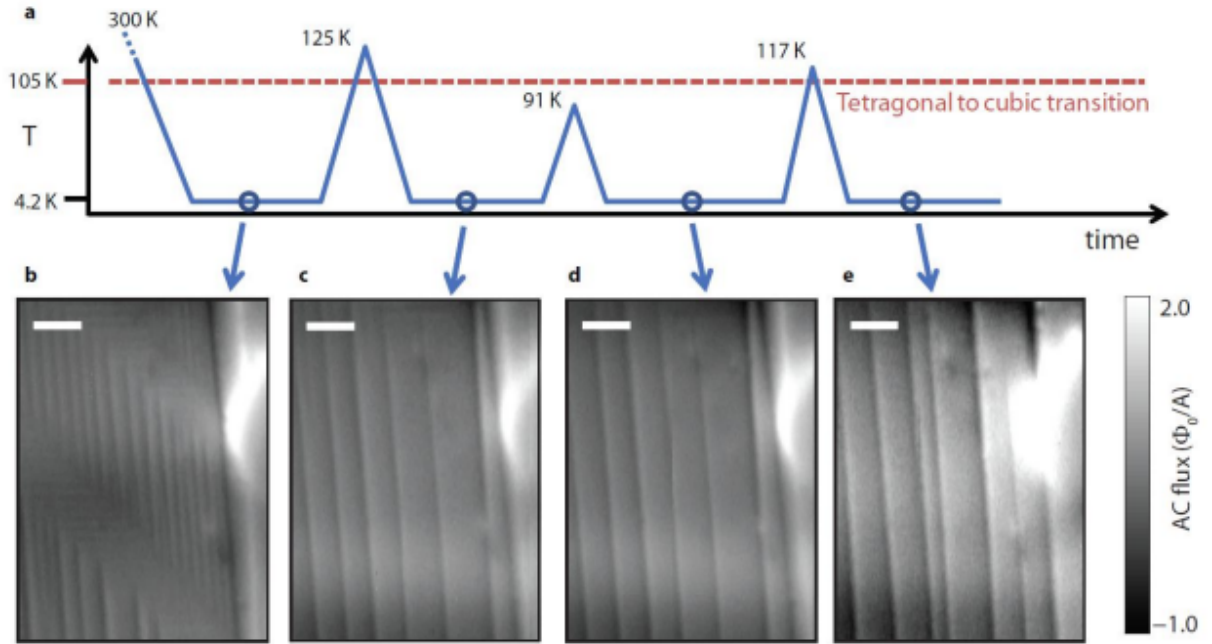


FIGURE 2.3: Current maps at the LAO/STO interface at 4.2 K obtained from the magnetic flux images captured by the pickup loop of scanning superconducting quantum interference device (SQUID). These images clearly demonstrate the formation of a channelled path of current flow at the interface below the phase transition. (b) - (e) shows the current map at 4.2 K after thermal cycling to different temperatures shown in (a). Thermal cycling to 125 K alters the pattern of the current flow (c) but thermal cycling to 91 K preserves the previously obtained pattern (d). The pattern of the channelled current flow changes every time when thermal cycling is conducted above the phase transition temperature (105 K). Adapted from [137].

like scanning tunnelling microscopy (STM), which rely on tunnelling, pose a challenge in imaging the interface which is buried underneath the surface.

With the advancement in the field of nanoscale probing devices, it is now possible to study buried interfaces and help us to get a better understanding of the influence of the domain structure of STO on the properties of the LAO/STO interface with great precision. The conductivity of the LAO/STO interface is considered to be homogeneous until 2013. But the scanning superconducting quantum interference device (SQUID) microscopy study conducted by Kalisky [137] and group revealed that at low temperatures the conductivity of the interface is no longer homogeneous. They revealed the presence of channelled current flow within the 2DEG. In this work, they used the SQUID's pick-up loop to capture the magnetic flux that is generated by the current flowing through the interface. These flux images are used to recreate the spatial map of current density within the 2DEG. At 4.2 K channelled current flow was observed in a different spatial map of current density. Another important observation of this study was that the distribution

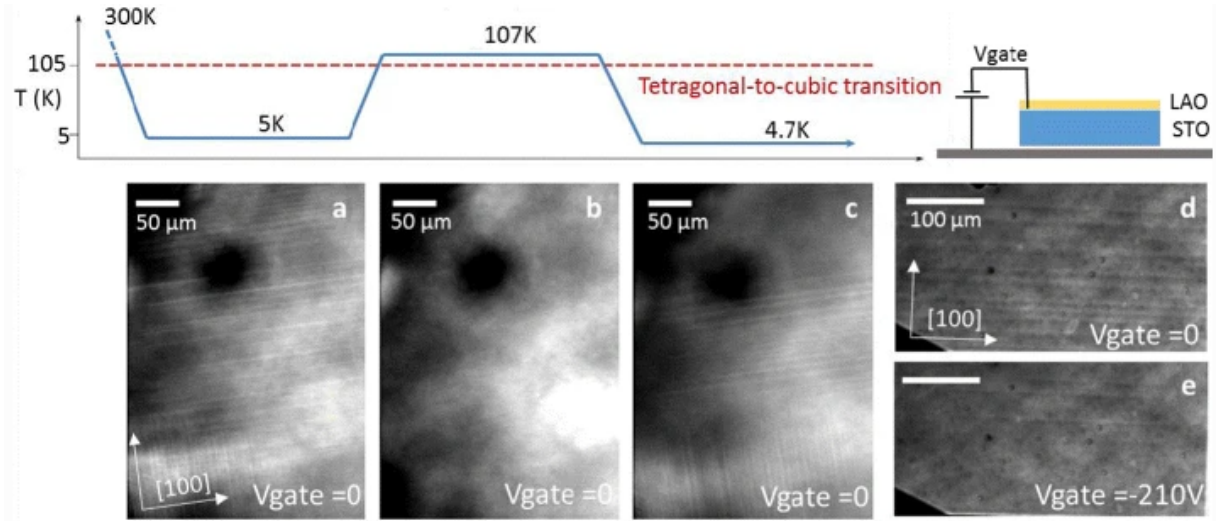


FIGURE 2.4: Polarised light microscopy image of the LAO/STO interface that reveals the domain structure taken at different temperatures. Domain patterns are observed only below the phase transition temperature ((a) and (c)). At 107 K domain structure disappears (b) and after the thermal cycling, the configuration of the domain patterns also changes (c). (d-e) shows the gate voltage dependence of the domain patterns. The domain patterns with no gate voltage are shown in (d). With the application of negative gate voltage, most of the domains disappear (e). Adapted from [141].

of current channel changes after thermal cycling above 105 K (Figure 2.3). No change in channel pattern has been observed with thermal cycling below 105 K. This provides further proof that the enhanced current flowing channels are formed as a result of phase transition in STO. The current flow can be enhanced along the (100) and the (110) STO cubic crystallographic directions depending on the domain structure.

A polarised light microscopic study is used to confirm the domain structure reconfiguration with temperature [141]. Domain structures are always present below 105 K but they totally disappear at temperatures above 105 K. Domain configuration changes every time the thermal cycling is performed above 105 K which supports the influence of domain formation in STO (Figure 2.4). [142] observed a strong modulation of the channel current flow of up to 95% when the microscopic current flow distribution and macroscopic resistance were simultaneously measured. They found that the interface is less resistive when applied current flows along the tetragonal stripes in comparison to current flowing perpendicular to the stripes.

Another study of the interface using scanning single electron transistors (SET) [136], a nanotube quantum dot as a scanning charge detector (Figure 2.5 a), did the imaging

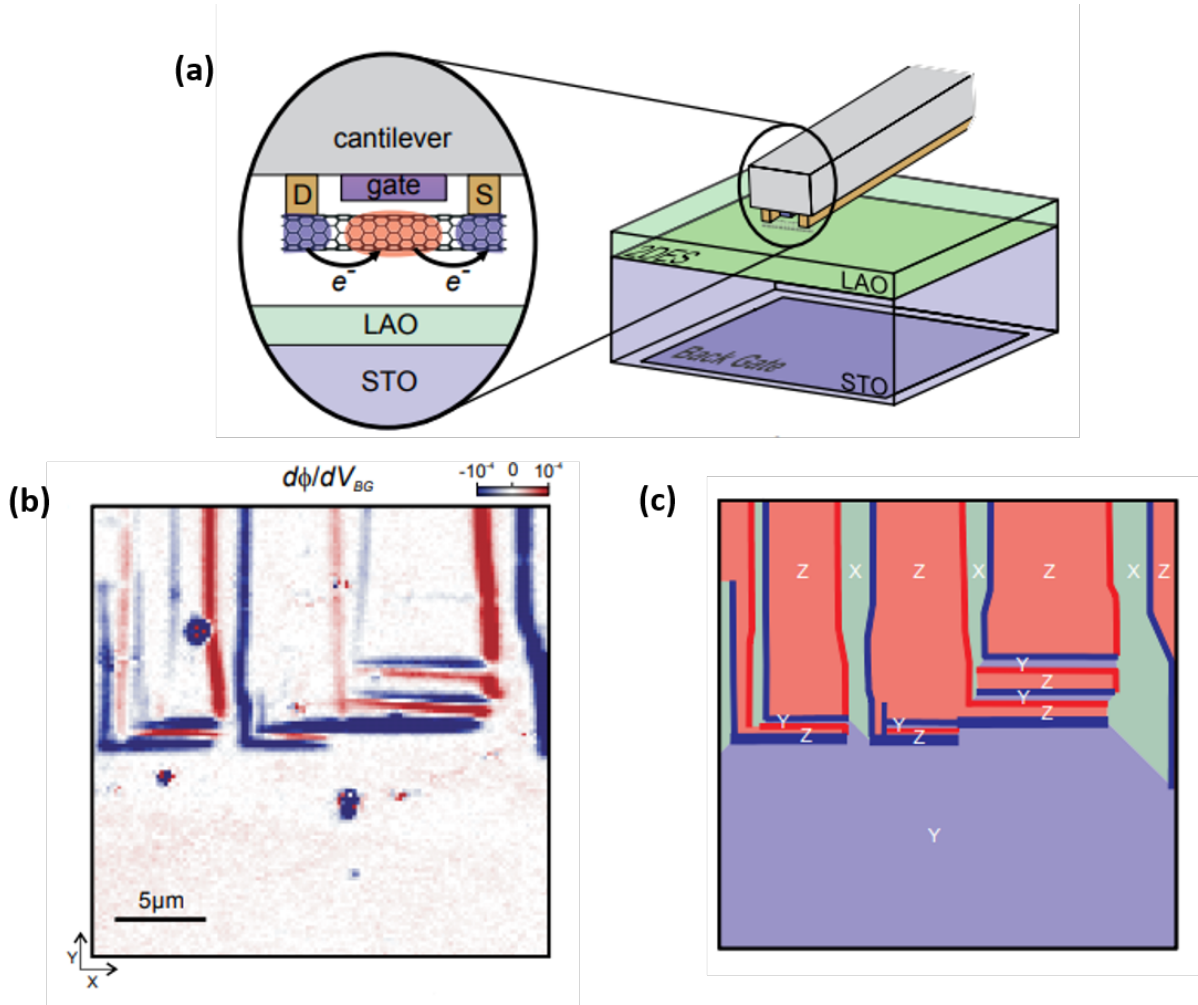


FIGURE 2.5: (a) schematic representation of nanotube SET probe which is scanning the surface of back gated LAO/STO interface. This set-up can be used to image the local electrostatic potential ( $\phi$ ) by monitoring the SET current. (b) Map of electromechanical response obtained by scanning SET. The red and blue stripes represent the rising or falling edge (red or blue) of the potential step induced by the oscillating back gate voltage. (c) Map of the domain orientation in (b). red and blue lines represent the domain boundaries. Adapted from [136]

on the nanoscale both mechanical properties and electrostatic landscapes with an unprecedented energy resolution. They generated a map of the domain structure from the electro-mechanical response from scanning SET as depicted in Figure 2.5 b, c. Notably, they have observed that the in-plane tetragonal domains (X and Y) have similar surface potential which differs from the out-of-plane domain (Z) by a value of  $\sim 1 \text{ mV}$ . Due to this difference in surface potential between domains, charges need to be transferred across the domain walls to keep the electrochemical equilibrium. This charge transfer leads to significant modulation of charge density along the domain walls which could lead to channelled current flow.

In the next section, we will discuss how the application of the electric field influences the domain wall dynamics and alters the properties of the interface.

## **2.3 Domain walls under the application of electric field**

As we already discussed, the formation of domains and domain walls plays an important role in charge conduction at the LAO/STO interface. Honig et al. [136] have revealed that on a microscopic level STO exhibits an anomalously large piezoelectric effect with notable special dependence. Through electrostatic imaging using a nanotube single-electron transistor, they have attributed the origin of this extrinsic piezoelectricity to the motion of tetragonal domains.

They also observed that the domain walls in STO are mobile under the application of gate voltage as shown in Figure 2.6. The domain walls in STO move at a rate of  $1\mu\text{mV}^{-1}$  with the gate voltage and after sufficiently large gate voltages, the interface becomes completely homogeneous. After a large gate voltage, the interface is free of out-of-plane domains (Z domains). The motion of the domains under the application of an electric field can be due to the dielectric anisotropy between in-plane and out-of-plane domains or due to the polar nature of domain walls providing a natural coupling to an applied gate voltage.

Further experiments confirm the domain wall motion under the application in bare STO substrate at low temperatures [143, 144], where they observe the expansion of in-plane domains. They have ruled out the domain wall polarity as the main driving force for this observation since domain wall polarity is oriented towards the apex of the twin and results in the non-zero polarity of X and Y (or X and Z) domain walls. Hence by application of an out-of-plane electric field, the expansion of Z domains should be favoured instead of X and Y domains. Also, they found that electric fields promote the expansion of in-plane domains (Figure 2.7) at the temperature where the evidence of domain wall polarity is weak. Dielectric anisotropy between in-plane and out-of-plane domains in STO is proposed to be the most likely candidate. The domain formation in STO is driven by an antiferrodistortive (AFD) lattice mode, with neighbouring  $TiO_6$  octahedra rotating in antiphase along the [001] axis [145, 146]. Domains with higher polarisability along the applied electric field are favoured and they showed that the polarisability is significantly larger along the normal to the AFD tilt axis, which is along the in-plane direction. As a result, an electric field leads to an expansion of the in-plane domains and above a threshold field a complete removal of the domains with out of plane long axis.

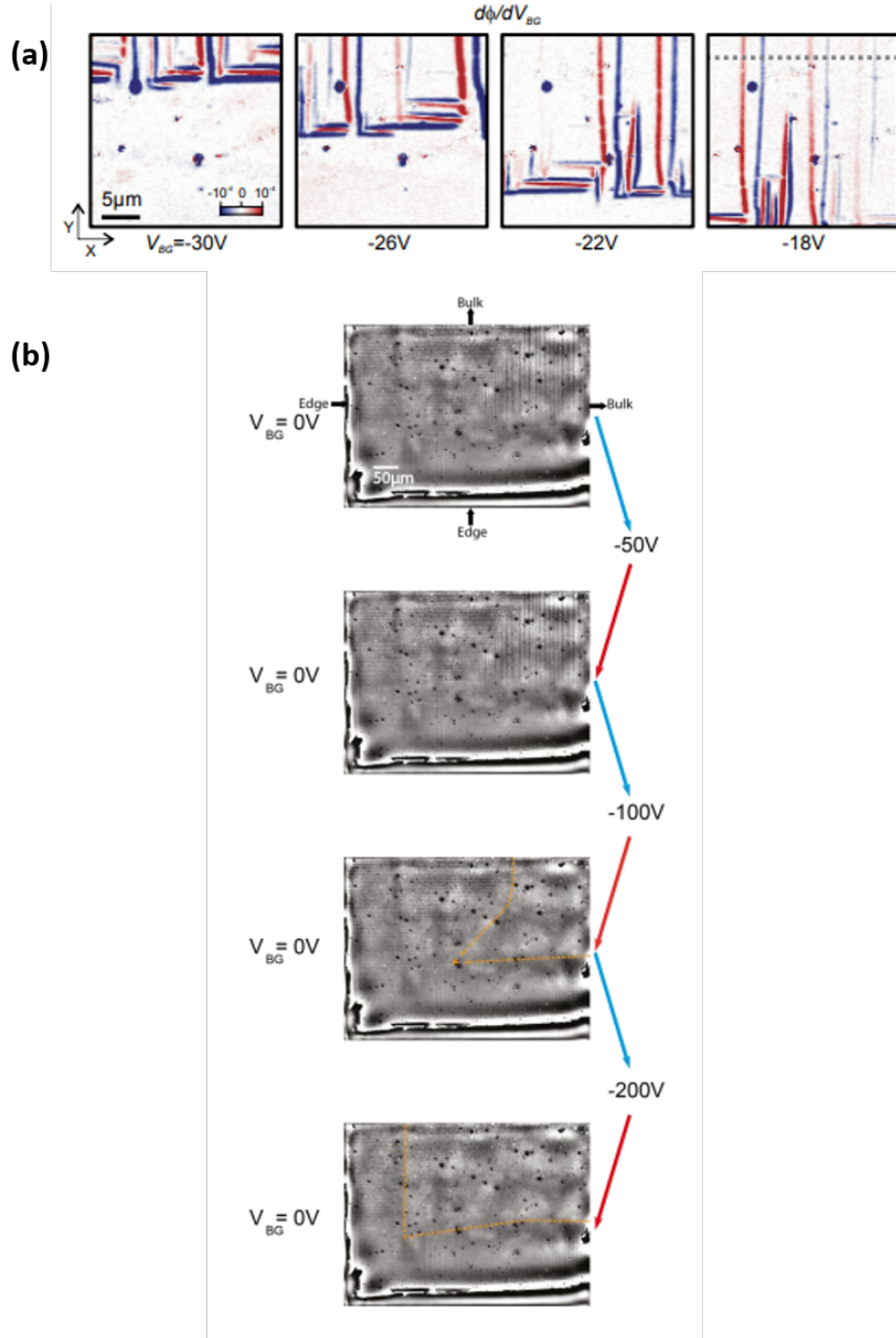


FIGURE 2.6: (a) Electromechanical response map of SET which represents gate induced domain wall motion. Decreasing the back gate voltage pushes the boundary between homogeneous and striped regions towards the edge of the sample. (b) shows the optical image of the LAO/STO interface at  $T = 30K$  and denotes how the application of gate voltage irreversibly modifies the domain orientation. Cycling the gate voltage to  $-50V$  and back to  $0V$  did not affect the domain distribution. However, cycling to higher gate voltages and back to  $0V$  clears the stripes except near the edges. Adapted from [136].

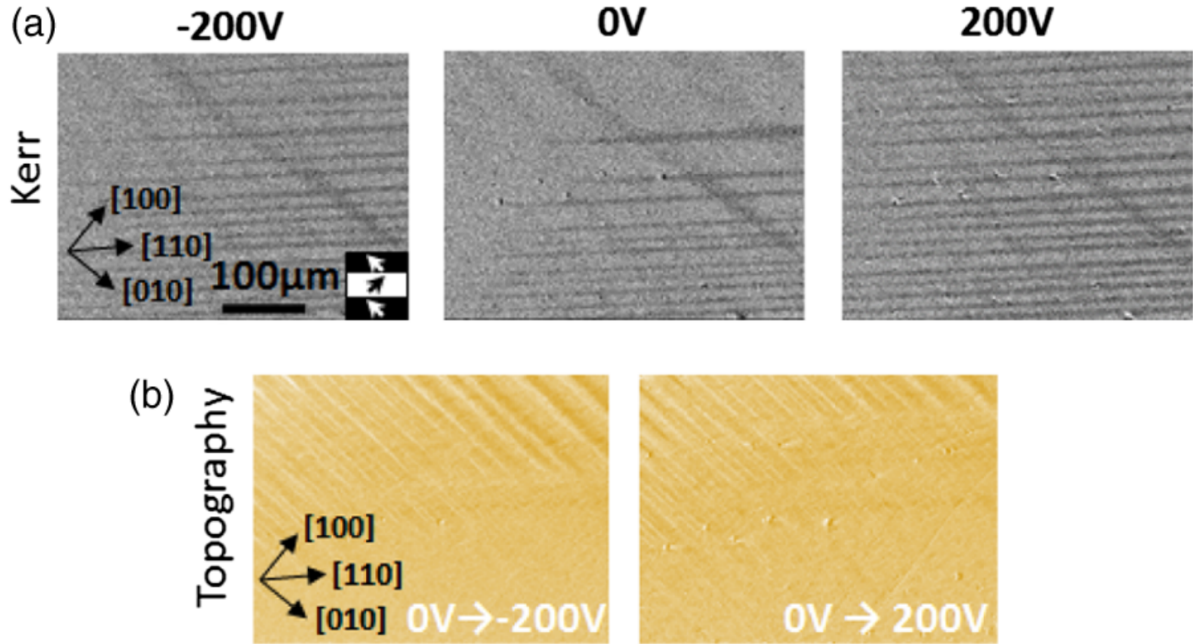


FIGURE 2.7: (a) Transverse MOKE images of the residual magnetic state at  $V = -200V, 0V, +200V$ . The horizontal stripes represent the domain wall between the in-plane domains (110). At higher gate voltage (irrespective of the polarity) there is a preferential selection of 110 domain walls. (b) Represents the image obtained after the subtraction of the optical images at two different gate voltages [ $(V_{G=0V} - V_{G=-200V})$  &  $(V_{G=0V} - V_{G=+200V})$ ] simultaneously taken with MOKE data as shown in (a). This data represented in (b) clearly shows the region where the 100 and 010 domain walls have disappeared. Adapted from [143].

In 2016 Ma et al.[147] used low-temperature scanning electron microscopy (LTSEM) and electron beam-induced current for the investigation of LAO/STO structures and mapping of tetragonal domains and electric field-induced ferroelectric domain walls in STO. LTSEM uses a periodically blanked focused electron beam scanned across the sample. It locally perturbs its electric conductivity with micron-scale spatial resolution and induces a voltage signal  $\Delta V$  across the sample. The signal  $\Delta V$  gives information about the electronic properties of the 2DEG. They not only demonstrated that highly conducting filaments exist but they also showed that these filaments may be surrounded by insulating areas. In order to investigate the response of the domain wall to the electric field, they use both the side gate and back gate configuration. They have observed that ferroelectricity is induced in the domain wall when a threshold electric field above 1.4 KV/cm is applied. These ferroelectric domain walls remain even after the electric field is switched back to zero. Thermal cycling to 100 K did not influence the presence of ferroelectric domain walls. Once the ferroelectricity is induced in the domain walls, they observed that the surrounding 2DEG near the domain walls is depleted for some distance forming



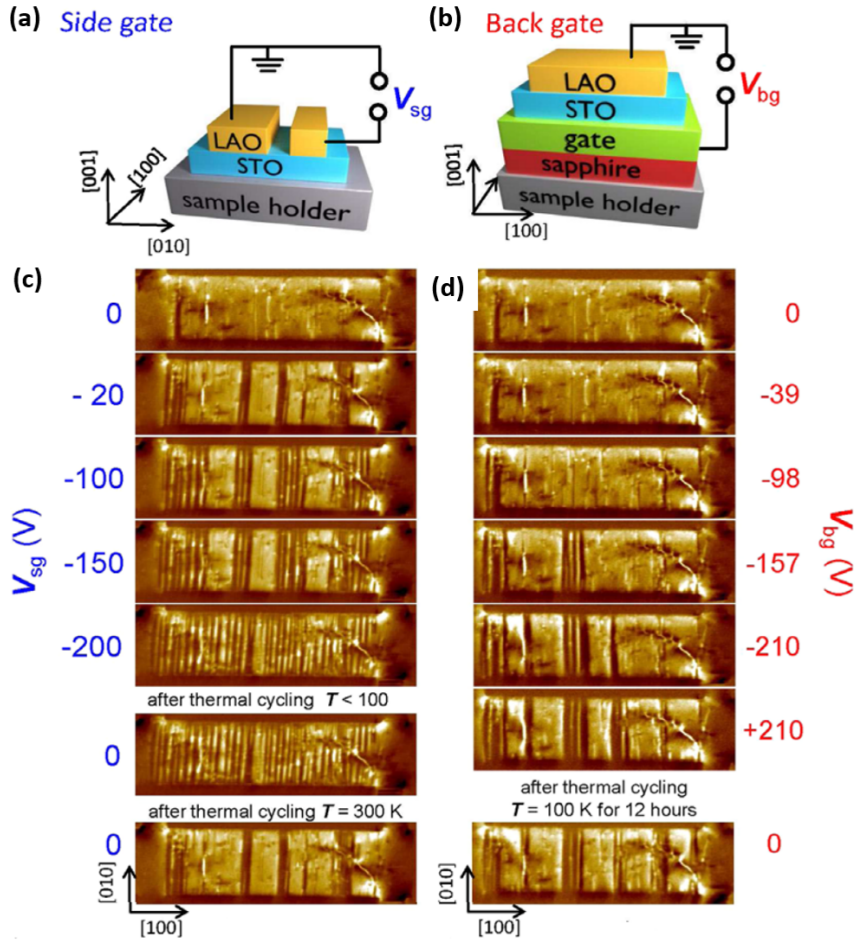


FIGURE 2.8: (a) and (b) represent the side and back gate configurations used for the low-temperature scanning electron microscopy (LTSEM) measurements. (c) LTSEM images for different side gate voltages form 0 V to -200 V and (d) for back gate voltages ranging from 0 V to -210 V at 5 K. The bright line represents the domain walls and the dark yellow stripes represent the domain between them. Adapted from [147]

a Schottky-like barrier. Furthermore, they observed that even above the phase transition temperatures the domain wall pattern may be partially preserved due to charging effects as shown in Figure 2.8

The preferential selection of specific domains under the application of gate voltages opens the door toward persistent tuning of the interface properties especially when the size of the structure is small as we see in the coming chapters.

## 2.4 Filament charge conduction in nanostructures

The effect of domain configuration becomes much more significant as the lateral size of the structure approaches the characteristic size of the domains. For large-area structures, inhomogeneous current flow will statistically average to zero, nullifying the presence of any anisotropic transport. However, their effect is prominent in nanostructures.

Drastic consequences of domain wall transport in LAO/STO nanostructures were first reported by Minhas et al [148]. They observed a huge resistance peak of several orders of magnitude higher than the normal value around 80 K during warming up a 100 nm structure (Figure 2.9). Such a huge peak was never observed in structures with a width greater than 100 nm. They have not reported the presence of resistance peaks in nanostructures more than 500 nm in width. However, some studies have reported the occurrence of small resistance peaks in large area LAO/STO structures [88, 149, 150] during warm-up. Such peaks only occur during warm-up from low temperatures, never during cool-down. The peak height depends on the minimum temperature, the minimum temperature from where the warm-up starts and above the critical temperature, the maximum resistance is not stable over time but rather returns to its normal state after some time as shown in Figure 2.10.

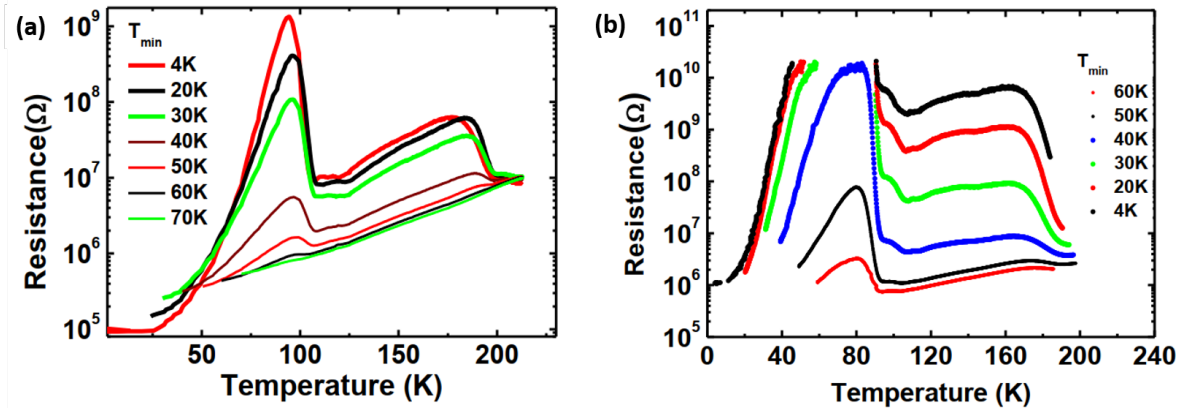


FIGURE 2.9: Temperature dependent resistance anomaly in two different 100 nm LAO/STO nanostructure. During warm-up, a pronounced resistance peak is always obtained at around 80 K. The normal state resistance is only restored at a much higher temperature compared to the phase transition temperature (105 K) resulting in an additional peak around 170 K. The height of the peak varies from sample to sample and also with each warm-up cycle performed on the same sample. Resistance peak vanishes when the  $T_{min} > 60$  K. Adapted from [148].

For explaining the observed effect, they proposed a filamentary model of charge transport in LAO/STO nanostructures (Figure 2.11). According to this model current-carrying

filaments are formed at the boundaries of domain walls during the structural phase transition in STO. These filaments are formed due to the combination of a large electric field at the domain boundaries and an increasing dielectric constant of STO with decreasing temperature, which leads to the accumulation of charge carriers at the boundaries. This leads to the formation of maze-like conducting patterns with conductivity along the filaments and the domains are mostly insulating. During warm-up, the filaments break due to phase transition and charges get redistributed and eventually, homogeneous conductivity is restored. However, they claimed that the relevant phase transition, in this case, is the one that happens at around 65 K, since the maximum of the resistance peak is always present at a temperature below 105 K. In addition, the absence of the resistance peak when the  $T_{min} > 60 K$  (Figure 2.9) also supports their claim.

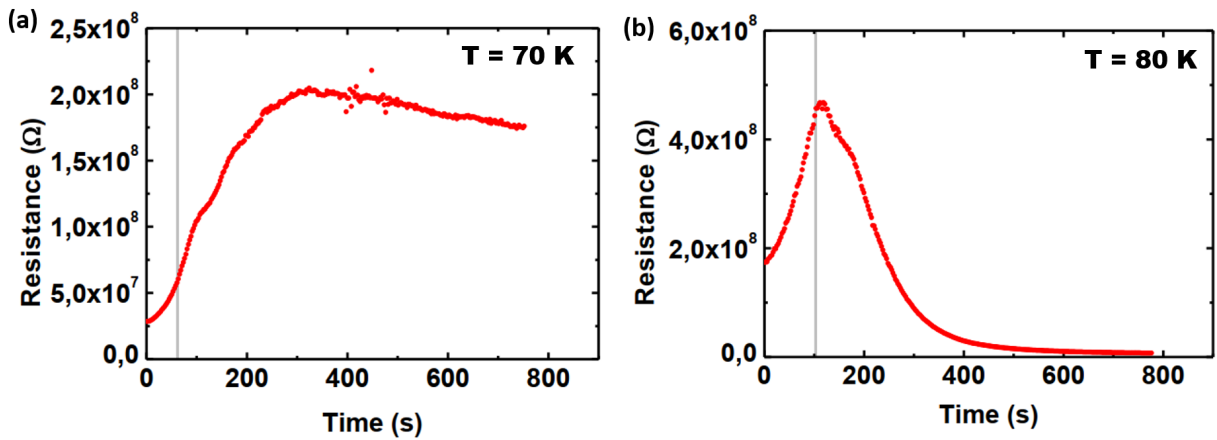


FIGURE 2.10: Stability of the resistance peak of a 100 nm structure over time at two different temperatures. (a) The sample is warmed up to 70 K after cooling down to 50 K and waiting for 12 minutes. A similar procedure is repeated after warming the sample to 80 K (b). As long as the temperature is below the temperature of the resistance peak (80 K), the resistance initially increases and remains constant after some time as in (a). Beyond 80 K, the resistance drops significantly after an initial increase and almost reaches the cooling curve value (b). Adapted from [148]

The number of current-carrying filaments is limited in the case of nanostructures. As a result of the breaking of the filament, the conduction path is temporarily interrupted, and the electrons pinned to the domain walls will become mobile and get attracted by the adjacent domain walls. In the case of smaller structures (say 100 nm), there could be as few as one domain wall present for conduction, breaking of the filament could increase the resistance to infinity. Large area samples have literally millions of current filaments due to their lateral size. The interruption of some of the filaments only leads to a redistribution of the current into other filaments, which is virtually undetectable. Also during cooling,

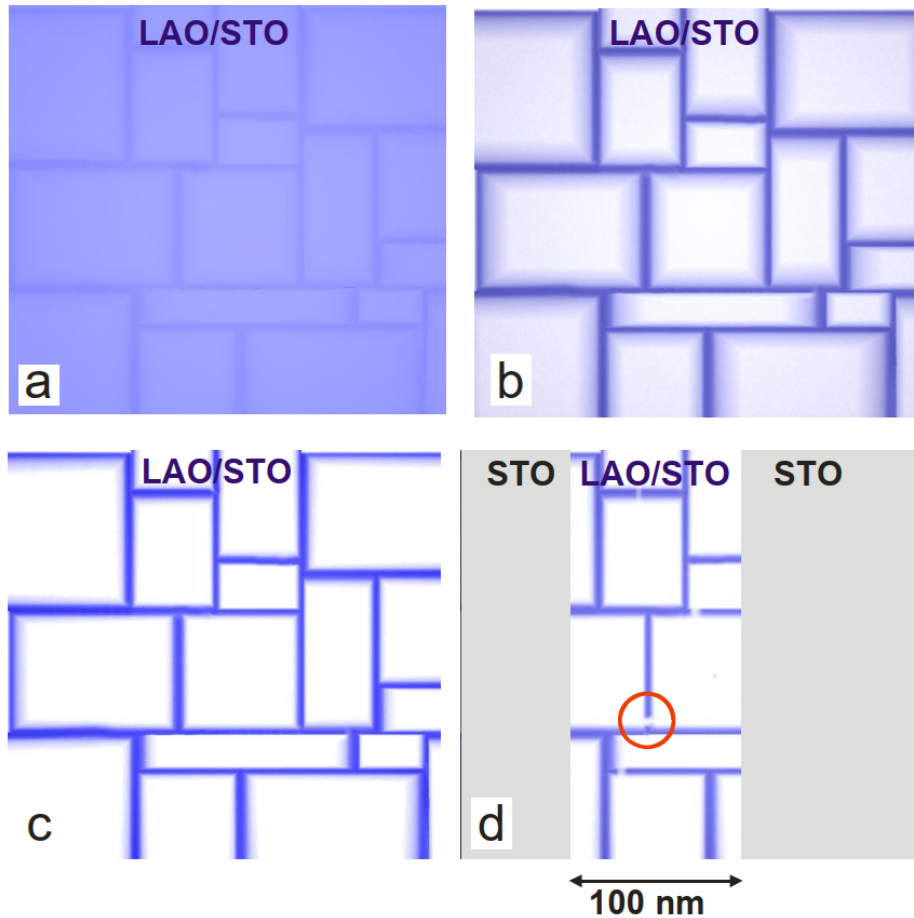


FIGURE 2.11: Simplistic sketch of charge conduction model to explain the resistance anomaly. (a) Below 105K charge conduction starts to concentrate in domain boundaries. (b) As the temperature is further decreased, more and more charge carriers start to accumulate at the domain walls due to increased polarity and dielectric constant of STO. (c) Conduction is only through domain walls (Blue areas) leaving the area between them insulating (White areas). (d) As the lateral size of the structure is decreased, the number of filaments is limited. During warm-up, near phase transition some filaments break (red circle) and conductance will break, increasing the resistance to almost infinity. Adapted from [148].

the effect is not visible since the accumulation of charges does not significantly alter the mobility.

## 2.5 Summary

Recent experiments have confirmed the presence of channelled current flow at the LAO/STO interface especially when the transport experiments are performed below the phase transition temperature of STO. The significance of this channelled current flow becomes more

dominant when the lateral size of the nanostructures approaches the scale of domain walls. Nanostructures exhibit many anomalies in electrical transport which can be explained only by conductivity through domain walls. However, for large-area structures, the charge transport mechanism can still be explained by assuming homogeneous current flow since a large number of domain walls averages out their individual effect on transport properties.

# 3

## Fabrication and nanopatterning of the $\text{LaAlO}_3/\text{SrTiO}_3$ interface

So far we have discussed the properties of the interface and how the transport properties are influenced by the domain walls. This chapter deals with experimental techniques involved in the layer-by-layer growth of  $\text{LaAlO}_3$  on top of  $\text{SrTiO}_3$  and the nanopatterning of the interface. The setup for electronic transport measurements is also discussed along with the results obtained for unpatterned samples.

### 3.1 Preparation of substrate and target

#### 3.1.1 $\text{TiO}_2$ terminated STO substrate

The first step toward the growth of LAO/STO nanostructures is the preparation of STO substrates. As we discussed in the previous chapter (see [chapter 1](#)), conducting interface is generated only when LAO is grown on top of the  $\text{TiO}_2$ -terminated STO substrate. The initial focus is to achieve  $\text{TiO}_2$  termination of the STO substrates, which were bought from CrysTech GmbH, Berlin (Germany), before proceeding to the growth of the LAO layer.

The typical size of the substrate used in this work is  $10 \times 5 \times 0.5 \text{ mm}^3$ .  $\text{TiO}_2$  termination of STO can be achieved using a well-known recipe by Koster et al. [39]. The substrates are cleaned with acetone, ethanol and isopropanol in an ultrasonic bath and finally dried with nitrogen gas. The next step is to put the substrates in DI water in

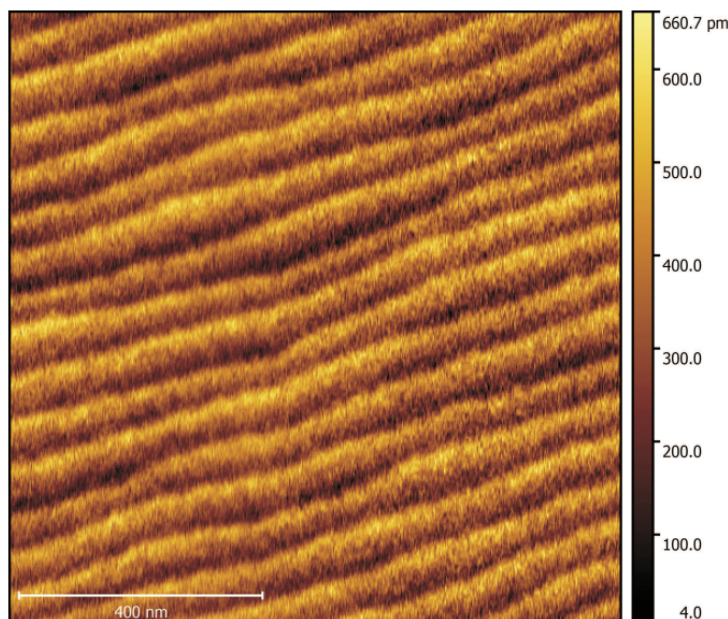


FIGURE 3.1: AFM image of the STO substrate after PLD deposition

the ultrasonic bath for 30 min. The water hydrolyzes SrO unit cell planes which are dissolved by buffered hydrofluoric acid (BHF) by putting the sample for 30 sec in the acid. Terminated STO substrates are annealed in an oxygen atmosphere at  $950^\circ\text{C}$  for 2 hours to obtain straight terrace edges. These steps yield a very clean, smooth and chemically well-defined surface which is suitable for layer-by-layer growth.

### **3.1.2 LAO target preparation**

Before every deposition, the stoichiometric LAO single crystal target is polished with fine sandpaper, wiped on hard lens tissue, rinsed with acetone and isopropanol and finally dried off with nitrogen. The cleaned target is then transferred into the deposition chamber and mounted on a rotatable multi-target holder which carries up to 5 different targets for the in situ growth of complex heterostructures. A final cleaning step is also performed before actual deposition by performing pre-ablation of a square area within the target for several minutes using the same parameter used for the film deposition.

## **3.2 Thin film deposition by PLD**

Now we will discuss the deposition of a thin film of  $\text{LaAlO}_3$  on  $\text{TiO}_2$  terminated  $\text{SrTiO}_3$  substrates. For precise layer-by-layer growth of LAO on STO with unit cell precision, we

use pulsed laser deposition (PLD). The advantages of using PLD and the procedures as well as standard parameters used for the growth of LaAlO<sub>3</sub> on SrTiO<sub>3</sub> are discussed in this section.

### **3.2.1 Pulsed laser deposition**

Pulsed laser deposition is one of the most popular and advanced physical vapour deposition techniques to deposit epitaxial multicomponent oxide thin films at an atomic scale. The key advantages of PLD are that it is a very reliable and flexible method for the deposition of high-quality thin films and many materials can be ablated with a well-controlled growth rate. This technique gained popularity in the later 1980s when PLD has been implemented for the epitaxial growth of high-temperature superconducting films of YBa<sub>2</sub>Cu<sub>3</sub>O<sub>7</sub> (YBCO) [151], which required a very specific stoichiometry in order to achieve the superconducting state. Since then PLD has been utilised for the growth of epitaxial thin films of a wide range of materials.

The sketch of the operation principle of PLD is shown in the [Figure 3.2](#). High-energy laser pulses are directed into a chamber (previously under a high vacuum) with a process gas atmosphere (oxygen) and focused toward the target material. The energy of laser pulses is absorbed below the target surface and if this energy is above the threshold value, the material gets removed, ionized, and accelerated away from the target surface resulting in the formation of a plasma plume. The wavelength of the laser used lies within the range of 200 - 400 nm which ensures that the penetration depth is within the thin surface of the target material and avoids the boiling of the surface. The plasma plume is directed forward and the heated substrate is placed at the end of the plasma plume. The ablated target material is deposited on the substrate and high temperatures at the substrate ensure high film crystallinity [152–155]. A stoichiometric and high-quality film growth can be controlled by adjusting the deposition parameters such as energy density on the target, background oxygen pressure, substrate temperature, target-to-substrate distance and laser pulse frequency. The high-quality film growth makes PLD a widely used method for film growth of complex materials over other deposition methods.

### **3.2.2 Experimental methods**

PLD set-up used for the thin film fabrication is shown in [Figure 3.3](#). In our work, we used a KrF Excimer Laser ( $\lambda = 248$  nm) for the ablation of the target material. The homogeneous part of the laser beam profile is selected by using an aperture. The PLD



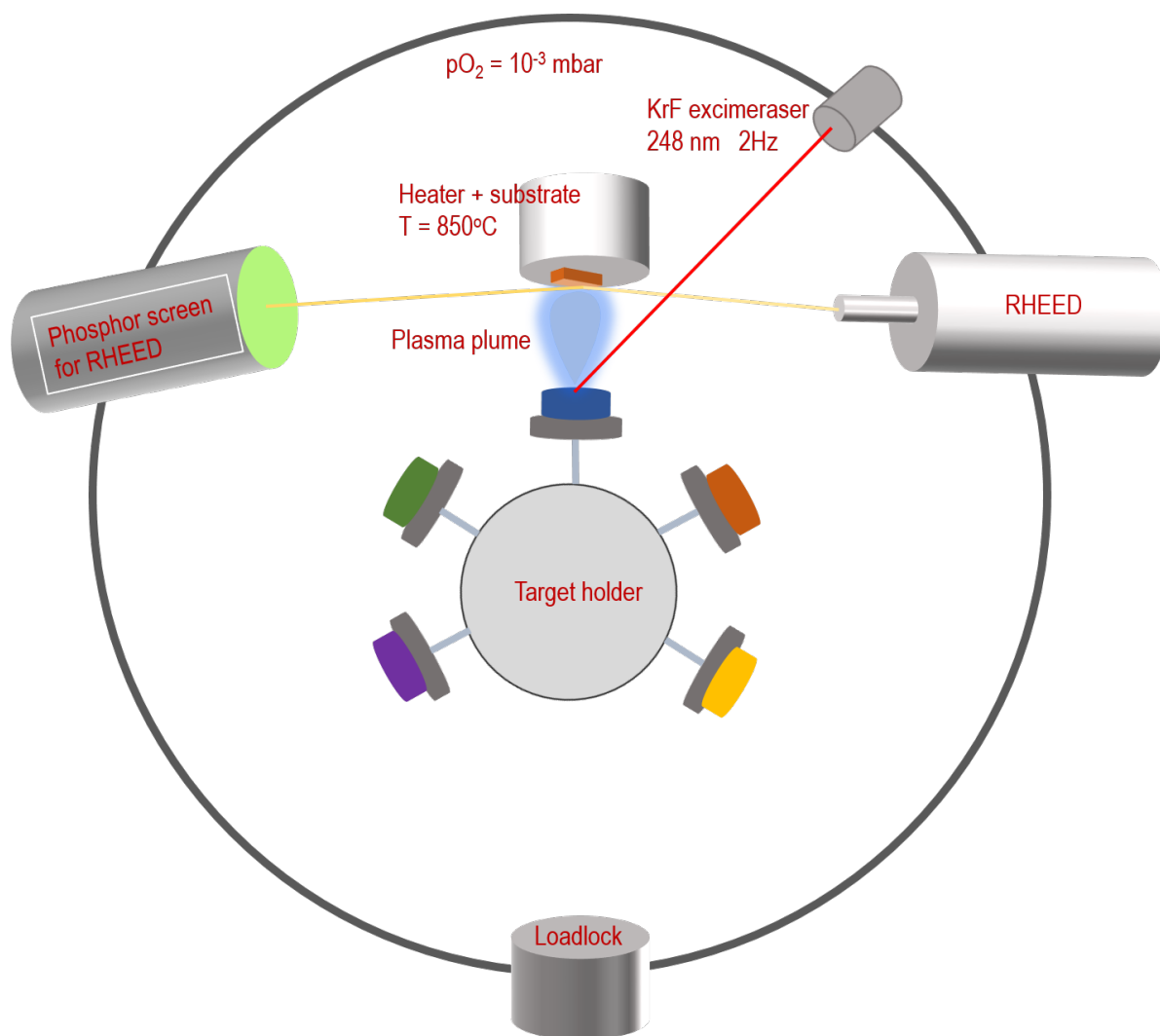


FIGURE 3.2: Schematic illustration of pulsed laser deposition (PLD) principle

high vacuum chamber is maintained at a base pressure in the range of  $10^{-8} - 10^{-9}$  mbar and is connected to a load-lock so that the substrates and targets can be mounted and exchanged without breaking the vacuum of the deposition chamber.

$\text{TiO}_2$ -terminated cleaned STO substrate is glued to the PLD heater using silver paint (dried at  $350^\circ\text{C}$  for 15 mins) in order to assure good thermal contact. The heater along with the substrate is then transferred into the deposition chamber via load lock. After transferring the heater, the temperature of the resistive heater is slowly ramped up using a computer-automated program and the temperature at the substrate surface is measured using a pyrometer. In-situ reflection high-energy electron diffraction (RHEED) is used during the growth to monitor the layer thickness down to the unit cell level. RHEED (reflection high energy electron diffraction) is a versatile technique that can be used to

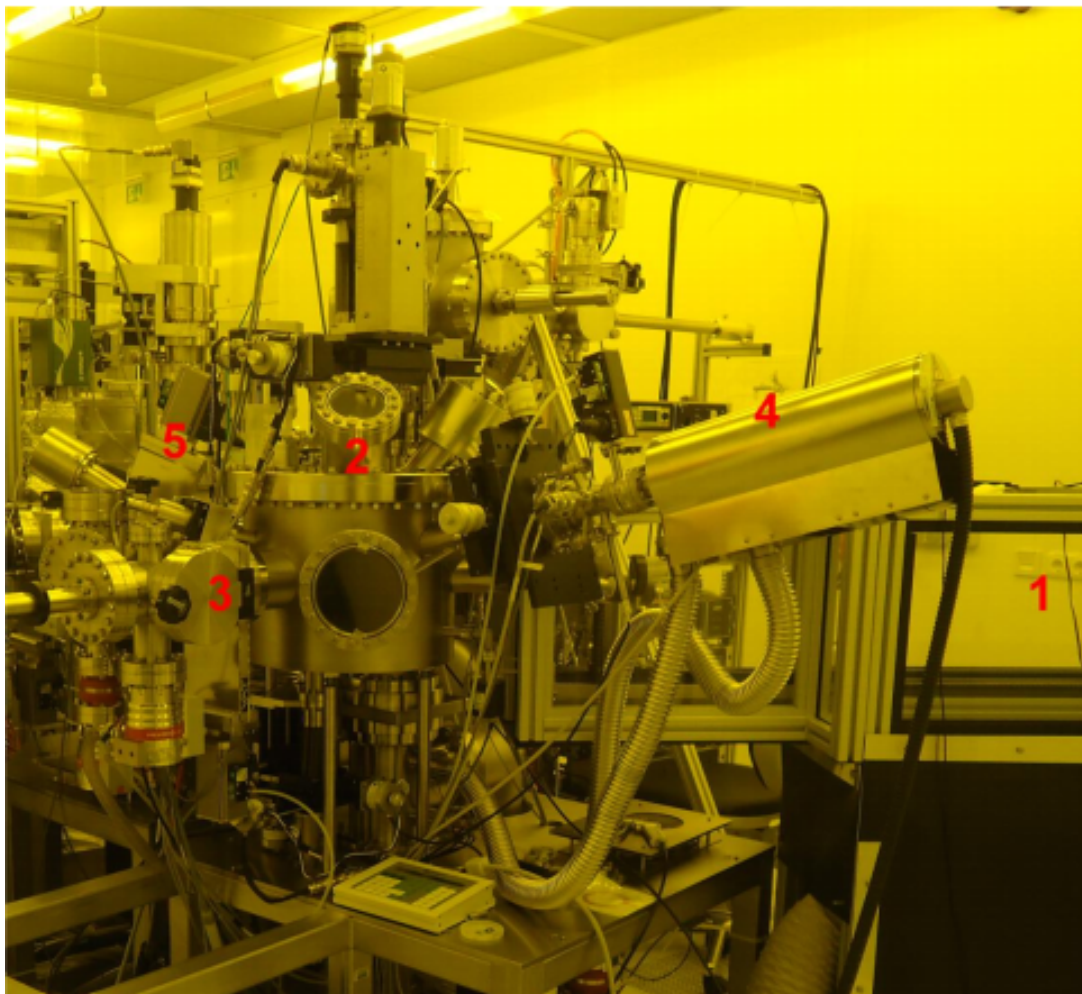


FIGURE 3.3: The PLD setup used in this work. (1) KrF Excimer Laser ( $\lambda=248\text{ nm}$ ). (2) Main deposition chamber. (3) Loadlock. (4) RHEED system. (5) CCD camera

precisely monitor film growth in the deposition chamber. The key benefits are that it is extremely surface sensitive and can be used in situ during crystal formation. Surface atoms diffract electrons, which provide information about the periodic arrangement of the surface atoms [156–159]. RHEED is installed in our PLD chamber and is always employed when growing LAO on STO substrate.

The heater temperature is ramped up to  $300\text{ }^\circ\text{C}$  with a ramp rate of  $15\text{ }^\circ\text{C}/\text{min}$  and then the RHEED signals are aligned. Once the RHEED signal is aligned, then the heater is ramped up to  $850\text{ }^\circ\text{C}$ . During the whole process, the background oxygen pressure is maintained at  $10^{-3}\text{ mbar}$ . Laser fluence and pulse frequency are kept at  $2\text{ J}/\text{cm}^2$  and  $2\text{ Hz}$ , respectively, during the deposition. A fixed distance of  $4\text{ cm}$  is maintained between the target and substrate during deposition. Prior to the actual deposition, the target is pre-ablated for  $5\text{ mins}$  at  $2\text{ Hz}$  to remove any possible surface contamination. After the

final realignment of the RHEED signal, the deposition of 6 unit cells of LAO is carried out. Finally, the samples are cooled down to room temperature while maintaining the oxygen background pressure at  $10^{-3}$  mbar with a smaller ramp rate ( $5^\circ\text{C}/\text{min}$ ).

Background oxygen pressure is very crucial in determining film quality. Background oxygen pressure mainly serves two purposes: firstly, it is used as a reactive species to attenuate and thermalize the plasma plume. Secondly, it is used to maintain the balance between differently charged species in the plume [152]. In addition to these, it is also used to control the kinetic energy, as well as the deposition rate of the ablated species [160]. In the case of the LAO/STO interface, the oxygen pressure has special importance since oxygen vacancies are considered to be one of the sources of doping [161]. Oxygen vacancies are formed in the STO substrate during the growth of thin films of LAO. Samples grown at low oxygen pressure ( $< 10^{-5}$  mbar) exhibits higher carrier density ( $\approx 10^{17} \text{cm}^{-2}$ ) and mobility ( $\approx 10^4 \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ ) at low temperature. These large values can be attributed to the formation of oxygen vacancies. However, when the oxygen pressure was relatively high ( $> 10^{-4}$  mbar), reduced carrier density ( $\approx 10^{14} \text{cm}^{-2}$ ) and mobility ( $\approx 10^3 \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ ) were reported at low temperatures. The role of oxygen vacancies is dominant in the interface conductivity of samples grown at low oxygen pressure. In our work, thin films (6 uc) are grown under oxygen pressure  $10^{-3}$  mbar in order to limit the possible doping by oxygen vacancies.

### **3.3 Nanopatterning of LAO/STO interface**

After the growth of high-quality thin films of LAO on top of TiO<sub>2</sub>-terminated STO, the next step is the nanopatterning of the interface. A reliable and reproducible nanopatterning technique is a crucial step toward successfully implementing the interface in state-of-the-art field-effect-based nanoelectronics. For the past few years, both direct and indirect patterning methods have been successfully implemented for the nanopatterning process. Direct nanopatterning involves using a chemical or dry etching process to remove the LAO film from the undesired area, thus eliminating the conductivity. However, dry etching methods need to be carried out carefully since exposure to high-energy ion beams creates a highly conducting layer on the SrTiO<sub>3</sub> substrate surface at room temperature as well as at cryogenic temperatures. This highly conducting layer makes the device application virtually impossible. An industrial-compatible nanopatterning process has been reported in Minhas et al. [162], which preserves the properties of the patterned structures over time at ambient conditions with dimensions down to 100 nm.

Different indirect patterning techniques were also used by various groups to pattern the LAO/STO interface. The term indirect-patterning technique is used because no physical patterning is done by using these techniques. In these techniques, either an amorphous LAO [163] or AlO<sub>x</sub> hard mask [164] or the conducting AFM tip [75], or low energy Ar-ion beam irradiation [165] was used to pattern the interface.

Schneider et al. [163] used sequential deposition of the LAO method for nanopatterning. In this method, the first 2 uc of epitaxial LAO were deposited on a TiO<sub>2</sub>-terminated (001) STO substrate using pulsed laser deposition at high temperature. The films were created from single-crystalline targets and then cooled down to room temperature in an oxygen environment. Following that, UV-lithography was performed, and amorphous LAO was deposited at room temperature before being patterned by lift-off. After patterning, a certain layer of LAO is deposited under optimal growth parameters resulting in epitaxial growth restricted to regions where the epitaxial LAO surface is still exposed. In contrast, crystalline growth was impeded in the areas covered by amorphous material. The smallest conducting structures created had a width of 200 nm.

Banerjee et al. [164] implemented the AlO<sub>x</sub>-based hard mask method, in which similar patterning steps are involved. At first, AlO<sub>x</sub> is deposited on the STO by PLD at room temperature, followed by patterning using UV lithography. The patterned structures were developed by a developer solution (OPD 4262) which also reacts with exposed aluminium oxide and forms water-soluble alkali-metal aluminates. As a result, the STO substrate was covered with amorphous aluminium oxide with structured openings. Finally, the LAO layer is deposited by high-temperature PLD and then cooled down to room temperature in the deposition atmosphere. Finally, the lift-off was done using a 4M aqueous NaOH solution to remove the AlO<sub>x</sub> layer with amorphous LAO on top.

Cen et al. [75] used a conducting atomic force microscope (AFM) probe to fabricate and eliminate conducting nanoscale structures at the LAO/STO interface. In this method, an insulating LAO/STO heterostructure sample (with 3 uc LAO) was used to induce interfacial conductivity. Oxygen vacancies were created at the LAO surface by the positively charged AFM tip, and these vacancies helped to add electrons to the STO conduction band. Conducting regions were consequently produced. These nanostructures could be used to demonstrate the quantum size effect. However, this method has the drawback that the structures are not stable under ambient circumstances. Furthermore, applying these approaches to create huge area devices or even integrated circuits is challenging.

Paolo et al. [165] employed the combination of optical and electron beam lithography, followed by low-energy ion beam irradiation, to pattern the quasi-two-dimensional electron

gas (q2DEG) at the LAO/STO interface. The LAO film deposited by high-temperature PLD deposition is followed by patterning using photo and e-beam lithography and low-energy Ar-ion irradiation. This patterning process is based on the fact that the decrease in interface conductivity under ion radiation owing to lattice damage is faster than the increase in substrate conductivity, leaving only a small process window for pattern formation. As a result, it is possible to make the interface insulating and prevent unintentional electron doping caused by oxygen vacancies by carefully controlling the irradiation dose. Using this patterning process, structures with lateral dimensions down to 50 nm wide could be fabricated. Even at low temperatures, the structures had long-lasting stability and good electrical transport characteristics. However, an increased resistivity is observed for smaller structures.

These indirect nanopatterning methods are not compatible with industrial processes. They have limited application due to the presence of residues of hard masks or the instability of patterned structures over time.

In this work, we used both direct and indirect nanopatterning techniques for patterning the LAO/STO interface. We compared the results to eliminate any artefacts arising from the etching process which could influence the results. These methods will be discussed in the following sections.

### **3.3.1 Direct nanopatterning method**

For the direct nanopatterning method, we used electron beam lithography [166–168] and chlorine base reactive ion etching (RIE) to pattern the LAO/STO interface while preserving the insulating properties of the interface.

We used a thin film of novolac-based image reversal photoresist for the patterning process. A thinned version of photoresist AR-U 4060 has been spin-coated on the LAO/STO substrate at 5000 rpm for 90 s, resulting in a 300 nm thin layer of resist coating. This resist can be used for positive as well as negative processes and also can be used for photolithography which makes it ideal for mix-and-match processes. The resist contains an amine component that exhibits no influence during positive processes. E-beam lithography is done with an energy of 30 KV and an aperture size of 10  $\mu\text{m}$ . Post-e-beam exposure, the resist is baked at 115 °C for 5 mins followed by UV flood exposure for 30 s. The post-exposure bake makes the amine in exposed areas reacts with indene carboxylic acid, and a cross-linking results which render exposed areas alkali-insoluble. Flood exposure is used to increase the efficiency of the negative process by exposing the unexposed resist to UV

resulting in the formation of alkali-soluble indene carboxylic acid. During UV exposure, the cross-linked area remains unaltered. The sample is developed using photolithographic developer solution AR-300-35 (we have used the developer in dilution of 1:1) followed by rinsing in distilled water. The typical undercut structures particularly well suited for lift-off processes will remain after development. The exposed pattern consists of Hall bars with different respective nominal widths between 100 nm and 500 nm. Large area bond pads have been patterned using the photolithography process performed in a maskless UV lithography machine (Microwriter ML3) using the same resist AR-U 4060.

After E-beam exposure, the sample was placed in an oxygen plasma chamber for a minute at low power to clean the surface before carrying out RIE. Reactive ion etching is performed in an inductively coupled plasma reactive ion etching system (ICP-RIE, Oxford Plasmalab 100) using a BCl<sub>3</sub>-based etching process. The optimum results were obtained with a gas (BCl<sub>3</sub>) flow of 30 sccm and an RF power of 80 W with an ICP power of 1200 W applied. The chamber pressure was held relatively low (6 mTorr) to enlarge the mean free path length of the ions, and the table temperature was maintained at 5 °C. We obtain an etching rate of  $4 \pm 1$  nm/min with these parameters. We fix the processing time of 75 sec to ensure the complete removal of the LAO layer by preserving the insulation behaviour of the STO substrate. After etching, the sample is placed in distilled water for a few minutes and then dried off using Nitrogen gas.

After etching, the resist is removed using N-Ethylpyrrolidone (NEP 300-76) at 80 °C for 1 hour. The resulting patterned structures are stable at ambient conditions. Large area bond pads were patterned using a microwriter and followed by titanium and gold deposition for bonding. The structures are bonded using gold wire for electrical transport measurements.

### **3.3.2 Indirect nanopatterning method**

Large area hall bars, as well as nanostructures, have been prepared using the indirect patterning method. We used AlO<sub>x</sub> based hard mask process, which has been previously employed in Banarjee et al. [164] with some modification. The fabrication process starts with the nanopatterning (e-beam lithography) or large area hall bar patterning (photolithography) as required on TiO<sub>2</sub> terminated STO substrate with an image reversal process using AR-U 4060 resist. After patterning and developing the desired structures using the parameters mentioned earlier (for both UV and e-beam process), we deposited 15 nm of

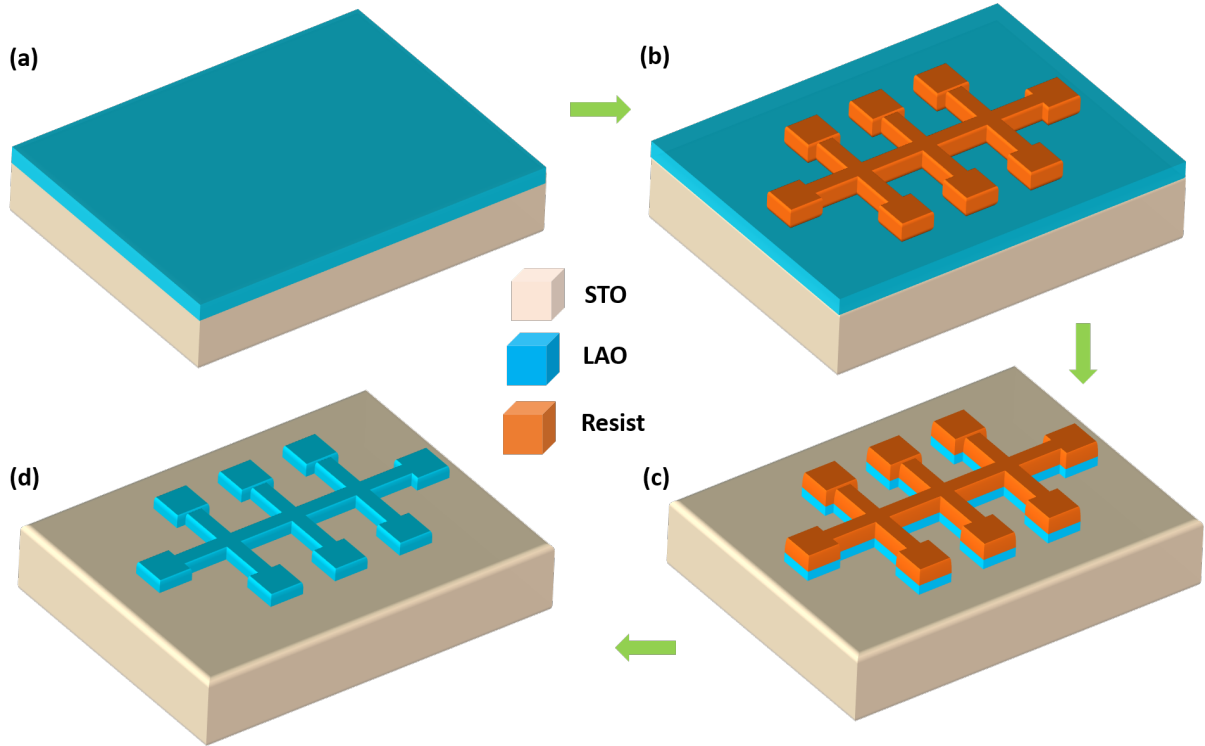


FIGURE 3.4: Step by step process in nanopatterning of the LAO/STO interface by etching method. (a) 6 u.c LAO is deposited on STO using PLD. (b) device patterning is done using lithography techniques. (c)  $\text{BCl}_3$  based ICP-RIE is performed to remove the unwanted LAO layer. (d) Liftoff is performed to remove the residual resist.

$\text{AlO}_x$  in the e-beam evaporation chamber. Lift-off is done by placing the sample in NEP 300-76 for 3 hours at  $80^\circ\text{C}$ . After the lift-off process, all the residual resist has been removed perfectly, leaving the substrate exposed only in the patterned area. Following the lift-off process, 6 u.c of LAO is grown on top of  $\text{TiO}_2$  terminated STO using PLD at  $850^\circ\text{C}$  with  $P_{\text{O}_2}$  of  $10^{-3}$  mbar. After deposition, the sample is slowly cooled down to room temperature while the oxygen pressure is maintained. Laser fluence and pulse frequency are kept at  $2 \text{ J/cm}^2$  and 2 Hz, respectively, during the deposition.

2DEG will not be generated in the substrate areas covered with amorphous aluminium oxide. Nanostructures down to 100 nm in width have been successfully fabricated using this indirect patterning method with good insulation between the structures.

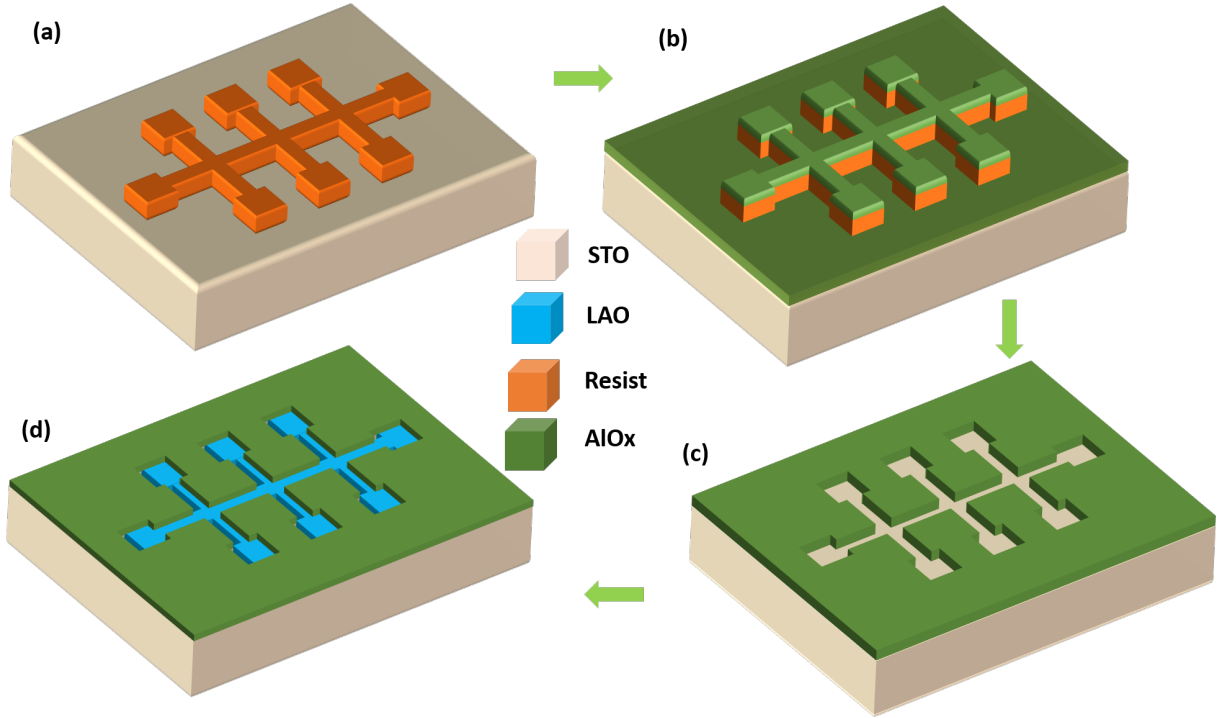


FIGURE 3.5: Patterning process using  $\text{AlO}_x$  mask method. (a) initially, patterning of the device is done using Lithography followed by deposition of a thin layer of  $\text{Al}_2\text{O}_3$  (b). (c) The lift-off is done to remove  $\text{Al}_2\text{O}_3$ . (d) LAO is deposited on top of STO using PLD in the final step. It should be noted that the amorphous LAO layer is deposited on top of the  $\text{Al}_2\text{O}_3$ , which is not shown in the diagram.

### 3.4 Electronic properties of the interface

The experimental setup for measuring electronic transport properties is described in this section. Electronic transport properties (such as conductivity, electron density, and mobility) provide further information regarding the quality of the thin film and its usability in future devices, in addition to structural properties. All transport measurements for the patterned structures are carried out in a Hall-bar geometry, while for the unpatterned structure, we use the van-der-Pauw method for transport measurements.

#### 3.4.1 Measurement setup

The samples are glued with low-temperature varnish in the chip carrier after patterning the Hall bars, as illustrated in [Figure 3.6 a](#), which are tailored to fit into the various experimental setups in the labs. At the probe station, preliminary characterisation, including the I/V curve, is performed at room temperature. This characterisation is done to check



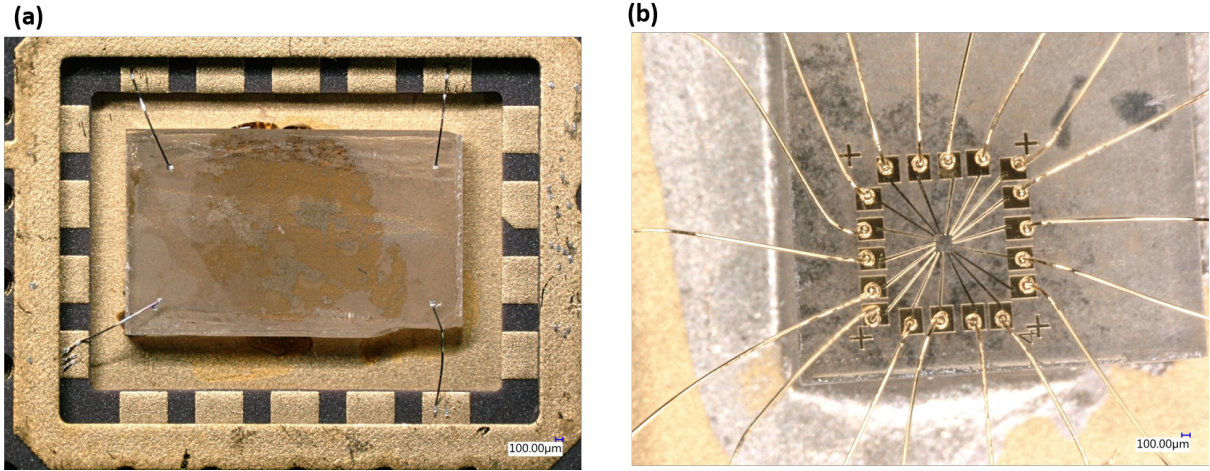


FIGURE 3.6: (a) Photo of a sample mounted on a chip carrier and contacted by Al wire bonds for van-der-Pauw measurements. (b) Shows the sample bonded by gold wire for hall bar measurements. This sample is attached to the chip carrier by silver paste for back gate contacts.

whether any devices are shorted. Following this preliminary test, gold pads of the chip carriers are wire-bonded to the Hall bars. The samples are bonded to the chip carrier via gold wire bonding (ball-to-wedge bonding). The electronic transport measurements are carried out in a  $^4\text{He}$  bath cryostat in the temperature range of 2 K - 300 K after the sample has been bonded. Temperature-dependent transport measurements are done during cool-down as well as during warm-up to identify the possible hysteresis.

The electronic transport measurement setup, as shown in [Figure 3.7](#), used in this thesis consists of an Oxford cryostat with variable temperature insert from 2 K - 300 K, temperature controller, two 7.5 Digit nanovoltmeters (Agilent 34420A) and peripheral components like a computer which is used to control the measurement setup by a suitable program (Labview virtual instruments). The output bias voltage is provided by a digital-analogue converter (DAC, self-built external equipment or input/output controllers installed on the computer) that can be addressed by the program. The digital voltage signal is converted to an analogue voltage, which is then applied to the measurement circuit. The determination of sample resistance is a crucial component of every transport investigation. By connecting a reference resistor  $R_{ref}$  in series with the sample  $R_s$  and grounding the other contact of the  $R_{ref}$ , sample resistance can be measured. The voltage drops across the sample and can be monitored using differential amplifiers (diff.amp.). Using Ohms Law, the voltage drop across  $R_{ref}$  is utilised to determine current (I). Both voltages must be monitored in this manner. This job demands the employment of a highly sensitive and precise two-channel voltmeter (Agilent 34420A) capable of measuring voltages in the nV range, as previously stated. For some specific experiments, we require two nanovoltmeters

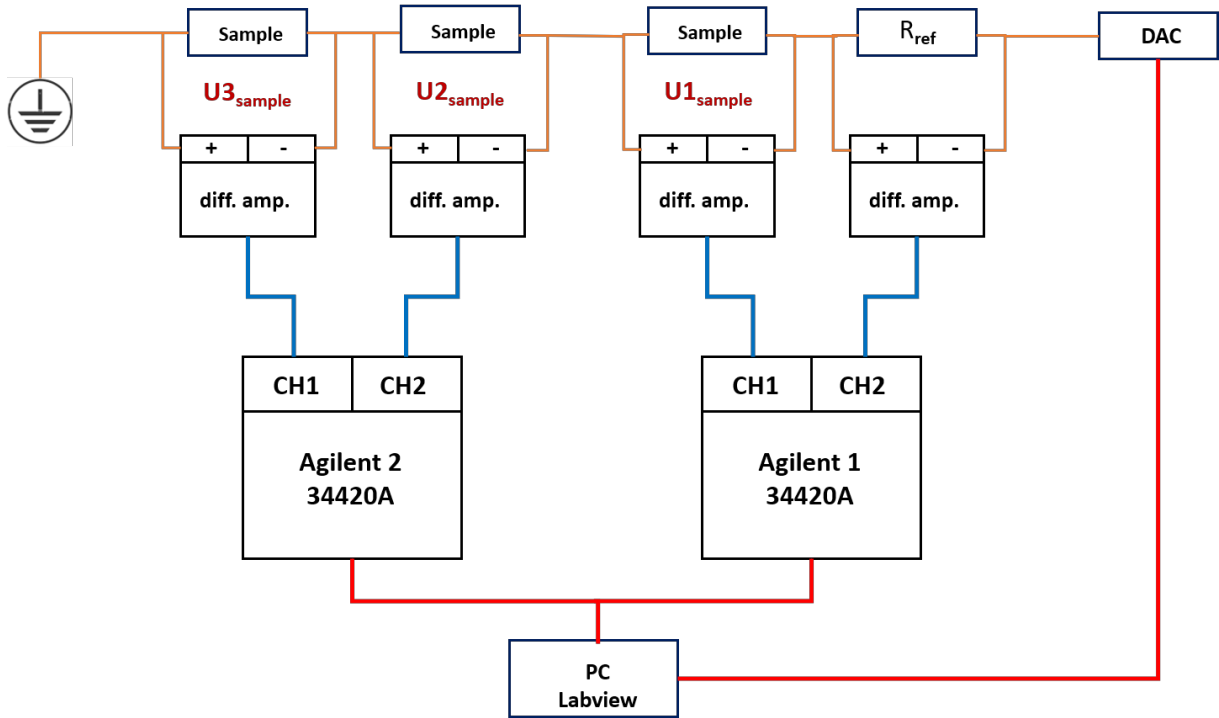


FIGURE 3.7: Schematic diagram of the measurement circuit including peripheral components (PC, digital-analogue-converter (DAC), Reference resistor ( $R_{ref}$ ), differential amplifiers (diff. amp.), Agilent voltmeter). This configuration is used to measure the sample resistance in the Hall-bar geometry.

since we have to measure four different voltages simultaneously (anisotropic MR measurements). Two channels of the second nanovoltmeter are employed for the additional two voltage measurements. As shown in the diagram (Figure 3.7), the voltmeter's output channel is connected to the measurement program. The maximum bias voltage that can be used for the measurement is limited to  $\pm 10$  V due to the limits of DAC ( $\pm 2$  V for the differential amplifiers). We mostly performed constant voltage measurements and typically used a voltage of 100 mV and reference resistance in the range from 10 k $\Omega$  - 1 M $\Omega$ .

### 3.4.2 Large area samples

We began this study by investigating unpatterned LAO/STO interfaces, that is, the LAO film and the electron gas that extends across the entire sample surface. The van-der-Pauw approach is used to contact these un-patterned materials for electronic transport

measurements. A variable temperature  $^4\text{He}$  bath cryostat is used to conduct the electronic transport experiments. Electronic transport experiments revealed a conducting electron gas at the interface between  $\text{TiO}_2$ -terminated STO and LAO for a 6 uc sample. [Figure 3.9 a](#) depicts the  $R(T)$  curve of a 6 uc sample. From 280 K to 4.2 K, a typical reduction in resistance of two orders of magnitude is observed at the conducting interface. These experiments indicate that the electrical properties of the samples are consistent with the polar discontinuity model proposed by Ohtomo and Hwang in their groundbreaking paper on the LAO/STO interface.

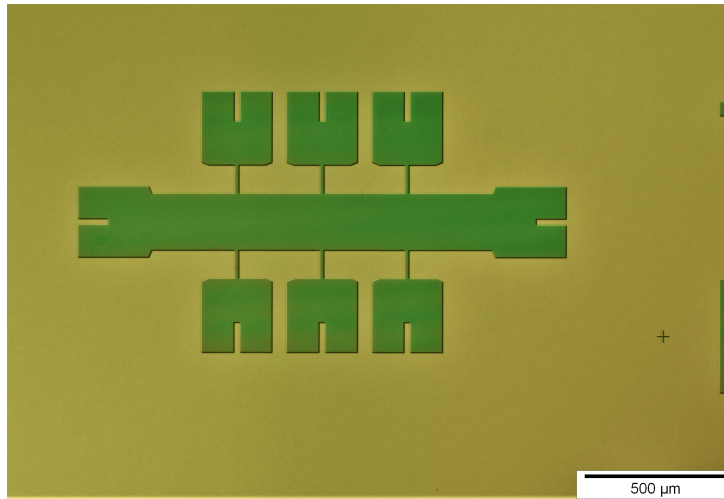


FIGURE 3.8: Optical microscopy image of 200  $\mu\text{m}$  wide hall bar.

The carrier density ( $n$ ) and carrier mobility ( $\mu$ ) in large area samples were calculated using hall measurements. The temperature-dependent carrier density and mobility are depicted in the diagram ([Figure 3.9 b](#)). Hall measurements show that the carrier density for all structures is in the range of  $n \sim 10^{13} \text{ cm}^{-2}$  at all temperatures, which is in good agreement with literature values. Thermally activated carriers were found in all of the samples. The carrier density increases rapidly until it reaches 100 K, at which point it becomes nearly constant, as shown in [Figure 3.9 b](#). The highest values of mobilities are in the range of  $\sim 2200 \text{ cm}^{-2} \text{ V}^{-1} \text{ s}^{-1}$  and  $\sim 10 \text{ cm}^{-2} \text{ V}^{-1} \text{ s}^{-1}$  at 4.2 K and 300 K respectively which is also in good agreement with the literature values.

### 3.4.3 Transport properties of nanostructures

The same measurement setup was used for the transport measurements of nanostructures also. At both room and low temperatures, the area between the structures acts as an insulator with resistance in the few 100 G $\Omega$  range. Down to 4.2 K, all fabricated Hall

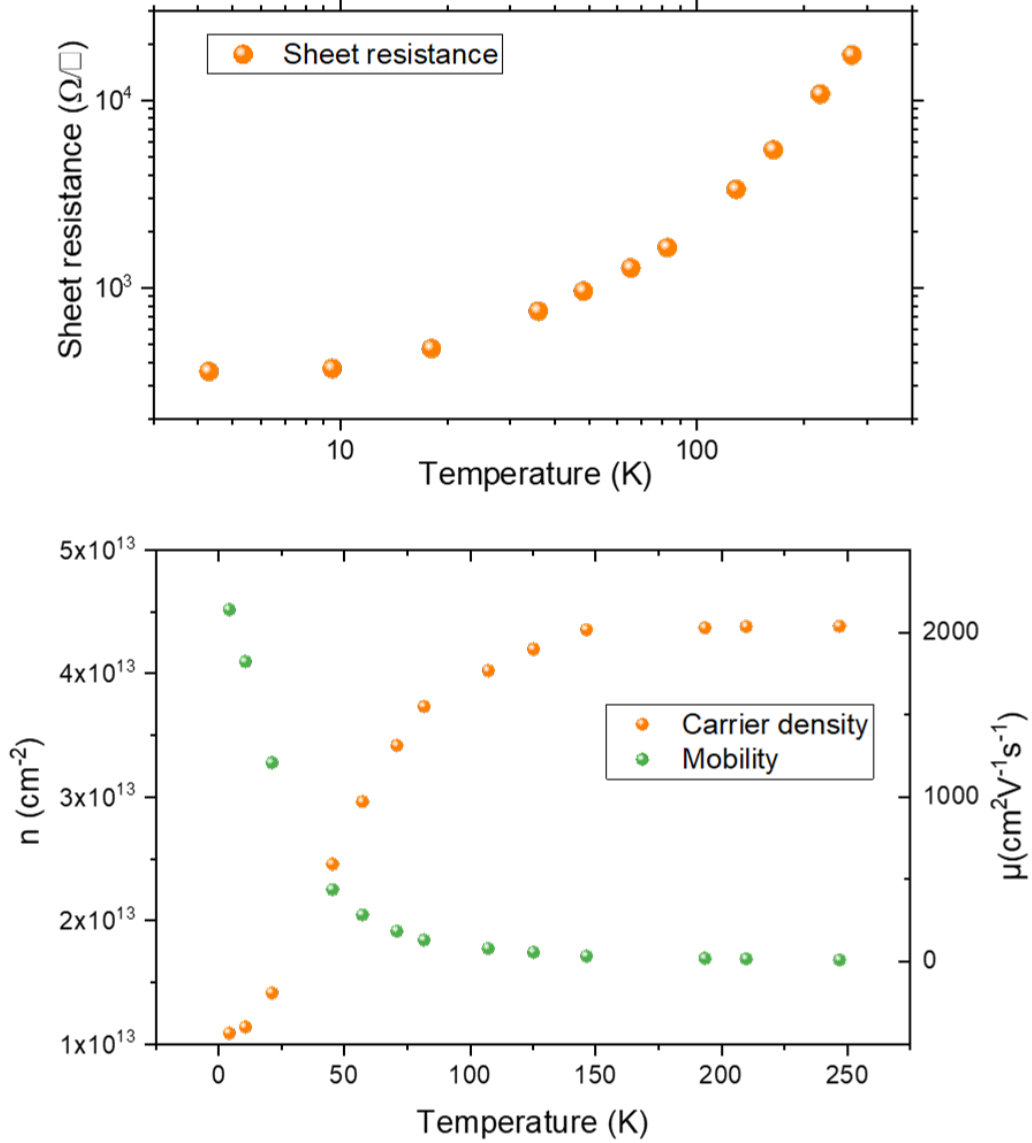


FIGURE 3.9: (a) Temperature dependent resistance of a 6 uc LAO/STO heterostructure. (b) Temperature-dependent carrier density ( $n$ ) and mobility ( $\mu$ ) of 6 uc LAO/STO.

bars exhibit metallic behaviour (see Figure 3.10 a). The small increase in resistance at low temperatures is not unique to nanoscale Hall bars but can also be found in large-area transport structures. The carrier density ( $n$ ) and carrier mobility ( $\mu$ ) in nanostructure samples were calculated using hall measurements as shown in Figure 3.10 b. Using the formula  $n = \frac{-1}{R_{He}}$ , the carrier density ( $n$ ) is calculated. The highest values of mobilities are in the range of  $\sim 550 \text{ cm}^{-2} \text{ V}^{-1} \text{ s}^{-1}$  and  $\sim 6 \text{ cm}^{-2} \text{ V}^{-1} \text{ s}^{-1}$  at 4.2 K and 300 K respectively. These values are lower than those reported in the literature at low temperatures. This decrease in mobility can be attributed to sidewall depletion after the etching process.

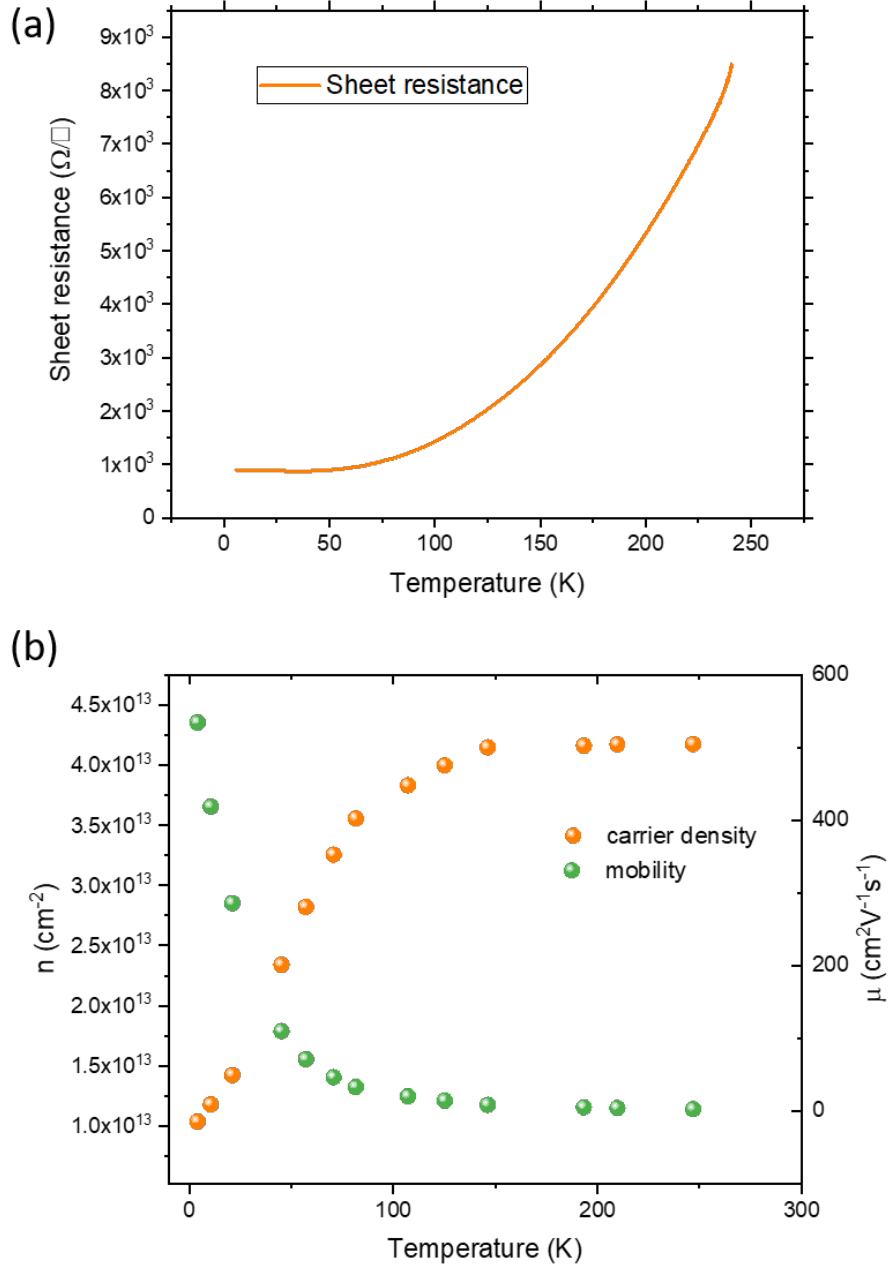


FIGURE 3.10: (a) Temperature dependent resistance of a 100 nm wide LAO/STO nanostructure during cool-down. (b) Temperature-dependent carrier density ( $n$ ) and mobility ( $\mu$ ) of a 100 nm wide nanostructure.

Because the conductivity of the depletion region is lower than that of the core region, it will affect the structure's mobility. Electron scattering at the nanostructures' edges could also be a contributing factor.

The resistance of the electron gas at the interface between two band insulators, LAO and STO, drops monotonically with temperature in large area Hall bars (Width = 200  $\mu\text{m}$ ),

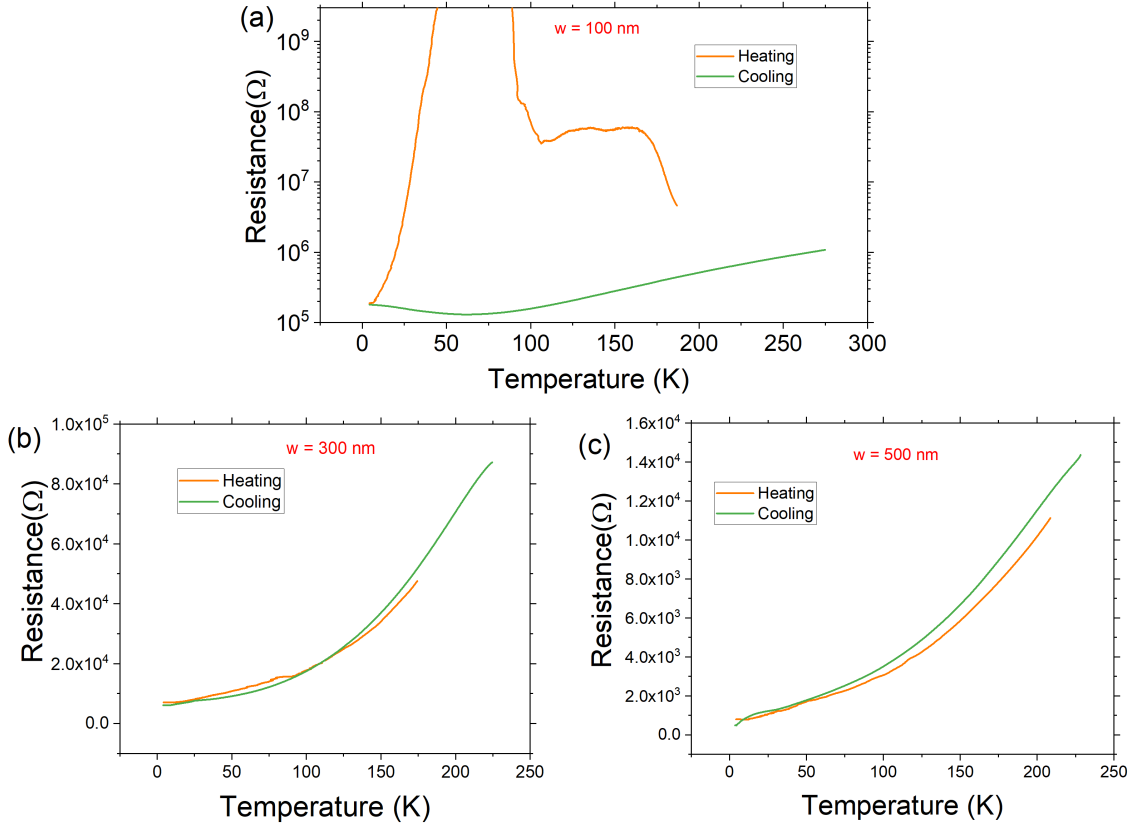


FIGURE 3.11: Here, we present the temperature-dependent resistance measurement carried out on nanostructures with different widths (both warm-up and cool-down). (a) Temperature-dependent resistance anomaly observed on 100 nm wide LAO/STO nanostructure during the warm-up at 80 K. (b) A small resistance peak has been observed for a 300 nm wide nanostructure. (c) For a 500 nm structure, the resistance anomaly is completely suppressed.

and the R-T curves during cooling and warm-up are identical. The resistance follows the same temperature dependence during the introduction and cool-down cycles. Both transport models, polar catastrophe, and the presence of oxygen vacancies agree with this behaviour. The transport in nanostructures has been reported in the literature; however, in one technique, nanopatterning was done using a conductive atomic force microscope (AFM) tip [75] which locally induces conductivity on a non-conducting interface. In contrast, in the other study, the LAO/STO interface was patterned using ion implantation [165]. It should be noted, however, that Aurino et al. [169] did not look into cool-down and warm-up curves. No effect of structural transition of the STO substrate on the LAO/STO interface has been observed in any of these studies.

When temperature-dependent resistance measurements were performed in nanostructured samples (Figure 3.11), a unique behaviour was observed. Even though the cooling

curve matches that of large-area structures, the warm-up curve shows one or two pronounced resistance peaks (around 80 K and 170 K) as in (Figure 3.11 a), which typically occur at temperatures associated with structural phase transitions in STO substrate and can be explained by the filamentary charge conduction model as described in section 2.4. The resistance peak vanishes as the lateral width of the structure becomes 500 nm (Figure 3.11 c), which is in excellent agreement with the literature [148].

### **3.5 Summary**

In this chapter, we discussed the fabrication tools and techniques utilised for the LAO/STO interface nanopatterning. Nanostructures were fabricated using direct and indirect patterning methods for better comparison of the results and to avoid any possible artefacts that may arise from the etching. In the direct patterning technique, we use ICP-RIE to fabricate nanostructures down to 100 nm and the  $\text{Al}_2\text{O}_3$  mask method was used for nanofabrication as an indirect patterning technique. In the final section, we discuss the transport properties of both large-area devices and nanostructures. Nanostructures (< 500 nm) always exhibit a resistance peak around 80 K during warm-up and can be linked to structural phase transition in STO.

# 4

## Magnetotransport measurement on the interface

This chapter <sup>1</sup> deals with the magnetoresistance measurements done on the LAO/STO interface to investigate the orientation-dependent anisotropy in MR. Interfaces between complex oxides show great potential for future electronics [12]. Since the discovery of the high mobility electron gas at the interface of  $LaAlO_3$  (LAO) and  $SrTiO_3$  (STO) in 2004 [9], a lot of studies have been conducted. Those studies revealed more interesting properties of the interface such as two-dimensional superconductivity, induced ferromagnetism, gate tunability, highly efficient spin-charge conversion etc [10, 13, 15, 28, 171, 172]. Enhanced room temperature mobility of LAO/STO nanowires [173] holds great promise towards its room temperature application. Studies conducted by Dubroka et al. [174] show that the confinement region of the electron gas extends into the STO substrate.

The influence of domain walls on the transport properties of the interface is discussed in detail in [chapter 2](#). Several studies have revealed that the domain patterns also affect other STO-based systems as well as bulk STO [175–179]. In confined systems, however, the domain walls can start to massively influence the transport properties. In 2017 Goble et al. [180] demonstrated that the resistivity perpendicular to a domain wall is higher than along the domain wall. Only recently, more evidence for domain wall conduction was presented by [181] who found a Hall-effect-like transverse resistance at zero fields that can be explained by asymmetrically distributed domain walls that lead to the appearance of transverse voltages upon current flow.

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<sup>1</sup>This result has been published in Ref. [170]. Part or whole of this published work is used in this chapter.



It is plausible that transport effects should exist that are dominated by the domain wall conductance and cannot be explained by the mainstream theory on LAO/STO interface conductivity. These effects would mainly appear in LAO/STO nanostructures, because for transport phenomena in large area LAO/STO the existing complex multiband models are clearly able to explain the observations based on a quasi 2D conducting interface. Based on a process for the fabrication of LAO/STO nanostructures [162] we have designed a number of experiments that should clearly reveal the interplay of domain wall conductivity, transport, and magnetotransport properties on the nanoscale. In LAO/STO we distinguish two types of domain walls. One type (type 1) is oriented perpendicular to the surface and along the  $[110]$  and  $[1\bar{1}0]$  crystalline directions in the substrate plane. The other type is oriented along the  $[100]$  and  $[010]$  crystalline directions in the plane but is tilted with respect to the surface. As a consequence not only the resistivity of the two types of domain walls may be different. A magnetic field nominally perpendicular to the 2DEG would be in plane of type 1 domain walls and tilted with respect to type 2 domain walls. This is crucial because in plane and (partly) perpendicular magnetic fields typically cause magnetoresistance that can be different in magnitude and/or sign, respectively. In addition, it should be noted that due to the different possible in-plane orientations of the different domain walls a current path through a structure can strongly vary in length and resistance depending on the contributing respective domain walls.

The consequences can be checked by the following investigations. 1) Because of the different domain wall types we expect a random distribution of resistance values at low temperatures for nominally identical nanostructures. Warming up through the phase transition and cooling down again should result in a different configuration and different resistance values for the same structure. 2) Because of the different types of domain walls and their possible alignment within the crystal lattice it may be possible that this randomness still shows some systematics with respect to the crystalline orientation of the nanostructures. 3) Magnetoresistance measurements in a perpendicular magnetic field on nanostructures with a low number of domain walls should yield a result different from large area LAO/STO and also strongly vary in magnitude and even sign because, with respect to the domain walls, the magnetic field is either in plane or tilted but never perpendicular. Also, these results should be modified by warm-up and cooling.

In this chapter, We will discuss the set of experiments in which a particular nanostructure design allows us to precisely verify/nullify these assumptions.

## 4.1 Sample Fabrication

The fabrication of the samples starts with the deposition of a 6-unit cell layer of LAO on  $TiO_2$  terminated STO (001) using Pulsed laser deposition (PLD) in an oxygen atmosphere with  $p_{O_2}$  of  $10^{-3}$  mbar at  $850^\circ\text{C}$ . Laser fluence and pulse frequency are kept at  $2\text{ J/cm}^2$  and 2 Hz, respectively. Reflection high energy electron diffraction (RHEED) is used to monitor the layer thickness with unit cell resolution during the growth. After deposition, the sample is slowly cooled down to room temperature while the oxygen pressure is maintained. A thin film of novolack-based image reversal resist is deposited by spin coating for patterning, as described in Section 3.5. For our negative process, we used AR-U4060 photoresist. Following that, e-beam lithography is used to expose the sample. The exposed pattern is made up of nanosized Hall bars up to 100 nm in dimension. The developer solution was used to develop the sample (AR-300-35, we have used the developer in dilution of 1:1). Following the development, the LAO layer is completely removed using a  $\text{BCl}_3$ -based reactive ion etching process in an inductively coupled plasma reactive ion etching system (ICP-RIE), Oxford Plasmalab 100. After etching, the resist is removed at  $60^\circ\text{C}$  for 3 hours with N-Ethylpyrrolidone. With this process, we are able to fabricate high-quality nanostructures with lateral dimensions down to 100 nm (Figure 4.2). The resulting patterned structures are stable at ambient conditions. The samples are bonded and electrical transport measurements are carried out in a  $^4\text{He}$  bath cryostat with a variable temperature insert equipped with a superconducting magnet that allows a maximum magnetic field of 10 T.

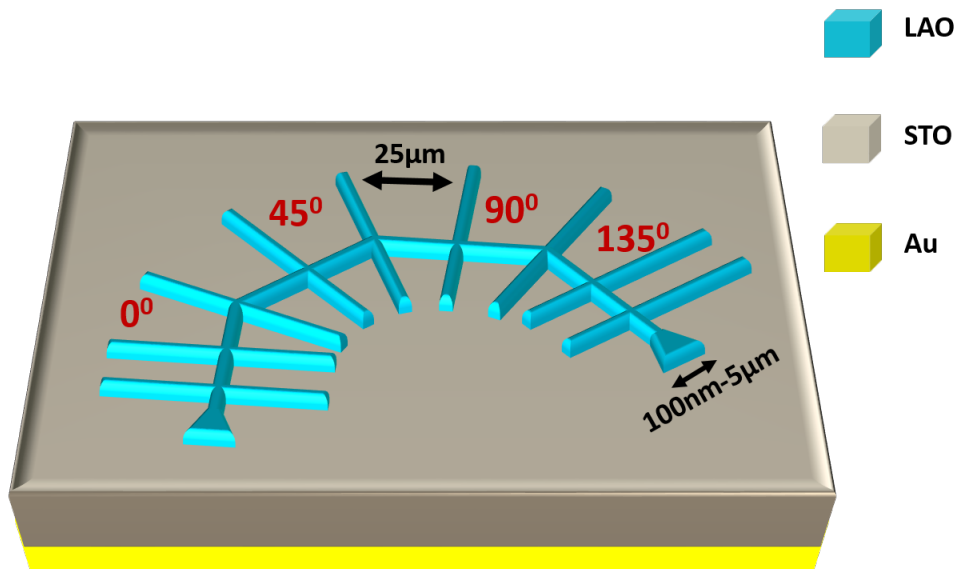


FIGURE 4.1: Sample geometry used for the measurements which is inspired from [182].

We used the sample geometry as shown in [Figure 4.1](#) for the experiments. This geometry is inspired by Hupfauer et al. [[182](#)] who used a similar structure, however, for a different purpose. We have a continuous Hall bar that consists of four connected segments, each with six voltage probes for the measurement of longitudinal or transversal resistance. The segments are aligned at  $0^\circ$ ,  $45^\circ$ ,  $90^\circ$ , and  $135^\circ$  with respect to the sample edge which corresponds to a major crystalline axis (100 or 010). The samples are cooled down at a rate of approx. 5 K/min and warm-up are done at a rate of approx. 2.5 K/min whenever required. The resistance is always measured in a four-probe geometry. Voltages are measured using custom-made zero drift voltage amplifiers and two Agilent 34420A 7.5 Digit nanovoltmeter with four measurement channels in total. Current is measured by measuring the voltage over a series resistor of  $1\text{M}\Omega$ . We apply a DC voltage of 100 mV across the sample and the series resistor. Because of the design, we are able to measure the resistance of 3 nanostructures oriented at different respective angles simultaneously keeping all other parameters constant thus providing higher reproducibility and better comparability of the results.

Now we will discuss the results obtained after the measurements on this special sample geometry. We have performed a series of measurements on structures with  $2\mu\text{m}$  to 100 nm in width to investigate the anisotropic transport properties of the LAO/STO interface.

## 4.2 Results

As a first test, we investigate the temperature dependence of the resistance for  $2\mu\text{m}$  wide structure of different respective crystalline orientations using the Hall bar geometry from [Figure 4.1](#) to carry out the resistance measurements. [Figure 4.3 a](#) shows the temperature dependence. Cooling curves for a set of differently oriented structures of  $2\mu\text{m}$  width show the typical metallic behaviour and do not show any anisotropy. This behaviour is as expected since a large number of domain walls in large-area structures averages out their individual contribution and we would not observe any effect.

In the next step, we investigated the magnetoresistance (MR) in differently oriented structures. For the MR measurements, the magnetic field is applied perpendicular to the sample surface. The field is swept from  $B=-6\text{ T}$  to  $B=+6\text{ T}$ . We first discuss the magnetoresistance for structures of  $2\mu\text{m}$  width. Independent from the orientation, these structures show a large positive magnetoresistance which is quadratic in the magnetic field as shown in [Figure 4.3 b](#). The large ordinary positive MR observed in the  $2\mu\text{m}$  wide bars showed a relative MR of  $\Delta R/R > 50\%$  at  $B=6\text{ T}$ . This out-of-plane positive MR is due to

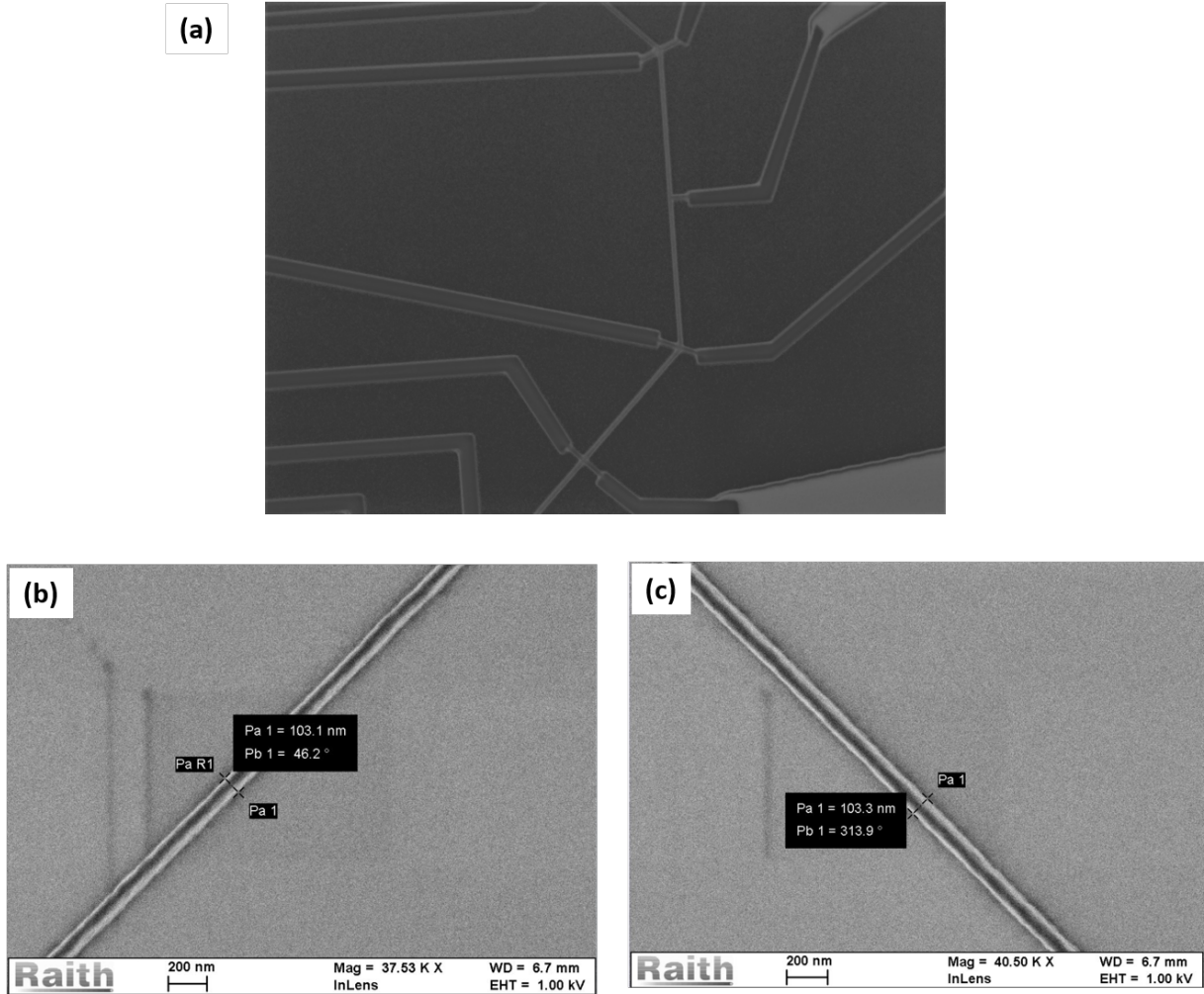


FIGURE 4.2: (a) Optical and (b),(c) SEM images of hall bars oriented at two different angles ( $45^\circ$  and  $135^\circ$ .)

orbital effects often dubbed as ordinary magnetoresistance [183–186]. This quadratic MR is in good agreement with existing multi-band models for large area LAO/STO because it can only appear when more than one band contribute to the transport cite [187–189]. It should be noted that there are small differences in the MR for differently oriented stripes; nevertheless, the main contribution is identical for all orientations.

#### 4.2.1 Anisotropic transport in LAO/STO nanostructures

We have investigated the temperature dependence of the resistance for four nanostructures of different respective crystalline orientations using the Hall bar geometry to carry out the resistance measurements. The results are shown in Figure 4.4 a. At room temperature, there is no significant difference in resistance between the four different orientations of

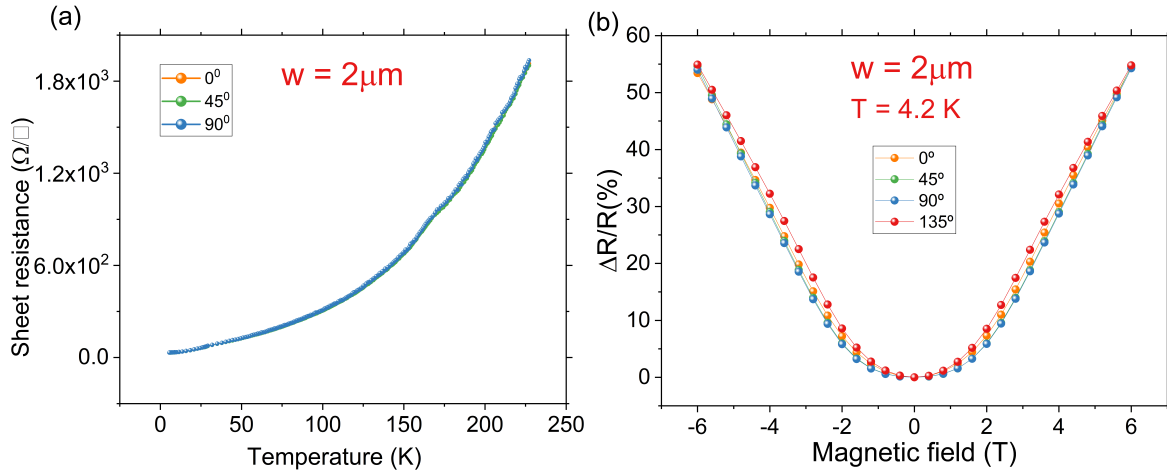


FIGURE 4.3: (a) Shows the temperature dependence of resistance for a large area ( $2 \mu\text{m}$ ) structure with three different orientation angles  $0^\circ$ ,  $45^\circ$  and  $90^\circ$ . (b) No anisotropy in magnetoresistance with orientation for a  $2 \mu\text{m}$  wide hall bar was observed.

the nanostructures. Also, during cool-down, the temperature decreases monotonically and identically for all four structures as expected, but only down to the approximate  $T_{PT}$  of STO (105 K). Below this temperature, the four respective resistance values start to deviate. For three of the crystalline directions, the resistance also starts to increase again below approximately 40 K, an effect that is not unknown for large-area structures. This increase at lower temperatures is often attributed to the onset of weak localization, electron-electron interaction, or the Kondo effect [10, 185, 190]. There is a significant difference in the sheet resistance at 4K for different orientations. After initial cooling down, the respective sheet resistance values for the four different orientations were  $1 \text{ k}\Omega/\square$  ( $0^\circ$ ),  $2.1 \text{ k}\Omega/\square$  ( $45^\circ$ ),  $1.6 \text{ k}\Omega/\square$  ( $90^\circ$ ), and  $1.4 \text{ k}\Omega/\square$  ( $135^\circ$ ). This difference in sheet resistance values along different stripes is in agreement with the random orientation of domain walls and filamentary conduction.

Orientation	Sheet resistance at 4.2K after initial cooldown	Sheet resistance at 4.2K after warmup cycle
$0^\circ$	$1 \text{ K}\Omega/\square$	$2 \text{ K}\Omega/\square$
$45^\circ$	$2.1 \text{ K}\Omega/\square$	$2.16 \text{ K}\Omega/\square$
$90^\circ$	$1.6 \text{ K}\Omega/\square$	$2.65 \text{ K}\Omega/\square$
$135^\circ$	$1.4 \text{ K}\Omega/\square$	$1.7 \text{ K}\Omega/\square$

TABLE 4.1: Shows the change in sheet resistance of 100nm structure after the warm-up cycle to 200K (above the phase transition temperature 105K)

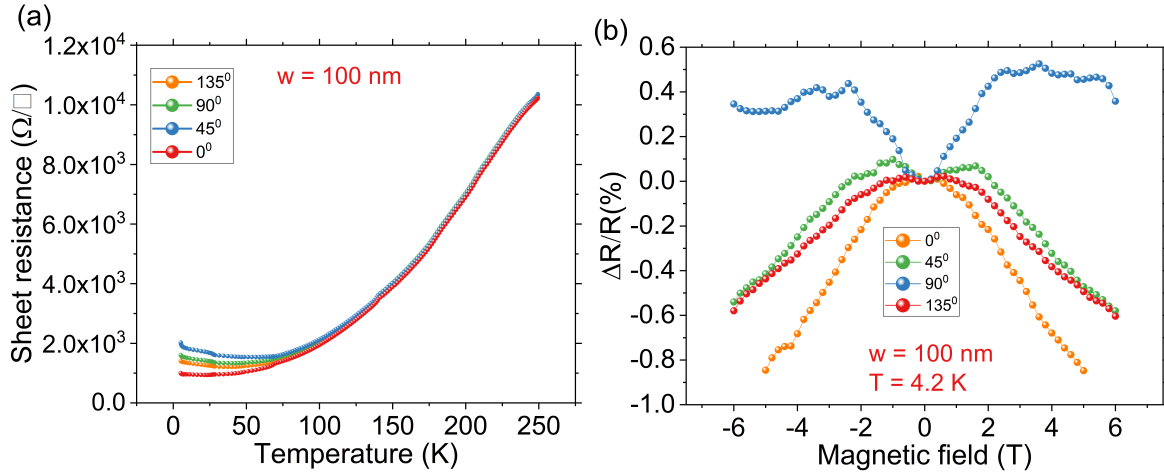


FIGURE 4.4: (a) variation of resistance with temperature for different orientations of a 100 nm structure (sample 1). A clear deviation of the resistance for differently aligned sections of the Hall bar appears when the temperature is below 100K. (b) Anisotropy in magnetoresistance with orientation in 100 nm was observed. For the nanostructures, the MR is small compared to the  $2\mu\text{m}$  structure.

If this variation in base temperature sheet resistance is linked to the random orientation and distribution of domain walls, warming the sample through the phase transition temperature should give completely different values. To confirm this, we test whether warming and cooling again through the  $T_{PT}$  changes the result of the experiment. For the sake of simplicity, we only measure the resistance at 4 K. We observed no significant change in sheet resistance when the sample is heated to  $T_{max} < T_{PT}$ . For heating with  $T_{max} > T_{PT}$  the sheet resistances change significantly but still randomly to  $2\text{ k}\Omega/\square$  ( $0^\circ$ ),  $2.2\text{ k}\Omega/\square$  ( $45^\circ$ ),  $2.7\text{ k}\Omega/\square$  ( $90^\circ$ ), and  $1.7\text{ k}\Omega/\square$  ( $135^\circ$ ). This is consistent with a random formation of domain walls at the  $T_{PT}$ . We have repeated the experiment several times and also for different structures. Although we might have expected a preference for higher or lower resistance values for certain crystalline orientations, we cannot observe any significant preference for higher or lower values for any crystalline direction. This can be due to too low a number of experiments for valid statistics or due to the absence or smallness of the effect.

Now we focus our attention on the magnetoresistance measurements. For better understanding and comparison, we have included results from two nominally identical samples labelled sample 1 and sample 2. For the MR measurements, the magnetic field is applied perpendicular to the sample surface. For nanostructures, we get a completely different MR behaviour w.r.t the orientation of the nanostructure. Figure 4.4 b shows MR curve

taken on a 100 nm structure. The measurement was carried out simultaneously for different parts of a single Hall bar with different respective crystalline orientations. We immediately notice that the relative MR of the structures is much smaller than for the larger structure. The large ordinary positive MR observed in the 2  $\mu\text{m}$  wide bars that showed a relative MR of  $\Delta R/R > 50\%$  at  $B=6\text{ T}$  [Figure 4.3 b] has completely vanished. The MR in the nanostructures is smaller than 1% for the first structure and a few % for the other one. Furthermore, the sign and/or magnitude of the MR differ for all orientations. The similarity of the curves for  $45^\circ$  and  $135^\circ$  for the first structure is purely random and cannot be reproduced on other samples. The fact that the magnitude of the MR in large area structures, as in Figure 4.3 b is at least one order of magnitude higher than for the nanostructures indicates that the physics associated with the origin of MR can be different as will be discussed in the later sections.

#### 4.2.2 Dependence on STO phase transition

In the next step, we investigate the MR after warm-up and cool-down through  $T_{PT}$ . Both structures were warmed up to 250 K and cooled down again to 4.2 K. Figure 4.5 a,b and Figure 4.5 c,d show the results for structures 1 and 2, respectively. In both cases, the MR has changed considerably. Especially for sample 2 we observe a change in magnitude and sign for all three measured directions. Further temperature sweeps show that the phase transition seems to be crucial for the effect. Figure 4.6 shows a further sequence of MR measurements after different warm-up and cooling cycles for sample 2. After the measurement from Figure 4.5, the sample was first warmed up to 75 K, which is below  $T_{PT}$ . The sample was kept at this temperature for 60 min and then cooled down to 4.2 K again. The resulting MR measurements look identical [Figure 4.6 b] to the previous ones. The sample is then warmed up to 220 K, which is above the  $T_{PT}$ . After again cooling down to 4.2 K, we observe a moderate change in the magnitude of the MR, especially for an angle of  $90^\circ$  [Figure 4.6 c]. Repeating the same sequence warming up to 75 K for one hour and cooling down yields no to little change in the MR behaviour [Figure 4.6 d]. Warming up again through  $T_{PT}$  ( $T_{max} = 220\text{ K}$ ) for one hour, however, results in a massive change [Figure 4.6 e]. For  $90^\circ$  and  $135^\circ$ , the MR is reduced by a factor of  $\approx 7$ . For the  $45^\circ$  direction, however, we observe a complete sign reversal of the MR.

As pointed out in Minhas et al.[148], the effect of the domain walls is very pronounced for structures as small as 100 nm but it averages out when the lateral size of the structures is even moderately increased to a few hundred nm. The investigation of further samples with lateral dimensions of 200 nm and 300 nm, respectively, confirms this statement.

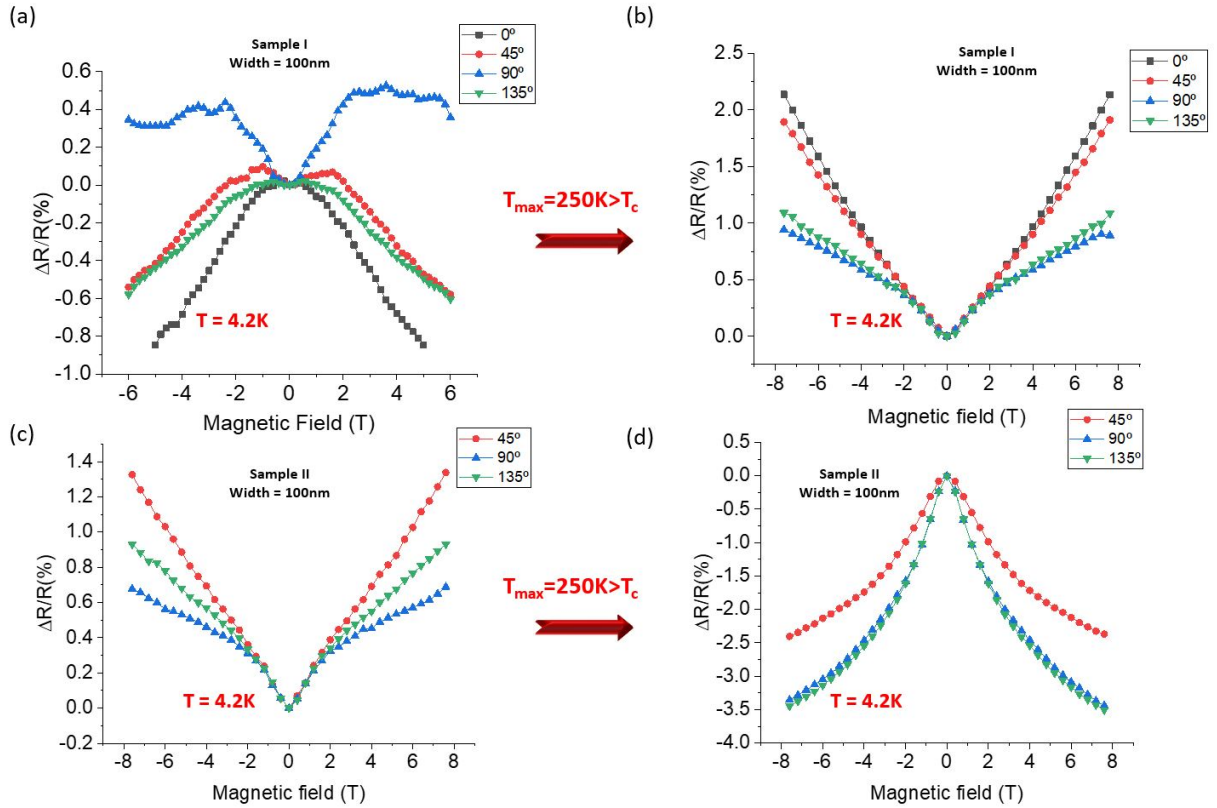


FIGURE 4.5: Variation in MR for two different samples when the warmup-cooldown cycle is performed to 250 K. Both samples are heated to 250 K, and after waiting for 1 hour, they are finally cooled down to 4.2 K and the measurements were done at 4.2 K. Both samples, sample 1 ((a) and (b)) and sample 2 ((c) and (d)) show a significant change in MR behaviour after the warm-up through the transition temperature. Not only the magnitude but also the sign of MR changes.

In Figure 4.7 we show the MR for 200 nm and 300 nm wide nanostructures and the change in MR when heating through  $T_{PT}$ . For the 200 nm structure [Figure 4.7 a and Figure 4.7 b], the MR obtained is hugely direction dependent and has a lower magnitude, just like in the case of the 100 nm structure. After cycling the temperature through  $T_{PT}$ , a significant change is observed. For a 300 nm wide structure [Figure 4.7 c and Figure 4.7 d], however, the MR is larger in magnitude and quadratic in nature, as was the case for the  $2\ \mu\text{m}$  structure [Figure 4.3 b] apparently recovering the contribution of the ordinary magnetoresistance. After sweeping the sample temperature through  $T_{PT}$ , the main quadratic behaviour remains unchanged. Only minor changes in magnitude appear as we might expect for a sample that is still close to the critical size.



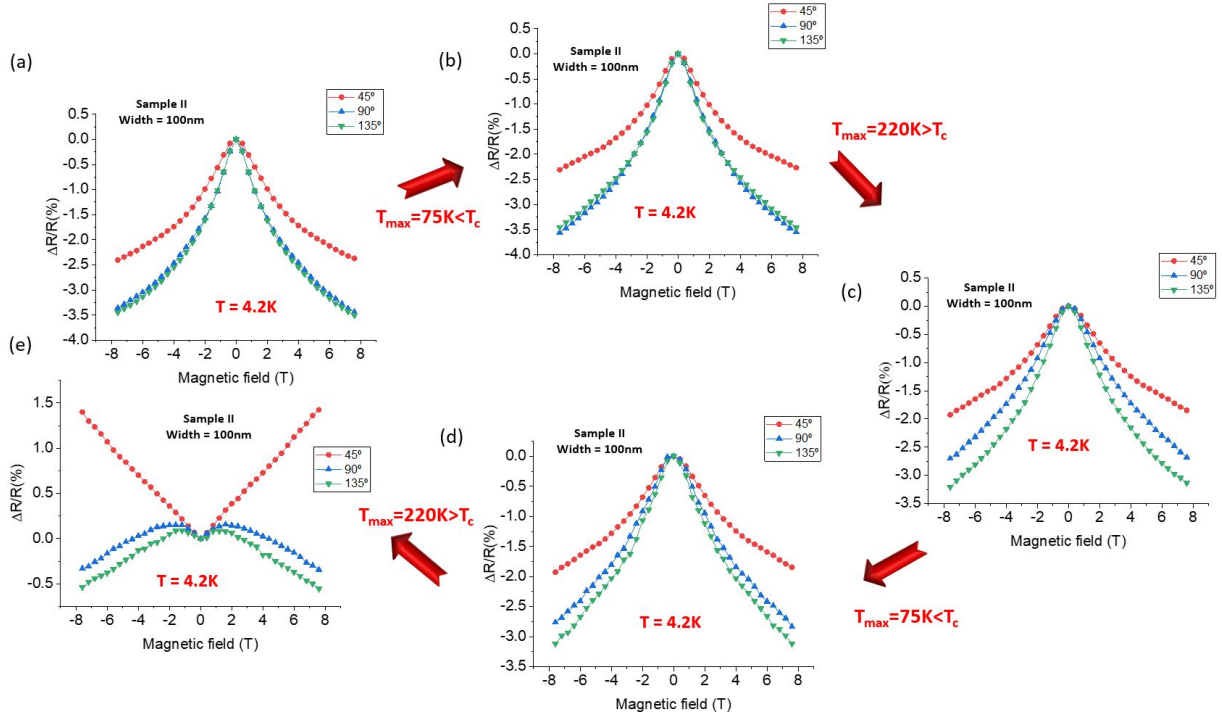


FIGURE 4.6: Shows how the structural phase transition of STO (105 K) influences the MR for sample 2. (a) shows the MR at 4.2 K after initial cool-down. (b) shows MR behavior at 4.2 K after warmup-cooldown cycle is performed to  $75\text{K} < T_c$  and (c) shows the MR at 4.2 K after warmup-cooldown cycle to  $220\text{K} > T_c$ . (d) No change in MR is observed. The subsequent warmup-cooldown cycle is performed to  $75\text{K} < T_c$ , but (e) significant change in MR is observed when the sample is heated to  $220\text{K} > T_c$  above the phase transition.

### 4.3 Discussion

We now discuss these results with respect to the initial assumptions:

1) As expected for conduction through interconnected domain walls, we observe the random scattering of resistance values not only for different crystalline directions. Even for a single segment cycling the temperature through  $T_{PT}$  leads to a change in low-temperature resistance. The different possible domain wall configurations may also cause the non-monotonicity of the resistance/temperature curve that sometimes is observed and sometimes not. It is easily understood that depending on the domain wall properties and the changing dielectric constant at low temperatures, rearrangement of the carrier distribution can lead to a change in resistance that can be either positive or negative.

2) A correlation between crystalline directions and resistance cannot be confirmed. However, it must be stated that due to the randomness of the domain wall distributions,

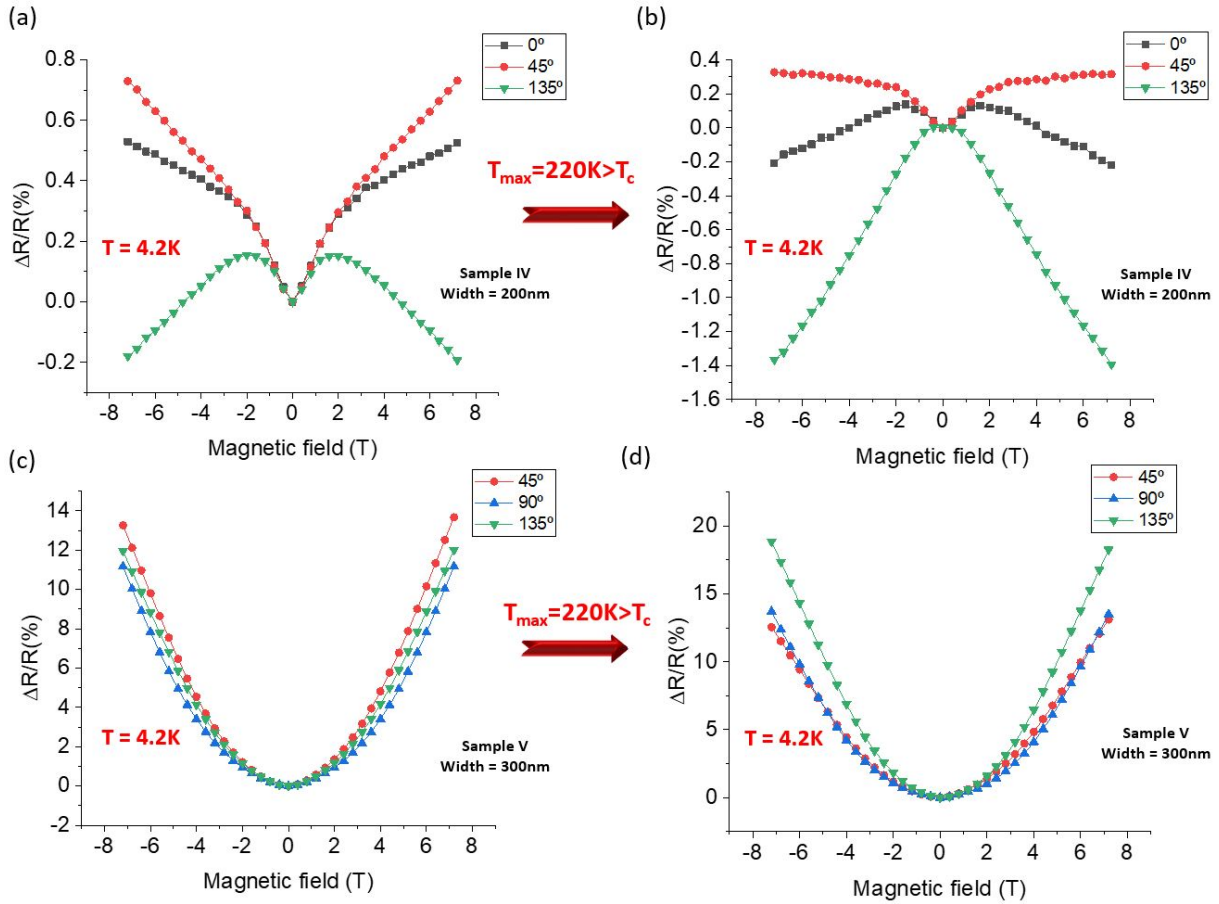


FIGURE 4.7: Shows how the MR measured at 4.2 K for (a) 200 nm structure and (c) 300 nm structure. 300 nm structure behaves more similarly to a large area structure, but the 200 nm structure resembles more of a 100 nm structure. Heating through the transition temperature results in a change in MR for both the 200 nm (b) and 300 nm (d) structure.

statistics on a much larger number of experiments would be necessary to either confirm or dismiss the assumption.

3) For the magnetoresistance, the results are more complex. For structures that are 200 nm wide or smaller, we distinguish three different types of MR. In some curves [Figure 4.5 b, Figure 4.5 c] we only observe a positive MR. Many curves show only a negative magnetoresistance, but in some cases, we also observe a crossover between the two shapes similar to that seen by [183] in LAO/STO with high carrier density or in other 2D disordered metals [191, 192]. None of the curves, however, shows a clear positive parabolic MR that would indicate dominating ordinary MR. Within our statistics, the type of curve does not depend on the crystalline orientation of the investigated segment and a warm-up cool-down cycle through  $T_{PT}$  can change the MR from one type to another. In the following, we will discuss the underlying physics.

Since the anisotropy in the temperature dependence of resistance occurs at low temperatures, it is most likely due to the effect of structural phase transition. The role of structural phase transition and domain wall has been discussed in detail on [chapter 2](#). Obviously, the total number of filaments is very large in large-area structures. It is to be noted that these filaments are statistically distributed. So no direct proportionality between the number of filaments with orientation or lateral size of the structures can be made. The only certain thing is that there is a limited number of filaments in nanostructures. Due to the limited number of filaments, their influence on transport is much more significant in nanostructures compared to large structures [148]. This effect is what we see in the temperature dependence of resistance in nanostructures. But in the case of 2  $\mu\text{m}$  structures, the statistical distribution of a large number of filaments results in averaging out of their effect. Thus, no anisotropy with direction can be observed. Due to this domain wall formation, the resistance deviates w.r.t orientation of nanostripes as the temperature is below 105 K and the anisotropy increases as the temperature is decreased further down to 4.2 K. We also observe that the resistance at 4.2 K changes slightly for all the orientations every time the warm-up cycle is done above the transition temperature, which again indicates the random distribution of filaments.

Out-of-plane measurements on 2  $\mu\text{m}$  structures give a significant positive MR with a magnitude greater than 50% ([Figure 4.3b](#)). At 4.2 K when a magnetic field of 7.2 T is applied, the quadratic behaviour is typical for ordinary magnetoresistance, which is understood as due to orbital scattering. There is no indication of crystalline direction dependence on MR here since all different orientation yields similar MR results. At the same time, the MR in nanostructures does not follow a similar trend of large area structures, especially 100 nm and 200 nm structures. Completely random behaviour was observed along different crystalline orientations.

The magnitude of MR observed in nanostructures is significantly smaller than the value obtained in large structures. Also, no longer quadratic dependence with the magnetic field is observed. This provides the first indication of the influence of domain walls in MR measurements. The completely random behaviour of MR once the sample is warmed up above the phase transition provides further evidence that the domain walls play a vital role in the transport properties. In some cases for 100 nm structure, there has been a total switching of MR behaviour as shown in [Figure 4.5](#), which was shocking but not unexpected since the number of filaments can be very limited as the lateral dimension is reduced. The systematic study showed that no change in MR was observed every time the warm-up and cool-down were performed, as long as the final temperature ( $T_{max}$ ) was kept below the transition temperature. [Figure 4.6](#) provides strong evidence towards

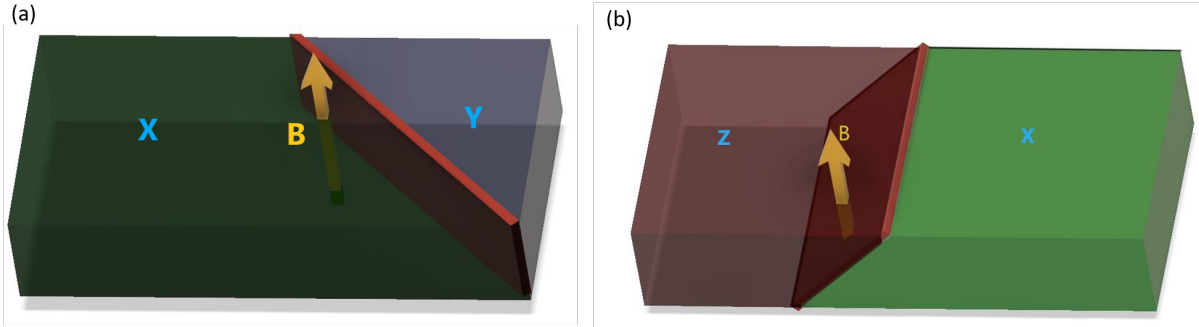


FIGURE 4.8: Schematic representation of two different configurations of domain walls. Rotation by  $90^\circ$  of these two gives the other two possible configurations. (a) For type 1 domain walls that extend perpendicularly into the STO, the out-of-plane magnetic field applied to the interface will act as an in-plane field and suppress the ordinary MR. In the case of type 2 domain walls (b), the magnetic field will be partially perpendicular since they are inclined at an angle of  $90^\circ$  as described in [136].

the influence of phase transition in transport. Whenever the sample is heated above phase transition, the domain walls get redistributed, resulting in a completely different configuration [137]. The influence of this domain wall redistribution is very significant as the width of the structure is reduced. To provide an explanation for this anisotropic behaviour, we have to consider the tetragonal domain configuration in STO following the phase transition. As a result of phase transition, Domains and domain walls in specific crystallographic directions are formed. But the key thing to note is that the domain walls extend into the STO at different angles. Domain walls at  $[110]$  and  $[1\bar{1}0]$  extend perpendicularly into the STO (Figure 4.8a) while domain walls at  $[100]$  and  $[010]$  make an angle of  $45^\circ$  with the normal to the surface (Figure 4.8b [136]). So when we apply a magnetic field perpendicular to the interface, domain walls at  $[110]$  and  $[1\bar{1}0]$  have an in-plane configuration while  $[100]$  and  $[010]$  make some angle with the magnetic field. As a result, we will have both in-plane and out-of-plane configurations simultaneously. This effect of this different configuration becomes significant once the number of domain walls is limited, which is the case in nanostructures.

It is well known that in a 2D or quasi-2D system like the domain walls, the orientation of the magnetic field with respect to the plane is crucial for magnetoresistance. For magnetic fields perpendicular to an unpatterned LAO/STO interface, the magnetoresistance is often dominated by the positive ordinary magnetoresistance contribution [183–186], which is attributed to orbital effects. As mentioned above, this contribution has a quadratic field dependence. Ordinary magnetoresistance is effectively suppressed if either the magnetic

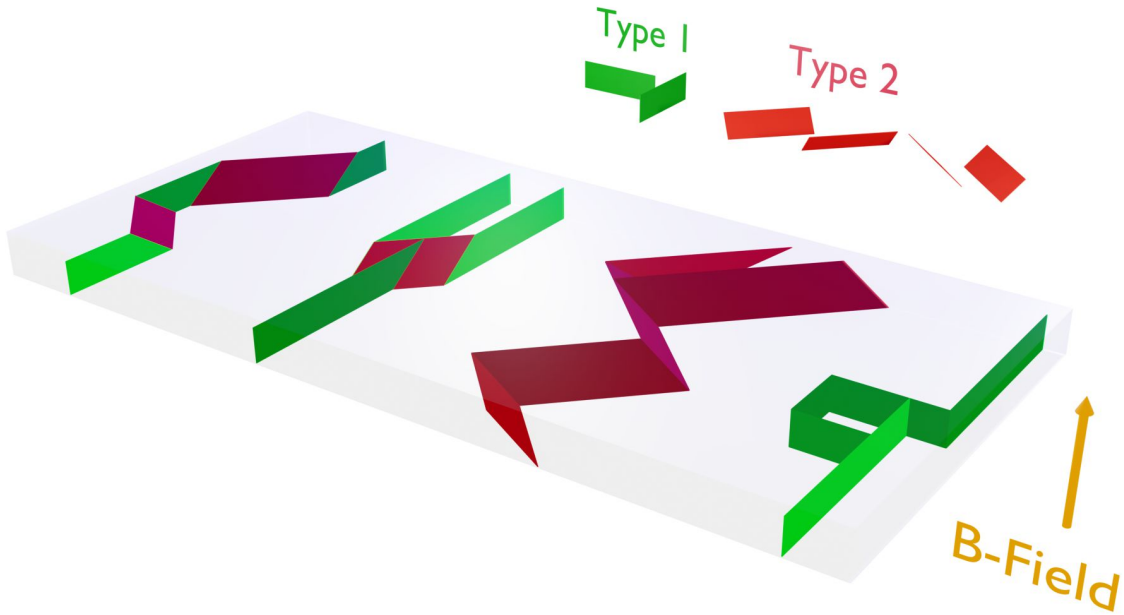


FIGURE 4.9: alignment of type 1 and type 2 domain walls in the STO and possible random combinations. All four combinations connect the front and the back of the slab. Obviously, it is possible to have combinations with different contributions from both types. Even for the same relative contribution, different total lengths of the domain wall path can be realized. So even for the same conduction direction, we may have very different combinations of domain walls in the conducting channel that may also have different resistance depending on their respective lengths.

field is applied in-plane or the dimensions of the structure are too small to allow for orbital effects. Because the type 1 and type 2 domain walls are either perpendicular to or tilted with respect to the surface, a field applied perpendicular to the interface and, thus, to the surface can never be perpendicular to either of these domain walls. In addition, the extent of the conducting domain walls into the STO is small, efficiently suppressing ordinary MR even for domain walls tilted with respect to the field. Without ordinary magnetoresistance to compete with, other contributions can start to dominate.

A small but purely negative MR [Figure 4.6 a-d] at low temperatures can be caused by weak localization (WL) [193]. A purely positive MR can be due to electron-electron interaction [185, 186, 194, 195] or weak antilocalization (WAL) [129]. The latter requires a significant spin-orbit coupling which at first glance is unexpected in STO that is composed of lighter elements. However, the domain walls at low temperatures are subject to large electric fields that may cause the WAL. Finally, a transition from positive to negative magnetoresistance in a single curve [Figure 4.6 e, Figure 4.7 a, Figure 4.7 b] is explained by

a crossover between WAL and WL [183, 191, 192]. Different domain wall MR with respect to the magnetic field orientation has been observed in BFO thin films [196]. In our case, we have a combination of both configurations. Negative domain wall magnetoresistance has been reported in BFO thin films when the field is applied in-plane to the domain walls [197]. There could be other possibilities like double exchange, which gives negative MR in mixed valence perovskites [198, 199], but the exact reason is still to be confirmed.

Alignment of type 1 and type 2 domain walls in the STO and their possible random combinations are shown in Figure 4.9. All four combinations of the domain walls connect the two ends of the conduction channel. Obviously, it is possible to have combinations with different contributions from both types. Even for the same relative contribution, different total lengths of the domain wall path can be realized. So even for the same conduction direction, we may have very different combinations of domain walls in the conducting channel that may also have different resistance depending on their respective lengths and also depending on their orientation angle different MR can be expected. A very limited number of conducting channels in nanostructures enhances the effect of orientation of domain walls compared to large area structures.

Unfortunately, it is not possible to design a simple model that quantitatively describes the resistance values based on two types of domain walls with fixed resistivity. Among other aspects, the conductivity of the domain walls is determined by the respective number of carriers in the domain wall. Assuming that the initial number of carriers is constant, different domain wall configurations with different total lengths and contributions from type 1 and type 2 must have different conductivity. They will thus contribute differently to the MR. It is unclear whether the carrier concentration is homogeneous through the domain walls or can vary between different positions.

## 4.4 Conclusion

We conducted some experiments to realize the consequences of this current-carrying filament on the transport properties of the interface. Our magnetoresistance measurements revealed a significant but random crystalline direction dependence in nanostructures ( $< 500\text{nm}$ ). The current-carrying filaments, which are linked to the structural phase transition of STO, also exhibit temperature dependence in our MR measurements. Warming up nanostructures above the transition temperature (105K) results in a significant change in MR results, even there is a change of sign in some cases. The results suggested no

clear-cut correlation between the particular direction and MR behaviour but primarily statistical relation.

In conclusion, we may state that in our experiments, we find effects that can be predicted based on the theory of filamentary transport but that do not fit the model of a quasi-2D electron gas with sheet conductivity at the LAO/STO interface. Both resistance and magnetoresistance have random values within a specific range consistent with the formation of two different types of conducting domain walls with different orientations with respect to the surface. The results point out the fact that in the case of small-area structures, the microscopic domain wall structure needs to be taken into account to explain various transport phenomena which the existing theories may not necessarily explain for large-area structures.

# 5

## Gate voltage induced changes in transport properties of the $\text{LaAlO}_3/\text{SrTiO}_3$ interface

Modern electronics are built on the foundation of silicon field-effect transistors (FETs). They are an inevitable component to operate the electrical devices we use every day, such as computers, cell phones and many more. A source (S) and drain (D), a conducting channel between them, and a gate (G) terminal constitute up a standard FET. A dielectric layer separates the gate electrode from the conducting channel. The conducting channel and gate together create two electrodes of a parallel plate capacitor in this configuration. Application of gate voltage causes charges in the conducting channel to build up or deplete. As a result, the conducting channel's resistance and carrier density are changed.

Compared to semiconductors, oxide materials exhibit various electrical and magnetic properties, making them suitable for field effect research. Oxides FETs are being studied in order to improve FET functioning and overcome the scaling limits of silicon-based devices. There are three common methods for electrical gating of LAO/STO structures namely back gating, top gating and side gating. Unlike back-gating, which applies the electrical field from the back and uses a thick STO substrate as the gate dielectric, top-gating applies the electrical field from the top and uses a thin LAO layer as the gate dielectric. Sometimes additional dielectric material has to be deposited to use as a gate insulator in top gating configuration. The 2DEG was depleted in the negatively biased state, and the application of gate voltage caused the metal-insulator transition. The back gate arrangement employs a higher dielectric constant of STO ( $\sim 300$ ) than LAO ( $\sim 25$ ). Back gating is a global technique which concentrates the electric field at the structures even for large area structures [200]. However, applying a back gate changes the carrier density in the whole sample upon application of the electric field. Moreover, the high



gate voltage up to several hundred of volts is required to achieve some reasonable effect [15, 102, 129, 201] due to the thickness of gate dielectric, which is typically 0.5 μm. Side gating allows for a large gate action with the application of small voltage. Here we make use of the dielectric constant of STO in between the gate and conduction channel. This distance can be varied from a few hundred nanometers to a few micrometres keeping the leakage current to a minimum. The side gate configuration acts like a local back gate. Top gate geometries allow for large electric fields at low voltages that are less dependent on structure size than on the thickness of the gate dielectric. However, in these experiments, the field is between the gate and the channel and does not penetrate deep into the STO substrate [202, 203]

The influence of the electric field on the domain walls has been discussed in the previous chapter. Structural phase transition of STO substrate at low temperature should also be considered while using back gating. This structural change results in the creation of domains within STO. It was recently discovered that domain walls are mobile under the application of electric fields, which couples to the domain walls, possibly through charged/polar domain walls or anisotropic electrostriction. The conductivity changes according to the movement of the domain walls, which has an impact on the characteristics of 2DEG at the LAO/STO interface. Also, ferroelectricity can be induced in the domain wall at higher electric fields, and the domain configuration can be irreversibly changed after the application of gate voltage. Application of the back gate voltage ( $V_G$ ) will add or remove electrons from the quantum well. An irreversible increase in sheet resistance has been reported after the application of positive  $V_G$ , which is absent with negative  $V_G$ . Biscaras et al. [204] show that the escape of high mobility electrons with the application of positive  $V_G$  occurs since the Fermi level lies intrinsically close to the top of the QW once the threshold number of electrons is reached and these electrons get trapped in trapping sites present in STO. Yin et al. [205] proposed the formation of trapping sites due to electromigration and clustering of oxygen vacancies in STO with the application of positive  $V_G$ . Such electron trapping can be a universal phenomenon in all STO-based heterostructures. Application of positive  $V_G$  can pull the 2DEG into the STO which further enhances the influence of domain walls. Similarly, negative  $V_G$  should push the 2DEG towards the LAO side, which nullifies the domain wall influence.

Large back gate voltages have to be applied to significantly modulate the electronic property [15, 102, 129, 201]. The requirement of large gate voltages can be tackled by the implementation of top [202, 203] and side gate voltages [68, 69, 130], which requires only small voltages to tune the property. Recently it has been shown that the effect of side gate voltage is comparable to local back gate voltage to the interface [130]. It is possible

to generate a large electric field using a small applied gate voltage by taking advantage of the larger dielectric constant of STO, along with the reduced effective thickness of gate dielectric. The application of larger electric fields has a multitude of effects on the interface. First of all, the electric field enhances the mobility of domain walls [136]. After a large gate voltage sweep, an irreversible preferential selection of particular domains and domain walls have been reported [136, 143, 144]. Secondly, when the applied electric field is above a particular threshold value, ferroelectricity is induced in the domain walls [147], which is persistent even after switching off the gate voltage. They have also observed that the 2DEG surrounding the ferroelectric domain walls was depleted for some distance, forming Schottky-like barrier. A recent study by Persky et al. [206] also confirms the inhomogeneity in the conductivity landscape with insulating areas near metal-insulator transition. They also describe the possibility that conducting patches exist within the insulating area or that branching of the current path can lead to dead ends reaching in the insulating area. Due to the lack of current flow, they were, however, not able to prove their existence by scanning SQUID microscopy. The significance of domain walls on the transport properties is more prominent in nanostructures  $< 500\text{nm}$  [148, 170] where it has been shown that the magnetoresistance in nanostructures is dependent on the orientation of domain walls. Moreover, the application of positive gate voltage enhances the trapping of charge carriers which in turn results in an irreversible change in sheet resistance [205, 207, 208].

We designed several experiments to demonstrate the influence of back gate and side gate voltages on the transport properties of LAO/STO nanostructures.

## 5.1 Results

In the previous chapter, we have shown that in nanostructures there exists direction-dependent anisotropy which can be attributed to the different orientations of domain walls. The application of back-gate voltage will push the electron out or pull them into the domain walls and could influence MR anisotropy. Here we will discuss the results from the series of experiments designed to observe the influence of back-gate voltage on MR anisotropy.

6 u.c of LAO is grown on top of  $TiO_2$  terminated STO using PLD at  $850^\circ\text{C}$  with  $P_{O_2}$  of  $10^{-3}$  mbar. Nanopatterning is done using reactive ion etching with  $BCl_3$  [162] as well as using  $Al_2O_3$  as a mask to eliminate any artefacts generated from the fabrication process. After the nanopatterning, 200 nm of gold has been deposited using an e-beam evaporation

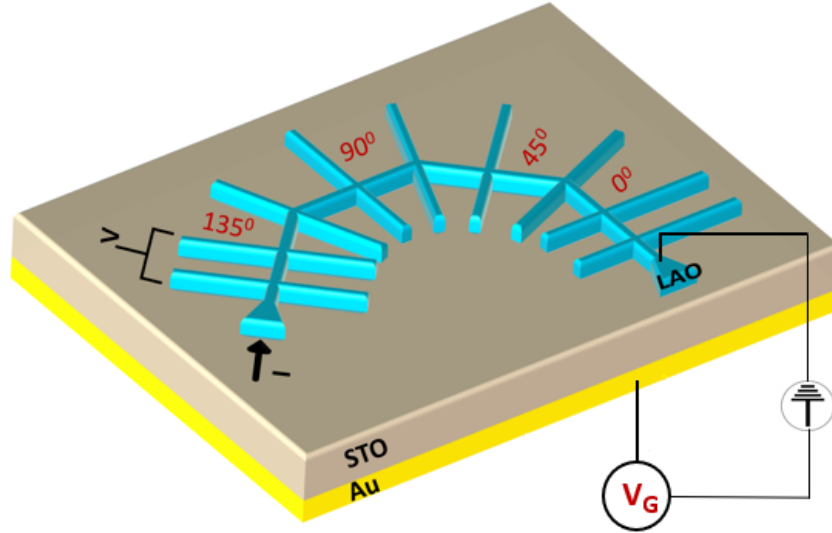


FIGURE 5.1: Sketch of the sample geometry used for measurement with dimensions. The Blue area represents the 2DEG. Channel width varies from 100 nm to 2  $\mu\text{m}$ . Gold on the back side of the sample is used for back gating.

system on the back surface for back-gate experiments. With both these processes we are able to fabricate high-quality nanostructures with lateral dimensions down to 100 nm. We used the sample geometry as shown in Figure 5.1 for the experiments.

### 5.1.1 Influence of back gate voltage on MR anisotropy

For the MR measurements, the magnetic field is applied perpendicular to the sample surface. The field is swept from  $B=-7\text{ T}$  to  $B=+7\text{ T}$ . The initial MR observed for 100 nm is smaller in magnitude (4%) and anisotropy with crystalline orientation is observed (Figure 5.2 a) which is consistent with the results observed in [170]. It should be noted that crystalline anisotropy varies with every temperature cycle above the phase transition due to the random redistribution of the domains. Now we applied back gate voltage and observed how the MR anisotropy changes. As the negative  $V_G$  is increased, the MR becomes more negative (Figure 5.2 c) and crystalline anisotropy vanishes. This increase in negative MR is attributed to the Weak localization (WL) effect [129]. As the positive  $V_G$  is increased, positive MR behaviour becomes more dominant and the anisotropy in MR becomes more significant as shown in Figure 5.2 b. Slowly but gradually the quadratic behaviour is being restored with positive  $V_G$ . We repeated the measurements on a 200 nm structure (Figure 5.3) which shows much more significant crystalline anisotropy than the previous 100 nm structure and the same behaviour was observed.

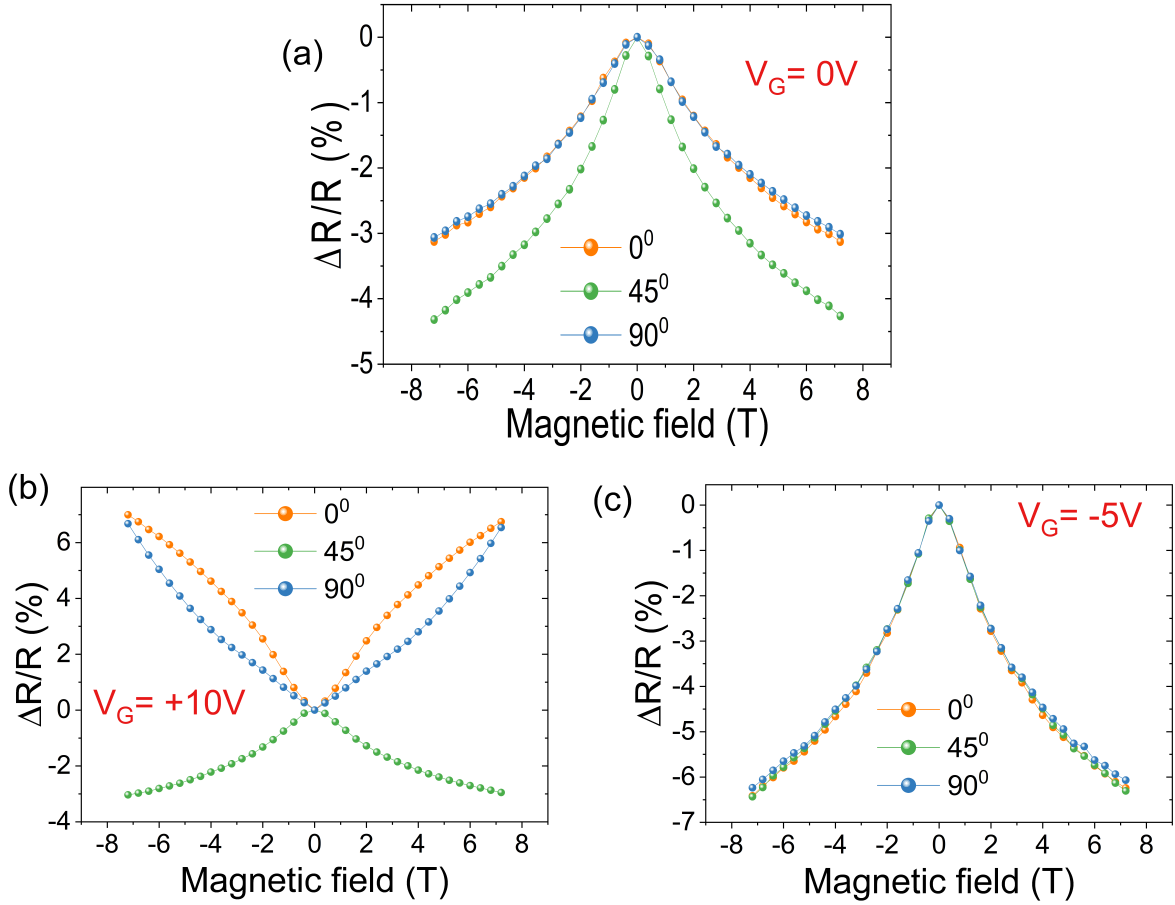


FIGURE 5.2: (a) shows the virgin state out-of-plane MR for 3 different orientations of 100 nm structure. Variation of MR with orientation angle is clearly visible. (b) shows the MR with  $V_G = +10\text{V}$  and (c) MR with  $V_G = -5\text{V}$

In the previous chapter (see [chapter 4](#)) we have demonstrated that the anisotropy in MR in nanostructures is due to the difference in distribution and orientation of domain walls in STO. Domain walls that are oriented at  $45^\circ$  and  $135^\circ$  extends perpendicularly into the STO while  $0^\circ$  and  $90^\circ$  are inclined at  $45^\circ$  angle [136]. As a result, the magnetic field applied perpendicular to the interface will have a different influence depending on the orientation, which results in MR anisotropy. By the application of  $V_G$ , the carriers can be pushed out of domain walls ( $+V_G$ ) or pulled into the STO domain walls ( $-V_G$ ). The anisotropy in MR is thus enhanced by  $+V_G$  and nullified by  $-V_G$ .

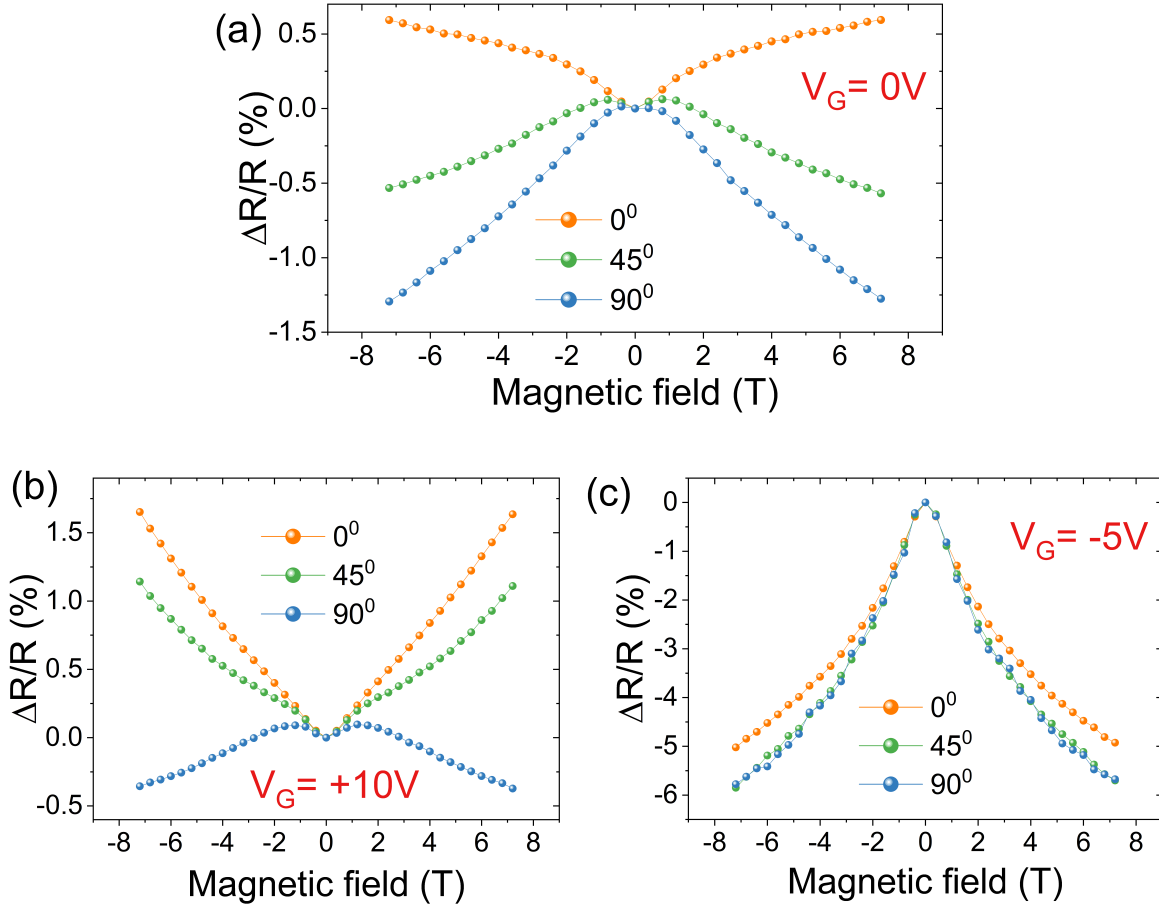


FIGURE 5.3: Here we show the similar behaviour of MR for 3 different orientation angles with gate voltage for 200 nm structure. (a) shows the virgin state MR. (b) MR with  $V_G = +10\text{V}$  (c) MR with  $V_G = -5\text{V}$ .

### 5.1.2 Irreversible changes in transport properties

After switching  $V_G$  back to 0 V, we repeated the MR measurement again. An irreversible change in MR was observed for 200 nm structure after the application of positive  $V_G$  as shown in Figure 5.4. Negative MR with a relatively large magnitude compared to the initial state was observed for all different orientations. But the application of negative  $V_G$  did not alter the MR behaviour. Such an irreversible change in MR was observed for 100 nm structure also (not shown here). From now onward we only focus on one orientation ( $0^\circ$ ) of nanostructure for better comparison of the results. The persistent MR was retained as long as the sample is not heated to temperatures above the phase transition temperature ( $T_{PT}$ ) 105 K of STO. In the Figure 5.5, we show the evolution of MR with gate voltage for 200 nm (Figure 5.5 a,b) and  $1\mu\text{m}$  (Figure 5.5 c,d) structure

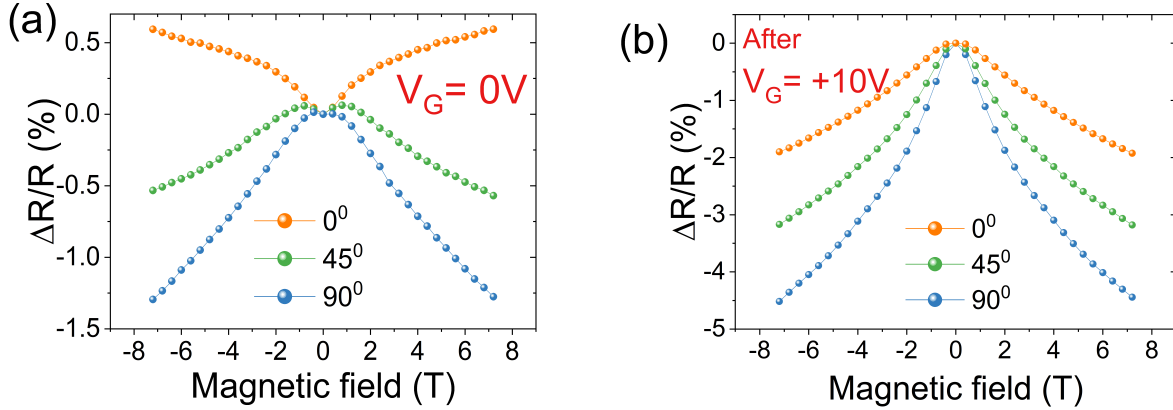


FIGURE 5.4: Persistent change in MR observed after the application of  $V_G = +10\text{V}$  for all 3 different orientations as shown in (b). A persistent negative MR with clear anisotropy with orientation angles has been observed after applying positive  $V_G$ . (a) Represents the virgin state MR.

which is oriented at an angle of  $0^\circ$  w.r.t to the edge of the sample. The persistent MR behaviour is also shown in the figure. These sets of experiments demonstrate that the persistent change in MR is absent with the application of negative  $V_G$  (Figure 5.5 b,d).

In addition, an irreversible increase in resistance has been observed after the application of positive  $V_G$  (Figure 5.6 c). As the  $V_{Gmax}$  is increased, the persistent ground state resistance also increases. As long as the  $V_G$  is kept less than  $V_{Gmax}$ , the gate sweep is reversible with no change in ground state resistance which is the similar behaviour reported earlier [204, 205]. The modulation of carrier density is also investigated as shown in Figure 5.6 c. With the application of positive  $V_G$ , charger carriers are added into the quantum well which results in increased carrier density. Similarly, the application of negative  $V_G$  electrons are removed from QW and thus carrier density is reduced. After the removal of negative  $V_G$ , the initial carrier ( $1.78 \times 10^{13}\text{cm}^{-2}$ ) density was restored. But positive  $V_G$  results in an irreversible decrease in carrier density. After the application of  $V_G = +8\text{V}$ , the carrier density was reduced to  $1.36 \times 10^{13}\text{cm}^{-2}$ .

We performed a temperature sweep after the application of  $V_G$  to investigate any gate voltage-induced effect during warm-up. A huge resistance anomaly has been reported for 100 nm structure around 80 K during warm-up [148] which can be explained by the breaking of current-carrying filaments during phase transition. But the effect of these breaking of filaments is less prominent for structures with dimensions 200 nm or more. Surprisingly we observe a huge resistance peak, which is an order of magnitude larger than previously reported, observe around 80 K for 200 nm structure after the application of

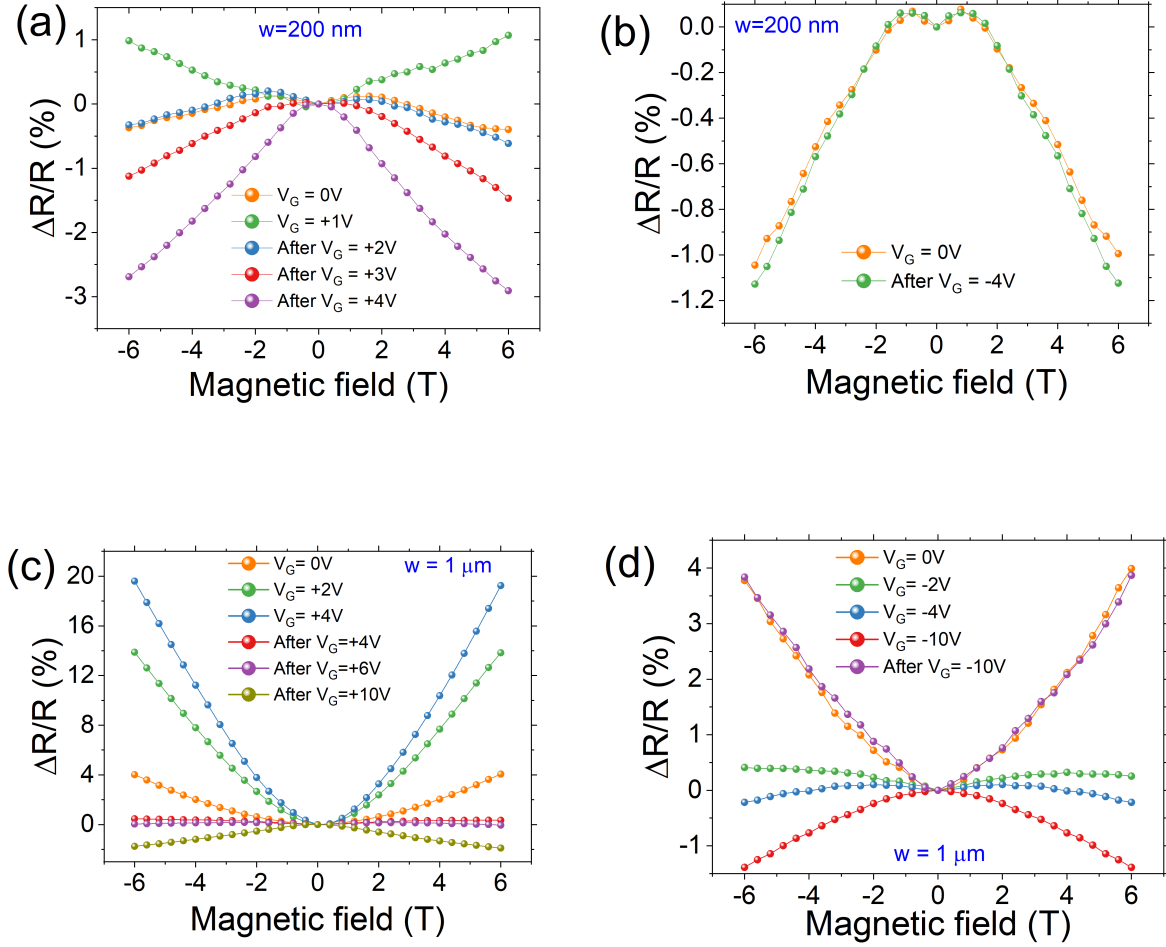


FIGURE 5.5: The influence of back gate voltage on the MR behaviour of 200 nm and  $1 \mu\text{m}$  structure for single orientation direction. The influence of  $+V_G$  is shown in (a) and (c) and  $-V_G$  is shown in (b) and (d). Persistent MR change is observed only after applying  $+V_G$  as shown in (a) and (c).

positive  $V_G$  (Figure 5.6 b). No such gate-induced peak is observed after applying negative  $V_G$  (Figure 5.6 b). However, for  $1 \mu\text{m}$  structure no such resistance anomaly was observed after the application of gate voltage (Figure 5.6 a) even though positive  $V_G$  induces a persistent negative MR which is smaller in magnitude compared to 200 nm structure (Figure 5.5 c).

## 5.2 Discussion

Application of positive back gate voltages results in the trapping of charge carriers and also can modulate the carrier concentration, which plays a key role in determining the

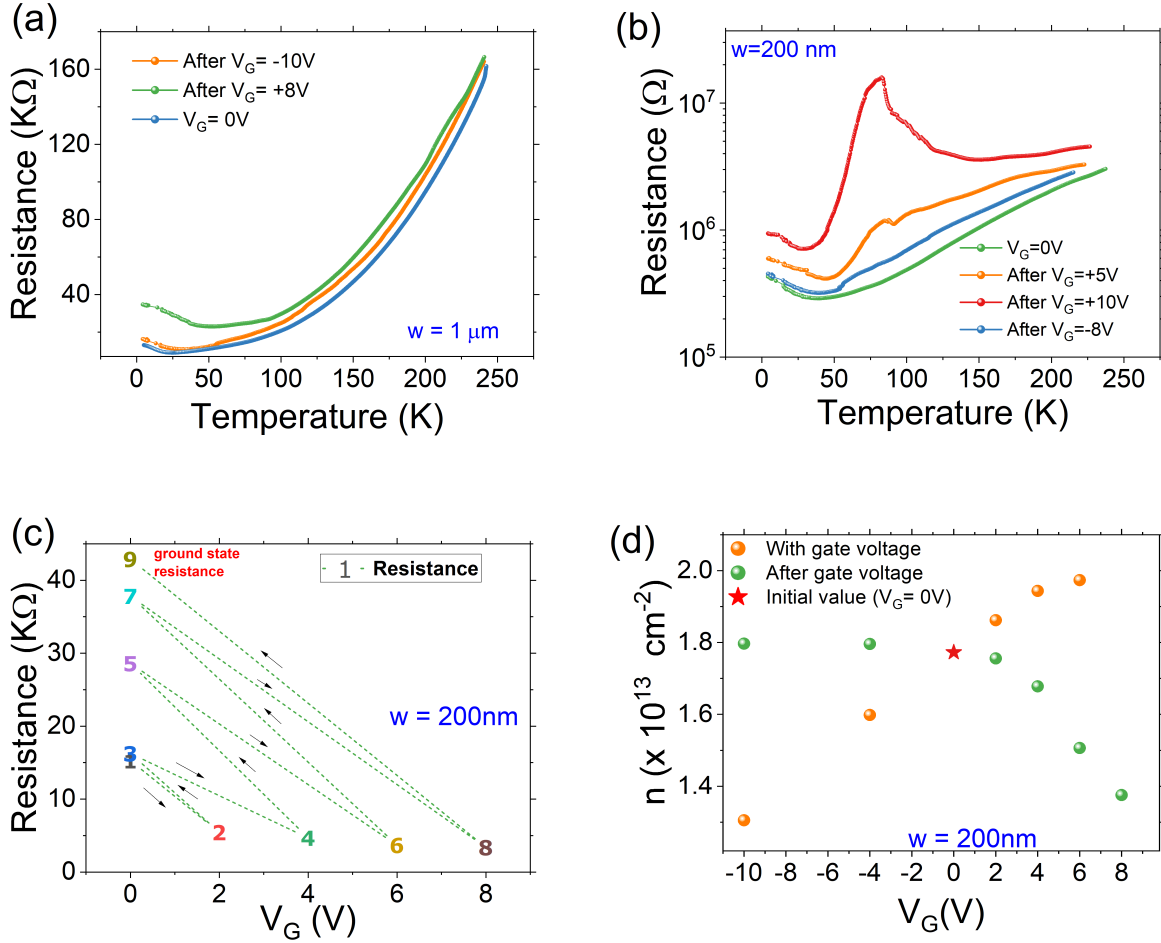


FIGURE 5.6: (a) No gate induced resistance peak observed for  $1 \mu\text{m}$  structure. (b)  $+V_G$  induces resistance peak at 80 K for 200 nm structure. No such modification happens after  $-V_G$  application. (c)  $+V_G$  induced increase in base line resistance and (d)  $V_G$  induced change in carrier density (with and after  $V_G$ ).

dominant scattering mechanism (WL or WAL). We will discuss these effects in detail here, which can explain the observed results well.

### 5.2.1 Electron trapping mechanism

Several studies have reported the trapping of electrons with the application of  $+V_G$  in LAO/STO heterostructures [205, 207, 208]. This electron trapping is due to the formation of oxygen vacancy clusters due to the electromigration of oxygen vacancies under the application of  $+V_G$  [205]. Such electron trapping is a universal phenomenon in STO-based heterostructures. The important finding is that the electron trapping phenomenon only



manifests itself at positive gate voltages and that the sweeps are always reversible when a negative voltage is applied. The electromigration and clustering of oxygen vacancies caused by both negative and positive gate voltages may be the cause. However, with negative voltages, the vacancies retract toward the back side of STO, resulting in very few in-gap states originating at the interface and reversible sweeps. When the voltage is positive, the vacancies move toward the interface and produce in-gap states that serve as electron traps. Additionally, it has been claimed that as temperature rises, electron trapping becomes less prominent. This is in agreement with the irreversible changes observed only after the application of  $+V_G$ . After the application of  $+V_G$ , the resistance is increased and the carrier density is decreased (Figure 5.6 c).

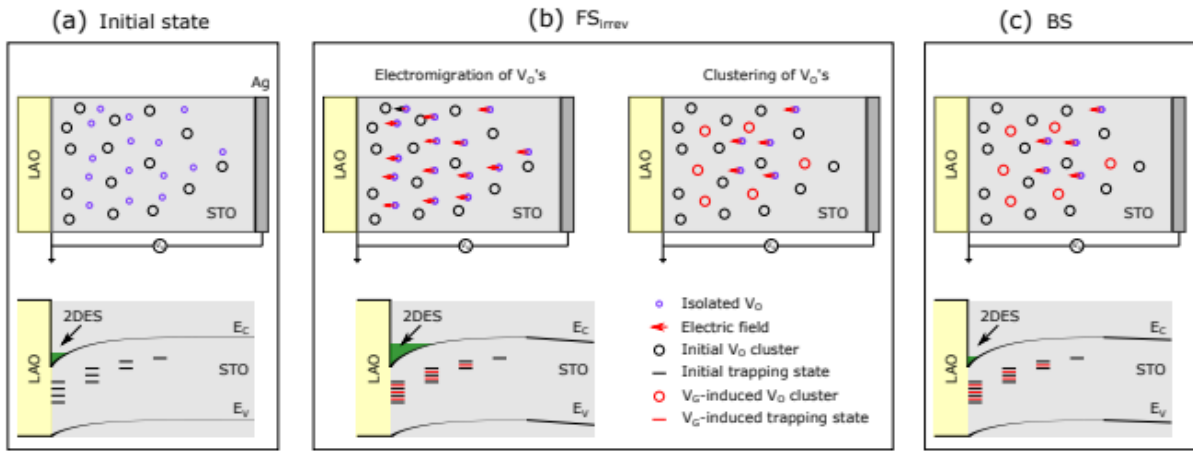


FIGURE 5.7: Schematic illustration of the trapping mechanism and band diagram of the LAO/STO interface under influence of an electric field. Adapted from [205]

After  $+V_G$ , electrons are trapped in the trapping sites created due to the clustering of oxygen vacancies, which reduces the number of interfacial electrons available for conduction. As a result, the conductivity is much more concentrated through the domain walls. The breaking of filaments will have a much more prominent effect in this scenario than before [148]. As a result, we observe a significantly higher resistance peak around 80 K during warm-up in 200 nm structure (Figure 5.6 b). The previously reported peak was much smaller. This observation cannot be solely explained by the electron trapping mechanism especially since such resistance peak is absent for 1  $\mu\text{m}$  structure (Figure 5.6 a). Combining the filamentary charge conduction model with the electron trapping mechanism, the breaking of filaments along with the thermal recovery of trapped electrons can result in a resistance peak, especially if the number of charge conducting filaments is limited ( $< 500 \text{ nm}$ ). As the size of the structure is increased, the presence of numerous domain walls nullifies the effect of filament breaking near  $T_{PT}$  of STO. The maximum

negative  $V_G$  applied in our experiments did not induce any persistent modification of the transport properties.

### **5.2.2 Influence of spin-orbit interaction**

We have discussed the influence of spin-orbit interaction in LAO/STO heterostructures in detail. Caviglia et al. [129] have revealed the influence of a large Rashba spin-orbit interaction on the transport properties of LAO/STO, whose magnitude can be modulated by the application of an external electric field. They observed that for large negative gate voltages, the inelastic scattering time is less than the spin relaxation time, showing that the influence of the spin-orbit interaction is modest when compared to the orbital effect of the magnetic field. Weak localization can be attributed to the quantum correction to conductivity in this domain. Above a threshold voltage, the spin relaxation time rapidly drops by three orders of magnitude when the voltage is raised, becoming less than the inelastic scattering time. On the other hand, as we increase the voltage, the inelastic scattering time essentially stays the same. A weak antilocalization regime with a strong spin-orbit interaction arises here.

Stornaiuolo et al. [130] have also reported the crossover between WL and WAL regimes in dependence on sheet conductance. The sheet conductance of the LAO/STO system has been modulated by side gate configuration. They notice a clear change from a WAL behaviour to a typical quadratic magnetoconductance for maximum conductance. This is due to the fact that, for increasing conductance, there occurs an increase in the elastic scattering time together with a decrease in the spin-orbit scattering time, which suppresses the WL regime. The evolution of the band filling in LAO/STO can be used to evaluate the evolution of SO coupling with carrier concentration. The confinement of the conducting electrons at the interface causes a splitting in the Ti  $3d - t_{2g}$  orbitals in this system, with the  $d_{xy}$  bands having the lowest energy [209]. Only the  $d_{xy}$  bands are filled when carrier concentrations are extremely low. The carrier concentration can be raised by the field effect, and the  $d_{xz}/d_{yz}$  bands begin to fill up. This two-band scenario is in agreement with previous studies [210, 211]. The progressive band filling has been shown to be related to the enhancement of the Rashba field [212] and hence spin-orbit interaction becomes the dominant scattering mechanism.

After the application of  $+V_G$ , the resistance is increased and the carrier density is decreased (Figure 5.6 c). As we have discussed above, at low carrier concentration, weak localisation (WL) is more dominant [129, 130, 212]. Only at higher carrier concentrations does weak antilocalisation (WAL) becomes the dominant due to increased spin-orbit

coupling. As a result, MR becomes positive with  $+V_G$  and negative with  $-V_G$ . Even after switching the  $V_G$  to 0 V, the carrier density is irreversibly decreased. The negative persistent MR (Figure 5.5 a and Figure 5.5 c) observed can be attributed to WL.

Applying higher electric fields, more diverse effects can be observed in the properties of the LAO/STO interface. Due to the limitation of our measurement setup, we could not provide hundreds of volts which is required to generate a high enough electric field in the back gate configuration. As an alternative, we use a side gate configuration which requires only a few volts to create larger electric fields as we will discuss in the next section.

### 5.3 Results: Side gating experiments

By implementing side gate configuration, we could largely modulate the 2-dimensional electron gas (2DEG) at the interface of LAO and STO with the application of small voltage and studied the influence of electric field on the transport properties of nanostructures.

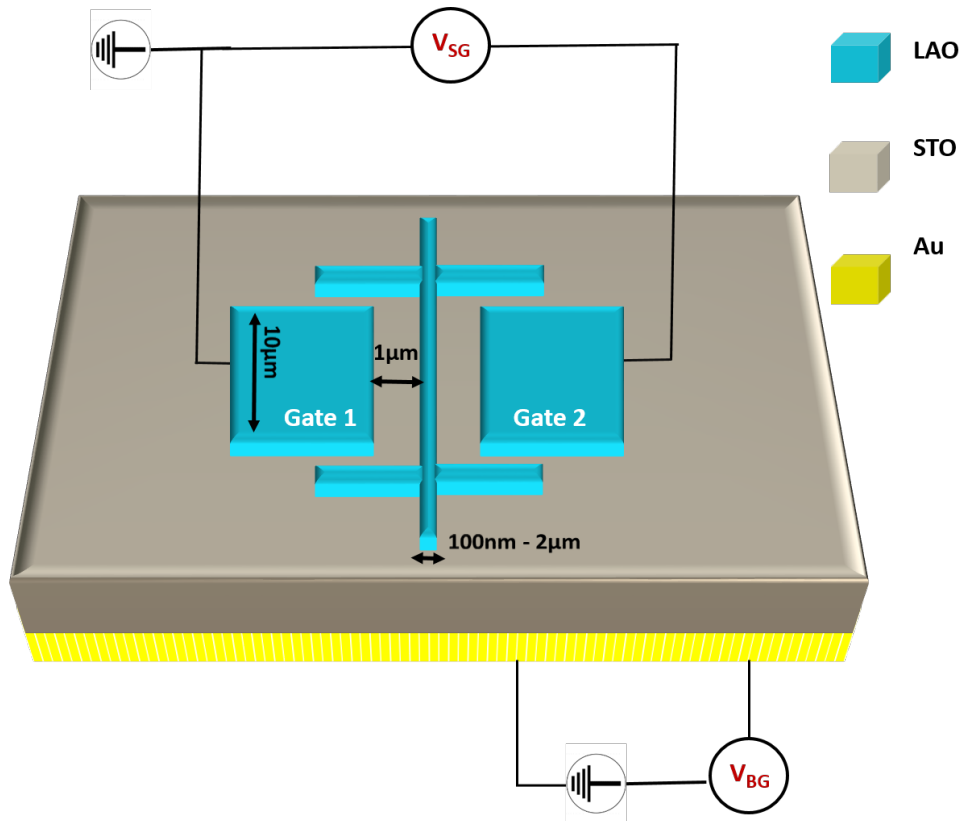


FIGURE 5.8: Sketch of the sample geometry used for the measurement. The Blue area represents the 2DEG. The channel width is varied from 100 nm to 2- $\mu$ m and the gate-channel separation is 1  $\mu$ m. Gold on the back side of the sample is used for back gating.

The sample fabrication method is the same as what we did for back-gating experiments. However, here we have lateral side gates instead of the back gate. The sample geometry used for the measurements is shown in Figure 5.8 where the lateral dimension of the structure varies from 100 nm to 2  $\mu\text{m}$  and the length of the conducting channel is 14  $\mu\text{m}$ . The side gates have a width of 10  $\mu\text{m}$  and are separated from the channel by a distance of 1  $\mu\text{m}$ . We have tried several gate-to-channel distances but found that for 1  $\mu\text{m}$ , the voltage efficiency of gating was higher at the same time by keeping the leakage current to a minimum.

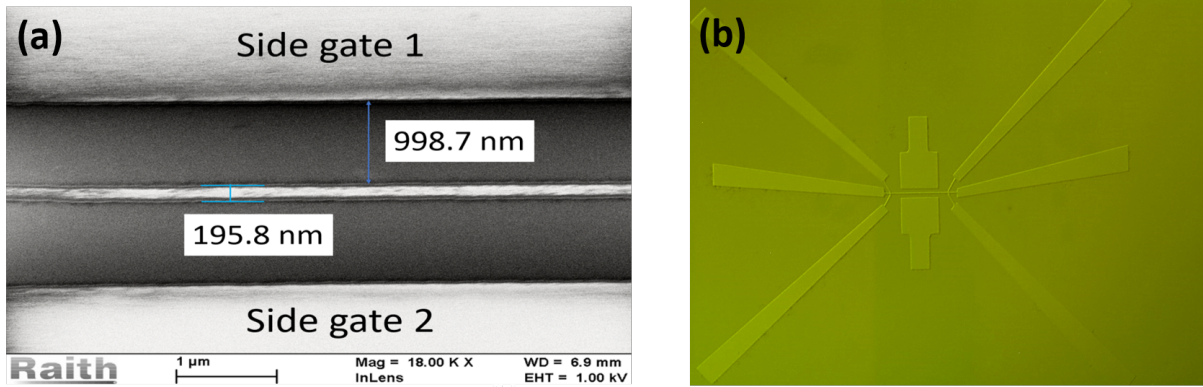


FIGURE 5.9: Shows an SEM image (a) and optical image (b) of a structure with a 200 nm wide channel and gate-channel separation is 1  $\mu\text{m}$ .

### 5.3.1 Charge modulation

Controlling the properties of the materials using an electric field is the key concept in modern electronics. As a first step, we investigate the influence of side gate voltage ( $V_{SG}$ ) on the resistance of the nanostructures. All the measurements we are going to present in this section are done at 4.2 K unless stated otherwise. For all the side gate measurements that are conducted in the following sections, we have considered only one specific orientation angle of the nanostructures, which was not the case with the MR anisotropy and back-gating measurements.

The application of side gate voltages significantly modulates the charge density of the LAO/STO interface as we show in Figure 5.10. A negative side-gate voltage  $V_{SG}$  of less than 1 V increases the channel resistance by four orders of magnitude. The saturation at approx. 2 G $\Omega$  appears only due to an offset in the current measurement that prevents the current measurement to indicate zero current. Increasing the channel width or gate channel separation strongly reduced the charge modulation as shown in Figure 5.10. This

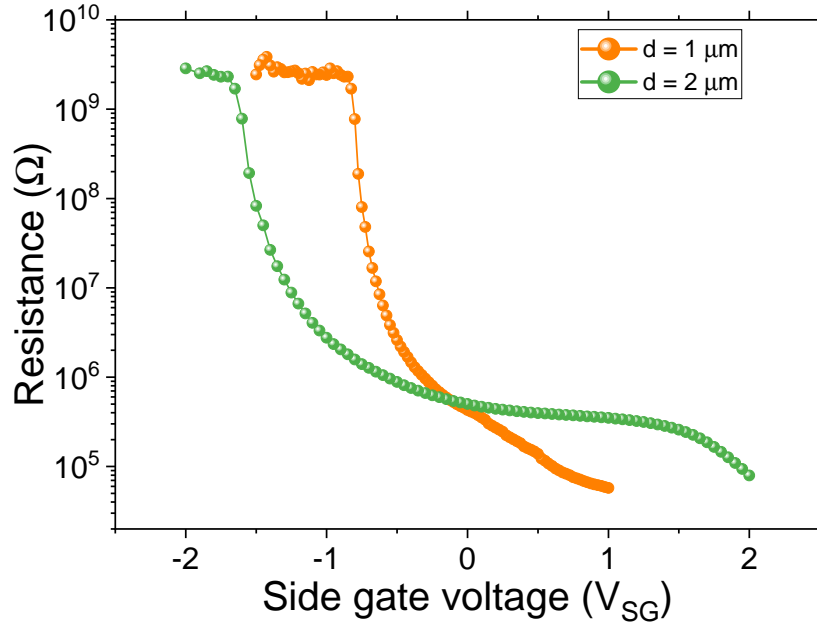


FIGURE 5.10: Resistance vs side gate voltage for a structure with a 200 nm wide channel. Saturation at around approx. 2 G $\Omega$  occurs because of an offset in the current measurement.

strong modulation has been achieved because of the high dielectric constant of STO. Since the thickness of the dielectric is small and due to better focusing of the field lines on the channel, a small gate voltage is enough to modulate the charge density significantly. It has to be noted that side gating act as a local back gate to the interface, where the field lines penetrate through the STO as shown in Figure 5.11 [130].

### 5.3.2 Field induced changes in MR

Next, the magnetoresistance (MR) in the virgin state after cool-down and its behaviour under applied gate voltage is investigated. For these measurements (Figure 5.12) the magnetic field is applied perpendicular to the sample surface. The field is swept from  $B=-6$  T to  $B=+6$  T. The initial MR without applied gate voltage is  $-1\%$  for a 200 nm and  $+4\%$  for a  $1 \mu\text{m}$  wide structure. This small MR with an arbitrary sign is consistent with former observations in [170]. With a small negative  $V_{SG}$  applied, the MR reverses sign to negative for  $1 \mu\text{m}$  (Figure 5.12 c) and becomes more negative for the 200 nm wide bar (Figure 5.12 a). This can be attributed to Weak localization (WL) [129]. Before applying a positive gate voltage, we warm up the sample to room temperature and cool it down again. This is necessary to restore the virgin state as will be discussed below. For positive  $V_{SG} = +0.55$  V, positive MR is observed for both structures indicating increased

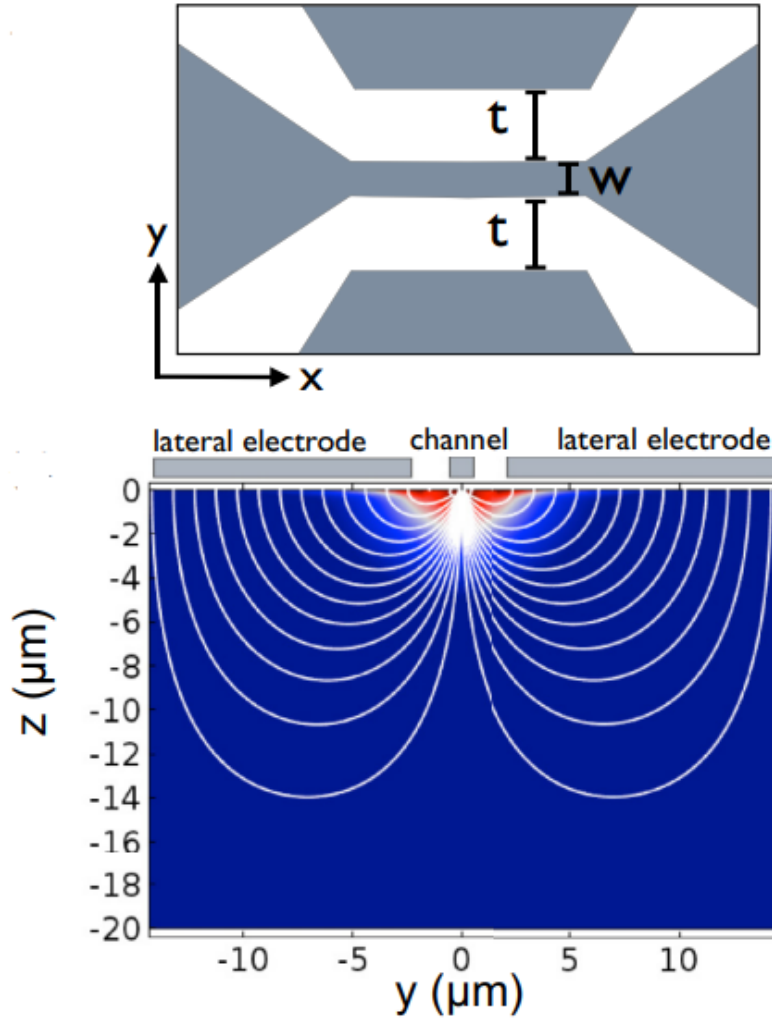


FIGURE 5.11: Simulation of electric field lines in similar side gate configuration used in ref. [130]

electron-electron scattering due to increasing charge carrier concentration or weak antilocalization starting to dominate because of increasing spin-orbit coupling [129]. For the  $1\ \mu\text{m}$  structure gradually the quadratic behaviour is restored (Figure 5.12 c), also pointing towards increased scattering.

In order to study gate-induced persistent modifications of the MR we use the following protocol: The sample is cooled down from room temperature (RT) to 4.2K with  $V_{SG} = 0\text{V}$ .  $V_{SG}$  is then swept from 0V to a value  $V_{SG_{max}}$ , kept at  $V_{SG_{max}}$  for 10 min and then decreased back to 0V, followed by the MR measurement. Then  $V_{SG}$  is swept to a larger  $V_{SG_{max}}$  (smaller for negative  $V_{SG_{max}}$ ), repeating the same procedure. This is repeated until the gate leakage current is larger than  $|I_G| = 1\text{nA}$ . Above a certain threshold of  $V_{SG_{max}}$  we always observe persistent modifications (Figure 5.12 b and Figure 5.12 d) that

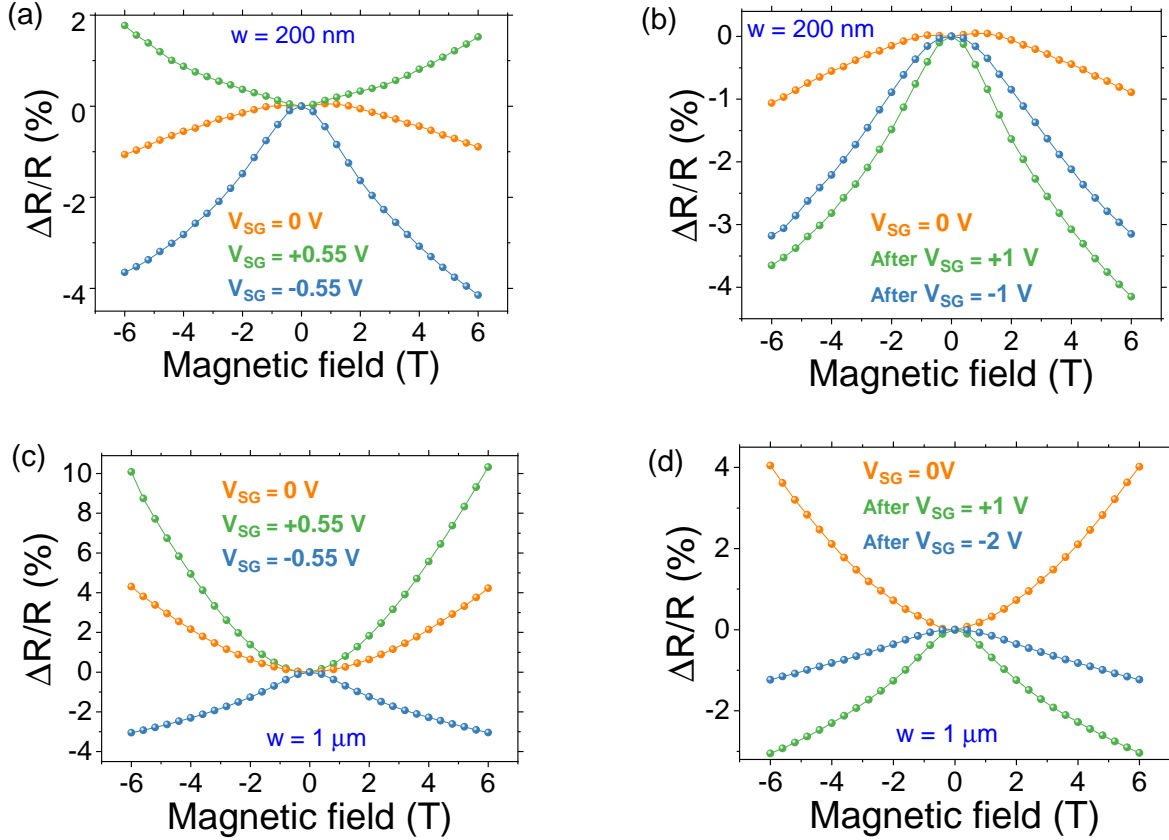


FIGURE 5.12: (a) shows the MR without gate voltage and with positive and negative applied side-gate voltage, respectively, for a 200 nm wide channel at 4.2 K. (c) shows results of the same experiment on a  $1 \mu\text{m}$  wide channel. (b) and (d) show the persistent negative MR after application of  $+V_{SG}$  and  $-V_{SG}$  when  $V_{SG}$  is again swept back to zero for 200 nm and  $1 \mu\text{m}$  wide channel, respectively.

qualitatively are independent of the sign of  $V_{SG}$ . After  $V_{SG}$  is switched off always a negative MR is observed that becomes larger with increasing  $|V_{SG}|$ . The magnitude of this effect is smaller for  $1 \mu\text{m}$  than for smaller structures (shown in Figure 5.13 a,b). This is understandable taking into account that the influence of domain walls decreases with increasing structure width [148, 170].

### 5.3.3 Change in persistent MR with temperature

To clearly relate this persistent MR to domain walls and to the structural phase transitions in STO ( $T_{PT_1} = 65 \text{ K}$  and  $T_{PT_2} = 105 \text{ K}$ ), we investigate whether the persistent MR remains stable after cycling the temperature (Figure 5.14) to different values below and above the phase transition temperatures. After applying the maximum gate voltage at

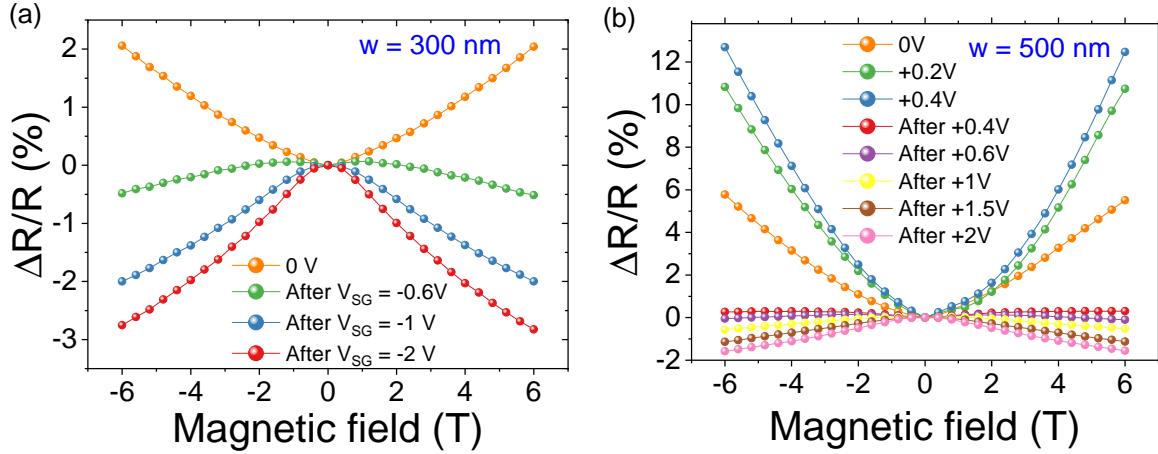


FIGURE 5.13: Side gate induced changes in MR on 300 nm (a) and 500 nm (b) structures.

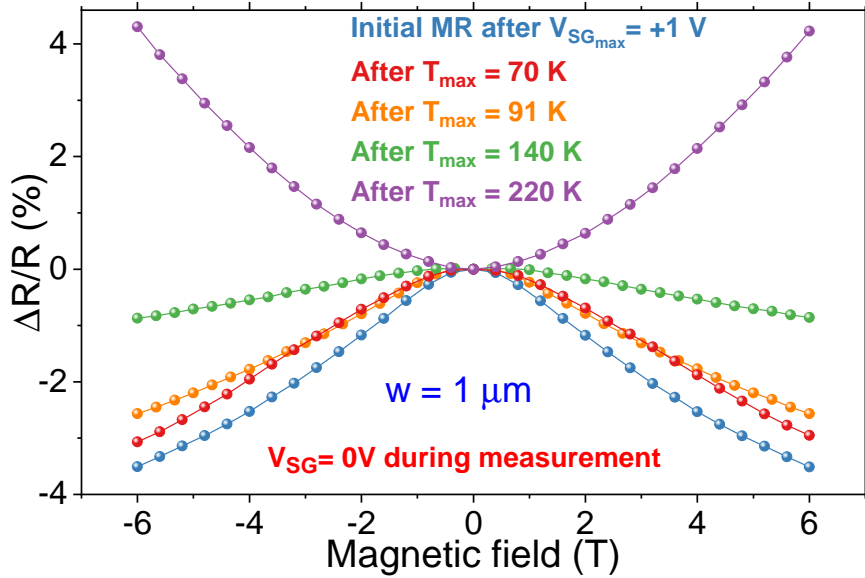


FIGURE 5.14: shows the influence of temperature sweeps on the persistent MR. The persistent MR is only slightly influenced by temperature sweeps to  $T=70$  K and 91 K, however, significant changes are observed when a warm-up cycle is performed to  $T=140$  K. However, a higher temperature sweep ( $T=220$  K) is required to restore the positive MR observed before any gate voltage was applied.



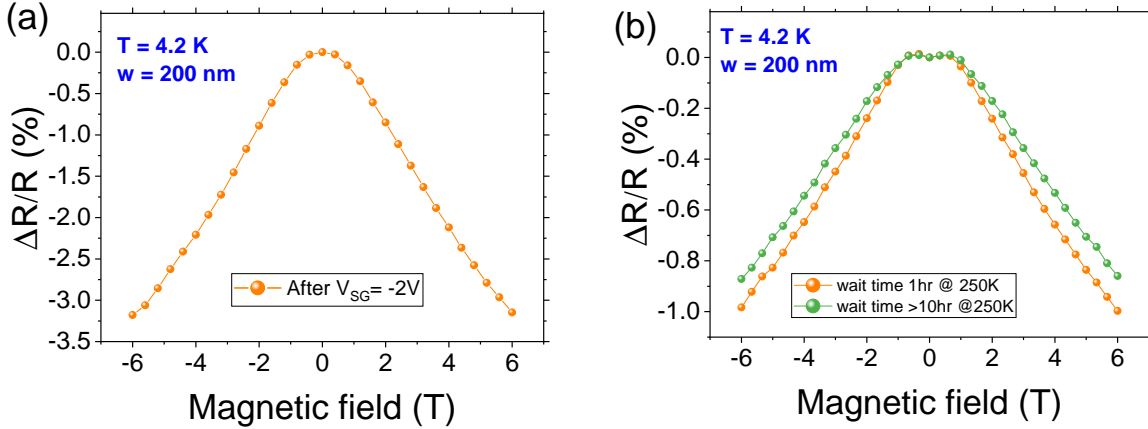


FIGURE 5.15: Here we show how the waiting time at higher temperatures affects the ground state MR. In (a) we present the side gate-induced negative MR at 4.2K. Two experiments were done (b) in which a sample was warmed from the (a) state to 250 K then remained at this temperature for two different respective times (1 hour and 10 hours) and was then cooled again to 4.2 K without side gating to observe if shorter or longer waiting times have any influence on virgin ground state MR. We observe that in both cases the ground state MR is reduced by the temperature cycle, however, there is almost no difference due to the different waiting times.

4.2 K and sweeping back to 0 V, we measured the persistent negative MR. We then warm up the sample to two different maximum temperatures  $T_1 = 70$  K and  $T_2 = 91$  K  $< T_{PT}$  and wait for one hour. Then the sample is cooled down to 4.2 K. An MR measurement after  $T_{max}=70$  K which is slightly above  $T_{PT_1} = 65$  K shows a small reduction of the negative MR. Warming the sample to  $T_{max}= 91$  K which is till below  $T_{PT_2} = 105$  K only slightly increases this tendency. However, the MR measurement done after warming the sample to  $T_{max}= 140$  K which is above  $T_{PT_2} = 105$  K and cooling down to 4.2 K reveals that the negative MR is almost neutralised, but the positive quadratic MR behaviour exhibited by the virgin state of the sample was not yet recovered. This could be due to the additional trapped charge carriers at the interface, which generated the second resistance peak at around 170 K. Further warm-up cycle done to  $T_{max}= 220$  K restores the ordinary MR behaviour of the sample.

### 5.3.4 Modification of sheet resistance and resistance anomaly

Besides the modification of the MR, applying either large positive or large negative gate voltages also induces a persistent increase in the base resistance at  $B=0$  (Figure 5.16 a). The persistent change in base resistance happens with both polarities of the gate voltage,

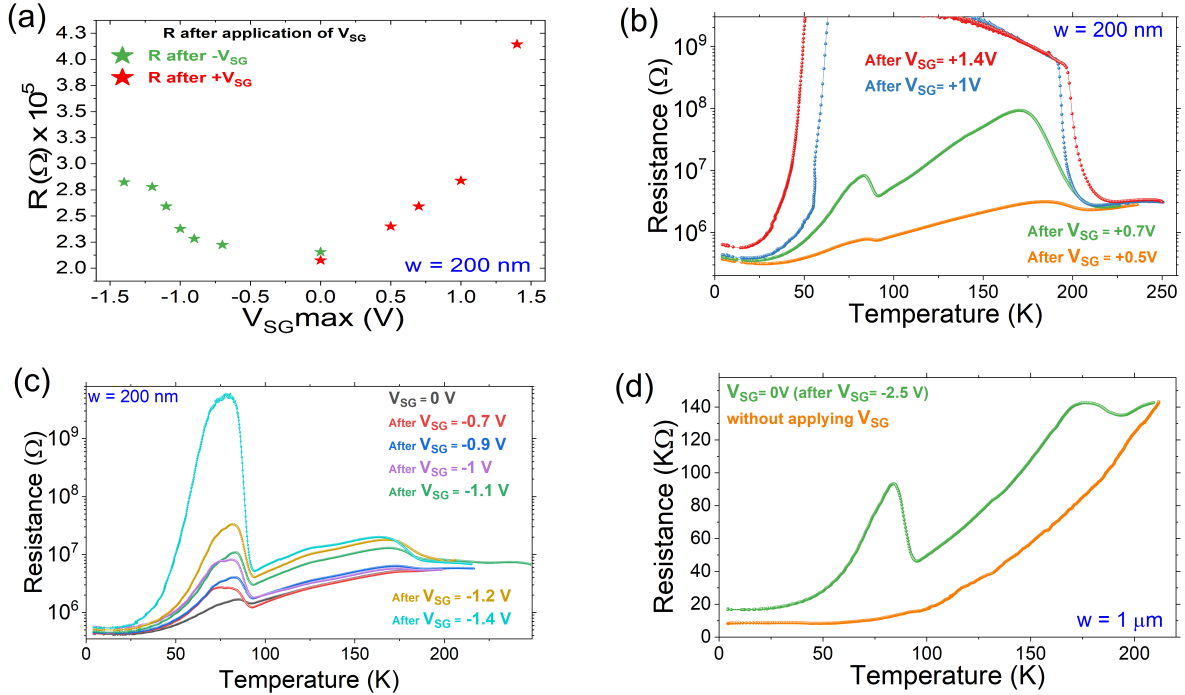


FIGURE 5.16: (a) Shows the persistent change in resistance after application of different positive or negative  $V_{SG}$ , respectively. (b) Temperature-dependent resistance anomaly after persistent modification by applying different positive  $V_{SG}$ . Larger  $|V_{SG}|$  leads to a larger peak during warm-up. Here we observe that the peak at  $T \approx 170$  K is increased (c) Temperature-dependent resistance anomaly in various persistent resistance states induced by a different negative respective  $V_{SG}$ . Similar to (b) larger  $|V_{SG}|$  leads to a larger peak. (d) Even in a  $1 \mu\text{m}$  wide structure where the anomaly is normally not observed in a virgin state, it appears after the application of  $V_{SG} = -2.5$  V.

which is a surprising observation. To gain a deeper insight we perform warm-up temperature sweeps at  $V_{SG} = 0$  after setting the high resistance state at  $T = 4.2$  K by applying a suitably high side-gate voltage. These sweeps are inspired by [148] where the domain wall structure led to large resistance peaks during warm-up for 100 nm wide structures. After gating, we see this huge anomaly even for a structure width of 200 nm which was not possible for ungated structures in [148]. Gate voltages of  $V_{SG} \geq +1$  V or  $V_{SG} \leq -1.4$  V both cause a massive resistance increase of more than three orders of magnitude that appears at  $T \approx 80$  K (Figure 5.16 b and Figure 5.16 c). Interestingly positive gate voltages cause a further anomaly at  $T \approx 170$  K that was also observed in [204, 213]. Even for a  $1 \mu\text{m}$  wide structure a resistance peak (+100%) can be induced by applying  $V_{SG} = 2.5$  V (Figure 5.16 d).

We also apply back-gate voltages, however, they either do not induce similarly large

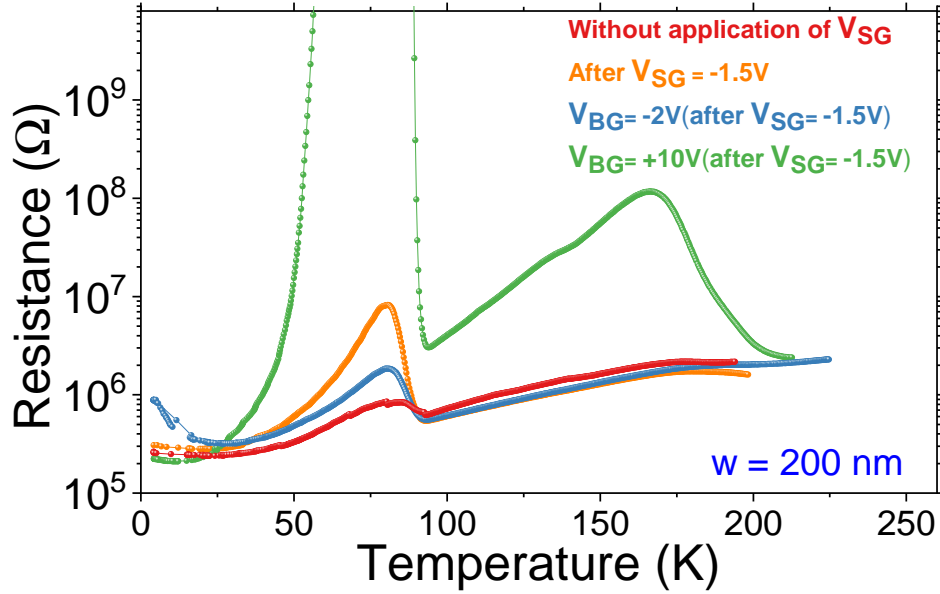


FIGURE 5.17: Influence of back gate voltage on the side-gate induced resistance anomaly. In a structure with only a weak anomaly (red) a negative side-gate voltage leads to an increase of the resistance peak by almost one order of magnitude (yellow). A positive back-gate voltage increases the resistance peak beyond the measurement limit, while a negative back-gate voltage reduces it almost to the original state.

effects or the fields that we can apply this way are too small to achieve a similar modification. Nevertheless, they can still be used to further tune the side-gate-induced persistent state. On a 200 nm wide structure that in the virgin state only shows a moderate resistance increase at 80 K during warm-up, we first apply a side-gate voltage of  $V_{SG} = -1.5\text{ V}$ . Repeating the warm-up procedure now shows a resistance increase at  $T=80\text{ K}$  of more than one order of magnitude. Because the persistent state is reset during the temperature sweep we again apply  $V_{SG} = -1.5\text{ V}$  after cooling to  $T=4.2\text{ K}$  and before performing another warm-up now with a constant back-gate voltage of  $V_{SG} = -2\text{ V}$ . This warm-up only shows a moderate resistance peak at  $T=80\text{ K}$  which, nevertheless, is still higher than the one observed in the virgin state. Repeating the sequence with a back-gate voltage of  $+10\text{ V}$  during warm-up, however, increases the resistance at  $T=80\text{ K}$  well beyond our measurement limit. Figure 5.17 shows the influence of the back-gate voltage on the resistance anomaly. The results are consistent with the negative gate voltage pushing the electrons out of the STO or at least out of the domain walls while a positive one pulls them into the domain walls and further depletes the surrounding area.

## 5.4 Discussion

By implementing the side gate configuration, we modulate the 2-dimensional electron gas (2DEG) at the interface of LAO and STO and studied the influence of the electric field on the transport properties of nanostructures. The electric field enhances the mobility of domain walls [136, 143, 144] and a large electric field induces ferroelectricity at the domain walls [147]. In nanostructures, the transport properties of the interface are predominantly influenced by the number and orientation of domain walls [148, 170]. So, the influence of the electric field will be very significant in small-sized structures. As the dimension of the structure is increased, the effect also decreases. The electric field induces a persistent change in the transport properties resulting from the change in domain wall properties and distribution.

An irreversible increase in resistance after back-gating has already been observed, however, only for positive back gate voltages [205, 207]. In those cases, the explanation was the trapping of electrons in in-gap trap states which are generated as a result of electromigration and clustering of oxygen vacancies in STO. No such irreversibility has been reported after the application of negative gate voltages as reported here, which is also not consistent with this explanation. Furthermore, in addition to the resistance increase we also observe the persistent changes in MR and the resistance anomaly during heating (even for structure larger than  $1\ \mu\text{m}$  as in Figure 5.18 c,d), indicating that the trapping is not the underlying mechanism in our case. A change in magnetoresistance might partly be explained by a change in carrier concentration [129]. Nevertheless, the partly random effect and its appearance for both gate voltage polarities would not be consistent with trapping but fits a change of the predominant domain wall type. The same holds for the resistance peaks observed during heating.

The main observations that cannot be explained by recent theories stand out by their appearance at both gate voltage polarities at high gate voltages. In the following, we will explain how they can be caused by an expansion of the domains and a resulting reduction of the number of domain walls. Ma et al. [147] showed that ferroelectricity can be induced in STO domain walls (no bulk ferroelectricity) if an electric field greater than a threshold value (1.4 kV/cm) is applied. The induced ferroelectric domain walls were persistent even after the gate voltage was switched back to zero. Several studies show that the application of a gate voltage can lead to preferential selection of in-plane domains in STO [136, 143]. This selection process is independent of the electric field direction and leads not only to a reduction of the number of the domain walls but also increases the average domain size and thus the average length of continuous domain walls with no branching. The expansion

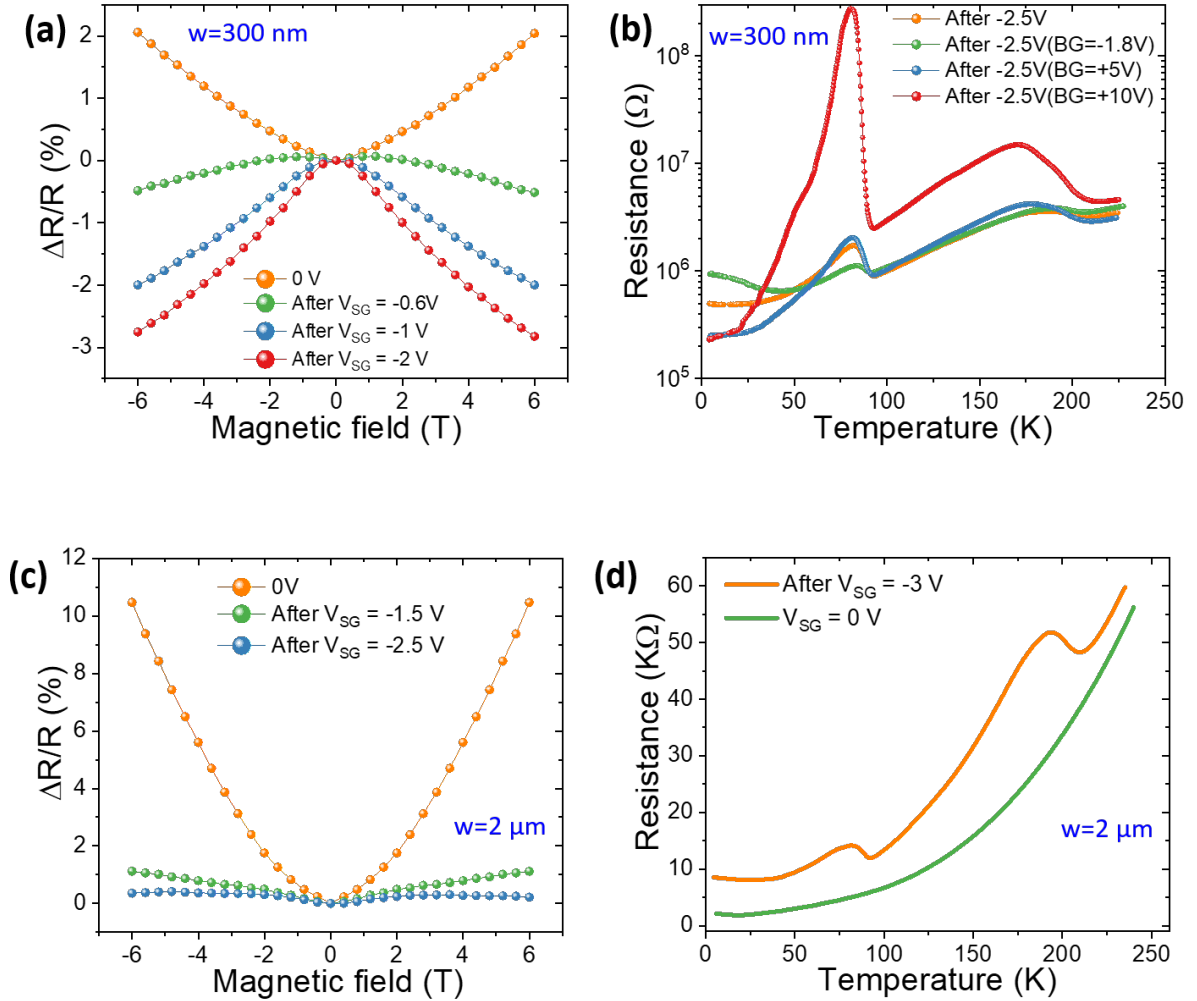


FIGURE 5.18: (a) Shows the MR in the virgin state after cool-down and after applying different side gate voltages  $V_{SG}$ , respectively, for a 300 nm wide structure. (b) Shows the gate-induced resistance peak around 80 K for the 300 nm wide structure and the dependence of resistance peak on the back gate voltage. Even for a  $2 \mu\text{m}$  wide structure a side gate voltage  $V_{SG}$  leads to the non-volatile appearance of domain wall-related transport effects as shown in (c) and (d).

of the in-plane domain occurs as a result of dielectric anisotropy of tetragonal STO [143]. Casals et al.[143] show that the polarizability is significantly larger along the normal to the AFD tilt axis. This implies that in-plane domains, as well as preferential domain wall types, are energetically favoured under an applied electric field. After removing the gate voltage, the domains are again equally stable and none of them is energetically favourable. Nevertheless, in case of a sufficiently large change in the domain landscape, this will only stabilize the new state but not restore the original domain structure. In addition, induced ferroelectric domain walls may hinder the restoration of the initial domain configuration.

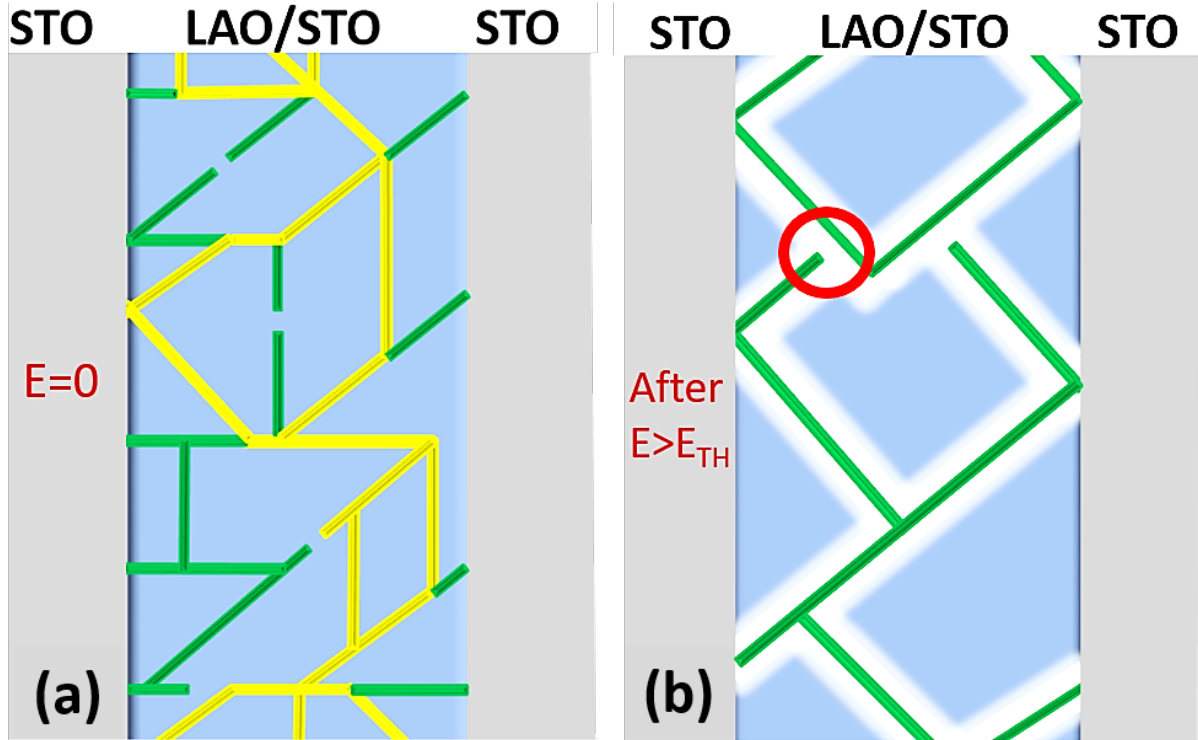


FIGURE 5.19: Simplified sketch of a scenario in which gate-induced growth of domain size changes the transport properties of an LAO/STO nanostructure. In the original domain wall pattern (a) even some breaks that may appear close to the phase transition will not interrupt the current path (yellow). When several domains are pushed out and the domain size increases (b), it is much more likely that in a nanostructure a single break interrupts the current path and effectively suppresses the current flow. Although logical, this picture is speculative because it does not include possible dead-end filaments or conducting patches in insulating areas that may exist according to [206]. Nevertheless, these would neither carry current nor would they contribute to the experimental observations.

This claim is supported by the requirement of threshold back gate voltage to observe the irreversible motion of domain walls [136].

The influence of domain growth is manifold. The most basic effect is on the baseline resistance (Figure 5.16 a). Assuming that the conductivity of the domain walls does not vary much, domain growth leads to an increase in baseline resistance because the number of parallel conductance channels is decreased while the average length of the channels increases. The further influence appears in the magnetotransport because the orientation of the domain wall plays a crucial role in determining MR behaviour. As a result of phase transition, two types of domain walls are formed: one type extends perpendicularly into the substrate while the other is inclined at an angle of  $45^\circ$  [136]. So magnetic field applied perpendicular to the surface will never be perpendicular to

these domain walls. As a result, ordinary MR is suppressed, and other contributions like Weak localisation (WL), weak anti-localisation (WAL) and electron-electron interactions start to dominate [170]. Different domain wall MR with respect to the magnetic field orientation has been observed in BFO thin films [197]. The domain walls between the in-plane domains extend perpendicularly into the substrate, and the applied field will act as an in-plane field to these domain walls (suppress ordinary MR). Also increased resistance after the application of side gate voltage enhances the WL effect [129, 130]. This provides a reasonable explanation for the negative MR behaviour.

The dependence of the persistent MR on temperature sweeps also confirms the theory presented by Minhas et al [148]. The persistent negative MR after the application of side gate voltage shows a slight change when the sample is heated to temperatures above  $T_{PT_1} = 65$  K but less than  $T_{PT_2} = 105$  K. This supports the claim made by Minhas et al. that the domain walls start to break after this low-temperature tetragonal to an orthorhombic phase transition. But no redistribution of the domain walls happens at  $T_{PT_1} = 65$  K. For the redistribution of the domain walls, the interface should be warmed above the cubic-tetragonal phase transition temperature  $T_{PT_2} = 105$  K [137]. Also, a partial redistribution of charge carriers will occur due to the loss of domain wall polarity at around 80 K which could also lead to a change in negative MR. However, after warmup - cooldown cycle to 140 K ( $> T_{PT_1} = 105$  K) the negative MR almost vanishes. This can be explained by the reorientation of domain walls after the phase transition. But the ordinary MR is not yet restored. After the warmup-cooldown cycle to  $T_{max} = 140$  K, the sample resistance at 4.2 K is much higher than the normal state resistance. This indicates that there is still some charge carrier trapping happening. This additional charge trapping is possibly due to the higher thermal energy required for de-trapping the previously trapped charge carriers or because of the surface cubic-tetragonal phase transition happening in STO at high temperatures that could be a source of electron trapping. The resistance curves always exhibit a second resistance peak at 170 K which indicates the release of trapped charge carriers. So we could assume the complete restoration of ground state resistance and MR occurs only after the temperature sweep to higher temperatures ( $T_{max} = 220$  K) as shown in [Figure 5.14](#)

The temperature-dependent resistance anomaly gives a further indication. Without a gate voltage, the effect is observed only in structures which are less than a few hundred nm in width. Applying a gate voltage extends this observation range at least to a structure size of at least 2  $\mu$ m which is compatible with the image of increasing domain size. But still, for larger structures, the effect does not appear which should be the case if carrier freeze-out were the origin. The onset of the resistance peak during warm-up always

appears well below 80 K [148]. The maximum is always at 80 K or slightly above. After continuing the warm-up of the sample, the resistance again increases forming a second peak at around 170 K. Even though the bulk structural phase transition temperature of STO is at 105 K [48], the nature of domain walls starts to modify at lower temperatures such as tetragonal to orthorhombic transition at 65 K [38, 48] has been reported for STO. The onset of the polarity of domain walls is reported at around 80 K [214]. Minhas et al. [148] have shown that the peak only appears when the sample is cooled below 65 K, showing the significance of the second phase transition. They have also demonstrated that the increased resistance during warm-up remains stable over time at temperatures of 60 K and 70 K, but the resistance drops almost to the cooling curve value after an initial increase when the temperature is held constant at 80 K. The changes in the nature of domain walls start to take place at lower temperatures. So the resistance peak should not necessarily coincide with the phase transition temperature of STO. Moreover, T=80 K nicely coincides with the onset of the polarity of the domain walls [214]. The earlier first-principles study has indicated the tendency of oxygen vacancies to migrate and accumulate at the domain walls [215]. Therefore, as the amplitude of the positive voltage increases, trapping centres like oxygen vacancies in domain walls increases in number, thus, the resistance grows. So this additional charge trapping enhances the effect when a positive side gate voltage is applied. Resistance peaks at 80 K and 170 K are higher for positive side gate voltage.

The additional peak that often appears at T $\approx$ 170 K is of a slightly different origin. Most likely, it is related to a different cubic-tetragonal structural transition observed at STO surfaces or interfaces at higher temperatures, as reported by Salman et al. [216]. It has been reported by Salman et al. [216] that a cubic-tetragonal transition takes place at  $\sim$ 150K when the surface layer of STO is 150 nm thick. Moreover, the critical temperature will monotonically increase as surface layer thickness decreases. It is, therefore, a reasonable inference that the outermost STO layers undergo a phase transition at temperatures  $\sim$ 170 K when warmed up, releasing confined charge carriers [217]. The tendency for the oxygen vacancies to migrate and accumulate at the domain walls has been previously reported [215]. When the temperature exceeds 170 K, the surface tetragonal-cubic transition takes place, and sheet resistance exhibits an abrupt drop due to the release of trapped carriers, which corresponds to the second peak and is enhanced by a positive side gate voltage. The positive side gate voltage also enhances this secondary peak. Especially the temperature-dependent measurements show that charge trapping is not absent but occurs in parallel with the changes in a domain structure. While increasing gate voltage increases the resistance peak for both polarities, the effect is even more pronounced for



positive gate voltages that should lead to additional carrier trapping. Because the removal of domain walls happens both at positive and negative fields, it cannot be reversed by reversed gate voltages. Only by warming up through the phase transition temperature can we restore a higher number of domains and domain walls.

## **5.5 Conclusion**

Our back-gating experiments showed that the application of back-gate voltage significantly changes the random crystalline anisotropy in MR in LAO/STO nanostructures. Application of positive  $V_G$  enhances MR anisotropy while negative  $V_G$  suppresses the MR anisotropy. Furthermore, positive  $V_G$  induces persistent modification in magnetotransport properties, even for  $1\ \mu\text{m}$  structure and a significantly large resistance peak is induced in 200 nm structure. These effects can be attributed to the gate voltage-induced trapping of electrons and the influence of domain walls on the transport properties of structures with a few hundred nm in dimensions.

The results from side gating experiments have significant consequences for the interpretation of low-temperature transport experiments in LAO/STO. Regardless of the results published on domain wall-related transport, most experiments ignore these properties in their interpretation, well knowing that in structures larger than a few hundred nm the effects average out, and large area transport properties are still a good approximation. Our experiments show that even a gate voltage as small as 1 V can change the domain structure and invalidate this paradigm. This gate voltage can change the domain size and decrease the number of domain walls. As a consequence, effects formerly restricted to structures of less than 200 nm in width can now appear in structures ten times as large. On the other hand, our experiments also show that there is an additional tuning knob to change the transport properties of this versatile material system persistently.

## *Summary and scope for Future Work*

The main objective of this PhD work was to study the role of domain walls on the transport properties of the LAO/STO interface. Most of the theoretical explanation of transport phenomena of the LAO/STO interface does not take into account the influence of domain walls. But recently, more and more studies have revealed the influence of domain walls in transport. Modulating charge conduction through the domain walls was first reported in 2013 and has been under investigation since then. The significance of domain walls becomes more enhanced when the lateral dimension of the structures becomes smaller (a few 100 nanometers), and many exciting effects show up which cannot be explained by the existing mainstream theory. Still, one has to take into account filamentary transport. The work in this thesis can be considered a follow-up study of the significance of domain walls in LAO/STO nanostructures. We have systematically studied how the orientation of domain walls influences the magnetotransport properties and field effect devices.

We have utilised a special sample geometry with large-area structures and nanostructures oriented at 4 different angles to study how the MR varies with orientation. No variation in MR and baseline resistance was observed with the orientation angle for large-area structures. This is because the influence of domain walls on transport is negligible in large-area structures as their effect averages out due to the presence of a large number of randomly oriented domain walls. Due to the random distribution of the domain walls, it is possible to have combinations with different contributions from both types of domain walls. Even for the same conduction direction, we may have very different combinations of domain walls in the conducting channel that may also have different resistance depending on their respective lengths. The magnitude, the sign of the MR, and the total resistance depend on the initial domain wall pattern, which is formed during cool-down. This pattern is random, and we have shown that different resistance and magnetoresistance states are achieved for different cool-downs through the structural phase transitions.

The out-of-plane magnetic field results in positive quadratic MR, which is due to the orbital effect and is often termed ordinary MR. However, when the magnetic field is in-plane, or the lateral size of the structures is small, the ordinary MR is effectively suppressed. Without ordinary magnetoresistance to compete with, other contributions like localisation effects and electron-electron interaction can start to dominate. Depending on the dominant scattering mechanism, the sign and magnitude of the MR vary. The random

redistribution of domain walls after the temperature sweep above the phase transition changes the domain types and configuration within the conducting channel. This, in turn, leads to a change in MR behaviour. The crystalline anisotropy of MR observed in LAO/STO nanostructures, which is not seen at large area 2D structures, can only be explained if we take domain walls into account.

Our next goal was to study the role of domain wall transport on field effect devices. We have successfully implemented side-gated and back-gated device configurations for this study. As previously reported, back gating experiments reveal that positive back gate voltage irreversibly modifies the MR and ground state resistance of the interface. These modifications are attributed to the trapping of electrons at oxygen vacancies.

Another important aspect of this thesis is that we observe major persistent modifications of the ground state irrespective of side gate voltage polarity. Former studies showed persistent changes attributed to charge carrier trapping and oxygen vacancies, which was supported by the fact that the modifications were only observed at positive gate voltages. Our side-gating techniques also allow us to observe these changes at negative gate voltages. The persistent modification of the domain wall pattern can only be reset (to repeat the experiment) by warming through the structural phase transition to remove all domain walls and cooling through the phase transition to create a new pattern. This pattern, however, will have a different number, length, and type of domain walls than the state obtained after the last initialization. We can now link these modifications to the expansion of domains which up to now was only observed by optical studies and that was not linked to changes in transport properties.

A second aspect of the side-gate measurements, which can only be demonstrated by the side-gating technique, is the observed scaling of the structure size in which domain-related transport effects are observed. As previously shown, transport through domain walls can dominate the conductivity in structures smaller than a few hundred nm. In larger structures, parallel conduction through parallel domain walls makes the effects small or even undetectable. In our experiments, we increase the average domain size and reduce the number of parallel domain walls. This way, we increase the size limit of 200 nm observed before to at least 2  $\mu\text{m}$ .

Each cool-down creates a state whose behaviour is consistent with the presence of domain wall transport and in which larger side gate voltages of both polarities induce an increase in resistance that is consistent with the growth of the domains. We see that the domain wall-related effects are strongest in small devices where the number of domain walls is small because the domain walls are in parallel, which leads to an inverse

proportionality of resistance and domain wall number. A hint of the desired effect is merely seen in the resistance anomaly during warm-up. There for very small structures where we may have only a single domain wall, breaking this wall leads to a jump to (almost) infinite resistance. In larger structures where we may have two domain walls breaking one of them only leads to a moderate resistance change. For more than two domain walls, the relative effect decreases dramatically. Reducing the number of domain walls by gating again increases the relative effect dramatically. It can even lead to a sizeable resistance anomaly in 1  $\mu\text{m}$  wide structures where this is normally not observed.

For the small-sized samples, the influence of the domain wall on the transport is very significant since they are limited in number. The orientation of the domain walls also plays a key role. Our results from the MR and gating experiments cannot be explained by a homogeneous interface but easily agree with filaments. They are even in agreement with the two types of domain walls in the STO that are differently oriented with respect to the surface. This thesis adds to a deeper understanding of the physics of the LAO/STO interface that is still highly relevant and even subject to more topics like spin pumping or spin-to-charge conversion, which all require the right picture of the interface properties for correct interpretation. This work also shows that there is an additional tuning knob to persistently change the transport properties of this versatile material system.

As a follow-up study, the influence of domain walls on the sub-Kelvin transport properties of the LAO/STO interface can be studied. It would be interesting to see how the orientation of the number of domain walls can affect the superconducting behaviour of the interface. Since we have demonstrated that side gating can be used to modify the interface's domain wall configuration persistently, side gating can be used to study the correlation between domain configuration and superconducting transition. These studies are more relevant since the findings of our work are not only limited to the LAO/STO interface but also applicable to other STO-based heterostructures and possibly to other heterostructures with modulated charge conduction through the domain walls.

Even though this thesis sheds light towards the roles of domain wall orientation and the field-induced domain wall motion on the transport properties of the LAO/STO interface, the exact picture is still not clear. So more theoretical and experimental works need to be conducted in this area to develop a complete model for domain wall transport.

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# List of Publications

## Journals

1. **Prasad, M. S.**, Schmidt, G., "Anisotropic magnetotransport in  $\text{LaAlO}_3/\text{SrTiO}_3$  nanostructures." *Physical Review B* 104, 054115 ( 2021)
2. **Prasad, M. S.**, Schmidt, G., "Persistent modification of magnetotransport properties in  $\text{LaAlO}_3/\text{SrTiO}_3$  by gate induced modification of structural domains." (*Phys. Rev. Research* 5, 013166 (2023))
3. **Prasad, M. S.**, Schmidt, G., "Back gate induced persistent change in transport properties in LAO/STO." (Under preparation)

## Conference contributions

1. **Mithun S. Prasad**, Mohsin Minhas, Alexander Müller, and Georg Schmidt, "Investigation of LAO/STO nanostructures", Poster, DPG, Berlin, Germany (2018)
2. **Mithun S. Prasad** and Georg Schmidt, "Anisotropic transport properties in LAO/STO nanostructures", Talk, DPG, Regensburg (2019)
3. **Mithun S. Prasad** and Georg Schmidt, " Anisotropic Magnetoresistance in LAO/STO nanostructures", Poster, DPG, Dresden (2021)

# Curriculum vitae

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## Education

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## Eidesstattliche Erklärung

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Weiterhin erkläre ich, dass ich bisher keine vergeblichen Promotionsversuche unternommen habe. Diese Dissertation hat in ihrer gegenwärtigen bzw. in einer anderen Fassung bisher keiner anderen Fakultät vorgelegen.

Mithun Sheena Prasad  
Halle (Saale), December 2023