Wideband impedance spectrum analyzer with arbitrary fine frequency resolution for in situ sensor applications

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Preface

The present thesis results from my work as research assistant at the Sensor and Measurement Technology group in the Institute of Micro and Sensor Systems at the Otto-von-Guericke-University Magdeburg.

First, I would like to express my special gratitude to my doctoral advisor Prof. Dr. Peter R. Hauptmann for providing me the opportunity to carry out my research work on an interesting and diversified topic, and for all guidance and support.

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Zusammenfassung

Die Verwendung moderner Sensoren erfordert geeignete Messmethoden und Messinstrumente, um die Sensorantwort hinsichtlich der Zielparameter des zu untersuchenden Mediums genau zu bestimmen. Das Impedanzspektrum des Sensors liefert vielfache Informationen, die Schlussfolgerungen über den Entwurf des entsprechenden Sensors, die Sensor-Medium Interaktion oder zur weitergehenden Modellierung zulassen. Zu diesem Zweck ist die Analyse des Sensorimpedanzspektrums in Laboranwendungen unter Verwendung handelsüblicher Messinstrumente weit verbreitet. Die vorliegende Arbeit stellt ein neues Elektroniksystem vor, das breitbandige Impedanzspektrumsanalyse für ortsveränderliche *in situ* Sensoranwendungen zur Verfügung stellt. Im Unterschied zu den umfangreichen Labormessinstrumenten zeichnet sich das entwickelte Elektroniksystem durch einen kompakten, eigenständigen Messaufbau für Sensoranwendungen im Labor sowie industriellen Bereich aus und ermöglicht eine sehr schnelle Messdatenerfassung.

Das Elektroniksystem ist hauptsächlich für Anwendungen von akustischen Mikrosensoren und kapazitiven Messsonden bestimmt. Mit diesen ausgewählten Sensoren wird den unterschiedlichen Anforderungen an schmalbandige and breitbandige Impedanzspektroskopie entsprochen. Damit kann das Elektroniksystem vielseitig für jeden Sensor verwendet werden, der elektrische oder mechanische (wie akustische) Signale in eine elektrische Impedanz wandelt. Unter Berücksichtigung der Hauptzielsetzung eines minimierten Schaltungsaufwandes wurde ein ausgereiftes Hybridsynthesizerdesign entwickelt, das verschiedene analoge und digitale Synthesetechniken kombiniert. Es bietet eine breite Frequenzabdeckung (10 kHz–1 GHz) mit beliebig feiner Frequenzauflösung (<1 Hz) sowie ausreichende Spektralqualität des Ausgangssignals. Eine signifikante Verringerung des Gesamtschaltungsdesigns sowie eine schnelle Sensordatenerfassung werden durch eine Direktabtasttechnik erreicht, die die hochfrequenten Messsignale ohne bedeutende analoge Signalaufbereitung analog-digital wandelt. Da die Gesamtmessgenauigkeit hauptsächlich von dem Signal-Rausch-Verhältnis der direkt abgetasteten Messsignale bestimmt wird, erfolgt die Bestimmung der Signalparameter (Amplitude und Phase) auf der Basis einer Optimierungsmethode zur Sinuskurvenanpassung. Eine deutliche Rauschminderung kann durch die Anzahl der gewählten Abtastwerte erreicht werden. Zur Unterstützung einer schnellen Messdatenerfassung wurde anstelle softwarebasierter Berechnungen der Sinuskurvenanpassung eine hardwarebasierte Implementierung der digitalen Signalverarbeitung in programmierbarer Logik realisiert.

Testmessungen mit definierten Lastimpedanzen bestätigten eine mit Labormessgeräten vergleichbare Messgenauigkeit. Konkrete Anwendungen des Elektroniksystems für die Impedanzspektroskopie an verschiedenen resonanten Mikrosensoren und mit einer kapazitiven Messsonde für die Flüssigkeitsanalytik werden demonstriert.

Abstract

The application of modern sensor devices requires appropriate measurement methods and sophisticated electronic instruments in order to precisely determine the sensor response with regard to the target parameters of a medium under study. The impedance spectrum of the sensor provides multiple information, which allows for conclusions about the design of the sensor device, the sensor-medium interaction, or for advanced modeling. For this purpose, the analysis of the sensor's impedance spectrum is well established in laboratory applications using commercial benchtop instruments. The present work introduces a novel electronics system that provides wideband high-frequency impedance spectrum analysis for portable *in situ* sensor applications. Unlike bulky benchtop instruments, the electronics system allows for a compact, stand-alone *in situ* measurement setup for laboratory as well as industrial sensor applications and very fast data acquisition.

The electronics system is primarily intended for sensor applications of acoustic microsensors and capacitive sensor probes. These particular sensor applications specify the different measurement requirements on wideband and narrowband impedance spectroscopy. This provides universal applicability of the electronics system to any appropriate sensor that transduces electrical or non-electrical (such as acoustic) signals into an electrical impedance. With regard to the main objective of minimizing circuit design, a sophisticated single-board hybrid synthesizer architecture combining various analog and digital synthesis techniques has been developed, which properly meets the requirements on broad frequency coverage (10 kHz–1 GHz) with arbitrary fine frequency resolution (<1 Hz), fast frequency settling, and good spectral quality of the output signal. Significant reduction of the total circuit design as well as fast sensor data acquisition are achieved by utilizing a direct-sampling technique that analog-to-digital converts the high-frequency measurement signals without decisive analog signal conditioning. Since the overall measurement precision primarily depends on the signal-to-noise ratio of the directly sampled signals, a sine-wave fitting algorithm for extracting the crucial signal parameters (amplitude and phase) is applied. Significant noise reduction can be achieved by the number of chosen samples. To support the fast data acquisition capability, instead of software computation of the sine-wave fitting, a complete hardware implementation of the digital signal processing into a field-programmable gate array has been realized.

Test measurements with well-defined impedance load conditions confirmed a sufficient measurement precision, which is comparable to that using a standard benchtop instrument. Applications of the electronics system for impedance spectroscopy on various acoustic microsensors and a capacitive sensor probe for in-liquid measurements are successfully demonstrated.

Contents

List of Symbols

A	amplitude parameter of the sine-wave fitting
	electrode area
B	amplitude parameter of the sine-wave fitting
	bandwidth
	susceptance
B_{loopll}	phase locked loop bandwidth of the local-oscillator
B_{pll}	phase locked loop bandwidth
B_{rfisa}	system bandwidth
B_{rfpll}	phase locked loop bandwidth of the radio-frequency-oscillator
b	amplitude resolution of the analog-to-digital converter
C	capacitance
C_{ext}	external parallel capacitance of the quartz resonator
C_0	static capacitance enclosing the quartz resonator
$C_0^{'}$	capacitance representing the mechanical elasticity of the quartz resonator
c_{q}	complex shear modulus of quartz
c_{ij}	coefficients of the sine-wave fit matrix
$\mathbf{D}$	parameter matrix of the sine-wave fitting
$\vec{D}$	electric displacement field
$\vec{D}_0$	electric displacement field in free space
d	amplitude resolution of the digital-to-analog converter
	electrode spacing
	thickness of the quartz resonator
$\lvert\mathbf{D}\rvert$	determinant
$\vec{E}$	electric field
e_{aq}	discrete amplitude quantization error sequence
e_{q}	piezoelectric constant of quartz
e_{pq}	discrete phase truncation error sequence
f	frequency

f_{adcclk}	sampling-clock frequency of the analog-to-digital converter
f_{base}	base frequency of the direct digital frequency synthesizer
f_i	input frequency
f_{dacclk}	sampling-clock frequency of the digital-to-analog converter
f_{ddfs}	frequency of the direct digital frequency synthesizer
$f_{ddfsclk}$	sampling-clock frequency of the direct digital frequency synthesizer
f_{lo}	loal oscillator frequency
f_{lopll}	output frequency of the local-oscillator phase locked loop
f_{if}	intermediate frequency
f_m	sideband frequency
f_o	output frequency
f_p	frequency at zero phase
f_{pd}	phase detector frequency
f_{pll}	frequency of the phase locked loop
f_{res}	resonance frequency at conductance maximum
f_{rfpll}	frequency of the radio-frequency phase locked loop
f_s	frequency at zero phase
	sampling-clock frequency
f_{vco}	voltage-controlled oscillator frequency
f_{Zmax}	frequency at maximum impedance
f_{Zmin}	frequency at minimum impedance
f_0	fundamental (mechanical) resonant frequency of the quartz resonator
G	conductance
	gain factor
	direct-current component of the sine-wave fitting
G_{dvgs}	digital-controllable gain range
G_L	complex shear modulus of the coated film
G_ε	conductance related to the dielectric loss factor
F	noise factor
FSR	full-scale ratio
i	index
I_s	complex response current
$\hat{I}_s$	response current amplitude
i_s	response current
J	integer number of sample points
j	index
K	effective gain factor of the phase locked loop
	electromechanical coupling coefficient of quartz

K_{CP}	gain factor of the charge-pump
k	complex current-to-voltage conversion factor
	discrete frequency-domain index
K_{VCO}	gain factor of the voltage controlled oscillator
L	single-sideband phase noise power
L_0	inductance representing the initial mass of the quartz resonator
M	integer number of cycles in the data record
	integer multiplication factor
N	feedback divider value
	integer divisions factor
N_{lo}	feedback divider value of the local-oscillator phase locked loop
N_T	transformer turn ratio
NF	noise floor power
n	discrete time-domain index
OTW	integer offset tuning word
P	numerical period
$\vec{P}$	electric polarization
P_{clk}	sampling-clock phase noise power
P_i	input phase noise power
P_{pd}	phase detector phase noise power
P_o	output phase noise power
P_s	total signal power
P_{ssb}	single-sideband power of phase noise in 1 Hz bandwidth
p	amplitude resolution of the analog-to-digital converter
Q	quality factor
R	reference divider value
	magnitude parameter
	resistance
R_{el}	electrical resistance of the quartz resonator
R_0	resistance representing the energy loss of the quartz resonator
RBW	resolution bandwidth of the spectrum analyzer
r	complex voltage ratio
	phase accumulator resolution
r_{clk}	clock ratio
r_{load}	complex voltage ratio for well-known impedance
r_{open}	complex voltage ratio for open circuit
r_{short}	complex voltage ratio for short circuit
S	discrete frequency-domain sequence

$SFDR$	spurious-free dynamic range
$SFDR_{ddfs}$	spurious-free dynamic range of the direct digital frequency synthesizer
SNR	signal-to-noise ratio
SNR_{adc}	signal-to-noise ratio of the analog-to-digital converter
SNR_{ddfs}	signal-to-noise ratio of the direct digital frequency synthesizer
SNR_{jitter}	signal-to-noise ratio attributed to sampling-time jitter
$SQNR_{adc}$	signal-to-quantization-noise ratio of the analog-to-digital converter
$SPTW$	integer sine-fit phase tuning word
s	Laplace operator
s_a	input signal port A
s_{adcclk}	clock signal of the analog-to-digital converter
s_b	input signal port B
s_{adcclk}	clock signal of the direct digital frequency synthesizer
s_i	input signal
s_{if}	intermediate signal
s_{lo}	output signal of the local oscillator
s_{lopll}	output signal of the local-oscillator phase locked loop
s_o	output signal
s_{rf}	output signal of the radio-frequency oscillator
s_{rfpll}	output signal of the radio-frequency-oscillator phase locked loop
s_{tcxo}	clock signal of the temperature controlled crystal oscillator
$T_{ddfsclk}$	sampling-period of the direct digital frequency synthesizer
t_s	sampling time
t_{set}	settling time
t_{sweep}	sweep time
t_{proc}	processing time
V_a	complex voltage port A
V_b	complex voltage port B
Vcc_{cp}	charge pump supply voltage
V_o	complex output voltage
$\hat{V}_o$	output voltage amplitude
V_s	complex response voltage
v_s	shear wave velocity
v_o	output voltage
w	phase resolution of the phase-to-waveform converter
X	integer value
X_{el}	electrical reactance of the quartz resonator
$\mathbf{x}$	parameter vector of the sine-wave fitting

Y	complex admittance
	integer value
Y_{el}	electrical admittance of the quartz resonator
$\mathbf{y}$	data record vector of the sine-wave fitting
Z	complex impedance
Z_C	characteristic impedance of low-impedances microstrip lines
Z_L	complex acoustic load impedance
	characteristic impedance of high-impedances microstrip lines
Z_{cq}	characteristic acoustic impedance of quartz
Z_{el}	complex electrical impedance of the quartz resonator
Z_{load}	complex load impedance
Z_0	characteristic system/line impedance
Z_1	series complex impedance
Z_2	series complex impedance
Z_m^L	complex motional impedance of the acoustic load
Z_m^0	complex motional impedance of the quartz resonator
α	empirical shape parameter
	acoustic phase shift
β	empirical shape parameter
χ	electric susceptibility
δ	dielectric loss angle
Δf	resonance frequency shift
Δf_{ddfs}	frequency-tuning range of the direct digital frequency synthesizer
Δm	added mass
ΔR	resonance resistance shift
$\Delta\varepsilon$	dielectric relaxations intensity
$\Delta\theta$	phase increment
ε	least square error
$\varepsilon(j\omega)$	complex relative dielectric permittivity
$\varepsilon'(\omega)$	relative dielectric permittivity
$\varepsilon''(\omega)$	dielectric loss factor
ε_0	dielectric permittivity of free space
ε_q	permittivity of quartz
ε_s	low-frequency limit of the complex dielectric permittivity
ε_∞	high-frequency limit of the complex dielectric permittivity
ϕ	phase angle
ϕ_o	output phase
ϕ_s	response phase

θ	discrete phase sequence
θ_{err}	error phase
θ_{pd}	input phase of the phase detector
θ_{vco}	phase of the voltage controlled oscillator
η_L	viscosity of the Newtonian liquid
λ	acoustic wavelength
ρ_L	density of the coated film
	density of the Newtonian liquid
ρ_q	density of quartz
σ_0	static conductivity
$\sigma_{aperture}$	aperture jitter
σ_{clk}	sampling-clock jitter
σ_t	sampling time jitter
τ_{relax}	dipole relaxation time
τ_1	characteristic time constant
τ_2	characteristic time constant
ω	angular frequency
ω_{gc}	gain crossover angular frequency
ω_n	natural frequency
ω_o	output angular frequency
ω_{relax}	dipole relaxation frequency
ξ	normalized frequency
ψ_{pm}	phase margin
ζ	damping factor
$\Re\{\}$	real part of a complex number
$\Im\{\}$	imaginary part of a complex number
$\angle$	denotes angle representation
$\gcd(x, y)$	greatest common divisor of x and y

Chapter 1
Introduction

1.1 Motivation

Sensors or sensor systems are decisive components in various scientific and industrial applications acquiring information for material characterization or process monitoring in gaseous, liquid, or solid media [1]. The purpose of the sensor is thereby to respond to a received stimulus that may have almost any conceivable physical, chemical or biological nature, and to convert it into a corresponding electrical signal, which is compatible with electronic circuits [2]. In response to the appropriate sensing effect, the sensor either converts the generally non-electrical value into an electrical signal in form of voltage, current, or charge, or modifies an applied electrical signal in the form of conductivity or resistance. For a sensor that is not generally regarded as a conductor of electricity, the modification of the applied electrical signal can also be sensed by the electrical impedance or admittance, respectively, of the sensor as a function of frequency. This method is well known as impedance spectroscopy and is generally employed to investigate the sensor response over a suitable frequency range to determine the physicochemical properties of the target media.

Over the last few decades electrochemical impedance spectroscopy has become a well established method in electrochemistry for characterizing the transport and transfer process in electrochemical systems or the electrical properties of materials of interest (solid or liquid) and their interfaces with electronically conducting electrodes. It is generally used to characterize coatings, electrochemical power sources (batteries, fuel cells), or corrosion phenomena [3]. Impedance spectroscopy is also widespread in sensor applications investigating dielectric properties of liquids, disperse systems, and biological systems [4]. Broadband dielectric spectroscopy of liquid media and bio-systems covers the enormous frequency range from approximately 10^{-6} Hz to almost 10^{13} Hz [5] [6].

Besides these traditional issues, impedance spectroscopy has also gained importance for in-liquid sensor applications of resonant piezoelectric bulk acoustic wave (BAW) sensors and surface acoustic wave (SAW) sensors. In particular, since the frequency response of quartz crystal resonators (QCR) vibrating in thickness shear mode is highly sensitive to an acoustic load in contact with their sensing surface, QCR devices are widely used for the quartz crystal microbalance (QCM) in the application of electrochemical and biochemical sensing in liquid media [7] [8] [9] [10]. Moreover, new high-temperature stable piezoelectric materials such as

langasite ($La_3Ga_5SiO_{14}$) and gallium-orthophosphate ($GaPO_4$) have been investigated recently to overcome the temperature limitation of quartz BAW devices. In an initial investigation, Fritze *et al.* presented in [11] a langasite BAW device that successfully operates as a microbalance up to temperatures as high as 900 °C. By adding a titanium dioxide film onto the langasite resonator, sensitivity to hydrogen gas was demonstrated. Recently, this has enabled new applications for BAW devices working as high-temperature acoustic wave gas sensors for sensing of conductivity and mass related changes induced in the gas sensitive film deposited onto the resonator [12].

In addition to the research on new piezoelectric materials for BAW devices, different methods for excitation of the thickness shear mode in a QCR device are also currently being investigated in order to introduce advanced liquid acoustic wave sensors [13]. Vetelino *et al.* presented a lateral field excited quartz acoustic wave sensor where both electrodes are located on one reference surface resulting in sensitivity to both mechanical (viscosity, density) and electrical (conductivity, permittivity) property changes of the liquid [14]. Furthermore, new sensor applications for film-coated lateral field excited QCR devices sensing film property changes caused by chemical (phosmet) or biological (*Escherichia coli*) analytes in solution are presented [15] [16] [17]. Motivated by the benefits of the lateral field excitation, a lithium tantalate ($LiTaO_3$) lateral field excited sensor with enhanced sensitivity for in-liquid sensor applications due to high frequency operation was introduced [18]. The prototype sensor at a fundamental frequency of 5.2 MHz is capable of operating at harmonics up to 1.4 GHz.

Unfortunately, operation of BAW sensors at high temperatures, in liquid media, or at high frequencies is accompanied by significant damping. This increases the requirements on oscillator based readout electronics generally used to obtain the frequency response of the particular BAW sensor [10] [19]. In order to determine the frequency response even under heavy load conditions, sophisticated readout electronics based on oscillator circuits with automatic gain control [20], or advanced lock-in techniques [21] [22] [23] [24] were recently introduced. Although the lock-in techniques claim to have the simplicity of oscillator circuits, they suffer from specializing to the particular sensor application. They must be specifically adjusted to the particular BAW device and do not allow for versatile application of the readout electronics. Furthermore, due to the applied lock-in technique, each circuit configuration is restricted to single mode operation and, thus, switching between different harmonics or between multi-sensor arrangements cannot easily be accomplished by single circuit designs. In contrast, the principle of measurement for impedance spectrum analysis does not have this kind of limitations since no lock-in technique is applied. Moreover, the evaluation of the entire impedance spectrum or admittance spectrum of the particular BAW resonator allows not only accurate determination of the frequency response but also proper sensor design, accurate modeling

of the sensor behavior, and better insight into the acoustic conditions at its sensing surface in order to obtain the physicochemical properties of the medium under study.

1.2 Techniques of impedance spectrum analysis

The fundamental approach of impedance spectrum analysis (also referred to as impedance spectroscopy) describes the method that determines the transfer function (voltage or current) of a device or system under investigation as a function of frequency by applying an electrical stimulus (voltage or current) with reasonably low amplitude to the electrodes of the particular device and records the response. In accordance with the aim of this work, the particular sensor constitutes the device under investigation whose measured response of the transfer function is related to the sensor impedance, which is related to the respective physical, chemical or biological properties of a medium under study. In principle, there are two basic measurement techniques widely used in the application of impedance spectrum analysis: time domain spectroscopy and frequency domain spectroscopy [3].

Time domain spectroscopy (TDS) determines the impedance by applying a frequency-rich perturbation stimulus to the sensor and measures the response signal as a function of time with a transient recorder. In order to extract the frequency-dependent impedance, a time-to-frequency transformation is needed that converts the recorded time-varying response into the frequency domain using digital computation methods. The time-to-frequency conversion methods are generally based on Fourier or Laplace transforms [25], or wavelet transform [26]. In general, any arbitrary time excitation (e.g. white noise, characteristic-shaped rectangular pulses, voltage steps, or combination of superimposed sine waves) can be used to obtain the impedance response as a function of frequency, provided that it has the necessary frequency content in the desired frequency range [27]. Beside these traditional frequency-rich excitation waveforms, sophisticated stimuli based on maximum length sequences [28] and biorthogonal symmetric wavelets [29] have been introduced recently. Beneficial of time domain spectroscopy, all frequency components of the spectrum are applied simultaneously and the whole spectrum is therefore obtained from a single set of data. However, the frequency resolution and the lowest frequency component are determined by the reciprocal of the total recording (sampling) time. In order to cover a broad frequency range, which demands a sampling frequency of at least twice the highest frequency component in the excitation waveform, and fine frequency resolution, this technique tends to be computation intensive and, thus, involves time-consuming calculations because a large number of samples must be recorded. Furthermore, with respect to the particular sensor application, optimization of both the specific shape of the excitation waveform and the time-to-frequency transformation is desired in order to obtain both the frequency coverage (resolution and range) needed and the enhanced

measurement accuracy desired [30]. Time domain spectroscopy is very popular for broadband dielectric spectroscopy in laboratory application [31].

Frequency domain spectroscopy (FDS) determines the impedance by applying a monochromatic (sinusoidal) stimulus to the sensor and measures the response signal. The impedance spectrum is obtained by sequential measurements for each single frequency considered to contribute to the spectrum. Beneficially, the experimental setup can easily be applied for various sensor applications because there is no need for a specifically adapted excitation waveform and data analysis of the response signal. However, this technique is based on incremental measurements at single frequencies and the measurement tends therefore to be time-consuming, in particular for sensor applications at lower frequencies.

In principle, both techniques allow broadband impedance spectroscopy of liquids and biosystems in various applications [5]. With time domain spectroscopy, however, it is challenging, and in practice not feasible, to exploit a versatile excitation waveform that allows wideband spectroscopy with an arbitrarily fine frequency resolution applicable to various sensor applications without the need for specific modification. Hence, time domain spectroscopy is well suited for broadband spectroscopy, especially adapted to applications in laboratories rather than for versatile and portable employment. In order to attain universal employment of the sensor electronics, this work is focused on frequency domain spectroscopy.

1.3 State of the art of sensor electronics

During the last decade, the number of custom-built electronics for impedance spectrum analysis has noticeably increased. Depending on the specific application, sophisticated electronics were introduced, which are specially suited for low frequency impedance measurements (up to 1 MHz) used by electrochemical impedance spectroscopy (EIS) electrical impedance tomography (EIT) [32] – [39], and for higher frequencies (up to 30 MHz) applied for resonant BAW sensors [40] [41] [42]. In general, their restriction of the frequency range is caused by the specific application as well as the electrical measurement technique applied and the available electronic components employed. Most of them are primarily based on analog signal conditioning techniques to selectively determine the parameter of the response-signal frequency. According to the principle of operation, analog techniques often require that the signal must be integrated over time, resulting in a time-consuming measurement method. When digital signal processing techniques are adopted, the proposed analyzer electronics mostly consists of conventional on-board processor boards or commercial off-board data acquisition cards (DAQ-cards). These solutions are often limited in their operating speed. Within the last few years integrated circuits (e.g. AD5933 from Analog Devices, Inc.), which comprise all necessary mixed analog/digital operations to perform impedance spectrum analysis up to

1 MHz, also became available. These components allow for very compact circuit designs, but these integrated solutions are still limited to lower frequencies.

In order to provide impedance spectrum analysis for sensor applications, researchers at the Institute of Micro and Sensor Systems have also introduced sophisticated custom-built electronics in the last decade [43]. In the 2001s, Schröder *et al.* presented a single-board network analyzer based inferface electronics primarily intended for quartz crystal microbalance applications [44]. The operation of the inferface electronics was confined to a frequency range of 5 MHz – 20 MHz and based on extensive analog signal processing. Latter had increased the time for data aquisition significantly. Hence, in order to provide very fast sensor data acquisition, in teamwork with Doerner we revised Schröder's *et al.* inferface electronics and presented a single-board electronics in the 2003s, which was primarily based on high-speed digital signal processing [45]. Unfavorable, this electronics was designed for stationary sensor applications in labaratories. With the objective of establishing impedance spectrum analysis for *in situ* sensor applications, we recently introduced in [46] a stand-alone, universal impedance spectrum analyzer electronics for laboratory as well as process automation applications. However, this analyzer electronics is limited to a maximum frequency of 150 MHz.

1.4 Conclusions for the development of a wideband impedance-spectrum-analyzer electronics

Presently, radio-frequency (RF) impedance spectroscopy over a broad frequency range is measured by standard benchtop instruments such as Network/Impedance Analyzers e.g. from Agilent, Inc., or Frequency Response Analyzers e.g. from Solatron, Inc.. Such benchtop instruments, however, are bulky, slow, restricted in the number of frequencies, and offer a large functionality that is not used in sensor applications. They are well suited for precision measurements in stationary (laboratory) applications rather than for portable *in situ* sensor applications. Furthermore, due to their generally moderate measurement rate, conventional benchtop instruments are not suitable for applications that require fast impedance spectroscopy analysis to track dynamic processes [26] [47], or for applications that utilize multi-sensor arrays to increase the sensitivity of the sensor system. In order to investigate the desired physicochemical properties of the medium under study, mathematical procedures extracting the specific parameter from the experimentally measured data are usually needed. These calculations, however, must be computed on external personal computers. Hence, there is a need for a stand-alone electronics that allows fast impedance spectrum analysis up to very high frequencies for portable *in situ* sensor applications.

This work aims to develop novel sensor electronics operating as a fast impedance spectrum analyzer with an enhanced frequency range and suitable for capacitive and resonant sensors.

Beside these specific sensor applications, in principle the electronics should be universally applicable to any sensor device that can be characterized by its impedance response in the specified frequency range. The RF frequency coverage is defined from 10 kHz to 1 GHz, with a fine frequency resolution of 1 mHz. This provides both narrowband impedance analysis required for resonant sensors and broadband impedance analysis over five frequency decades required to employ capacitive sensors for the dielectric spectroscopy. According to the IEC-444 standard for the measurement of quartz crystal unit parameters [48], the noise level of the excitation signal in the vicinity of ±10 % to the carrier (stimulus frequency) have to be attenuated to a level of at least –60 dBc with respect to the carrier level. In addition, the power level of spurious signals and harmonics has to sufficiently be suppressed (usual attenuation: -40 dBc with respect to the carrier level). According to the specific sensor configuration, the power level of the stimulus shall be adjustable in the range from -20 dBm up to +15 dBm and controlled over the frequency range to ensure constant power conditions. In order to overcome the limited frequency resolution of conventional benchtop instruments, the number of frequencies for both wideband and narrowband impedance analysis may not be restricted. However, this must not delay the measurement period significantly. To achieve fast spectrum acquisition rates, a measurement period that is significant lower than 1 ms for one frequency point is desired. Hence, in order to allow for fast impedance spectrum analysis, both a synthesizer design with a very short frequency settling time and an analyzer design with a high-speed data processing technique must be developed. Finally, in contrast to commercial benchtop RF instruments, a compact design of the entire RF impedance spectrum analyzer electronics (referred to as RFISA electronics system in the following) is aimed at, which allows for portable measurement setups to establish *in situ* impedance spectrum analysis for sensor applications in laboratory as well as in industrial applications. Consequently, the development of sophisticated wideband analyzer electronics with minimized complexity of the circuit design but without deteriorated measurement accuracy is needed.

The motivation has specified the requirements of the RFISA electronics system to give a guideline for electronics development. The theoretical background in Chapter 2 comprises the fundamentals and basic models for bulk acoustic wave resonators vibrating in thickness shear mode and capacitive sensor probes applied for in-liquid dielectric spectroscopy. The theory is limited to the fundamentals to preserve general validity for several sensor applications. A survey of conventional RF synthesizer topologies will be given in Chapter 3. A compact hybrid synthesizer topology combining various analog and digital synthesis techniques will be introduced. Crucial design tradeoffs affecting the overall circuit complexity will be considered in Chapter 4. The circuit design of the RFISA electronics system will be described in Chapter 5. An overview of the digital system design implementation will be presented in Chapter 6. The work will be completed with measurement results in Chapter 7, and the summary and future advances in Chapter 8.

Chapter 2
Theoretical background

This chapter starts with an introduction to the principle of measurement for impedance spectrum analysis and describes the generic components of the analyzer electronics. After that, the primary topic is focused on the target sensing parameters of impedance responses obtained from bulk acoustic wave sensors vibrating in thickness shear mode and capacitive sensor probes employed for in-liquid dielectric spectroscopy. The theory is limited to the fundamentals to preserve general validity for several sensor applications. These representatives for acoustic microsensor applications (narrowband impedance spectroscopy) and capacitive sensor applications (wideband impedance spectroscopy) are chosen because they specify different measurement requirements on the frequency and impedance coverage for a versatile employment of the electronics system.

2.1 Principle of measurement for impedance spectrum analysis

The fundamental approach of frequency-domain impedance spectroscopy is to apply a low-voltage sinusoidal signal $s_o = v_o(t) = \hat{V}_o \sin(\omega_o t + \phi_o)$, where $\hat{V}_o$ is the signal amplitude, $\omega_o = 2\pi f_o$ the angular frequency, f_o the stimulation frequency, and ϕ_o the phase, to the sensor and measure the resulting current response $i_s(t) = \hat{I}_s \sin(\omega_o t + \phi_s)$, where $\hat{I}_s$ is the response amplitude and ϕ_s the impedance-dependent phase difference between the voltage signal applied and the current signal responded.

The term spectroscopy is derived from the fact that the impedance is measured not only at a single frequency but also in a certain frequency range, allowing for determining the impedance as function of frequency. This is accomplished by sweeping the stimulation frequency f_o and measuring the current response at the respective frequency.

In the frequency domain, the frequency-dependent, complex impedance is defined by the complex generalization of the Ohm's law as the ratio of the Fourier transform of the complex voltage, $V_o(j\omega) = |V_o(\omega)| \angle \phi_o(\omega)$ where $|V_o(\omega)|$ is the magnitude, and complex current, $I_s(j\omega) = |I_s(\omega)| \angle \phi_s(\omega)$ where $|I_s(\omega)|$ is the magnitude,

$$Z(j\omega) = \frac{V_o(j\omega)}{I_s(j\omega)} = R(\omega) + jX(\omega) = |Z(\omega)| \angle \phi(\omega) \tag{2.1}$$

where $R(\omega) = \Re\{Z(\mathrm{j}\omega)\} = |Z(\omega)| \cdot \cos(\phi(\omega))$ is the resistance constituting the real part of the complex impedance, $X(\omega) = \Im\{Z(\mathrm{j}\omega)\} = |Z(\omega)| \cdot \sin(\phi(\omega))$ is the reactance constituting the imaginary part of the complex impedance, $|Z(\omega)| = \sqrt{R^2(\omega) + X^2(\omega)} = |V_\mathrm{o}(\omega)| / |I_\mathrm{s}(\omega)|$ is the magnitude, and $\phi(\omega) = \arctan(X(\omega) / R(\omega)) = \phi_\mathrm{o}(\omega) - \phi_\mathrm{s}(\omega)$ is the phase angle. Resistance and reactance express the rectangular-coordinate form of $Z(\mathrm{j}\omega)$ whereas magnitude and phase angle express the polar form of $Z(\mathrm{j}\omega)$. The reciprocal of the impedance is the admittance, $Y(\mathrm{j}\omega)$, given by $Z(\mathrm{j}\omega)^{-1} = Y(\mathrm{j}\omega) = G(\omega) + \mathrm{j}B(\omega)$ where $G(\omega) = \Re\{Y(\mathrm{j}\omega)\}$ is the conductance and $B(\omega) = \Im\{Y(\mathrm{j}\omega)\}$ the susceptance.

In general, electronic instruments recording the response signal are voltage sensitive rather than current sensitive and thus a current-to-voltage conversion is usually required. The current-to-voltage conversion can be expressed as $V_s(\mathrm{j}\omega) = k(\mathrm{j}\omega) \cdot I_s(\mathrm{j}\omega)$ where $k(\mathrm{j}\omega)$ describes the frequency-dependent, complex conversion factor and $V_\mathrm{s}(\mathrm{j}\omega)$ the resulting complex voltage. The conversion factor is specified by the particular conversion technique, namely the circuitry accomplishing the conversion, and must accurately be defined at each single frequency.

In practice, the conversion factor is determined by a calibration routine. Inserting $k(\mathrm{j}\omega)$ into (2.1) yields $Z(\mathrm{j}\omega) = k(\mathrm{j}\omega) \cdot V_\mathrm{o}(\mathrm{j}\omega) / V_\mathrm{s}(\mathrm{j}\omega) = k(\mathrm{j}\omega) \cdot r(\mathrm{j}\omega)$, where $r(\mathrm{j}\omega)$ is the frequency-dependent complex voltage ratio. Furthermore, Schröder points out that it is not essential to determine $V_\mathrm{o}(\mathrm{j}\omega)$ and $V_\mathrm{s}(\mathrm{j}\omega)$ directly [49]. Provided that the current-to-voltage conversion exhibits a linear transfer function, two voltages that are not directly related to the sensor impedance can also be recorded for determination the sensor impedance by a measured voltage ratio. This allows a general expression of the principle of impedance measurement given by

$$Z(\mathrm{j}\omega) = k(\mathrm{j}\omega) \cdot \frac{V_\mathrm{a}(\mathrm{j}\omega)}{V_\mathrm{b}(\mathrm{j}\omega)} = k(\mathrm{j}\omega) \cdot r(\mathrm{j}\omega) \tag{2.2}$$

where $V_\mathrm{a}(\mathrm{j}\omega)$ and $V_\mathrm{b}(\mathrm{j}\omega)$ are the frequency-dependent, complex voltages to be measured. With the application of Schröder's calibration routine [44] [49], the residuals of the circuitry can be defined as a four-terminal network and the unknown impedance $Z(\mathrm{j}\omega)$ is precisely determined by

$$Z(\mathrm{j}\omega) = k(\mathrm{j}\omega) \cdot r(\mathrm{j}\omega) = Z_\mathrm{load}(\mathrm{j}\omega) \cdot \frac{r_\mathrm{open}(\mathrm{j}\omega) - r_\mathrm{load}(\mathrm{j}\omega)}{r_\mathrm{load}(\mathrm{j}\omega) - r_\mathrm{short}(\mathrm{j}\omega)} \cdot \frac{r_\mathrm{short}(\mathrm{j}\omega) - r(\mathrm{j}\omega)}{r(\mathrm{j}\omega) - r_\mathrm{open}(\mathrm{j}\omega)} \tag{2.3}$$

where $r_\mathrm{open}(\mathrm{j}\omega)$ is the frequency-dependent, complex ratio for the load condition open circuit ($Z \to \infty$), $r_\mathrm{short}(\mathrm{j}\omega)$ for the load condition short circuit ($Z \to 0$), and $r_\mathrm{load}(\mathrm{j}\omega)$ for the load condition well-known calibration impedance ($Z = Z_\mathrm{load}$). Obvious from (2.1), impedance is a

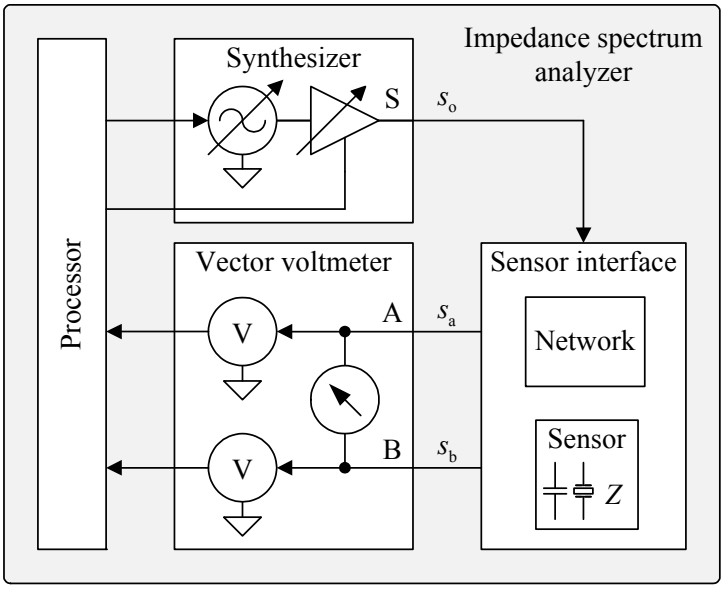

Figure 2-1 Simplified block diagram of a generic impedance spectrum analyzer.

complex number implying complex demodulation of the voltages $V_a(j\omega)$ and $V_b(j\omega)$. Complex demodulation of the voltages requires frequency-selective determination of the inphase component (0°, according to the real part) and quadrature component (90°, according to the imaginary part) of the recorded signals s_a and s_b, where s_a is the signal related to the sinusoidal voltage of channel A and s_b the signal related to sinusoidal voltage of channel B.

The generic components of an electronic instrument performing impedance spectroscopy are shown in Figure 2-1. In order to accomplish the basic functionality, four internal units are essential for an impedance spectrum analyzer:

- The **synthesizer** unit that stimulates the sensors by generating a low-voltage sinusoidal stimulus, s_o, with incremental swept excitation frequency, f_o.
- The **sensor interface** unit that electrically and mechanically connects the sensor with the analyzer and provides signal separation into s_a and s_b.
- The digital **vector voltmeter** that digitizes s_a and s_b and computes the complex demodulation for determining the complex voltage ratio $r(j\omega)$ at the respective stimulus frequency.
- The **processor** unit that computes the complex sensor impedance according to (2.2) and extracts the specific parameter from the sensor's frequency response with regard to the target sensor application.

2.2 Impedance spectroscopy on bulk acoustic wave sensors

Acoustic wave sensors utilize perturbation of a mechanical wave as the sensing mechanism. Their principle of operation is a traveling wave combined with a confinement structure to produce a standing wave whose frequency is determined by the velocity of the traveling wave and the dimensions of the confinement structure [50]. Consequently, acoustic wave devices are sensitive to changes in the characteristics of the path, intrinsic and extrinsic to the device, over which the wave propagates. A specific selectivity is typically achieved by coating a surface region of the particular acoustic wave device with a thin sensitive film. However, acoustic sensing is possible only when the thin film or the adjacent medium interacts with the acoustic modes. Acoustic wave sensors are widely employed in physical, chemical, and biochemical applications [10] [51] [52] [53]. Generally, acoustic wave devices are classified by the mode of wave propagation through or on the particular piezoelectric substrate material [52] [54]. If the wave propagates through the substrate of the device, the wave is referred to as bulk acoustic wave. The most commonly used bulk acoustic wave (BAW) devices are the thickness shear mode resonators, which are the focus in the following. Other acoustic wave sensors utilized for sensor application are the surface acoustic wave (SAW) device, the acoustic plate mode (APM) device, and the flexural plate wave (FPW) device.

In principle, BAW resonators exploit piezoelectric materials to generate the acoustic wave by the converse piezoelectric effect. Piezoelectricity, which was discovered by Jacques and Pierre Curie in 1880 [55], is referred to the generation of electrical charges on the surface of the piezoelectric material by imposition of appropriate mechanical stress to it. Conversely, mechanical deformation arises by applying an electric field to the piezoelectric material. Furthermore, the application of an oscillating electric field on a properly designed BAW resonator generates a mechanical wave that propagates through the material. Any kind of piezoelectric material can principally be employed in order to design BAW resonators vibrating in thickness shear mode. The most common crystalline materials used for BAW resonators are alpha quartz (SiO_2) and lithium tantalate ($LiTaO_3$). Recently, the piezoelectric material langasite ($La_3Ga_5SiO_{14}$) is introduced as alternative to quartz. Langasite resonators are mainly employed in sensor applications at high temperature because they exhibit bulk oscillations at temperatures of at least 1400°C [56]. In order to understand the fundamentals of BAW devices vibrating in thickness shear mode (referred to as TSM resonators in the following), an introduction in the theory is given in the subsequent sections. Detailed explanation can be found in the literature, e.g. in [50] [54] [57]. Since crystalline alpha quartz (AT-cut) is the most common piezoelectric material for TSM resonators, the following remarks are focused on quartz crystal resonators (QCR). The piezoelectric material langasite and alpha quartz belong to the same crystal class and thus approaches known for quartz crystal resonators can also be applied for langasite crystal resonators.

2.2.1 Thickness shear mode excitation of quartz crystal resonators

QCR devices vibrating in the thickness shear mode are excited by an external RF alternating electrical field applied to the piezoelectric material. Depending on the piezoelectric properties and the crystalline orientation within the resonator disk, a pure TSM in a AT-cut QCR device can be excited with an electric field parallel to the disk normal (thickness field excitation, TFE) or perpendicular to the disk normal (lateral field excitation, LFE) [50].

The most common form of thickness-shear-mode excitation is the thickness field excitation. Such TFE-TSM resonator typically consists of a thin disk of the particular piezoelectric material with circular electrodes patterned on both surfaces, as shown in Figure 2-2a. The application of an electric field between the opposite electrodes (parallel to the disk normal) results in a shear deformation across the resonator thickness, d. Furthermore, an RF alternating electric field generates shear (transverse) waves that propagate in thickness direction between the opposite electrodes, reflect at the resonator surfaces, superpose with itself, and produce standing waves that bring the resonator disk into resonance. For a standing acoustic wave to appear, the thickness of the resonator must equal an odd multiple of half the acoustic wavelength $\lambda = v_s / f_N$ where v_s is the shear wave velocity and f_N the resonant frequency. Resonance occurs at each odd harmonics (modes) of the fundamental frequency $f_N = N \cdot v_s / (2d)$ where $N = 1,3,5,\ldots$. Any change of the acoustic properties at the resonator surfaces results in a perturbation of the wave propagation and can be observed by changes of the resonant frequency or the entire electrical resonance spectrum. Acoustic wave sensors based on TSM resonators exhibit best sensitivity for the first modes and for higher operating frequencies.

Based on QCR devices, the classical sensor application of TFE-TSM resonators is microgravimetry, which was initially introduced by Sauerbrey in the 1959s. He demonstrated the extremely sensitive nature of QCR devices and presented the cardinal relation between the shift of the QCR's resonant frequency and a thin, rigid added mass, Δm, of a deposited film on its surface [58]

$$\Delta f = -2 f_0 \frac{\Delta m}{A \cdot \sqrt{c_q \cdot \rho_q}} \tag{2.4}$$

where f_0 is the fundamental (mechanical) resonant frequency, c_q the quartz shear modulus, ρ_q the quartz density, and A the electrode area. In the 1985s, Kanazawa and Gordon expanded Sauerbrey's description for measurements in Newtonian liquid media and presented in [59] the relationship between the frequency shift and the square root of the density, ρ_L, and viscosity, η_L, of the Newtonian liquid, which is in contact with the QCR device,

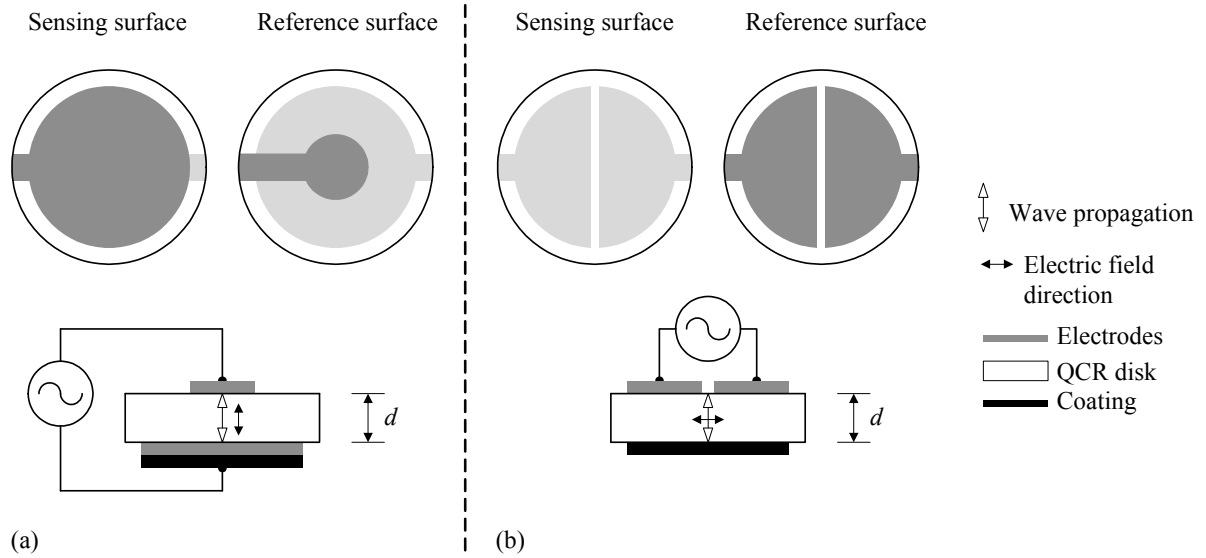

Figure 2-2 Electrode placement and driving electric field direction for thickness shear mode vibration of a piezoelectric quartz crystal resonator by (a) thickness field excitation (electric field is in the direction of the acoustic wave propagation) and (b) lateral field excitation (electric field is in the plane perpendicular to acoustic wave propagation). (Top view is marked by the dark area)

$$\Delta f = -f_0^{3/2} \sqrt{\frac{\eta_L \cdot \rho_L}{\pi \cdot c_q \cdot \rho_q}} \,. \tag{2.5}$$

Caused from viscous loading, operation in liquid media additionally involves significant damping of the QCR device. The acoustic energy dissipation, which is represented by a resistance shift $\Delta R \sim (\eta_L \rho_L)^{0.5}$, exhibits also proportionality to the square root of the density-viscosity product of the corresponding liquid [60] [61] [62] [63]. Hence, since recent decades QCR devices are widely employed for gravimetric and non-gravimetric applications of the quartz crystal microbalance (QCM) to sense mechanical loading effects (mass, density, and viscoelasticity) originated from the medium in contact with the QCR [9] [60] [64] [65] [66].

With respect to the crystallographic axes of the AT-cut QCR disk, lateral field excitation of shear (transverse) waves arises from an arrangement of the electrodes that produce a driving field parallel to the major surfaces (perpendicular to the disk normal) [67] [68]. As shown in Figure 2-2b, the applied electric field is in the plane of the plate and the acoustic wave propagation is in thickness direction, perpendicular to the electric field. For lateral excitation of a pure TSM in an AT-cut QCR disk, the driving electric field must be in the direction of the crystallographic *Z'*-axis and the gap must be parallel to the *X*-axis. The electric field can excite an acoustic wave normal to its direction because the piezoelectric matrix of the crystalline material couples electrical and mechanical fields of varying orientations.

Lateral field excitation of a TSM resonator was first exploited by Atanasoff and Hart to determine the elastic stiffness constants of quartz in the 1940s [69]. Other applications were focused on high-precision frequency control elements [70]. Recently, Vetelino *et al.* studied the lateral field excitation in the application of a new LFE-TSM resonator for in-liquid sensing [14] [15]. Based on their works, Hempel *et al.* started to investigate the entire impedance spectrum of the LFE-TFE resonator in order to emphasize the benefits of the lateral field excitation in advanced sensor applications [71] [72] [73]. Advantageously, in an LFE-TSM sensor design, both electrodes are located on only one (reference) surface and the exciting electric field is not only confined to the quartz crystal but also penetrates into the adjacent medium. Hence, the bare (sensing) surface of the LFE-TSM device, which interacts directly with the target analyte, allows an increased sensitivity to both mechanical (mass, density, viscoelasticity) and electrical (conductivity, relative permittivity) property changes. In contrast, in a conventional TFE-TSM sensor design, the sensing electrode shields most of the TSM electric field penetration into the adjacent medium with only a small fringing field at the sensing electrode boundary penetrating into the adjacent medium, resulting in a minimal sensitivity to electrical property changes [74]. The LFE-TSM resonator's high sensitivity to the electrical properties of an adjacent medium arises from a coupled acustoelectric effect [71]. A change of the electrical boundary conditions at the bare crystal-medium interface (sensing surface) considerably influences the direction of the driving electric field and its distribution inside the crystal disk. This crucially alters the piezoelectric excitation mechanism, which is reflected in the acoustic properties of the LFE-TSM resonator.

2.2.2 Modeling the sensor response of TFE-TSM resonators

The acoustic interaction between the loaded TFE-TSM resonator and the adjacent medium (acoustic load) influences the electrical response of the sensor device considerably. In order to analyze the measured sensor response with respect to the properties of the adjacent medium, an electrical equivalent circuit approach describing the relation between the sensor impedance measured by the RFISA electronics system and the acoustic wave propagation influenced by the medium is required. In general, the wideband transmission line model (TLM) introduced in [50] [54] can be used to describe both the (piezoelectric) transformation between electrical and mechanical vibration and the propagation of acoustic waves in the system acoustic device-coating-medium in analogy to electrical waves.

One representation of the TLM is the equivalent circuit from Krimholtz, Leedom, and Matthaei (referred to as KLM-model) depicted in Figure 2-3a [75]. Definitions for the equivalent elements and a detailed model description can be found in [63] [76] [77]. The model is based on a one-dimensional solution of the equations of acoustic wave propagation and assumes a sensor configuration with infinite lateral dimensions compared to a finite thickness of the

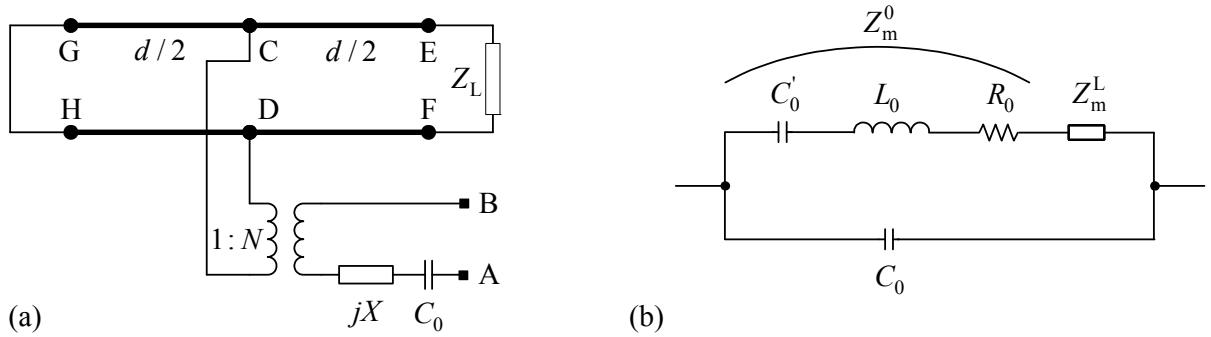

Figure 2-3 Models of a loaded QCR device vibrating in thickness shear mode: (a) KLM representation of the transmission line model and (b) extended BvD equivalent circuit.

crystal resonator. Usually, this is properly fulfilled by the design of the particular TFE-TSM resonator. For a single-side coated sensor (stress free surface at port GH) with an acoustic load at port EF, the relation between the complex acoustic load impedance, Z_L, acting at the sensitive surface of the crystal resonator and the measurable complex electrical impedance, Z_{el}, at the electrical port AB is given by

$$Z_{el}(j\omega) = \frac{1}{j\omega C_0} \cdot \left(1 - \frac{K^2}{\alpha} \cdot \frac{2\tan(\alpha/2) - jZ_L/Z_{cq}}{1 - jZ_L/Z_{cq} \cdot \alpha} \right) \tag{2.6}$$

where ω is the angular oscillating frequency, $K^2 = e_q^2 / (\varepsilon_q \cdot c_q)$ is electromechanical coupling coefficient of the quartz material, e_q the piezoelectric constant, ε_q the permittivity, $\alpha = \omega \cdot d \cdot \sqrt{\rho_q / c_q}$ the acoustic phase shift inside the QCR device, and $Z_{cq} = \sqrt{\rho_q \cdot c_q}$ the characteristic acoustic impedance of the QCR device. The static capacitance enclosing the resonator is $C_0 = \varepsilon_q \cdot A / d$ where A is the electrode area and d the thickness of the crystal resonator. The acoustic load impedance represents the overall acoustic load at the interface between the sensor and the coating. It is related to all changes in the sensitive coating induced by chemical or physical effects. From (2.6) it is apparent that a change in $Z_L(j\omega)$ results in a change of $Z_{el}(j\omega)$. In general, the acoustic load impedance generated from a single film is a frequency-dependent, complex number given by

$$Z_L(j\omega) = j \cdot \sqrt{\rho_L \cdot G_L} \cdot \tan(\omega \cdot d \cdot \sqrt{\rho_L / G_L}) \tag{2.7}$$

where ρ_L is the density and $G_L(j\omega)$ the (complex) shear modulus of the coated film. The real part of $G_L(j\omega)$ is the shear storage modulus corresponding to the load's capability for acoustic energy storage, and the imaginary part of $G_L(j\omega)$ is the shear-loss modulus corresponding to the load's capability for acoustic energy dissipation.

At frequencies close to the resonance and provided that the resonator is weakly loaded, the KLM model can be simplified to the extended Butterworth-van-Dyke (BvD) equivalent circuit (Figure 2-3b), which provides the electro-mechanical analogy by lumped elements [60] [78] [79] [80] [81]. The extended BvD equivalent circuit for a loaded TFE-TSM resonator combines a parallel and series resonance circuit (motional branch). With the approximation of $\tan(\alpha/2) \approx 4\alpha/\left(\pi^2 - \alpha^2\right)$ for the acoustic phase shift near the resonance, $Z_{\mathrm{el}}(\mathrm{j}\omega)$ in (2.6) can be rewritten as

$$Z_{\mathrm{el}}(\mathrm{j}\omega) = \frac{1}{\mathrm{j}\omega\left(C_0 + C_{\mathrm{ext}}\right)} \Big\| \left(Z_{\mathrm{m}}^{0} + Z_{\mathrm{m}}^{\mathrm{L}}\right) = R_{\mathrm{el}}(\omega) + \mathrm{j}X_{\mathrm{el}}(\omega) \tag{2.8}$$

where $R_{\mathrm{el}}(\omega)$ is the resistance, $X_{\mathrm{el}}(\omega)$ the reactance, and C_{ext} the external parallel capacitance accounting to all parasitic effects of packaging or connecting. The complex motional impedance

$$Z_{\mathrm{m}}^{0}(\mathrm{j}\omega) = R_0 + \mathrm{j}\omega L_0 + \frac{1}{\mathrm{j}\omega C_0'} \tag{2.9}$$

arises from the mechanical resonance of the unperturbed TSM resonator, and, in series, the complex motional load impedance $Z_{\mathrm{m}}^{\mathrm{L}}$ is directly proportional to the acoustic load

$$Z_{\mathrm{m}}^{\mathrm{L}}(\mathrm{j}\omega) = \frac{1}{\omega C_0} \cdot \frac{\alpha}{4K^2} \cdot \frac{Z_{\mathrm{L}}}{Z_{\mathrm{cq}}} \cdot \left(1 - \frac{\mathrm{j} \cdot Z_{\mathrm{L}} / Z_{\mathrm{cq}}}{2\tan(\alpha/2)}\right)^{-1}. \tag{2.10}$$

The electrical admittance representation of (2.8) is $Y_{\mathrm{el}}(\mathrm{j}\omega) = Z_{\mathrm{el}}^{-1}(\mathrm{j}\omega) = G_{\mathrm{el}}(\omega) + \mathrm{j}B_{\mathrm{el}}(\omega)$, where $G_{\mathrm{el}}(\omega)$ is the conductance and $B_{\mathrm{el}}(\omega)$ the susceptance. The lumped elements of the unperturbed TFE-TSM resonator described by Z_{m}^{0} represent mechanical energy losses and storage at the surface and depend on the resonator's parameter. The capacitance C_0' represents the mechanical elasticity of the QCR device, the inductance L_0 the initial mass, and the resistance R_0 the energy loss. Definitions for the equivalent elements of the unperturbed TFE-TSM resonator in relation to physical characteristics can be found in [50] [60] [63] [78] [79].

An approximation of the (complex) acoustic load impedance Z_{L} acting at the sensitive surface of the TFE-TSM resonator in direct relation to the measurable resonance parameters, namely the resonant frequency shift, Δf, and the change in the motional resistance, ΔR, in the extended BvD equivalent circuit, can be obtained from the acoustic load concept (ALC), which was introduced by Lucklum *et al.* [76] [79] [81] [82]. The change in the motional resistance is equivalent to a change in the resonator's quality factor, $Q = \omega L_0 / R_0$, due to the external load or any other reason of acoustic energy dissipation.

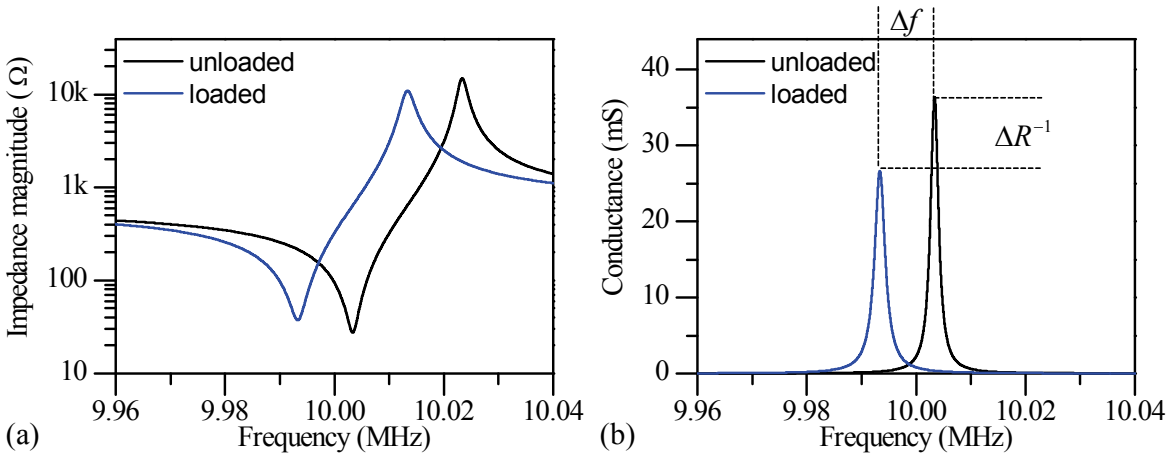

Figure 2-4 Representation of (a) the impedance magnitude spectrum and (b) the conductance spectrum for unloaded and loaded quartz crystal resonators.

In principle, the ALC approximation can be applied for almost all typical load situations such as thin rigid films, viscous liquids, and viscoelastic polymers, which are typically used for chemical and biochemical sensing in liquid or gaseous media. As the primary result of the ALC approximation, the imaginary part of the acoustic load is related to the shift, Δf, of the resonant frequency, f_{res}, at the frequency point where the conductance spectrum becomes a maximum ($G_{\mathrm{el,max}} = G_{\mathrm{el}}(f_{\mathrm{res}})$)

$$\frac{\Delta f}{f_0} = -\frac{\Im\{Z_{\mathrm{L}}\}}{\pi Z_{\mathrm{cq}}} \tag{2.11}$$

where f_0 is the resonant frequency of the bare resonator (see Figure 2-4). The real part of the acoustic load is related to the acoustic energy dissipation and is obtained by the change in the equivalent resistance ($G_{\mathrm{el,max}} = G_{\mathrm{el}}(f_{\mathrm{res}}) = (R_0 + \Delta R)^{-1}$)

$$\frac{\Delta R}{2\omega L_0} = \frac{\Re\{Z_{\mathrm{L}}\}}{\pi Z_{\mathrm{cq}}}. \tag{2.12}$$

In sensor applications it is essential to determine Δf and ΔR at the correct frequency in the resonance spectrum of the TFE-TSM resonator. As shown in Figure 2-5, four different resonant frequencies are discernable when damping of the TFE-TSM resonator occurs. At the low-impedance resonance, the series resonant frequency separates into f_{Zmin} the frequency at minimal impedance magnitude and f_{s} the frequency at zero phase at the low frequency branch. Similar, at the high-impdence anitresonance, the antiresonant frequency separates into f_{p} the frequency at zero phase at the high frequency branch and f_{Zmax} the frequency at maximum impedance magnitude [78].

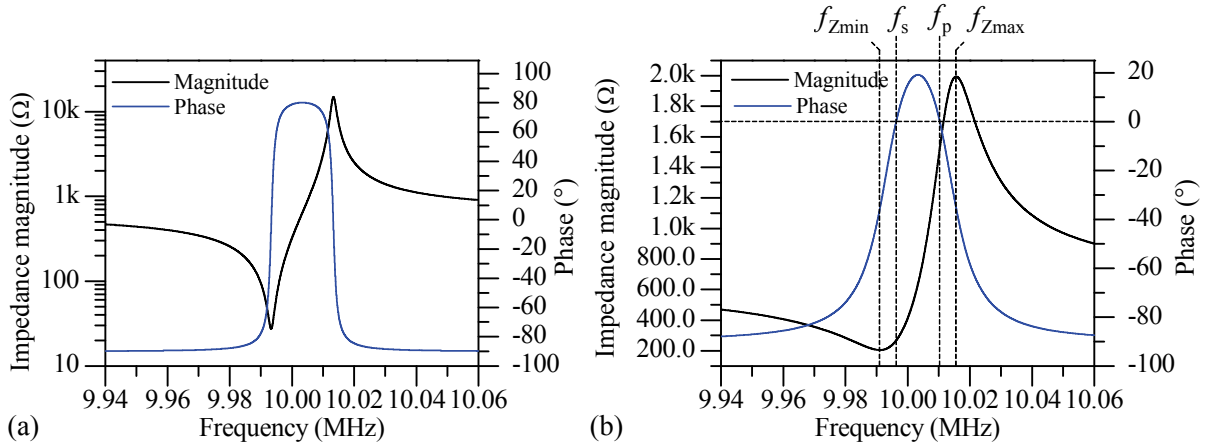

Figure 2-5 Impedance magnitude as a function of frequency for (a) low damping and (b) high damping of a quartz crystal resonator.

2.3 Dielectric spectroscopy on liquids

Dielectric permittivity describes the interaction of a matter with an electric field. Dielectric spectroscopy measures the complex dielectric permittivity, $\varepsilon(\mathrm{j}\omega)$, of the matter as function of frequency. It can be applied to materials that are, in general, regarded as non-conducting. The frequency range extends over nearly 18 orders in magnitude: from the µHz to the THz range close to the infrared region [5] [83]. Dielectric spectroscopy is sensitive to dipolar species as well as localized charges in a material [3]. It determines their strength, their kinetics and their interactions. Dielectric spectroscopy also provides access to indirect values in particular the concentration of a specific component or mixture. Thus, dielectric spectroscopy is well suited for electrical characterization of dielectric material properties. When applying for process monitoring an appropriate sensor device is required. With respect to the target application of capacitive sensor probes intended for *in situ* investigation of liquid substances [46] [84] [85], the following explanations are focused on in-liquid dielectric spectroscopy. The focus arises from its current importance in (bio-) chemical applications where dielectric spectroscopy is used to sense the molecular behavior of liquid substances [5]. The following subsections provide a short introduction into the fundamental principle of dielectric spectroscopy. A comprehensive explanation can be found in several textbooks, e.g. in [3] [6] [83] [86] [87].

2.3.1 Dielectric mechanism

For illustration of electric polarization, the parallel-plate capacitor in Figure 2-6 is assumed with the free space capacitance $C_0 = \varepsilon_0 \cdot A / d$, where $\varepsilon_0 \approx 8.854 \cdot 10^{-12}$ [F/m] is the dielectric permittivity of free space, A the electrode area, and d the metal electrode spacing. Generally, a isotropic, dielectric medium filled into the capacitor increases the capacitance to

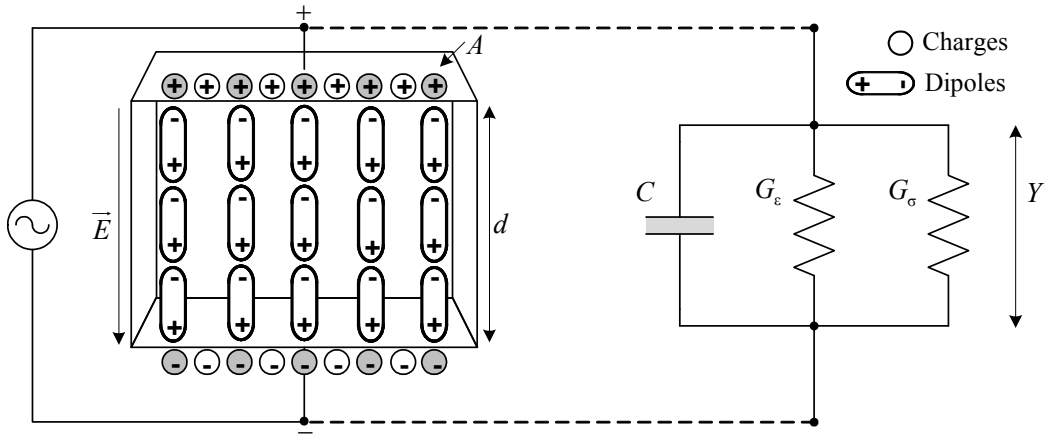

Figure 2-6 Schematic representation of a parallel-plate capacitor filled with a homogenous medium (left) and its parallel lumped-element circuit equivalent (right).

$C = \varepsilon \cdot C_0 = \varepsilon \cdot \varepsilon_0 \cdot A/d$, where the relative dielectric permittivity ε describes the dielectric properties of the medium. When an electric field is applied to a filled capacitor, the charges on the electrodes polarize the molecules of the medium. With small electric field strengths, $\vec{E}$, the electric displacement is given by

$$\vec{D} = \varepsilon_0 \cdot \varepsilon \cdot \vec{E} = \varepsilon_0 \cdot \vec{E} + \vec{P} = \vec{D}_0 + \vec{P} \tag{2.13}$$

where $\vec{P} = \chi \cdot \varepsilon_0 \cdot \vec{E}$ is the polarization of the dielectric material and describes the dielectric displacement that originates from the response of the dielectric medium to an external field. Hence, $\vec{D}$ in (2.13) can be separated into the free space contribution, $\vec{D}_0$, and the contribution, $\vec{P}$, of the medium. The electric susceptibility $\chi = (\varepsilon - 1)$ represents a measure how the dielectric material polarizes under the influence of an external electric field. With the application of an alternating electric field, the relative permittivity is a complex, frequency-dependent function given by

$$\varepsilon(\mathrm{j}\omega) = \varepsilon'(\omega) - \mathrm{j}\varepsilon''(\omega) = \left|\varepsilon(\mathrm{j}\omega)\right| \angle \delta \tag{2.14}$$

where $\omega = 2\pi f$ is the angular frequency of the alternating electric field and δ the dielectric loss angle [6]. The real part $\varepsilon'(\omega) = \Re\{\varepsilon(\mathrm{j}\omega)\}$ is defined as permittivity. It represents the component of the polarization in-phase with $\vec{E}$ and is a measure of energy storage. The imaginary part $\varepsilon''(\omega) = \Im\{\varepsilon(\mathrm{j}\omega)\}$ is defined as dielectric loss. It represents the component of polarization 90° out-of-phase with $\vec{E}$ and is measure of energy dissipation.

In general, different polarization effects contribute together to the overall dielectric permittivity and influcene the frequency response of $\varepsilon(\mathrm{j}\omega)$ as shown in Figure 2-7 [6] [83] [87] [88].

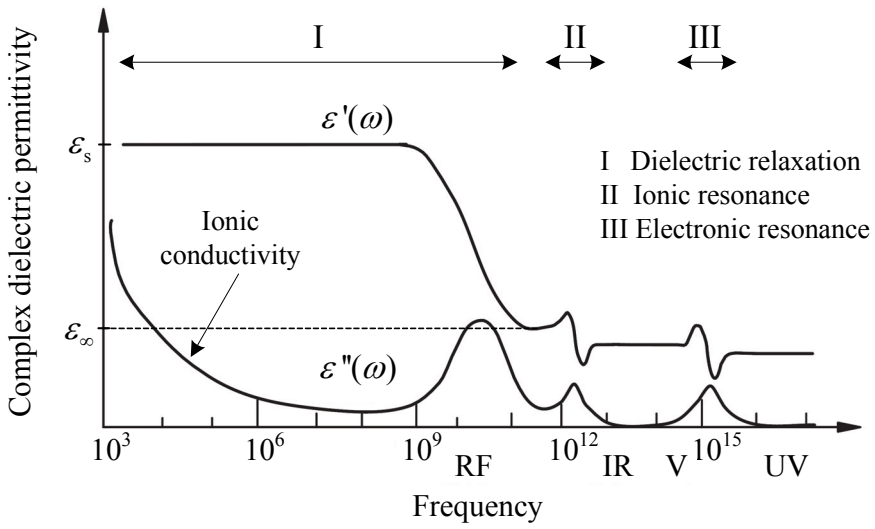

Figure 2-7 Schematic representation of the frequency response of dielectric mechanisms for the frequency ranges: radio frequency (RF), infrared frequency (IR), visible light (V), and ultra violet (UV).

Resonance effects are associated with electronic or atomic polarization and arise from the rotations of atoms, ions, or electrons. The resonant frequency of the electronic polarization is in the range from 10^{14} Hz to 10^{15} Hz and for the atomic polarization in the range from 10^{12} Hz to 10^{13} Hz. They are at infra-red (IR) or visisble light (V) and ultra violet (UV) frequencies, respectively, and therefore out of the scope of this work. Relaxation effects are associated with permanent and induced molecular dipoles and associated with orientation polarization. Dielectric relaxation is usually observed in the frequency range from 10^3 Hz to 10^{10} Hz, which includes the intended frequency range of the scope of this work.

At low frequencies the electric field changes slowly enough to allow dipoles to reach equilibrium conditions before the electric field has changed. For frequencies at which the dipole orientations cannot follow the alternating electric field, the orientation polarization fails to reach its equilibrium conditions and contributes less and less to the polarization as the frequency rises. The absorption of the electric field's energy leads to energy dissipation, resulting in a corresponding peak of the loss factor $\varepsilon''(\omega)$ at the characteristic relaxation frequency ω_{relax}. The characteristic time constant of such a relaxation process, which is the time for reaching new equilibrium after changing the excitation, is the relaxation time, $\tau_{\text{relax}} = \omega_{\text{relax}}^{-1}$, of the medium under study. Above the relaxation frequency, the electric field is too fast to influence the dipole rotation. A first comprehensive derivation of the theory modeling the dielectric relaxation as a function of frequency was established by Debye. For non-interacting molecular dipoles rotating in a non-polar viscous environment, he introduced the Debye relaxation spectral function in the 1929s [86]

$$\varepsilon(\mathrm{j}\omega) = \varepsilon_\infty + \frac{\varepsilon_s - \varepsilon_\infty}{1 + \mathrm{j}\omega\tau_{\mathrm{relax}}} \tag{2.15}$$

where ε_∞ is the high-frequency limit and ε_s the low-frequency (static) limit of the complex dielectric permittivity $\varepsilon(\mathrm{j}\omega)$. The parameters $\Delta\varepsilon = \varepsilon_s - \varepsilon_\infty$ (dielectric relaxations intensity) and τ_{relax} determine the characteristic Debye relaxations parameter. Equation (2.15) describes the dielectric spectrum of only a single Debye relaxation and does not include particle interactions. It applies therefore to gases and dilute solutions only. The dielectric response of liquids deviates from the Debye relaxation due to the dipole-dipole interaction. For representation and comparison of experimental data obtained from non-Debye dielectric spectra, it is recommended in [89] to modify Debye's equation by the Havriliak-Negami function

$$\varepsilon(\mathrm{j}\omega) = \varepsilon_\infty + \frac{\varepsilon_s - \varepsilon_\infty}{\left[1 + \left(\mathrm{j}\omega\tau_{\mathrm{relax}}\right)^{\alpha}\right]^{\beta}} \tag{2.16}$$

where $0 < \alpha < 1$ and $0 < \beta \leq 1$ are empirical shape parameter describing the broadness and asymmetry of the loss peak, respectively. They are introduced to account for higher-order relaxations processes. Depending on the molecular structure of the liquid under study, more than one relaxations process generally exists and thus each relaxations process has to be considered separately. A comprehensive overview for dielectric spectroscopy data treatment is given e.g. in [3] [6] [89].

At low frequencies, the overall DC conductivity, σ_0, can be originated from several conductions mechanism, but, in general, ionic conduction is the most prevalent mechanism. Ionic conductivity is caused by free ions in the liquid and introduces losses only. At low frequencies, the effect of ionic conductivity is inversely proportional to the frequency and appears as 1/*f*-slope of the $\varepsilon''(\omega)$ curve. To account for the effective increase in $\varepsilon''(\omega)$, (2.14) must be extended by the constant conductivity

$$\varepsilon(\mathrm{j}\omega) = \varepsilon'(\omega) - \mathrm{j}\left(\varepsilon''(\omega) + \frac{\sigma_0}{\omega \cdot \varepsilon_0}\right). \tag{2.17}$$

Obviously, for low frequencies the conductivity contributions may significantly affect the dielectric contributions to $\varepsilon''(\omega)$. To reduce the conductivity effect in the evaluation of measured spectral data, a higher frequency range for measurement must be chosen.

2.3.2 Principle of measurement

With regard to the design of Doerner's sensor probe [46], in-liquid dielectric spectroscopy measures the impedance spectrum $Z(\mathrm{j}\omega)$ of a liquid medium under study arranged between two electrodes, comprising a capacitive sensor probe as schematically represented in Figure 2-6. The dielectric properties of the liquid medium, which is filled into or rinsed through the capacitive sensor probe, are determined by performing an isothermal measure as a function of frequency. Thus, an alternating electric field with variable stimulus frequency f_0 is applied to the pair of parallel sensing electrodes and interacts with the electric dipole moments of the liquid. The frequency-dependent, complex dielectric permittivity $\varepsilon(\mathrm{j}\omega)$ spectra are evaluated from either the measured impedance $Z(\mathrm{j}\omega)$ or the admittance $Y(\mathrm{j}\omega)$ spectra of the capacitive sensor probe.

Assuming a homogenous dielectric medium under study and a well-defined geometry of the parallel-plate configuration so that fringing field effects are negligible, technically it is convenient to model the electrical/dielectric properties by a generic capacitive sensor probe represented as appropriate lumped-element circuit equivalent [6]. As shown in Figure 2-6, it includes a complex admittance (Y) that comprises an ideal capacitor (C) related to $\varepsilon'(\omega)$ in parallel with a ideal electrical resistor (G_ε^{-1}) related to $\varepsilon''(\omega)$ and a electrical conductance (G_σ) related to the liquid's DC conductivity σ_0. Opposed to the series lumped-element circuit equivalent, the parallel equivalent circuit is the natural representation where physical phenomena (conductivity and polarization) occur in parallel [3]. Conversion into the complex impedance representation can be done by $Z(\mathrm{j}\omega) = 1/Y(\mathrm{j}\omega)$.

By application of (2.17), the frequency-dependent, complex admittance to be measured is

$$Y(\mathrm{j}\omega) = G(\omega) + \mathrm{j}B(\omega) = G_\sigma + G_\varepsilon + \mathrm{j}\omega\varepsilon(\mathrm{j}\omega)C_0 = \omega C_0\left[\left(\varepsilon''(\omega) + \mathrm{j}\varepsilon'(\omega)\right) + \frac{\sigma_0}{\omega\varepsilon_0}\right]. \quad (2.18)$$

Proposed that $Y(\mathrm{j}\omega)$ is accurately determined by applying an adequate calibration method (e.g. as introduced in section 2.1), the dielectric frequency response of the liquid media under study, namely the spectra of the dielectric properties $\varepsilon'(\omega)$ and $\varepsilon''(\omega)$, can be evaluated from the measured susceptance $B(\omega)$ and conductance $G(\omega)$ spectra, respectively.

The generic lumped-element circuit equivalent described above does not account for the specific relaxation and conduction phenomena originated from the frequency-dependent electrical/dielectric properties of the liquid media filled into the capacitive sensor probe. To evaluate the dielectric frequency response, approaches for electro-physical modeling of the electrical/dielectric properties by a well-defined equivalent circuit must additionally account the specific molecular structure of the liquid substance and the effects of the electrode-dielectric in-

terface. Various approaches for modeling the dielectric relaxation phenomena in accordance to the dielectric medium and application are presented in e.g. [3] [6] [83].

2.4 Summary and conclusions

The aim of the previous chapter was to provide the fundamental theory of impedance spectrum analysis in the application of resonant microsensors based on TSM bulk acoustic wave resonators (narrowband impedance spectroscopy) and capacitive sensors probes used for in-liquid dielectric spectroscopy (wideband impedance spectroscopy). These particular sensor applications were chosen because they specify different requirements on the measurement of impedance spectroscopy, which must properly be met by the RFISA electronics system.

As described, a TSM resonator is highly sensitive to property changes of the acoustic and electrical conditions at its sensing surface. The sensor response is reflected in the shifts of the crucial resonance parameters Δf and ΔR. They are exactly extracted from the maximum of the resonator's conductance spectra, which must be finely measured in the vicinity of the resonance. Since the sensitivity significantly increases with increasing fundamental frequency or when taking into account additional evaluation of harmonics, this entails narrowband impedance spectroscopy (usually in the order of 1% of the fundamental resonance) with arbitrarily fine frequency resolution (<1 Hz) in the vicinity of a high fundamental frequency (MHz-range). Additionally, due to the resonator's high Q-factor (usually in the order of 10^6 for an unloaded quartz crystal resonator), evaluation of the entire impedance spectrum not only at the low-impedance resonance but also at the high-impedance antiresonance implies accurate measurements over a wide impedance range (from few ohms up to several kiloohms). This is also essential when significant damping of the resonator's vibration in the specific sensor application (e.g. in liquids [64] or at high temperature [56]) occurs.

In contrast, in-liquid dielectric spectroscopy for determination relaxations phenomena using a capacitive sensor probe implies admittance measurements over a broad frequency range from some Hertz up to the GHz-range to extract the medium properties $\varepsilon'(\omega)$ and $\varepsilon''(\omega)$, and, in particular, the characteristic relaxations parameters τ_{relax} and $\Delta\varepsilon$. In this application of wideband impedance spectroscopy, broad frequency coverage with a large number of frequency points is required whereas fine frequency resolution is not essential. In order to reduce the effect of the liquid's ionic conductivity in the evaluation of measured spectral data, a lower frequency bound at 10 kHz is preferred. The upper frequency is limited to a maximum frequency of 1 GHz due to the principle of measurement using a broadband capacitive sensor probe.

Chapter 3
Survey of RF synthesizer topologies

With the aim of defining a target synthesizer topology with minimized circuit complexity for implementation in the impedance spectrum analyzer electronics, an overview of conventional synthesizer topologies suitable for radio frequency generation of sinusoidal waveforms is presented in following chapter. At first, the requirements, which determine the selection and the key components of the target synthesizer topology, are specified. Various generic topologies of conventional synthesizer designs along with their main characteristics are analyzed. A hybrid synthesizer topology, which includes the key components from each of these synthesizer architecures, is finally presented.

3.1 Overview of coherent frequency synthesis techniques

Kroupa [90], Goldberg [91] and Popiel [92] in similar manner, define a coherent frequency synthesizer as a system, which generates one or more frequencies derived from a single time base (frequency reference). Hence, the frequency ratio of the output frequency, f_o, to the reference (input) frequency, f_i, is a rational fraction given by topology

$$\xi = f_o / f_i = X / Y \tag{3.1}$$

where X and Y are mutually prime integers, and ξ is the normalized frequency. In this case, the output frequency and the reference frequency are in harmonic relation and the stability and accuracy of f_o are the same as stability and accuracy of f_i.

For frequency-swept stimulation of the target sensor, the frequency synthesizer unit in the RFISA electronics system must provide an agile sinewave source with low phase noise, low spurious content, and arbitrary fine frequency resolution. Generally, there are several established synthesizer topologies, which have been comprehensively described and investigated in the past [92] [93] [94]. Allthough all synthesizer topology share common features, they also exhibit significant differences as a result of the specifc system requirements that must be met [95] [96] [97] [98]. The particular design challenge for application in the RFISA electronics system is to find a reasonable compromise between the desired minimized circuit design and the synthesizer performance described before.

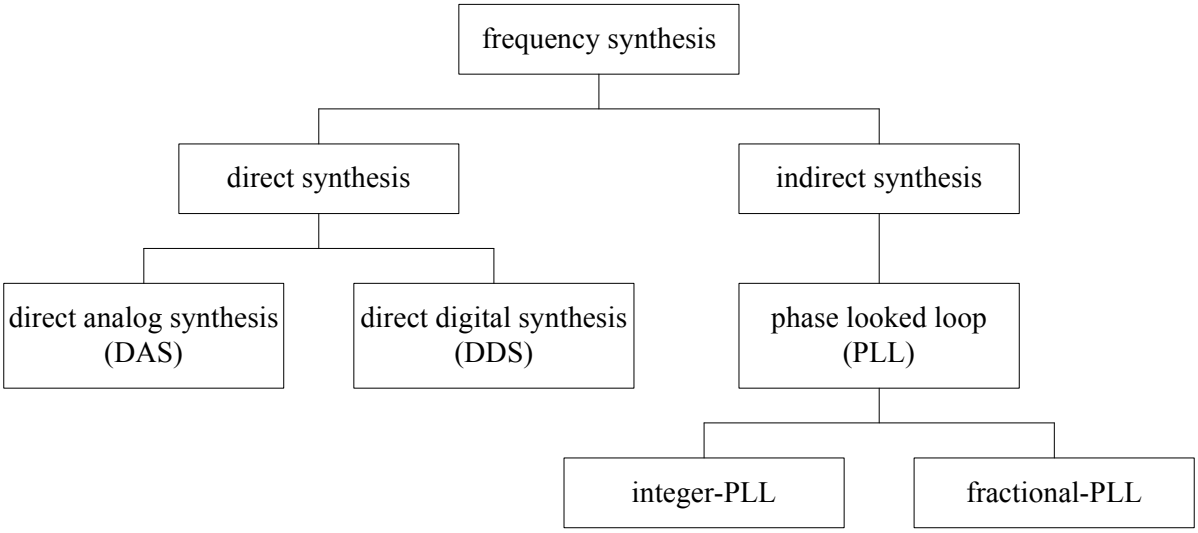

Figure 3-1 Classification of coherent frequency synthesis techniques.

Generally, there are four conventional techniques for coherent RF sinewave synthesizes, which allow for implementation in the RFISA electronics system. As shown in Figure 3-1, they can be classified into two basic categories: direct and indirect synthesis. The direct synthesis technique generates an output frequency derived from the single reference straightforward whereas the indirect synthesis technique generates the output frequency by utilizing a feedback system [96]. All these techniques have significant advantages and disadvantages. The requirements, which must be considered for comparison and evaluation of the particular synthesizer topologies, are:

- the frequency coverage (tuning range and resolution),
- the agility (tuning speed),
- the narrowband spectral quality (spurious signals[1] and phase noise[2]),
- the wideband spectral quality (harmonics and sub-harmonics),
- the circuit complexity.

Ideally, the output of a frequency synthesizer is a single sinusoidal signal, constant in both amplitude and phase, and represented by a single line in the frequency domain. Thus, amplitude and phase modulation and spurious signals are contaminants that must be avoided or, more practically, kept below the prescribed levels. A well-designed synthesizer is amplitude stable and therefore noise originated from phase modulation and spurious signals is predominant [99]. Phase noise is a critical design parameter in all synthesizer applications, but the

[1] Spurious signals (abbreviated spurs) are undesired spectral components that appear at the output of the synthesizer, in addition to the carrier signal with frequency f_o [131].

[2] Phase noise is the common denomination given to the energy present in the power spectrum of synthesizers, in addition to the carrier and to deterministic spurious signals, representing unintended phase modulation of the carrier signal [131].

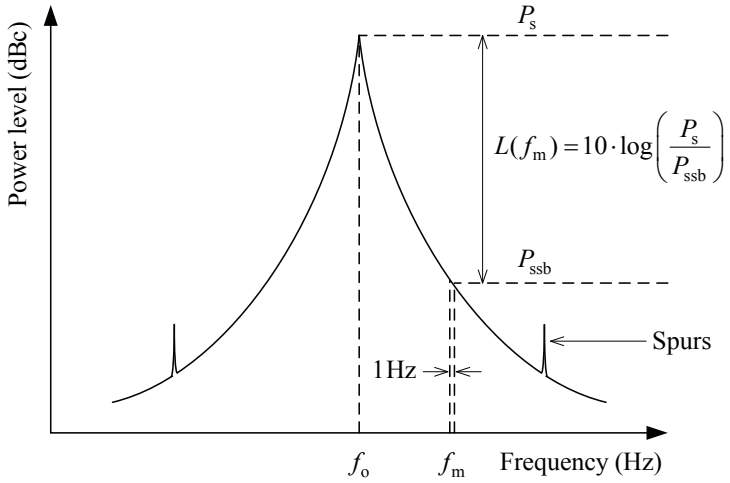

Figure 3-2 Representation of the single-sideband phase noise to carrier ratio.

critical frequencies where the noise is primarily important depend on the particular application. The contaminations of the narrowband spectral purity may be random or discrete. As shown in Figure 3-2 there are two types of phase fluctuations in a narrowband close to the carrier (fundamental output frequency f_o): the discrete spurious signals and the phase noise. The phase noise is random in nature and originated from random walk, flicker noise, and white noise. In practice, the most common characterization of phase noise of a signal source in the frequency domain is the single-sideband phase noise given by $L(f_m) = 10 \cdot \log(P_s / P_{ssb})$ in dBc/Hz [99]. It is defined as the ratio of single-sideband power of phase noise, P_{ssb}, at $f_o \pm f_m$ in a 1 Hz bandwidth, where f_o is the carrier and f_m is the sideband frequency, with respect to the total signal power, P_s.

3.2 Direct analog synthesis

In direct analog synthesis (DAS) (Figure 3-3), the output frequency, f_o, is obtained directly from the input reference frequency, f_i, by the frequency operation of mixing, multiplication, division, switching, and filtering [92]. Although many variations for the DAS architecture are feasible, for an efficient implementation of the circuit design operation in repeatable stages of decades, in which the output of one stage serves as the input of the next identical stage, is usually preferred [91]. The output frequency is given by

$$f_o = f_1 + \frac{f_2}{10} + \frac{f_3}{100} + \ldots = f_1 + \sum_{j=1}^{J} f_{j+1} \cdot 10^{-j} \tag{3.2}$$

where f_i are the base frequencies for the corresponding stage and J is the number of intermediate stages. The output frequency coverage, namely the frequency resolution and the fre-

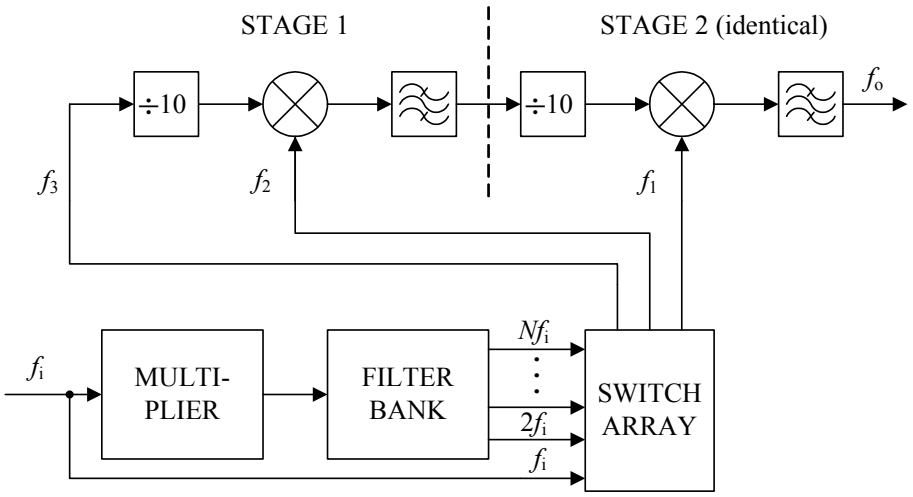

Figure 3-3 Direct analog synthesizer architecture with two identical stages.

quency range, correlates with the gradation of the base frequencies and the number of intermediate stages, thus increasing the design complexity and overall component count [98].

The direct analog synthesis is mathematically described by operation of frequency division ($f_o = f_i / N$, where N is the integer division factor), frequency multiplication ($f_o = f_i \cdot M$, where M is the integer multiplication factor), and frequency mixing. The latter is also related to frequency addition and subtraction. In practice, frequency division can be accomplished by analog circuits, which can be based on regenerative divider circuits [100] [101] or injection locked oscillators [102], and digital counter stages [93]. Analog circuit operation of frequency multiplication can only be accomplished by electronics that are capable of exhibiting controlled nonlinear input-to-output transfer behavior. Nonlinear distortion is essential to generate new frequencies through the process of harmonic generation from the signal present at its input [103] [104]. The nonlinear operation of the electronics, however, produces an output signal that is rich in integer multiples (harmonics), which are all in relation to the input signal. The undesired harmonics can be on the order of or greater than the output frequency f_o, and, thus, sufficient filtering is mandatory to suppress them or, more practically, to keep them below a prescribed power level.

When two input signals, additive or multiplicative, are applied to a nonlinear analog circuit, the nonlinearity produces two output frequencies, one at the frequency sum and another at the frequency difference between them. This frequency operation is referred to as (frequency) mixing, mathematically represented by the multiplication $s_o = s_{lo} \times s_{rf}$, where s_{lo} and s_{rf} are the corresponding input signals and s_o the output signal. However, because of the necessary nonlinearity of the mixer circuit, not only the desired sum and difference frequencies but also feedthroughs of the input signals, harmonics of the input signals, and intermodulation products occur at the mixer output simultaneously, given by [103] [105]

$$f_{\mathrm{o}} = \left| n \cdot f_{\mathrm{lo}} \pm m \cdot f_{\mathrm{rf}} \right| \tag{3.3}$$

where $m, n \in \mathbb{N}$, and f_{lo} and f_{rf} are the corresponding input frequencies expressed in the typical mixer notation [94]. Hence, sufficient filter stages applied to the output and input signals are mandatory to suppress the undesired spurious sidebands.

The advantages of direct analog synthesizers are the fast agility, which depends solely on the switching time between the base frequencies and the response time of the filters, and, in theory, the almost arbitrarily fine frequency resolution [91]. In particular, when the intermediate stages operate at high frequency, the agility of the synthesizer mainly depends on the speed of the switch, which is generally fast, and does not depend on the settling time of the filter. Consequently, a well-designed DAS architecture provides fast frequency hopping in which the frequency resolution can be designed very fine without affecting the agility of the synthesizer.

The disadvantages of the DAS architecture are the complex size and, in general, the poor phase noise performance [96]. A DAS architecture with wide absolute output frequency range and fine frequency resolution requires a sufficient number of intermediate stages and RF analog circuit operations, thus making the design of the synthesizer difficult and hardware intensive. Furthermore, an increasing number of analog circuits, and in particular an increasing number of mixer and multiplier circuits, will significantly decrease the spectral purity at the synthesizer's output due to the affinity to generate an excessive number of spurious signals that have to be filtered sufficiently [97]. Adequate phase noise characteristics can only be achieved by proper designing with low noise components such that the additive phase noise of all components is considerable smaller than the multiplied phase noise of the reference frequency [97].

3.3 Direct digital frequency synthesis

Direct digital frequency synthesizer (DDFS), also referred to as direct digital synthesis (DDS), produces an output signal in which the signal waveform is purely synthesized in the digital domain and then converted into the analog domain by a digital-to-analog converter (DAC) [91] [106] [107]. The DDFS is driven by the sampling clock, f_{ddsclk}, and operates as reversed sampled system generating samples of a predefined sinusoidal waveform instead of sampling a waveform. The basic architecture of an accumulator based DDFS, which was firstly introduced by Tierney *et al.* in the 1971s [108], is depicted in Figure 3-4. In principle, it comprises two stages: (1) a numerical controlled oscillator (NCO) stage operating in the digital domain, and (2) a mixed/analog stage converting the sinusoidal waveform into the analog domain. The output frequency of the DDFS is given by [106]

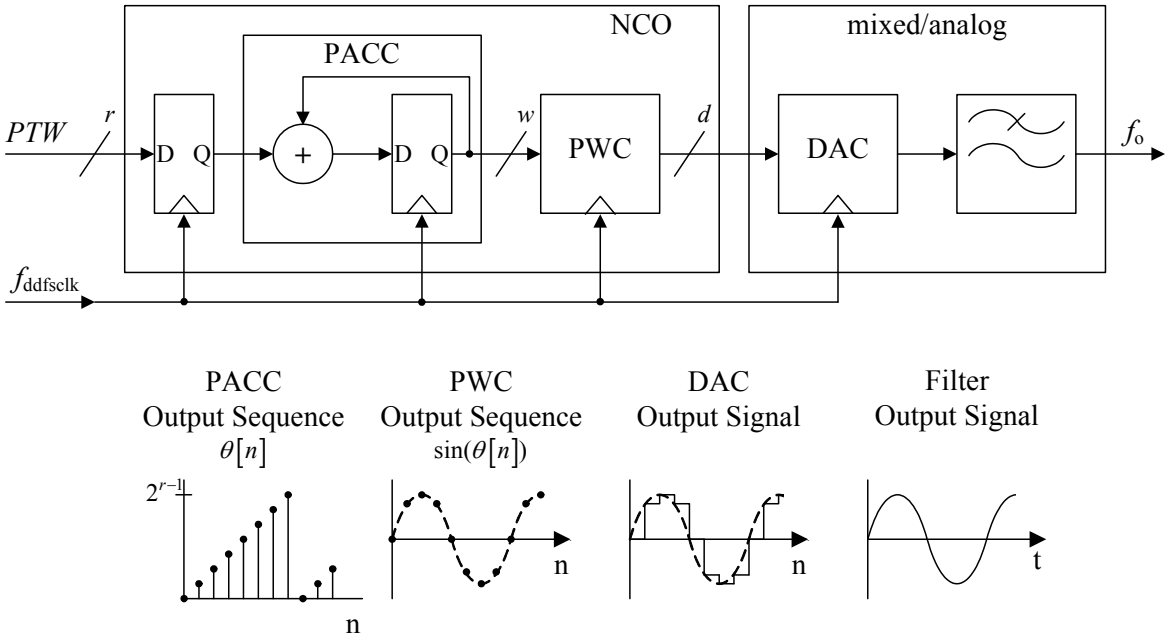

Figure 3-4 Topology and signal flow of a direct digital frequency synthesizer.

$$f_o = \frac{\lfloor PTW \rfloor}{2^r} \cdot f_{ddfsclk} \tag{3.4}$$

where $\lfloor \ \rfloor$ denotes truncation to integer values. *PTW* is the phase tuning word that represents the *r*-bit binary expression of the phase increment (rate of phase change per clock period) $\Delta\theta = 2\pi \cdot f_o / f_{ddfsclk}$, where $2^r \triangleq 2\pi$. The *PTW* is loaded into the input register of a periodically overflowing phase accumulator (PACC) that produces the time-variant phase argument $\theta[n] = (\phi[n-1] + \Delta\theta)_{\text{mod } N}$ where $mod\, N$ ($N = 2\pi$) describes the modulo operation of the PACC and *n* is the discrete time-domain index. The discrete phase sequence is then truncated to *w* bit to address the phase-to-waveform converter (PWC) that converts the instantaneous phase argument into corresponding *d*-bit amplitude samples of the sinusoidal waveform $\sin(\theta[n])$. Finally, the output waveform of the NCO is clocked into the DAC that generates an analog staircase approximation of the digital sinusoidal waveform.

The average rate at which the PACC overflows establishes the desired output frequency (3.4). For large values of *PTW*, the phase sequence $\theta[n]$ increases and overflows at a faster rate, and, thus, a higher frequency will be synthesized. Since the DDFS constitutes a sampled system, the output spectrum contains the desired output frequency f_o and, in addition, aliased frequencies (images) that occurs at multiples of $f_{ddfsclk} \pm f_o$ in the corresponding Nyquist zone (NZ) (shown in Figure 3-5) [109]. Hence, a subsequent reconstruction filter at the DAC output is mandatory to attenuate the aliased frequency components. The output power of

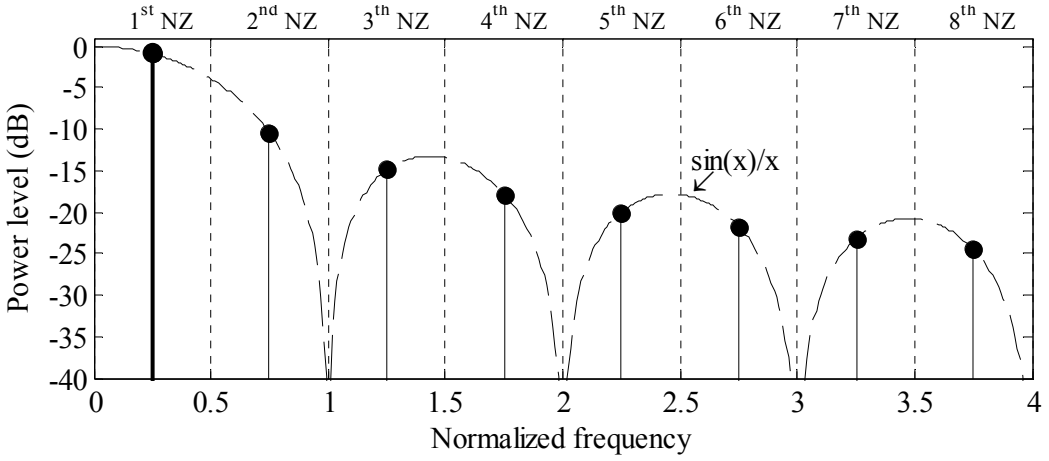

Figure 3-5 Spectrum of a sampled sinusoidal output waveform normalized to sampling clock. (thick line represents the fundamental line)

DDFS is inherently affected by the roll-off characteristic of the sin(*x*)/*x* envelope caused by the sample and hold operation of the DAC.

The advantage of the DDFS architecture is the capability to tune the output frequency with both arbitrarily fine frequency resolution, which is determined by *r* (typically 32 or 48 bit), and fast frequency hopping. From (3.4) it is obvious that frequency setting is rapidly accomplished by reprogramming the input register with the new *PTW*. Since the DDFS, in principle, acts as high-resolution frequency divider with f_{ddsclk} as its input and f_{o} as its output, the phase noise of the clock source is improved by $20\log(f_{\mathrm{o}} / f_{\mathrm{ddfsclk}})$, in decibels (dB), to the output [99] [105] [110]. Thus, large $f_{\mathrm{o}} / f_{\mathrm{ddfsclk}}$ ratios are desired. Moreover, commercial integrated circuits (IC) are available executing all DDFS functions on a single IC. Such DDFS-ICs require solely the external reconstruction filter and allows therefore for designing the entire synthesizer architecture with small size and low complexity.

The disadvantages of the DDFS architecture are the limited RF output frequency range, the power consumption with increasing clock rate, and the relatively high noise and spurious signal level [97] [91] [106] [107]. Imperfections in the sinusoidal waveform generation by NCO, which are inherently caused from numerical distortion due to finite-word length effects and the linearity limitations of the DAC cause harmonically related spurs and phase modulation spurs around the carrier f_{o} [111]. The phase modulation spurs can be as close as $f_{\mathrm{ddfsclk}} / 2^{r}$ to f_{o} [112]. The maximum output frequency from the DDS architecture is fundamentally limited by the Nyquist criterion[3] to a bandwidth of $f_{\mathrm{ddfsclk}} / 2$. However, in practice, the finite roll-off characteristic of the analog reconstruction filter limits again the frequency upper

[3] A continuous-time signal, whose spectral content is limited to frequencies smaller than half of the sampling frequency, can be recovered from its sampled version if the sampling rate is larger than twice the maximum signal bandwidth [190].

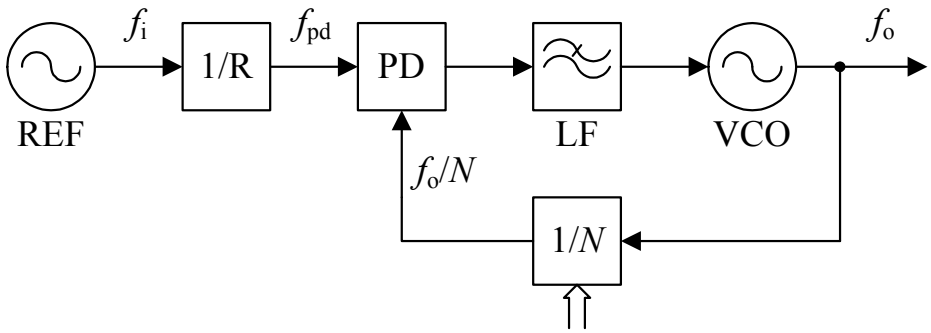

Figure 3-6 Generic topology of integer-N PLL synthesizers.

bound to approximately 40% of f_{clk} to allow for reasonable suppression of the aliased and spurious frequencies situated close to $f_{ddfsclk}/2$ [91].

3.4 Indirect frequency synthesis by integer-N PLL

Indirect frequency synthesis utilizes the principle of phase locking feedback in generating frequency increments. Phase locked loop (PLL) synthesizers have been widely used in the last decades and they are still today the most suitable technique for synthesis of sinusoidal waveforms with high and very high frequency. Although the particular PLL architectures may take large variety topologies and complexity depending upon the specification that they must meet, they all have in common the use of single-loop or multi-loop designs of the classic PLL topology introduced by Gruen in the 1953s [113].

The basic integer-N PLL topology in Figure 3-6 constitutes a conventional negative-feedback control loop. It contains five essential elements [114] [115] [116]: (1) a programmable reference divider (1/R) producing the phase detector frequency, f_{pd}; (2) a phase detector (PD); (3) an low-pass loop filter (LF); (4) a voltage-controlled oscillator (VCO) tuning the output frequency, f_o; and (5) a programmable feedback divider (1/N) producing the divided feed-back signal for the phase detector.

The phase detector compares the phase of the periodic input signal against the phase of the divided VCO signal. Thus, the output of the phase detector is a measure of the phase error between the two inputs. Since phase detectors are generally nonlinear circuits, the phase error signal consists of a DC component, which is roughly proportional to phase error, and, in addition, higher frequency components. Hence, the error signal of the phase detector must be low-pass filtered by the loop filter, whose DC control output is applied to the VCO. The control signal adjusts the VCO frequency in a direction that the phase error between the input signal and the divided VCO signal becomes zero.

When the loop is phase locked (zero phase error), the control signal sets the average frequency f_o of the VCO equal to an integer multiple N of the average frequency of phase detector f_{pd} given by

$$f_o = f_{pd} \cdot N = f_i \cdot N / R \tag{3.5}$$

where N is the integer value of the feedback divider and R the integer value of the reference divider. From (3.5) it is apparent that the output frequency f_o can simply be changed by reprogramming the divider value N to a new value. This allows for tuning across the frequency range of the employed VCO in integer steps. The total output frequency range is determined by the tuning range of the particular VCO.

The advantages of the integer-N PLL synthesizer are the ability to generate high-stable output frequencies in a wide range by up-converting the input signal f_i with low frequency into the desired output signal f_o with high frequency and the reduced level of spurious signals owing to the low-pass filter action of the loop [97] [114] [115] [116]. No block in the PLL topology has to operate at frequencies higher than the output frequency. Furthermore, commercial ICs are available executing all PLL functions on a single IC. This allows for designing the entire synthesizer architecture with small size and lower complexity. The PLL-IC requires only an external reference source, a VCO, and external components for the loop filter design.

The disadvantage of the integer-N PLL synthesizer is that the minimum frequency resolution, or minimum step size, equals f_{pd}. Hence, for a conventional integer-N PLL synthesizer that shall be capable of frequency hopping with fine resolution a low reference frequency f_i and a high reference divider value R are essential. However, the loop bandwidth must be chosen significantly lower than f_{pd} to keep proper stability of the feedback loop and to achieve good low-pass filtering of input and loop noise [114] [115] [116]. Since the loop bandwidth is indirectly proportional to the settling time of the loop, a low loop bandwidth results in a slow tuning speed of the PLL. This adversely affects the capability of an integer-N PLL synthesizer to tune the output with both fine and fast frequency hopping. Furthermore, large division ratios $1/N$ are mandatory to provide high frequency outputs f_o with fine tuning resolution f_{pd}. A high loop multiplication factor N, however, significantly increases the phase noise of the RF output signal [99]. Hence, there is always a tradeoff between the output frequency range, the frequency resolution (f_{pd}), the loop bandwidth (related to f_{pd}), and the loop settling time. A smaller loop bandwidth will improve the noise level but at the expense of the settling time. A larger loop bandwidth yields the opposite effect. [105] [110] [117]

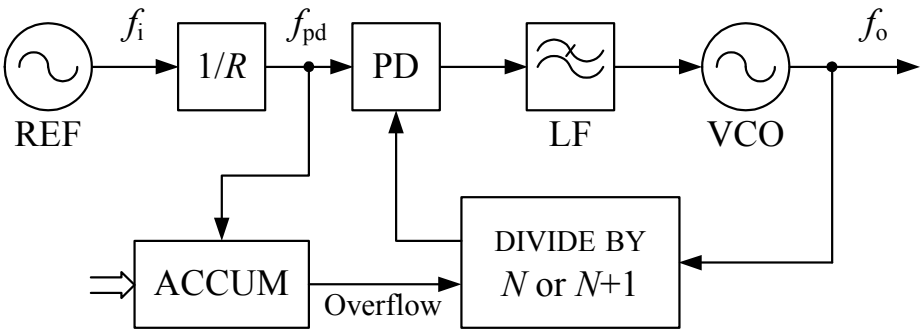

Figure 3-7 Generic topology of fractional-N PLL synthesizers.

3.5 Indirect frequency synthesis by fractional-N PLL

As opposed to the integer-N PLL, the fractional-N PLL architecture in Figure 3-7 consists of a programmable feedback divider, whose alternating division ratio N or (N+1) is controlled by the repetitive overflow signal of a programmable accumulator (ACCUM). Its input, KW, is the m-bit binary representation of the fractional part of the divider ratio. The non-integer frequency ratio of the fractional-N PLL is given by

$$f_o = (N + F) \cdot f_{pd} \tag{3.6}$$

where N is the integer and F ($0 \le F < 1$) the fractional value of the divider [118]. The duty cycle of the ACCUM output signal equals F and, thus, the average division ratio is equal to the non-integer division ratio.

To achieve fractional dividing, the feedback divider operates as alternating integer divider. Hence, fractional-N counting is attained only on average, not uniformly, and the switching between division by N and (N+1) causes excessive phase jitter appearing as discrete spurs close to the carrier f_o at the loop output [114] [118]. These spurs occur in pairs to f_o at an offset frequency of $\pm 0.1 \cdot F \cdot f_{pd}$ and its harmonics [114] [116] [115]. There are several noise cancellation techniques to improve the spectral purity, which, however, claim more circuit complexity. In particular, the use of Δ-Σ modulation techniques results in beneficial shaping of the phase noise by spreading the discrete spur energy evenly across some frequency range [119] [120] [121]. The noise is effectively attenuated by the low-pass filtering action of the loop.

The advantage of the fractional-N PLL synthesizer is the capability to generate output frequencies with finer frequency resolution than f_{pd} because the division ratio in the feedback loop does not have to be an integer. Therefore, an f_{pd} that is higher than the required frequency step size can be used, which allows for smaller value N, wider loop bandwidth and, respec-

tively, faster frequency setling. Moreover, a smaller N factor yields to lower input-to-output noise amplification.

The disadvantage of the fractional-N PLL synthesizer results from the increased phase noise caused by, in general, the high level of discrete spurs close to f_o. Consequently, noise cancellation techniques and a sufficient low loop bandwidth are required to reduce the noise level by the low-pass filtering characteristic of the loop. The intensity of the spurs exerts therefore on both the spectral purity and the tuning speed of the fractional-N PLL synthesizer.

3.6 Comparison and conclusions

A comparison of the introduced topologies for conventional RF synthesizers is summarized in Table 3-1. Since the RFISA synthesizer unit must provide a compact and agile signal source capable of sinusoidal waveform generation from 10 kHz to 1 GHz with arbitrarily fine frequency resolution, no single architecture in Table 3-1 meets all requirements alone.

Table 3-1 Comparison of RF synthesizer topologies.

specification	DAS	DDFS	integer-N PLL	fractional-N PLL
tuning range	o	+	++	++
resolution	++	++	– –	+
tuning time	+	++	– –	o
spurious noise	o	– –	++	–
phase noise	+	+	o	o
power consumption	–	–	++	++
circuit complexity	– –	++	++	++

– – very bad o adequate ++ very good

Although a proper designed direct analog synthesizer allows for fast waveform synthesis with fine frequency resolution, the hardware complexity, which rapidly increases for wideband application, makes a conventional DAS architecture only practicable for narrowband frequency applications in either low or high frequency range [98].

The availability of PLL and DDFS ICs, allow very compact circuit designs for the RFISA synthesizer unit. However, for wideband DDFS operation up to 1 GHz it is imperative to

clock the DDFS with at least 2 GHz to fulfill the Nyquist criterion. Although the IC technology has rapidly advanced, presented CMOS[4] devices for DDFS with on-chip DAC can only be clocked with a maximum frequency of 1 GHz [122] [123]. Thus, their application is limited to output frequencies up to ≈ 400 MHz. A recently introduced DDFS device based on GaAs[5] technology offers now clock frequencies up to 10 GHz and can cover the desired output frequency range [124]. The state-of-the-art for commercial available DDFS-ICs, however, is still confined to a CMOS device with maximum clock frequency of 1 GHz (e.g. AD9912 from Analog Devices, Inc.).

In contrast to DDFS-ICs, the technology advances have enabled single PLL-ICs operating far above 1 GHz [125] [126]. Even a PLL-IC with integrated VCO was recently reported that operates up to 50 GHz [127]. Hence, a large number of commercial PLL-ICs suitable for particular applications are introduced to the market by many manufactures. With the application of single-loop PLL architectures, however, it is not feasible to achieve all: very fine frequency resolution, fast tuning speed, low phase noise, and low spur contamination. Moreover, the frequency tuning range of conventional VCOs is normally limited and, thus, they do not cover alone the desired output tuning range from 10 kHz up to 1 GHz.

In conclusion, since no synthesizer topology provides all requirements specified in section 1.4, a compact design approach combining the respective advantages is required. The hybrid synthesizer topology in Figure 3-8 comprises therefore a combination of two integer-N PLLs, which operate above 1 GHz. The PLL signals are applied to a mixer that, according to (3.3), down-converts the signals to the desired output signal, s_o. The hybrid topology shows the general mixer terminology where the frequency-fixed RF-PLL signal, s_{rf}, which will be frequency converted, is applied to the mixer's RF-port (radio frequency port). The frequency-shifting signal, s_{lo}, from the tunable LO-PLL is applied to the LO-port (local oscillator port) and the output signal, s_{if}, appears at the IF-port (intermediate frequency port). To select the desired down-converted output signal s_o, the output signal s_{if} is low-pass filtered by the IF-Filter having a pass-band bandwidth of $B_{if} = 1\text{GHz}$. The tuning bandwidth of the LO-PLL frequency, f_{lopll}, is specified at $f_{rfpll} + 1\text{GHz}$ where f_{rfpll} is the fixed RF-PLL frequency. This theoretically yields a tunable output frequency in the range of $\text{DC} \le f_o \le 1\text{GHz}$. The fast and fine frequency-hopping capability of the DDFS is exploited for fine-tuning the LO-PLL frequency f_{lopll} with the the DDFS frequency, f_{ddfs}.

Using (3.3), (3.4), (3.5), and provided that low-pass filtering is applied yield the mathematical expression for the desired down-converted output frequency

[4] Complementary metal-oxide semiconductor (CMOS)

[5] Gallium arsenide (GaAs)

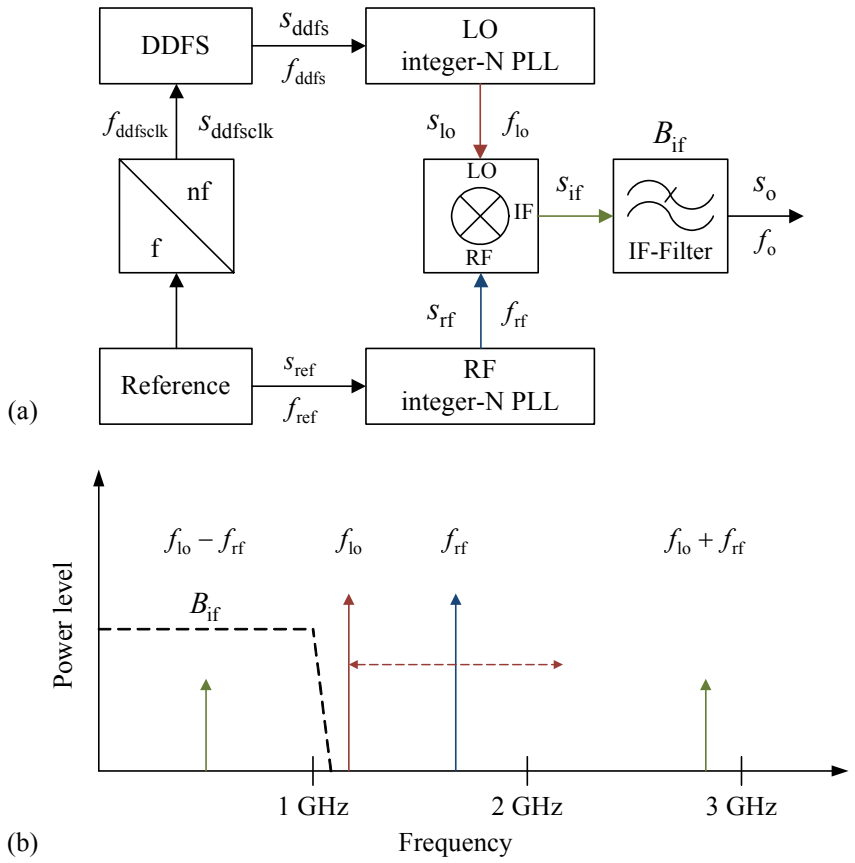

Figure 3-8 Overview of the hybrid synthesizer: (a) topology and (b) frequency conversion scheme.

$$f_o = f_{loPll} - f_{rfPll} = \frac{N_{loPll}}{R_{loPll}} \cdot f_{ddfs} - f_{rfPll} = \frac{N_{loPll}}{R_{loPll}} \cdot \frac{\lfloor PTW \rfloor}{2^r} \cdot f_{ddfsclk} - f_{rfPll} \,. \tag{3.7}$$

where the $\lfloor \ \rfloor$ denotes the truncation to integer, N_{loPll} is the value the LO-PLL's feedback divider and R_{loPll} the value of the LO-PLL's reference divider. Since the RF-PLL is frequency fixed, the DDFS determine the overall frequency resolution of the hybrid synthesizer topology. Hence, with rearranging of (3.7) and neglecting the term that describes the RF-PLL, the NCO's phase accumulator resolution, which is needed to meet the specified minimum frequency resolution of the RFISA synthesizer unit, is given by

$$r = \left\lceil \frac{\ln\left(\frac{N_{loPll}}{R_{loPll}} \cdot \frac{1}{f_{o,min}} \cdot f_{ddfsclk}\right)}{\ln(2)} \right\rceil \tag{3.8}$$

where $\lceil \ \rceil$ denotes the ceiling operation and $f_{o,min}$ is the minimum output frequency of the synthesizer unit.

Chapter 4
Design tradeoffs

This chapter is focused on the design considerations that have decisive impact on the complexity of the electronics system. The chapter is divided into the design considerations for the wideband-tuning DDFS-driven LO-PLL and the wideband digital vector voltmeter. The design of the DDFS-driven LO-PLL significantly influences the spurs and noise performance of the proposed hybrid synthesizer topology. Based on the review of the PLL basics and the spurious contamination at the DDFS output frequency, the design challenge of finding a reasonable tradeoff between the requirements on minimized circuit complexity, fast frequency settling, and good spectral quality of the output signal of the DDFS-driven LO-PLL is described. Crucial specifications for the design of the DDFS are concluded. A direct sampling technique is proposed, which significantly reduces the complexity of the analog circuit design for the digital vector voltmeter. For parameter extraction of the directly sampled signals, a digital signal processing method based on sine-wave fitting is introduced.

4.1 Design considerations for the hybrid synthesizer unit

The proposed hybrid synthesizer architecture in Figure 3-8 advantageously combines various analog and digital frequency synthesies techniques. However, crucial design aspects must be considered to gainfully emphasize their individual benefits. The main design challenge consists of finding a reasonable tradeoff between the requirements on minimized circuit complexity, fast frequency settling, and good spectral quality of the output signal.

In order to meet the requirements on the spectral quality as specified in section 1.4, minimizing the noise and spurs content of the output spectrum of the RFISA synthesizer unit is mandatory. Since the RF-PLL is frequency-fixed, the output signal can be sufficiently band-pass filtered to allow for minimizing the noise and spur contamination at the RF-PLL frequency. However, due to the wideband LO-PLL design, the spectral purity of the LO-PLL signal significantly influences the quality of the down-converted IF-signal. The mixing process superposes the LO-PLL signal spectrum on the RF-PLL signal spectrum and thus translates the LO-PLL phase noise and spurious signals to the IF-signal spectrum as well. Hence, the band of noise and spurious signals originated from LO-PLL signal spectrum surrounds the IF-signal spectrum. Consequently, to achieve maximum spectral quality of the RFISA synthesiz-

er output signal, the noise and spurious content of the LO-PLL output spectrum within the bandwidth of $f_{\mathrm{lopll}} \pm B_{\mathrm{if}}$ must meet the spectral requirements specified in section 1.4. Hence, the challenge for the DDFS-driven LO-PLL consists of finding a reasonable tradeoff between the requirements on proper loop action, fast frequency settling, and minimum spurious content of the LO-PLL output spectrum. Latter is mainly affected by the close-to-carrier spurious performance of the DDFS output signal. Evaluation of the PLL design aspects and the spurious signals in direct digital frequency synthesizers is therefore mandatory to allow for a spur-optimized circuit design of the DDFS-driven LO-PLL along with minimzed complexity.

4.1.1 Design aspects of charge-pump phase locked loops

Nowadays, virtually all ICs for high frequency PLL-based frequency synthesizers utilize a PFD/CP structure. It combines a digital phase/frequency detector (PFD) with input frequency f_{pd} followed by a charge pump (CP). The purpose of the charge pump is to convert the logic states of the PFD into analog signals (charge pump current, i_{cp}) by generating positive and negative charges. For controlling the VCO's output frequency, f_{vco}, the low-pass loop filter converts the charges into the tuning voltage. An overview of important design parameters for the configuration of charge-pump PLLs follows. A comprehensive theory is presented in several textbooks, e.g. [114] [115] [116] [128].

In general, charge-pump PLLs are inherently and inescapably nonlinear circuits. Thus, the mathematical model of a PLL is described by a nonlinear differential equation. Furthermore, the charge-pump PLL performs a discrete-time (sampled) system because of the time-variant switching of the combined PFD and CP operation. If, however, the loop bandwidth, B_{pll}, is narrow compared to the sampling frequency of the charge pump f_{pd}, the operation of the loop can be investigated by continuous-time (averaged) analysis [128]. Moreover, in steady state working mode θ_{err} is generally small, which is a condition normally attained when the loop is locked, and the loop may be approximated by a linear feedback model [114]. According to the control theory for feedback systems, the loop transfer function, $H(s)$, and the error transfer function, $E(s)$, for the linear charge-pump PLL model in Figure 4-1 are given by

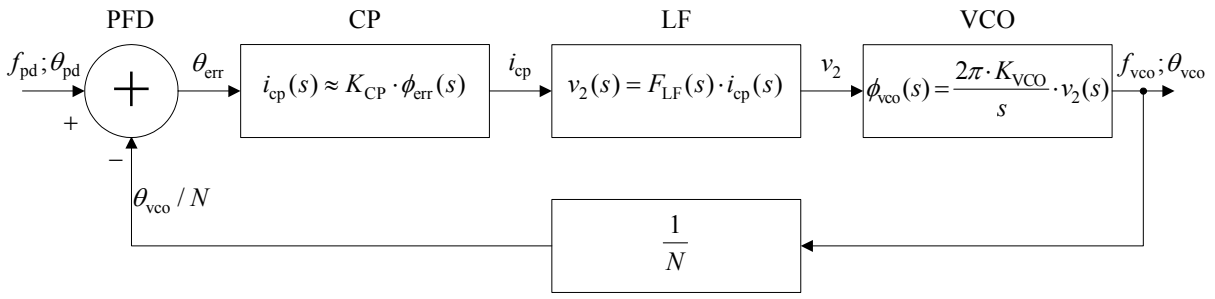

Figure 4-1 Linear model and transfer functions of a charge-pump PLL.

$$H(s)=\frac{\theta_{\mathrm{vco}}(s)}{\theta_{\mathrm{pd}}(s)}=\frac{G_{\mathrm{F}}(s)}{1+G_{\mathrm{F}}(s)G_{\mathrm{R}}(s)}=\frac{K_{\mathrm{CP}}\cdot F_{\mathrm{LP}}(s)\cdot 2\pi\cdot K_{\mathrm{VCO}}}{s+K_{\mathrm{CP}}\cdot F_{\mathrm{LP}}(s)\cdot 2\pi\cdot K_{\mathrm{VCO}}/N}=\frac{N\cdot K\cdot F_{\mathrm{LP}}(s)}{s+K\cdot F_{\mathrm{LP}}(s)} \quad (4.1)$$

$$E(s)=\frac{\theta_{\mathrm{err}}(s)}{\theta_{\mathrm{pd}}(s)}=\frac{1}{1+G_{\mathrm{F}}(s)\cdot G_{\mathrm{R}}(s)}=\frac{s}{s+K\cdot F_{\mathrm{LP}}(s)}. \quad (4.2)$$

where $s=\mathrm{j}\omega=\mathrm{j}2\pi f$ is the Laplace operator, θ_{pd} the PFD input phase, θ_{vco} the VCO phase on the PLL output, and θ_{err} the error phase. $G_{\mathrm{F}}(s)$ and $G_{\mathrm{R}}(s)$ are the forward and reverse transfer functions, respectively, $K_{\mathrm{CP}}=I_{\mathrm{CP}}/2\pi$ the combined gain factor of the PFD/CP, I_{CP} is the nominal (average) charge-pump current, K_{VCO} the VCO gain factor, $F_{\mathrm{LP}}(s)$ the loop filter transfer function, and $K=K_{\mathrm{CP}}\cdot 2\pi\cdot K_{\mathrm{VCO}}/N$ is the effective gain factor.

A typical charge pump generally comprises two current switches pumping or extracting current into or from the loop filter. The loop filter converts the series of pulses into an average voltage proportional to the average current. Generally, the low-pass characteristic can significantly be improved with increasing filter order. However, to maintain proper loop stability it is recommended to use low-pass filter designs that lead to a second-order PLL or approximately to a second-order PLL by neglecting higher order effects [114]. To achieve a second-order PLL, a single-pole filter transfer function such as given by $F_{\mathrm{LP}}(s)=(s\cdot\tau_2+1)/(s\cdot\tau_1)$, where τ_1 and τ_2 are the specific time constants of the filter design, must be applied. Inserting $F_{\mathrm{LP}}(s)$ into (4.1) and (4.2) yields the second-order transfer functions

$$H(s)=\frac{N\cdot K\cdot(s\cdot\tau_2+1)/\tau_1}{s^2+s\cdot K\cdot\tau_2/\tau_1+K/\tau_1}=N\cdot\frac{2\cdot\zeta\cdot\omega_{\mathrm{n}}\cdot s+{\omega_{\mathrm{n}}}^2}{s^2+2\cdot\zeta\cdot\omega_{\mathrm{n}}\cdot s+{\omega_{\mathrm{n}}}^2} \quad (4.3)$$

$$E(s)=\frac{s^2}{s^2+2\cdot\zeta\cdot\omega_{\mathrm{n}}\cdot s+{\omega_{\mathrm{n}}}^2} \quad (4.4)$$

where $\omega_{\mathrm{n}}=\sqrt{K/\tau_1}$ is the natural frequency of the loop and $\zeta=\tau_2\cdot\omega_{\mathrm{n}}/2$ is the damping factor. Natural frequency and damping factor are the basic loop parameters to specify the second-order charge-pump PLL and to define the PLL loop bandwidth, B_{pll}.

The amplitude responses for $|H(s)|$ and $|E(s)|$ for various values of ζ are plotted in Figure 4-2. Inspection of their specific nature reveals the two basic categories of phase-filtering operations, which generally appears in a PLL. The basic character of $H(s)$ performs a low-pass filtering operation on the phase modulation of the input signal and allows that input phase modulation within the loop bandwidth B_{pll} (referred to as in-band in the following) is transferred to the VCO output phase. In contrast, input phase modulation outside the loop bandwidth (referred to as out-band in following) is attenuated. The character of $E(s)$ performs a

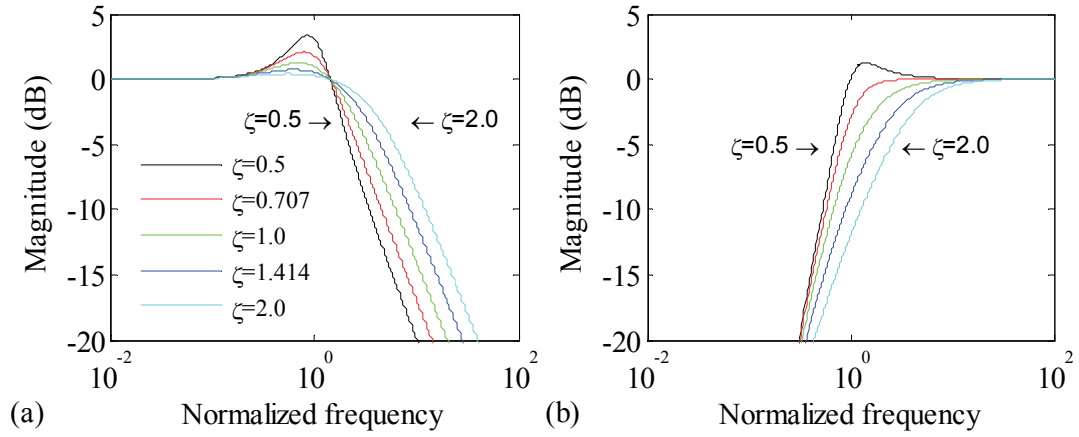

Figure 4-2 Magnitude response of a simulated second-order PLL for different damping factors normalized to natural frequency: (a) loop transfer function and (b) error transfer function in double logarithm scale.

complementary high-pass filtering operation. As shown in Figure 4-2, the damping factor singnificantly affects the -3 dB cutoff frequency and the gain peaking. The latter will be transformed into overshoot in the time-domain transient response of the loop.

Settling time, which is also related to the loop transfer function, is another important performance aspect. PLL settling time is determined by the time necessary for the PLL to settle within a specified frequency window after a frequency change has been occurred. Analytically, the settling time is a function of ω_n and ζ, and can be obtained from the time-domain transient response. In general, PLL settling time is inverse proportional to the loop bandwidth.

Since the PLL is a feedback system, oscillation will arise whenever the denominator in (4.3) equals zero. Consequently, proper choice of the loop parameters is essential to maintain loop stability. There are two sources for the stability limit in charge-pump PLLs. The first stability limit arises from the sampling operation. Gardner points out in [128] that a second-order charge-pump PLL will become unstable if the loop gain is made so large that the loop bandwidth becomes comparable to the sampling frequency f_{pd}. Hence, to avoid loop instability, the minimum input frequency has to exceed at least ten times the loop bandwidth (Gardner's stability limit: ($10B_{pll} < f_{pd}$). The second stability limit derives from the conventional control theory and will be obtained from the open-loop characteristic.

With application of the Bode plot criterion of stability [114], the stability of a PLL is measured by the phase margin, ψ_{pm}, of the open-loop transfer function $G(j\omega) = G_F(j\omega) \cdot G_R(j\omega)$. The phase margin is given by $\psi_{pm} = \angle[G(j\omega_{gc})] + \pi$ where ω_{gc} is the gain crossover frequency defined by $|G(j\omega_{gc})| = 1$ (0 dB). A PLL is stable if $\psi_{pm} > 0$ and unstable if $\psi_{pm} < 0$. For proper loop stability, a PLL should have a phase margin of at least 45°. The Bode plot for the open loop gain and phase of (4.3) is shown in Figure 4-3 for several values of ζ, where

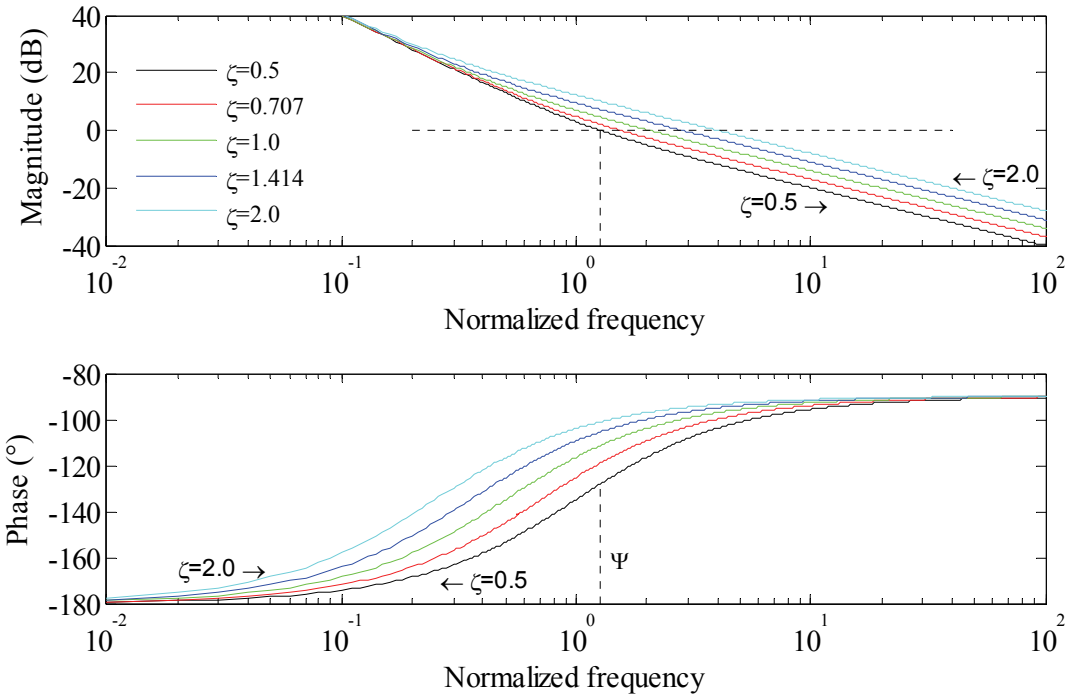

Figure 4-3 Frequency response of the simulated open loop gain for a second-order PLL for different damping factors normalized to natural frequency.

the phase margin for $\zeta = 0.5$ is exemplified. From Figure 4-3 it is apparent that higher damping factors significantly improve the phase margin and thus the stability of the loop.

In terms of PLL performance, the phase noise and spurs characteristic of the output signal is another important design tradeoff. There are, in principle, three sources of noise in PLL systems [117] [129] [130]: (a) noise introduced by the reference source that generates the phase detector frequency f_{pd}; (b) noise originated from the loop components (phase detector, charge pump, loop filter, frequency divider); and (c) noise introduced by the VCO. Due to the low-pass characteristic of the loop transfer function (4.3), the out-band noise originated from (a) and (b) will effectively be attenuated whereas the in-band noise will be amplified by the loop gain and translated to the VCO output. At the output of a single-loop PLL, the power level (in dB) of in-band noise (and spurs) is significantly increased by the value of N given by

$$P_{\mathrm{o}} = P_{\mathrm{pd}} + 20 \cdot \log(N) \tag{4.5}$$

where P_{pd} is the summed up additive noise power (in dB) sourced from (a) and (b). Hence, the PLL's output phase noise and spurious characteristic is adversely affected by large feedback-divider ratios. In contrast, due to the high-pass characteristic of the error transfer function (4.4), the VCO's in-band phase noise close to the carrier f_{vco} is attenuated. Thus, com-

pared to a free-running VCO, the PLL may improve the in-band noise characteristic of the phase-locked VCO.

In addition to the various noise sources, non-idealities in the combined PFD/CP operation cause feedthrough of the phase detector frequency f_{pd}. It appears as modulation on the VCO tuning voltage. Due to the sampling action of the PFD/CP, the modulation occurs on the VCO output frequency as high-level frequency modulation sidebands at multiples of f_{pd}. The sideband spurs are given by $f_{\mathrm{vco}} \pm n \cdot f_{\mathrm{pd}}$ where $n \in \mathbb{N}$ [131]. In general, feedthrough of f_{pd} is mainly caused by leakage current effects originated from the charge pump, VCO, loop filter components, and from mismatch in the charge-pump up and down current sources. These effects inevitably enforced alternating correction pulses even in the lock condition of the loop. The relative amplitude of the spurious signals is determined by the trans-impedance of the loop filter, the magnitude of the DC leakage current, and the value of the phase detector frequency. It is independent on the nominal charge-pump current [132].

In summary, the design of the basic loop parameter bandwidth and damping, which are mainly determined by the loop filter characteristic, involves several tradeoffs to achieve the required overall performance with respect to settling time, in-band and out-band phase noise, loop stability, and spurs suppression. The design tradeoffs are summarized in Table 4-1. Obviously, a wide loop bandwidth is essential to allow for fast frequency settling of an integer-N PLL. To achieve also good spectral quality of the output signal, a low feedback-divider value must be preferred to avoid significant amplification of the power level of in-band noise and sideband spurs. In accordance to Gardner's stability limit, an integer-N PLL design with wide loop bandwidth and low feedback-divider value, however, requires a high-frequency phase detector input signal with excellent in-band ($f_{\mathrm{pd}} \pm B_{\mathrm{lopll}}$) spectral quality to avoid deterioration of the output spectral quality.

Table 4-1 Summary of PLL design tradeoffs.

design tradeoffs	loop bandwidth	damping
faster settling	wide	under
better stability	narrow	over
lower in-band phase noise	narrow	—
better spur suppression	narrow	—
low overshoot	—	over

4.1.2 Spurious signals in direct digital frequency synthesizers

As mentioned in Section 3.3, the main disadvantage of the DDFS is the typical high spurious and noise content in the output spectrum. This is caused by quantization effects of the numerical controlled oscillator (NCO) operation and linearity limitations of the digital-to-analog converter (DAC) operation. Particularly, the DDFS output spectrum suffers from spurs that appear very close to the carrier, f_{ddfs}, difficult to suppress by the reconstruction filter.

Spectra of the discrete NCO output sequences for different normalized output frequencies $\xi = f_{\mathrm{ddfs}} / f_{\mathrm{ddfsclk}}$, which are generated very close to each other, are shown in Figure 4-4. The spectra were computed using the Discrete Fourier Transform with 7-term Blackman-Harris window. A NCO design with a phase accumulator (PACC) resolution of $r = 32$ bit, a phase-to-waveform converter (PWC) input resolution of $w = 12$ bit, and an output amplitude resolution of $d = 10$ bit was chosen. Since Figure 4-4 shows spectra prior to digital-to-analog conversion of the discrete NCO sequence, the plots reveal the frequency response due to algorithm nonlinearities (numerical distortions) inherent in the NCO. It is evident from comparing the spectra that even a small change of frequency results in a significant change of spectral shape of the NCO output sequence. The DDFS output spectra will additionally be corrupted by the operation of the particular DAC. Thus, knowledge about the sources of spurious sig-

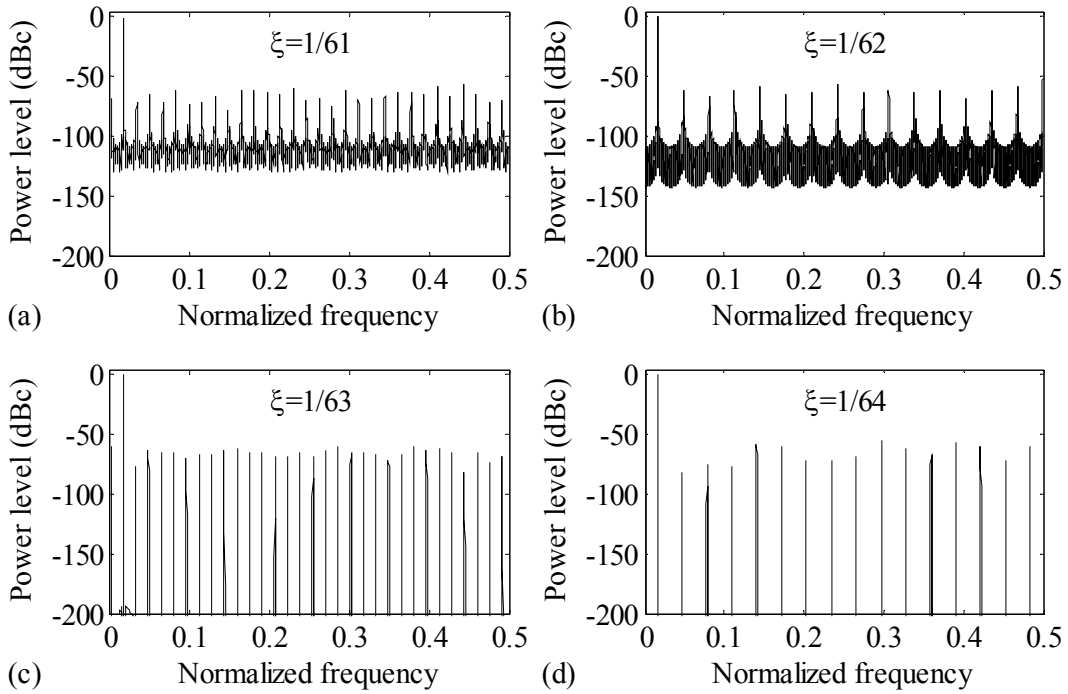

Figure 4-4 Spectra of sinusoidal waveforms generated by a numerical controlled oscillator for various normalized output frequencies (frequency axis is normalized to the sampling clock frequency).

nals and their expected amplitudes and frequencies are requied for appropriate configuration of the DDFS architecture to achieve a high-frequency DDFS output signal with good in-band ($f_{\mathrm{ddfs}} \pm B_{\mathrm{pll}}$) spectral quality.

In addition to the images of the desired signal frequency (see section 3.3), a conventional DDFS architecture has six principal sources of noise and spurious signals [106] [107]:

(1) numerical distortion due to quantization of the phase tuning word,
(2) numerical distortion due to truncation of the phase accumulator bits,
(3) numerical distortion due to quantization of the sinusoidal waveform samples,
(4) numerical distortion due to the algorithm of the sinusoidal waveform representation,
(5) distortion due to the nonlinearities of the digital-to-analog converter, and
(6) phase noise of the sampling clock.

The sources of numerical distortions are originated from the NCO operation. The numerical distortions appear simultaneously and exercise mutual influence on each other [111]. Due to the periodical operation of the NCO in the digital domain, all parameters, mathematical operations, and numerical distortions are represented by numbers and thus deterministic. Hence, the periodicities of the desired signal sequence and the quantization errors can completely be calculated, e.g. by computing the Discrete Fourier Transform as shown before. Due to the inherent sampling operation of the DDFS, aliasing causes that the spurious signals originated from numerical distortions may fold back into the desired DDFS output bandwidth. Spurious frequencies greater than the Nyquist frequency are folded back within the 1st Nyquist zone and possibility overlapping. Frequencies in odd Nyquist zones fold back directly onto the 1st Nyquist zone while spurious frequencies in the even zones fold back in mirror fashion onto the 1st Nyquist zone. This result in a high density of spurious signals close to f_{ddfs} .

The numerical distortions due to truncation of the PACC's instantaneous phase word addressing the PWC (as shown in Figure 3-4), and due to the quantization of the amplitude samples present a major contribution to the spurious content at the DDFS output frequency. Combining both effects, the numerical sequence of the NCO in the DDFS architecture is given by

$$x_{\mathrm{nco}}[n] = e_{\mathrm{aq}}[n] + \sum_{n=-\infty}^{\infty} \sin\left(\frac{2\pi}{2^r} \cdot \left(\lfloor PTW \rfloor \cdot n - e_{\mathrm{pq}}[n]\right)\right) \tag{4.6}$$

where $\lfloor \ \rfloor$ denotes truncation to integer values, n is the discrete time-domain index, $e_{\mathrm{aq}}[n]$ the quantization error sequence associated with amplitude quantization, and $e_{\mathrm{pq}}[n]$ the quantization error sequence associated with phase truncation [106]. The phase and amplitude sample sequences of the NCO are periodic. Consequently, the corresponding quantization error sequences are periodic in the time domain as well, and the errors therefore appear as discrete

spectral lines in the frequency domain. The amplitude quantization, which is permanently present, causes harmonically related spurs whereas phase truncation produces phase modulation spurs close the desired carrier f_{ddfs} [111].

Phase truncation of the instantaneous phase accumulator output sequence before being fed to the PWC is essential in a conventional DDFS architecture to maintain the PWC memory size ($2^r \times d$ bits) reasonable without sacrificing frequency resolution. Only *w* most significant bits out of all *r* bits are retained and $b = r - w$ least significant bits are discarded. Phase truncation occurs only when $\gcd(PTW, 2^r) < 2^b$, where $\gcd(x, y)$ represents the greatest common divisor of *PTW* and 2^r. If $\gcd(PTW, 2^r) \geq 2^b$, then the phase increment bits are zeros below 2^b and no phase error occurs. However, there are only 2^b phase tuning words out of a total of 2^r that do not generate phase truncation related spurs. The phase error sequence $e_{\text{eq}}[n]$ can be modeled as the sampled values of a continuous time sawtooth waveform identical to the waveforms in Figure 4-5, but generated by a phase accumulator with *b*-bit word length. This yield an equivalent input phase tuning word of $(PTW)_{\text{mod } b}$ where $(x)_{\text{mod } b}$ describes taking the integer residue of a number modulo 2^b [133].

Phase truncation spurs are proportional to the weight of the discarded bits and, therefore, are not typically issues. In general, there are different methods of functional mapping from phase to sine amplitude in DDFS designs [107] [134]. Pratical implementations of the PWC operation may employ simple look-up table operation or algorithm approximations of the sinusoidal waveform representation. Due to the finite precision, the non-ideal waveform representation causes additional numerical distortions, resulting in different sets of spurious signals specific to the PWC implementation.

A comprehensive analytical derivation of the phase truncation effects has been elaborated by several authors in the past, particularly by Mehrgardt [135], Nicholas *et al.* [133], Kroupa [136] [137] [138], and Jenq [139]. They presented analytical expressions for computation and thus for prediction of the relative magnitude and the spectral distribution of the phase truncation spurs. Torosyan *et al*. recently presented in [140] an algorithm for computation of DDFS output spur magnitudes and locations in the presence of both phase truncation and arbitrary (non-ideal) implementation of the mapping function into the PWC. Exact prediction of the spurious frequencies allows for suitable frequency planning with low spurious contamination at the DDFS output frequency when narrowband frequency tuning is desired. For wideband frequency tuning, however, suitable frequency planning is not feasible.

A main result is that the number of phase truncation spurs, given by $(2^b / \gcd(PTW, 2^b)) - 1$, and their magnitude only depend on *PTW* through $\gcd(PTW, 2^b)$ [133]. Values of *PTW* that have the same $\gcd(PTW, 2^b)$ result in output spectrums with the same number of spurs and with their respective amplitudes unchanged. Only the position of each phase truncation spur is

altered and depends on the content of the discarded bits. The worst case phase truncation spur is obtained when $\gcd(PTW, 2^b) = 2^{b-1}$ and its level describes the minimum carrier-to-spur ratio of the phase truncation spurs

$$SFDR_{\text{ddfs}} = 6.02 \cdot w - 3.92 \tag{4.7}$$

where SFDR is the spurious-free dynamic range[6] in dBc, w is the number of non-truncated phase word bits addressing the PWC [133] [139]. The sum of the discrete spurs due to quantization of the amplitude samples is approximately equal to the integrated signal-to-noise ratio[7], in dB

$$SNR_{\text{ddfs}} = 6.02 \cdot d + 1.76 \tag{4.8}$$

where d is the bit width of the amplitude samples [91] [106] [141]. Obviously from (4.7) and (4.8), to ensure that the high level spurious signals due to phase truncation do not exceed the background noise floor caused by amplitude quantization, it is necessary to specify

$$w \geq d + 2\,. \tag{4.9}$$

As the consequence of operating in the discrete domain with finite accuracy and not in the continuum domain, the behavior of the DDFS spurious spectrum for different values of the phase tuning word *PTW* is intrinsically linked to the numerical properties of the phase accumulator [133]. While the NCO generates a average output frequency given by (3.4), there is another numerical period that is generated by the periodicity of the discrete phase accumulator output sequence $\theta[n]$. The numerical period of $\theta[n]$ is defined as the minimum value P for which $\theta[n] = \theta[n+P]$ for all n.

As shown in Figure 4-5, the numerical period P depends on the value of *PTW*. In general, the numerical period P (in clock cycles), is given by $P = 2^r / \gcd(PTW, 2^r) \leq 2^r$ where $\gcd(x, y)$ represents the greatest common divisor of *PTW* and 2^r. Nicholas *et al.* reports in [133] that the spectrum of the numerical sequence of the NCO prior to digital-to-analog conversion is characterized by a discrete spectrum consisting of P spectral lines. The spectral lines are uniformly spaced on the frequency axis and symmetric about the origin in the frequency domain. The spectral lines of the numerical sequence are harmonically related to the base frequency given by

[6] Spurious-free dynamic range (SFDR) is the power ratio of the carrier (fundamental) and the largest harmonically or non-harmonically related spur [191].

[7] Signal-to-noise ratio (SNR) is the ratio of the signal power and the noise power within a certain bandwidth, usually, the Nyquist bandwidth, e.g., half the sampling frequency [191].

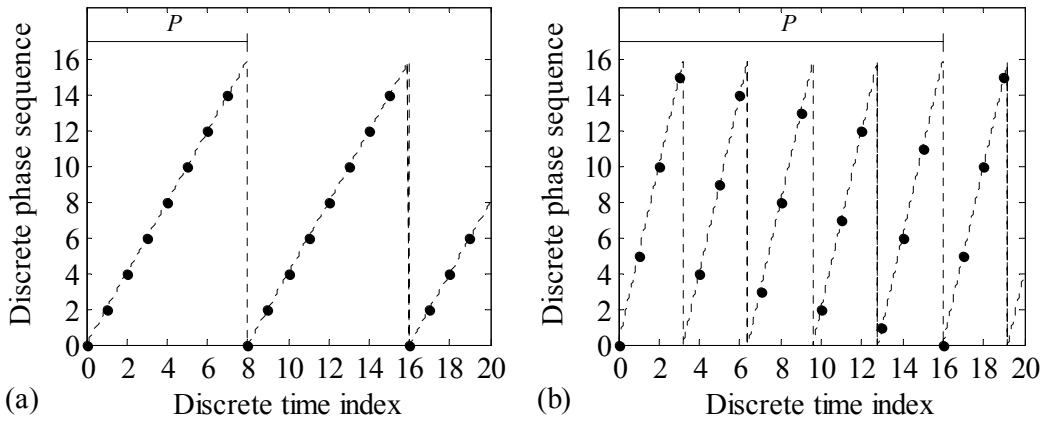

Figure 4-5 Output phase sequence of a 4-bit phase accumulator for a phase tuning word of (a) two and (b) five.

$$f_{\text{base}} = k \cdot \frac{\gcd(PTW, 2^r)}{2^r} \cdot f_{\text{ddfsclk}} \tag{4.10}$$

where $k \in \mathbb{N}, 0 \le k \le P-1$. Equation (4.10) also includes the location of the desired output frequency f_{ddfs}. There are only *r*-1 phase tuning words that satisfy $P \cdot T_{\text{ddfsclk}} = T_{\text{ddfs}} = f_{\text{ddfs}}{}^{-1}$ due to $\gcd(PTW, 2^r) = PTW$. The majority of phase tuning words, however, create a residual phase word at the point at which the phase accumulator overflows. This cause a disparity between the phase accumulator period $P \cdot T_{\text{ddfsclk}}$ and the desired average signal period T_{o}. As mentioned, *r* must be very large ($r > 24$) to achieve fine frequency resolution at high DDFS clock frequency. This, however, yield a large number of spectral lines in the output spectrum, resulting in spurious phase modulation very close to carrier f_{ddfs} [107]. For example, if *PTW* is an odd integer then $P = 2^r$ in all cases. Obviously from (4.10), an odd integer value of *PTW* produces spur components that are symmetrically located in pairs around the carrier f_{ddfs} as close as $f_{\text{ddfsclk}} / 2^r$.

Although, all numerical distortions are theoretically predictable, the predictability of the entire DDFS noise and spurs contamination is lost in the mixed analog/digital stage of the DDFS, namely due to the non-linear and non-ideal DAC attributes. Their mathematical analysis is difficult and the ability to predict the spectral performance is only as good as the DAC model or the knowledge about the real performance of the digital-to-analog conversion is [91]. Vankka [106] confirms this and supplements the only reliable method for obtaining knowledge about the spectral and noise purity is to have the DAC characterized by hardware test in the laboratory. In particular, DAC nonlinearities, switching transients, and sampling clock feedthrough introduce harmonics of the carrier f_{ddfs}, harmonics of the sampling clock f_{ddfsclk},

and numerous mixing products of the harmonics. This produces significant harmonic distortion at the DDFS output.

If the DDFS sampling clock suffers from jitter, then the NCO and the DAC will non-uniformly be clocked. This yields a spreading of the spectral lines at the DDFS output frequency, deteriorating the spurious performance close to the carrier f_{ddfs} as well. Consequently, the output phase noise performance must be improved by a large ratio between f_{ddfsclk} and f_{ddfs} given by $P_{\mathrm{o}} = P_{\mathrm{clk}} + 20\log(f_{\mathrm{ddfsclk}} / f_{\mathrm{ddfs}})$ where P_{clk} (in dB) is the phase noise of the sampling clock [106].

In summary, the various noise and spur sources critically affect both the wideband and the narrowband spurious content of the DDFS output spectrum. The numerical operation of the phase accumulator and the phase tuning word determine the distribution of the spurious signals at the DDFS output frequency. Due to the, in general, high values of *r* for the required fine frequency resolution of the DDFS, a high density of spurious signals close to f_{ddfs} appear at the DDFS output frequency. However, the level of the spurious signals is affected by the particular design of the phase-to-wavefrom converter implementation and the digital-to-analog converter. The latter contributes additional harmonic distortions due to its non-ideal conversion characteristic. The predictability of the spur frequencies aids in the choice of an optimal frequency plan to achieve excellent close-to-carrier spurious performance in narrowband tuning application. However, this is not feasible for wideband application. Since the high level close-to-carrier spurious signals due to numerical distortions are inevitable for high-frequency operation with fine frequency resolution, proper configuration of the NCO design according to (4.9) is essential to allow for generating high-frequency DDFS output signals with good in-band ($f_{\mathrm{ddfs}} \pm B_{\mathrm{pll}}$) spurious performance.

4.1.3 Hybrid phase locked loops

In principle, there are two hybrid topologies for fast-settling DDFS-driven PLLs, which allow for DDFS-driven PLL designs with wide loop bandwidth in spite of the high level spur contamination at the DDFS output frequency: (a) the narrowband-tuning DDFS-driven PLL and (b) the DDFS-driven (offset) translation loop (Figure 4-6) [142] [143]. The PLL provides in both designs the coarse frequency steps whereas the DDFS provides the fine interpolation steps between the coarse steps.

In the narrowband-tuning DDFS-driven PLL design, a band-pass filter confines the spurious content of the DDFS output spectrum to a narrow bandwidth. In this application, a wide loop bandwidth can be chosen to provide both fast frequency settling and good spectral quality of the PLL ouput signal. Generally, crystal filters with steep band-pass characteristic are employed to achieve good spurs suppression. With regard to the sampling clock frequency of the

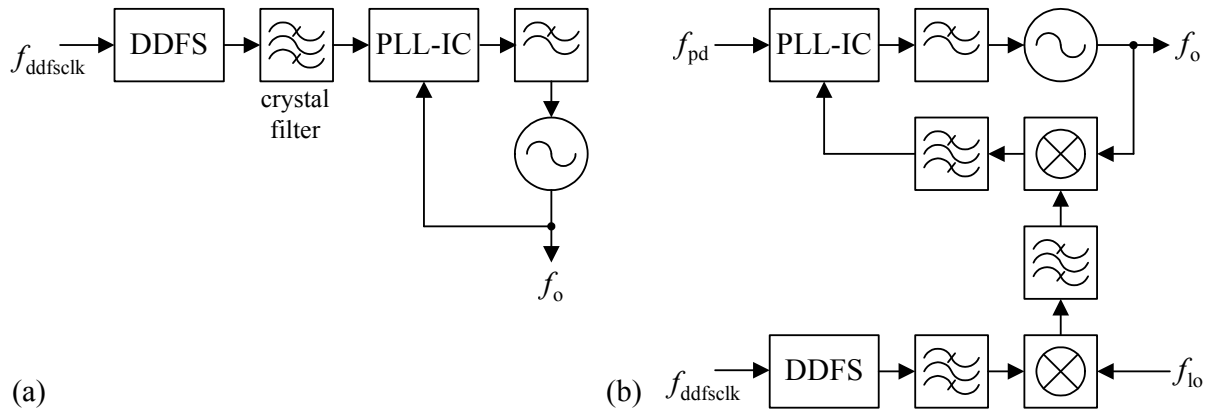

Figure 4-6 Topologies for (a) narrowband-tuning DDFS-driven PLL and (b) DDFS-driven translation loop.

DDFS and the center frequency of the band-pass crystal filter, a well-chosen narrowband frequency plan of the DDFS output signal allows for driving the PLL with low spurs contamination. According to the bandwidth of the band-pass filter, a DDFS tuning bandwidth of $\Delta f_{ddfs} = f_{ddfs,0} / N_{min}$ is required to provide continuous frequency coverage, where $f_{ddfs,0}$ is the DDFS center frequency and N_{min} the minimum value of the PLL feedback divider. Advantageously, a high $f_{ddfs,0}$ allows low values of *N*. However, since the PLL is narrowband driven by the DDFS, *N* is not constant over the required wideband tuning range of the RFISA synthesizer unit. In accordance to (4.5), increasing *N* values, however, may critically affect the spurious content of the LO-PLL output signal when tuning over the total frequency range.

In contrast, the DDFS-driven translation loop utilizes the up-converted and filtered DDFS output signal to fine modulate the fed back VCO frequency. Provided that low-pass filtering is applied, the output frequency is given by $f_o = N \cdot f_{pd} \pm (f_{lo} \pm f_{ddfs})$ where f_{lo} is the intermediate frequency required to up-convert the DDFS output. Generally, f_{lo} must be generated by a second frequency-fixed PLL. Since this feedback loop topology is based on frequency translation rather than frequency multiplication of f_{ddfs}, the spurious content of the DDFS output spectrum is not amplified by *N*. Hence, the DDFS-driven translation loop provides wide PLL loop bandwidths and large values of *N* while maintaining good spurious performance of the output signal. However, this is at the expense of significantly increased circuit complexity.

4.1.4 Conclusions for the synthesizer unit

The aim of the previous subsections was the analysis of the fundamentals of PLL and DDFS designs because the DDFS-driven LO-PLL mainly affects the overall performance of the RFISA synthesizer unit. The considerations were focused on the main synthesizer requirements on fast frequency settling and good spurious performance of the LO-PLL output signal.

It was shown that there is a strong tradeoff involved in selecting the bandwidth of PLL for fast frequency settling. A wide loop bandwidth allows fast frequency settling but does not sufficiently attenuate the high-level wideband spurious content of the DDFS output spectrum. Due to the fundamental PLL operation based on frequency multiplication-by *N*, the spurious content of the DDFS output spectrum within $f_{\mathrm{ddfs}} \pm B_{\mathrm{pll}}$ will be amplified by *N* according to (4.5), whereas their frequency offset from the DDFS carrier remains unchanged, thus deteriorating the close-to-carrier spurious content of the LO-PLL ouput spectrum significantly. Summarizing the considerations, the following design specifications can be concluded.

In consideration of the primary objective of minimizing the overall circuitry, a wide loop bandwidth B_{pll} and a low damping factor ζ of the LO-PLL design are inevitably in order to allow fast frequency settling of a single PLL topology. For this application, DDFS-driven PLL translation loops are able to synthesize output signals over a wide frequency range with excellent spectral quality and fast frequency settling. However, applying a DDFS-driven PLL translation loop would significantly increase the overall circuit complexity of the RFISA synthesizer unit. Hence, a DDFS-driven PLL translation is not preferred. As a consequence of the wide loop bandwidth B_{pll}, the feedback divider value *N* of the LO-PLL must be kept constant and as low as possible to avoid significant amplification of the in-band noise and spurs. Due to the constant value of the feedback divider, a narrowband-tuning DDFS-driven PLL design is not applicable. Consequently, a wideband-tuning DDFS-driven PLL design is mandatory.

With regard to Gardner's stability criterion ($10 f_{\mathrm{ddfs}} > B_{\mathrm{pll}}$), a wideband-tuning DDFS-driven PLL design with low feedback divider value *N* and wide loop bandwidth B_{pll} implies a wide-tunable DDFS design with high-frequency output signals and good close-to-carrier spur performance. Since the spurious content of the output signal of the DDFS-driven LO-PLL mainly determines the output spur performance of the RFISA synthesizer unit, the DDFS output spectrum in the range of $f_{\mathrm{ddfs}} \pm B_{\mathrm{pll}}$ must exhibit a minimum signal-to-noise ratio of

$$SNR_{\mathrm{ddfs,min}} = 20 \cdot \log(N)\,\mathrm{dB} + 60\,\mathrm{dB} \tag{4.11}$$

and a minimum spurious-free dynamic range of

$$SFDR_{\mathrm{ddfs,min}} = 20 \cdot \log(N)\,\mathrm{dBc} + 40\,\mathrm{dBc} \tag{4.12}$$

for all signals to be generated over the total DDFS frequency-tuning range. The respective values of 60 dB and 40 dBc are taken from the specifications in section 1.4. Consequently, the design efforts for the DDFS must overcome the contrast between high-frequency signal generation along with fine tuning resolution and excellent close-to-carrier spur performance.

4.2 Design considerations for the digital vector voltmeter unit

The digital vector voltmeter unit in the RFISA electronics system (see Figure 5-1) must perform the frequency-selective complex demodulation of the input signal s_a and s_b (the term s_a or s_b is combined to $s_{a,b}$ in the following) in order to extract the vector components, namely the real and imaginary components, of $s_{a,b}$. In principle, a digital vector voltmeter combines a demodulation receiver, whose system design is comparable with conventional digital communications receiver, with the frequency selectivity of a spectrum analyzer, which examines the spectral composition of an input waveform. Obviously, the impedance measurement accuracy of the RFISA electronics is mainly affected by the vector measurement accuracy of the digital vector voltmeter. Hence, a system topology is required, which meets the requirements on both compact circuitry and excellent vector measurement accuracy up to a frequency of 1 GHz.

4.2.1 Review of analog front-end topologies

In principle, complex demodulation of a signal into its inphase (0°) and quadrature (90°) components can be accomplished either in the analog domain before digitizing (Figure 4-7a) or in the digital domain (Figure 4-7b-c) after digitizing.

The generic topology of the analog complex demodulator is based on phase-sensitive demodulation [144]. In general, the analog complex demodulator comprises a tunable RF reference oscillator (REFOSC) synchronized to the exact frequency of the input signal and a quadrature demodulator (QMIX). The QMIX separates the respective inphase and quadrature components of the input signal and the low-pass filters extract the desired DC signals, which will finally be digitized by the analog-to-digital converter (ADC). To achieve separation into the inphase and quadrature components, the signal of the reference oscillator must be split into two signals having a phase shift of exact 90° with respect to one another. Mathematically, the quadrature demodulator multiplies the input signal by two signals being orthogonal to each other and having the same frequency as the input signal. After low-pass filtering (time-averaging), the integrated DC signals are phase-sensitively rectified versions of the input signal and proportional to the real and imaginary part of the input signal.

Although the topology of the analog complex demodulator is able to achieve high frequency selectivity and excellent noise suppression, it also entails four drawbacks. First, additional circuitry for a tunable RF reference oscillator that has to be phase-locked to the input signal, a parallel set of mixers, and low-pass filters are required. Second, to attain excellent noise suppression, extended time-averaging is required to extract low-noise DC signals. Obviously, this would significantly increase the measurement time of the RFISA electronics system. Third, an accurately matched wideband circuit design is essential to avoid imbalances between the in-

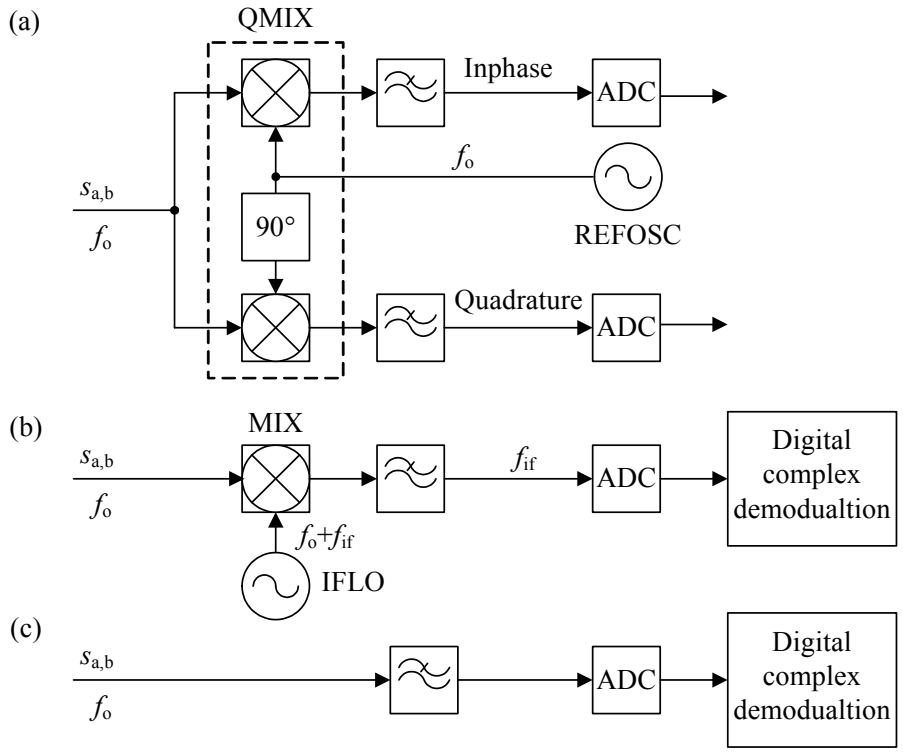

Figure 4-7 Generic analog front-end topologies for (a) analog complex demodulator, (b) IF-sampling digital complex demodulator, and (c) direct-sampling digital complex demodulator.

phase and quadrature reference signals. This, however, will be challenging for the required frequency range from 10 kHz to 1 GHz. Fourth, any DC offsets as well as their drifts at the input of the ADCs must properly be compensated to avoid measurement errors. Hence, an increased complexity of the circuit design is required to ensure that offset drifts are negligible.

The IF-sampling topology in Figure 4-7b overcomes the drawbacks of the analog complex demodulator because complex demodulation of the input signal is accomplished in the digital domain, reducing the complexity of the analog circuitry. In principle, this topology is based on a (super-) heterodyne digital receiver architecture well-established in modern communications receiver designs [145] [146] [147] [148]. Usually, the high-frequency input signal is frequency converted by one or more mixer stages (MIX) to a fixed, lower intermediate frequency, f_{if}, and then analog-to-digital converted by the ADC. Subsequent, digital signal processing (DSP) techniques process and provide the complex demodulation. Due to the technical advances in the analog/digital circuit technology in the last decade [149], fast digital signal processing can be attained, reducing the time for data recording and computation significantly. Frequency conversion to a fixed intermediate frequency is well-established in RF wideband digital receiver applications in order to simplify the requirements on the dynamic specifications of the following ADC. This, however, is at the expense of additional circuitry for the tunable local oscillator (IFLO).

Based on the primary objective of minimizing the circuit design of the RFISA digital voltmeter, the direct-sampling topology (Figure 4-7c) that directly digitized the input signal without frequency down-conversion is preferred. This approach not only allows for fast signal processing but also significant reduction of the analog circuit design to the minimum number of components that are elementally required.

4.2.2 Design considerations for a wideband direct-sampling analog front-end

The primary difficulty in establishing a practical direct-sampling topology is caused by the wideband design needed. The direct sampling technique beneficially decreases the complexity of the circuitry, but at the expense of increased requirements on the high-frequency performance of the primary analog components (filter, amplifier, ADC). In particular, due to the wide input bandwidth, the analog front-end and the ADC have to process the complete signal bandwidth up to 1 GHz without sacrificing performance. Furthermore, because adequate suppression of noise and distortion by a wideband anti-aliasing filter in front of the ADC is not feasible, a low-noise overall front-end design is essential in order to achieve maximum measurement performance of the RFISA electronics system. The most critical component to select for the design of the analog front-end is the ADC because the direct-sampling topology cannot establish if the high-frequency input signals cannot properly be converted from the analog domain into the digital domain. Unfortunately, there is a strong technology tradeoff between sampling frequency, resolution, and analog input bandwidth of the ADC. This has significant impact on the choice of the available ADC-IC [150].

Since the ADC in the RFISA digital vector voltmeter must process the full sweeping bandwidth of the synthesizer unit, an analog input bandwidth of at least 1 GHz is essential. Hence, it is imperative that the resolution and the sampling frequency of the ADC have to be chosen with regard to the 1 GHz analog input bandwidth. In order to maintain the Nyquist criterion, in principle, a sampling frequency of at least 2 GHz is required. However, Walden has shown in [151] that at sampling frequencies ranging from 2 MHz to 4 GHz, resolution (starting from a stated resolution of 20 bit) falls of by ~1 bit for every doubling of the sampling frequency and the average improvement is only ~1.5 bits for any given sampling frequency over six–eight years. Consequently, the specifications based on the technology limitations on sampling frequency, amplitude resolution, and input bandwidth of available ADC-ICs dictate the overall system design of the RFISA digital vector voltmeter and place the most constraints on it.

The ADC translates the continuous analog signal $s_{\mathrm{a,b}}(t)$ applied at its input into the digital representation $s_{\mathrm{a,b}}[n]$, where $n \in \mathbb{N}$ is the discrete-time index, by performing sampling and subsequent quantization. Thus, the theoretical maximum signal-to-noise ratio of a given ADC

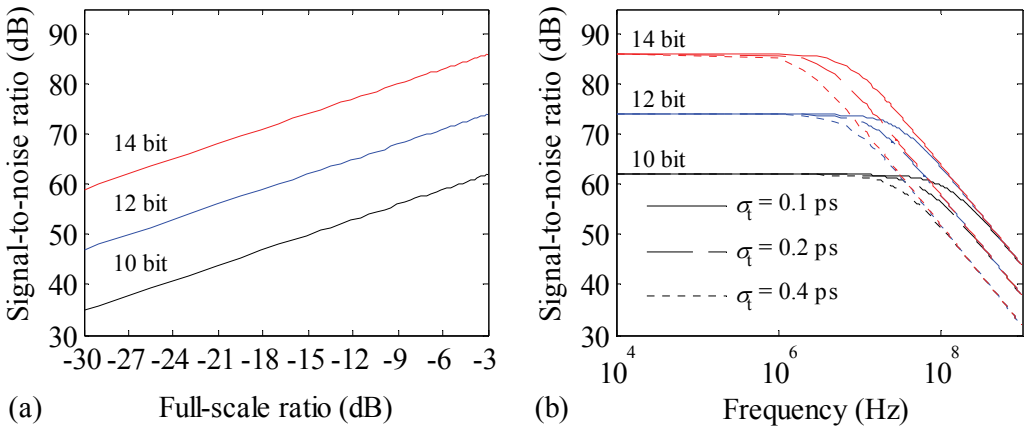

Figure 4-8 Signal-to-noise ratio (a) as a function of the full-scale ratio for different ADC resolutions and (b) as a function of the frequency (semi-logarithm plot) for different ADC resolutions and sampling time jitters at full-scale input amplitude.

is confined to the quantization of the input signal. Assuming a sinusoidal input signal, the signal-to-quantization-noise ratio (in dB) measured over the total Nyquist bandwidth from DC to half of the sampling frequency is $SQNR_{\text{adc}} = 6.02 \cdot p + 4.77 + 20 \cdot \log(FSR)$, where p in bit is the resolution of the ADC and FSR the ratio between the root-mean-square value of the input signal and the ADC's maximum input peak voltage [148]. Figure 4-8a plots simulated values of $SQNR_{\text{adc}}$ for various p values as a function of the input signal level and reveals a significant degradation of the theoretical maximum level with decreasing input amplitude level.

The signal-to-noise ratio of an ADC, however, is not only limited by the quantization but also by the sampling time jitter (also termed as aperture or sampling-time uncertainty), σ_{t}, [152] [153]. Sampling time jitter produces a random variation of the sample-to-sample time, leading directly to errors in the accuracy of the instantaneous signal amplitude converted. Jitter in the time domain is equivalent to phase noise in the frequency domain. It appears as wideband noise on the sampling clock and therefore degrades the noise floor performance of the ADC. In general, the sampling time jitter is the root sum square $\sigma_{\text{t}}^2 = \sigma_{\text{clk}}^2 + \sigma_{\text{aperture}}^2$ of the root-mean-square jitter of the sampling clock, σ_{clk}, and the intrinsic root-mean-square aperture jitter, σ_{aperture}, of the particular ADC.

Assuming an ADC without quantization noise, the theoretical maximum signal-to-noise ratio attributed to sampling-time jitter is given by $SNR_{\text{jitter}} = 20 \cdot \log\left(2\pi \cdot f_{\text{i}} \cdot \sigma_{\text{t}}\right)^{-1}$ where f_{i} is the input signal frequency of the ADC [154]. Evidently, SNR_{jitter} is dependent on the input frequency and independent of the sampling frequency. Because the quantization noise and the error due to the sampling time jitter are statistically independent, they can be added to obtain the total signal-to-noise ratio, SNR_{adc}, (4.13) [155]. As shown in Figure 4-8b, the required

1 GHz system bandwidth of the RFISA electronics system significantly deteriorates the total signal-to-noise ratio of the ADC and decreases therefore its effective resolution as well.

$$SNR_{\text{adc}} = 10 \cdot \log\left(\left(\frac{1}{10^{\frac{SQNR_{\text{adc}}}{10}}} + \frac{1}{10^{\frac{SNR_{\text{jitter}}}{10}}} \right)^{-1} \right) \tag{4.13}$$

The noise contribution of the individual analog components in front of the ADC is defined by their corresponding noise factor $F = SNR_{\text{i}} / SNR_{\text{o}}$, where SNR_{i} is the input signal-to-noise ratio due to thermal noise and SNR_{o} is the component output signal-to-noise ratio [99] [156]. The noise figure is a measure of how much the signal-to-noise ratio degrades as the signal passes through the component. The F values of active components are usually supplied by the manufacturers, given as noise figure $NF = 10 \cdot \log F$ in dB. In the case of passive components, the F value equals the loss of the passive components. The cascaded noise figure in dB of all components of the analog front-end is given by [157]

$$NF_{\text{total}} = 10 \cdot \log\left(F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \ldots \right) = 10 \cdot \log\left(1 + \sum_{i=1}^{n} \frac{(F_i - 1)}{\prod_{j=0}^{i-1} G_j} \right) \tag{4.14}$$

where F_i represents F at the ith component ($i \in \mathbb{N}$), G_j represents the gain at the jth component ($j \in \mathbb{N}$), and $n \in \mathbb{N}$ represents the overall number of components. It is apparent from (4.14) that the first component dominates the total noise figure. In order to keep the total noise floor of the components of the analog front-end below the ADC noise level, it is necessary to maintain

$$-N_0 - NF_{\text{total}} - 10 \cdot \log(B_{\text{rfisa}} / 1\text{Hz}) > SNR_{\text{adc}} \tag{4.15}$$

where $N_0 = -174\,\text{dBm/Hz}$ is the source thermal noise floor normalized to 1 Hz bandwidth at room temperature of 290 K and B_{rfisa} is system bandwidth of the RFISA electronics [99]. Evidently, solus the wide RFISA system bandwidth of $B_{\text{rfisa}} = 10^9$ Hz critically deteriorates the noise floor by 90 dBm.

4.2.3 Digital signal processing methods for parameter estimation of sampled sinusoidal waveforms

Obvious from the principle of the direct-sampling technique, a frequency-selective DSP algorithm is needed, which properly estimates the vector parameters, namely the magnitude and phase or the real and imaginary components, from the samples of the sinusoidal input signal recorded. The discrete-time (sampled) sequence of the sinusoidal input signal can be represented by $s_{\mathrm{a,b}}[n] = R\sin(2\pi f_{\mathrm{o}} n t_{\mathrm{s}} + \phi) + G$, where R is the amplitude, f_{o} the signal frequency, $t_{\mathrm{s}} = f_{\mathrm{s}}^{-1}$ the sampling time, f_{s} the sampling frequency, ϕ the phase, G the DC component, and $n \in \mathbb{N}$ the discrete-time index. In principle, the vector parameters of $s_{\mathrm{a,b}}[n]$ can be obtained by frequency-domain data analysis or time-domain data analysis [158].

Frequency-domain data analysis

Frequency-domain analysis of a record of sampled sinusoidal waveform data is generally based on the Discrete Fourier Transform (DFT) [109]. The DFT is a mathematical algorithm used to determine the frequency (spectral) content of a discrete signal sequence by translating the amplitude data recorded (sampled) in the time domain into amplitude data as function of frequency in the frequency domain. Because of the periodic nature of the DFT, performing the DFT assumes that the record of the sampled data repeats exactly with a period of $J \cdot t_{\mathrm{s}}$ where $J \in \mathbb{N}$ is the total number of samples. This presupposes coherent sampling, which is defined by $J \cdot f_{\mathrm{o}} = M \cdot f_{\mathrm{s}}$ where $M \in \mathbb{N}$ is the integer number of cycles of the input signal in the data record period $J \cdot t_{\mathrm{s}}$. Coherent sampling provides a DFT spectrum that exhibits only frequency lines corresponding to the input frequency f_{o} and their harmonics. However, whenever the record of the sampled data is captured by non-coherent sampling, the first and the last sample in the record are discontinuous to one another. This spreads the energy of a spectral line over the whole range of frequencies (spectral leakage) and distorts the estimation of the corresponding vector parameters [159] [160].

In order to minimize the spectral leakage, specific windowing weighting functions in the time domain prior to performing the DFT are generally applied. A comprehensive overview of different types of time window functions can be found in [109] [161]. Windowing the input data is equivalent to convolving the spectrum of the original signal with the spectrum of the window. The DFT spectrum of the discrete signal sequence can be obtained from a set of complex exponentials — exponential form —

$$S_{\mathrm{a,b}}[k] = \sum_{n=0}^{J-1} s_{\mathrm{a,b}}[n] \cdot w[n] \cdot e^{-\mathrm{j}2\pi nk/J} \quad 0 \le k \le J-1 \tag{4.16}$$

or, equivalently, with Euler's relationship $e^{-\mathrm{j}\phi} = \cos(\phi) - \mathrm{j}\sin(\phi)$ from a set of complete orthonormal basis functions — rectangular form —

$$S_{\mathrm{a,b}}[k] = \sum_{n=0}^{J-1} s_{\mathrm{a,b}}[n] \cdot w[n] \cdot \left(\cos\left(2\pi nk/J\right) - \mathrm{j}\cdot\sin\left(2\pi nk/J\right)\right) \quad 0 \le k \le J-1 \tag{4.17}$$

where, $J \in \mathbb{N}$ is the total number of samples, $n \in \mathbb{N}$ the discrete time-domain index, $k \in \mathbb{N}$ the discrete frequency-domain index of the DFT output, and $w[n]$ represents the particular discrete windowing function.

The DFT algorithm in (4.16) produces the associated frequency domain (spectrum) representation of $s_{\mathrm{a,b}}[n]$ by forming a weighted sum of complex exponential functions with the complex amplitude and phase as weighting terms at each frequency, allowing for analysis of the amplitude and phase spectrum of $s_{\mathrm{a,b}}[n]$. The rectangular form of the DFT (4.17) yields the respective spectra for the real and imaginary components of $s_{\mathrm{a,b}}[n]$. In contrast to the conventional application of the DFT algorithm, the vector parameter of $s_{\mathrm{a,b}}[n]$ can frequency-selectively be extracted at a single frequency, namely at the known stimulus frequency f_{o} generated by the RFISA synthesizer unit, rather than for the complete spectrum. This single-point DFT decreases the discrete frequency-domain index to $k = 1$ in (4.16) and (4.17), simplifying the computation complexity of the DFT considerably.

Time-domain data analysis

Time-domain analysis of a record of sampled sinusoidal data is based on sine-wave curve fitting (SFIT) algorithm that is commonly used in ADC testing [158] [162] and specified in the IEEE-Standard-1057 [163]. The standard provides algorithms for both three-parameter estimation (amplitude, phase, and DC offset) at known signal frequency and four-parameter estimation (amplitude, phase, DC offset, and signal frequency) for unknown signal frequency. Since the frequency f_{o} of the discrete-time sequence $s_{\mathrm{a,b}}[n]$ is known, the SFIT method can be reduced to three-parameter estimation.

In principle, the SFIT algorithm (4.18) best fits the recorded samples with a sine-wave model $R\sin(\alpha+\phi)+G = A\cos(\alpha)+B\sin(\alpha)+G$ by determining the function parameters (amplitude $A = R\sin(\phi)$, amplitude $B = R\cos(\phi)$, and DC-component G) that minimize the least square error, ε, between the recorded samples and the generic analytical formula of the sinusoidal waveform.

$$\sum_{n=1}^{J}\left(s_{\mathrm{a,b}}[n] - A_{\mathrm{a,b}}\cos\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) - B_{\mathrm{a,b}}\sin\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) - G_{\mathrm{a,b}}\right)^2 = \varepsilon \to \min . \tag{4.18}$$

In order to estimate the target parameter $A_{a,b}$, $B_{a,b}$, and $G_{a,b}$, the least-squares solution

$$\mathbf{x} = \left(\mathbf{D}^{T}\mathbf{D}\right)^{-1}\left(\mathbf{D}^{T}\mathbf{y}\right) \tag{4.19}$$

that minimizes (4.18) must be computed, where ^{T} denotes transpose, $\mathbf{x} = \begin{bmatrix} A & B & G \end{bmatrix}^{T}$ is the vector of the estimated parameter, $\mathbf{D}$ the matrix (4.20) that linearly relates the estimated parameters and the vector $\mathbf{y} = \begin{bmatrix} s_{a,b}(1) & s_{a,b}(2) & .. & s_{a,b}(J) \end{bmatrix}^{T}$ represents the data record [164].

$$\mathbf{D} = \begin{bmatrix} \cos(2\pi f 1 t_s) & \sin(2\pi f 1 t_s) & 1 \\ \cos(2\pi f 2 t_s) & \sin(2\pi f 2 t_s) & 1 \\ \vdots & \vdots & \vdots \\ \cos(2\pi f J t_s) & \sin(2\pi f J t_s) & 1 \end{bmatrix} \tag{4.20}$$

For computed values of $A_{a,b}$ and $B_{a,b}$, the corresponding vector parameters magnitude $R_{a,b} = \sqrt{A_{a,b}^{2} + B_{a,b}^{2}}$ and phase $\phi = \arctan(A/B)$ of the recorded signals $s_{a,b}$ and their complex representation in rectangular form $s_{a,b} = V_{a,b}(j\omega) = B_{a,b}(\omega) + jA_{a,b}(\omega)$ may be found. In contrast to the single-point DFT, the estimated parameter for magnitude and phase are not influenced by signal offsets because the corresponding DC-component *G* is determined separately and can therefore be discarded.

Comparison between DFT and SFIT

The DFT (with and without windowing) and the SFIT are widely used in the application of ADC testing and, thus, several comparative studies have been presented in the last decade [158] [165] [166]. The studies were focused on algorithm accuracy, noise performance, and DSP implementation as the final purpose. In principle, the single-point DFT and the SFIT algorithm act as a very narrow band-pass filter centered on the signal frequency. This allows for high frequency selectivity, sufficient noise suppression, and robustness to make types of harmonic errors caused by nonlinearities of the analog front-end design negligible.

The single-point DFT without windowing and the three-parameter SFIT exhibit very good agreement under coherent sampling conditions (see Figure 4-9a), because both methods are equivalent in this case. Unfortunately, in the wideband application of the RFISA electronics system, the conditions for coherent sampling are difficult to achieve and non-coherent sampling is the general case. As shown in Figure 4-9b, the sensitivity of the single-point DFT under non-coherent sampling conditions is substantially higher and implementation of an appropriate window function is essential. However, different window functions support different applications and choosing an appropriate window function and the specific coefficients is challenging [167]. Generally, window functions with narrow main lobe will have enhanced

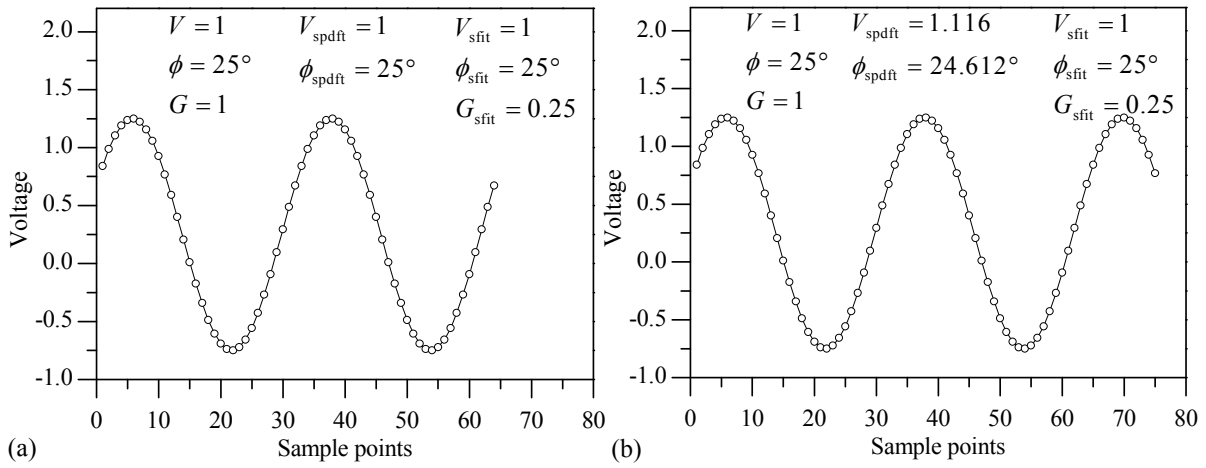

Figure 4-9 Representation of (a) coherent sampling and (b) non-coherent sampling. The sine-wave parameters, which are estimated using the single-point DFT without windowing (index spdft) and the sine-wave fitting method (index sfit), are presented in the respective plots. The default values are labeled without index. Obviously, the single-point DFT without windowing exhibits significant parameter variances under non-coherent sampling conditions.

frequency selectively, but usually at the expense of high side lobes that cause lower overall noise attenuation.

Although windowed single-point DFT and three-parameter SFIT, in general, show good agreement under non-coherent sampling conditions, it is reported in [166] that a slightly better performance can be obtained with the three-parameter SFIT, which, in statistical terms, provide minimum variance linear estimators for the desired vector parameter (amplitude and phase) of sampled sinusoidal signals.

Furthermore, it is reported in [168] that windowing generally tends to increase the sensitivity to noise and worsens therefore the variance of the estimated parameters. The slightly better performance of the SFIT method, however, is attained at the expanse of increased complexity of the algorithm compared to the simpler DSP implementation of the single-point DFT with windowing. The accuracy of both methods is directly affected by the total number of samples recorded, in particular in the presence of high noise levels [158]. Consequently, a DSP implementation with scalable number of samples is aspired in order to achieve adequate noise insensitivity. However, if the single-point DFT method is applied with variable number of samples, different sets of window coefficients must be pre-calculated and on-board stored. This decreases the flexibility of the particular DSP implementation significantly, in particular for stand-alone operation in the specific sensor application. In the case of the three-parameter SFIT, as shown in Figure 4-10, the noise insensitivity improves greatly as the number of samples is increased without changing the DSP implementation.

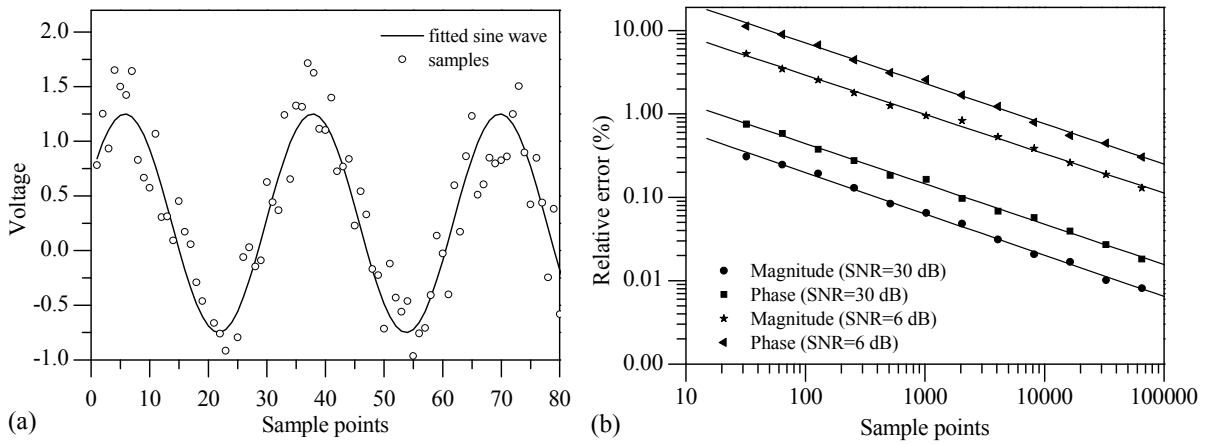

Figure 4-10 Figure (a) shows an example of non-coherent sampled values impaired by randomized amplitude noise (average signal-to-noise ratio is 6dB) and the fitted sine-wave curve. Figure (b) represents the relative error (with respect to the default values in Figure 4-9) of the sine-wave parameter magnitude and phase as function of the number of sample points for the non-coherent sampled sine-wave in plot (a). The parameters are estimated by the sine-wave fitting method for different signal-to-noise ratios. The noise values are chosen in accordance to the ADC's signal-to-noise deterioration shown in Figure 4-8.

4.2.4 Conclusions for the design of the wideband digital vector voltmeter

Accuracy and precision of the impedance spectroscopy data are directly affected by both the analog circuit design and the applied data processing algorithm of the RFISA digital vector voltmeter. The aim of the previous sections was therefore to evaluate critical design parameters for the wideband RFISA digital vector voltmeter unit.

Based on the main objective of minimizing the overall circuitry of the RFISA electronics system, the proposed direct-sampling topology is preferred because it considerably reduces the quantity of the analog components and offers the most flexibility. However, due to the direct sampling of the input signals, the ADC must process the complete RFISA system bandwidth of 1 GHz and sufficient noise suppression by an anti-aliasing filter in front of the ADC is not feasible. Moreover, it was shown that, in particular, the wide RFISA system bandwidth critically impairs the noise floor of the analog front-end. Coherent sampling is usually essential to attain minimum variance of parameter estimation by the particular DSP algorithm. The condition for coherent sampling, however, demands exact frequency adjustment of the sampling clock f_s with respect to the instantaneous signal frequency f_o. With regard to the main objective of minimizing the circuitry of the RFISA electronics system, coherent sampling is not feasible for a wideband-tuning application with arbitrary fine frequency resolution.

Summarizing, two conclusions are essential for the circuit design of an appropriate direct-sampling analog-front end with 1 GHz bandwidth for the digital vector voltmeter unit:

(1) In order to attain high signal-to-noise ratio of a given ADC, low-jitter sampling-clock generation and gain control to adjust the level of the input signal with respect to ADC's full-scale level are mandatory. Adequate gain control and sampling-clock generation, however, increases the circuitry of the analog front-end design. In spite of this extra circuitry, a minimum number of analog components must be aspired in order to avoid additional noise contamination and to maintain the noise level of the analog front-end below the signal-to-noise ratio of the ADC.
(2) Due to the decreased signal-to-noise ratio at high frequencies caused by the inevitable sample clock jitter and the 1 GHz system bandwidth of the analog front-end design, adequate noise insensitivity of the subsequent DSP algorithm under coherent and non-coherent sampling conditions is required. Therefore, in spite of the increased complexity of the DSP algorithm, the sine-wave fitting is preferred because it offers better impact on the noise suppression by simple adjustment of the total number of samples. This allows for changing easily between very fast measurements (small number of sample points) and very precise measurement (large number of sample points) without the need for modification of the particular DSP implementation.

Although the technical advances in the analog/digital circuit technology in the last decade have significantly increased the clock speed of available ADC-ICs, it is still impossible to employ an ADC that features all: high resolution, high analog input bandwidth of at least 1 GHz, and clock frequencies far above 2 GHz in order to avoid aliasing. Hence, with the application of the RFISA electronics system for broadband impedance spectroscopy up to 1 GHz, undersampling of the signals that must be recorded is inevitable. However, since both the input signal frequency f_o and the sampling frequency f_s are always known, the aliasing frequencies $|nf_s \pm f_o|$, where $n \in \mathbb{N}$, are known as well, allowing for correct application of the SFIT algorithm even when undersampling conditions occur.

Chapter 5
The electronics system

The following chapter describes the hardware of the developed RFISA electronics system in detail. With regard to the conclusions presented in the previous chapter, the concept of the overall system design is introduced. Subsequently, the hardware design of the primary units is comprehensively described. The design process was essentially determined by the electronic components because they impose the most constraints on the configuration of the circuitry. Based on the specifications of the key analog devices, the configuration of the circuit design is described. Compact microstrip filter designs are presented, which exhibit steep roll-off and attenuation characteristics while maintaining a minimal geometry for small-sized implementation on the printed circuit board. With regard to the primary application of resonant microsensors and capacitive sensor probes, various sensor interface electronics are described.

5.1 Overview of the electronics concept

The principle of impedance spectrum analysis described in section 2.1 requires a sophisticated electronics system design to ensure accurate measurements over the broad frequency range from 10 kHz to 1 GHz. The overall configuration of the RFISA electronics system is shown in Figure 5-1 and comprises seven internal system units:

(1) the wideband frequency synthesizer (SYN) unit,
(2) the wideband direct-sampling digital vector voltmeter (DVVM) unit,
(3) the sensor interface (SENSINT) unit,
(4) the clock synthesizer (CLKSYN), unit
(5) the processor (PRO) unit,
(6) the temperature measurement unit (TEMP), and
(7) the DC power supply (PWRSUP) unit.

In addition to the basic operation for impedance spectrum analysis, which is accomplished by (1) and (2), the functionality of the RFISA electronics is extended by a precision temperature measurement of the target media. This is necessary to take into account the influence of the medium temperature on the sensor response. The principle of measurement is based on conventional platinum temperature (PT1000) sensors connectable inside the specific sensor probe in 2-wire or 4-wire configuration. Hence, precession temperature measurements close to the

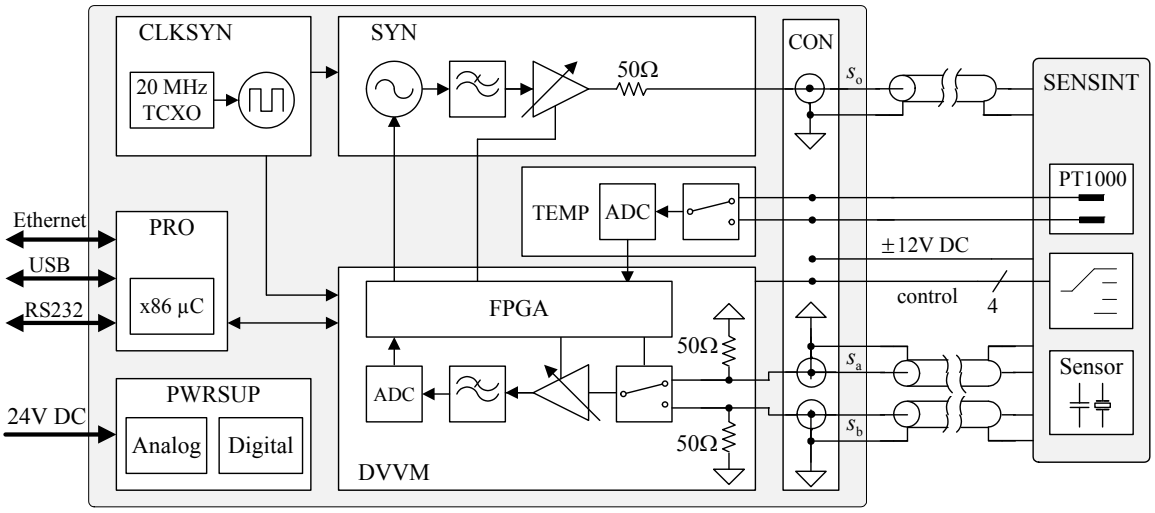

Figure 5-1 Overview of the RFISA electronics system.

sensor device can be achieved. Since the internal system units have to be individually clocked with high frequencies, a precision clock synthesizer unit is also implemented to attain enhanced clock distribution with low jitter performance.

The processor unit includes a powerful 32-bit single-board computer and allows stand-alone operation of the RFISA electronics system for extensive data evaluation and process controlling in both laboratory and industrial applications. It also provides the interface to external system components such as a personal computer or an LCD-module (liquid crystal display) for data visualization. The DC power supply unit, which is separated into analog and digital power supply, provides the management and distribution of the DC power for the different sections of the RFISA electronics system. Finally, the internal system units are parallel controlled by the field-programmable gate array logic (FPGA). In addition, the high-speed digital signal processing for the sine-wave fitting computation of the signals recorded is also accomplished by the FPGA.

The input and output ports of the RFISA electronics includes precision coaxial jacks of $50\,\Omega$ characteristic impedance to allow matching to the characteristic impedance of standard coaxial cables. In order to ensure optimum operation at high frequency, the characteristic impedance (system impedance) of the RFISA electronic is specified with $Z_0 = 50\,\Omega$, too. Beside the three coaxial jacks, the connector (CON) between the RFISA main electronics and the separate SENSINT includes: ± 12 V analog power supply lines, 4 digital control lines, and signal lines for two PT1000 sensors.

The following sections describe the design of the primary system units of the RFISA electronics system (SYN, DVVM, CLKSYN, PRO, SENSINT) in some detail. A complete description of the SYN and DVVM hardware design can be found in [169].

5.2 Frequency synthesizer unit

As introduced in section 3.6, the necessary hybrid architecture of the wideband synthesizer unit contains three basic stages: (1) the frequency-fixed RF-PLL; (2) the tunable DDFS-driven LO-PLL; and (3) the IF output stage (IF-OUT). Beside these basic parts, an automatic level control (ALC) loop was implemented to adjust and control the output source power by an analog-controlled variable-gain amplifier (VGA). Furthermore, in order to avoid that the settling time of the frequency slows the measurement rate of the RFISA electronics system down, the synthesizer unit was primarily designed with regard to fast frequency-hopping and compact circuit design, in compromise with sufficient suppression of spurious signals and phase noise. The configuration and, thus, the primary circuitry of the developed synthesizer architecture depicted in Figure 5-2 are directly linked to the available components and their given specifications. The key components are listed in Appendix A2.

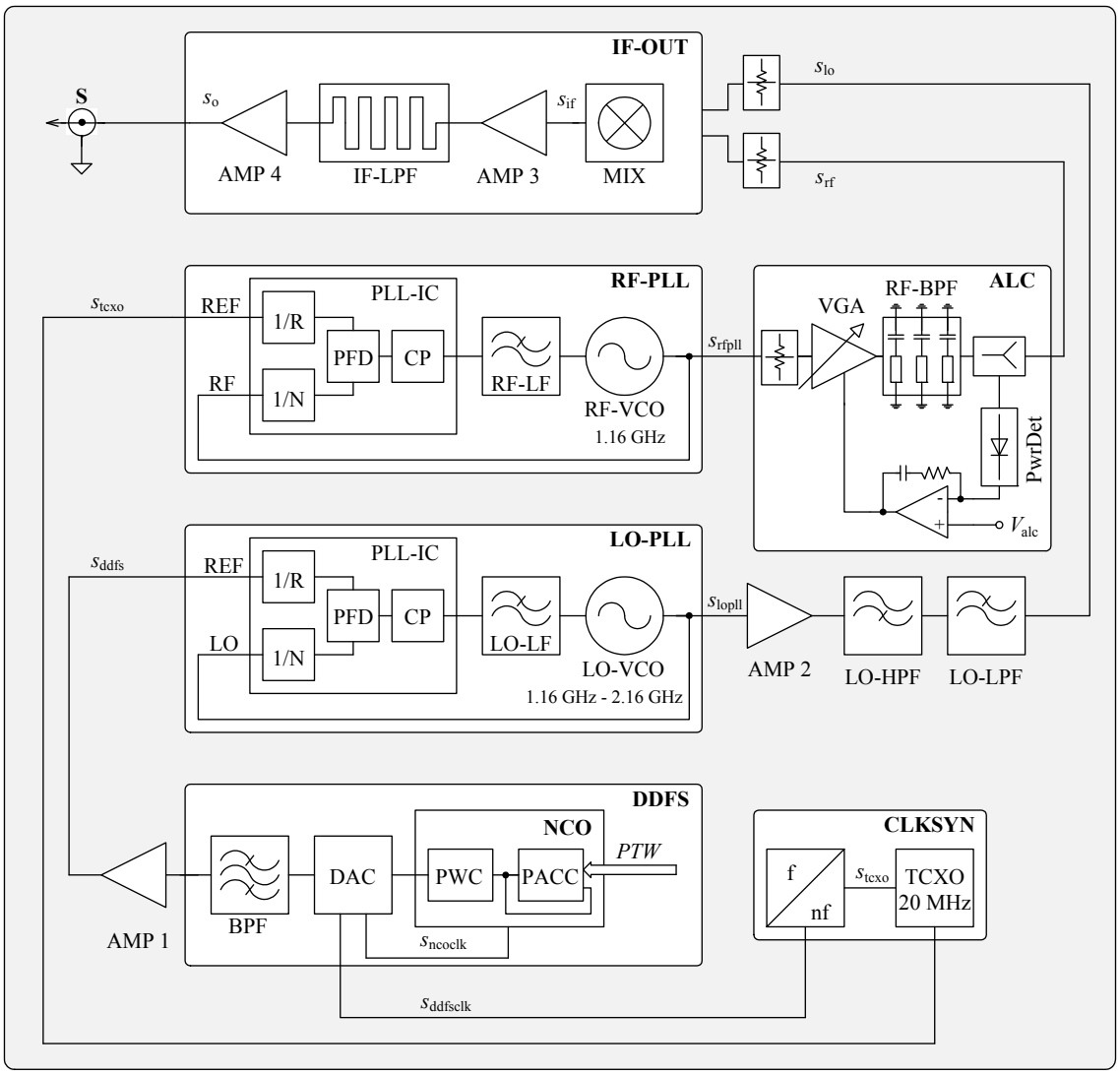

Figure 5-2 Topology of the RFISA synthesizer unit.

The system master clock signal , s_{tcxo} , of the entire RFISA electronics is sourced from a high quality temperature controlled crystal oscillator (TCXO) that offers a 20 MHz square-wave frequency reference, f_{tcxo} , with low phase noise and high frequency stability. The two PLL-IC are based on conventional charge-pump phase lock technique. Subsequent to the LO-PLL, the low-pass filter (LO-LPF) and the high-pass filter (LO-HPF) are ceramic filters and comprise a band-pass characteristic together. The band-pass filter (RF-BPF) following the RF-PLL and the low-pass filter (IF-LPF) on the intermediate output of the mixer are self-designed filter structures based on microstrip geometries.

The amplifiers (AMP 1 – 4) are based on a monolithic amplifier offering fixed gain of 18 dB, wideband operation up to 4 GHz, internal $50\,\Omega$ input and output matching, and low noise figure of 4 dB. The VGA is a high performance voltage-controlled gain amplifier/attenuator offering a linear-in-dB gain control function, a wide gain-control range of 56 dB (adjustable from -34 dB up to +22 dB), and a frequency range up to 3 GHz. It provides adequate gain to cover the gain range of 35 dB in order to adjust the output power level of the RFISA electronics within the specification given in section 1.4.

In order to achieve the desired output frequency coverage with the application of frequency down-conversion, a wideband VCO (LO-VCO) that exhibits a tuning range of 1 GHz was chosen for the LO-PLL stage. The given frequency tuning range (specified in the data sheet) determines the entire design of the RFISA synthesizer unit. The minimum frequency of the LO-VCO specified the fixed frequency of the RF-VCO at

$$f_{\text{rfpll}} = 1.16\,\text{GHz} \tag{5.1}$$

and the tuning bounds of the LO-PLL at

$$1.16001\,\text{GHz} \le f_{\text{lopll}} \le 2.16\,\text{GHz}\,. \tag{5.2}$$

By application of (3.3), the desired output frequency range after mixing and filtering is

$$10\,\text{kHz} \le f_{\text{o}} \le 1\,\text{GHz}\,. \tag{5.3}$$

The tuning bounds of the LO-PLL, namely $f_{\text{lopll,min}} = 1.16001\,\text{GHz}$ and $f_{\text{lopll,max}} = 2.16\,\text{GHz}$, inevitably determines the design of the loop and, thus, the specification of the DDFS, too.

In order to achieve the required low value of the feedback divider of the DDFS-driven LO-PLL (see section 4.1.4), the phase detector frequency of the corresponding PLL-IC has to be chosen as high as feasible. Since the maximum phase detector frequency, $f_{\text{pd,max}}$, of the

PLL-IC is restricted to 104 MHz, the minimum value of the LO-PLL feedback divider is assessed at $\lfloor f_{\mathrm{lopll,max}} / f_{\mathrm{pd,max}} \rfloor = 21$ where $\lfloor \ \rfloor$ denotes truncation to integer. However, to allow practical utilizing of the divider ratio for computation by FPGA, the value of the LO-PLL feedback divider was chosen at a power-of-two

$$N_{\mathrm{lopll}} = 32 . \tag{5.4}$$

Consequently, N_{lopll} dictates the output frequency range of the DDFS at

$$\begin{aligned} f_{\mathrm{ddfs,min}} &= f_{\mathrm{lopll,min}} / N_{\mathrm{lopll}} = 36.25\,\mathrm{MHz} \\ f_{\mathrm{ddfs,max}} &= f_{\mathrm{lopll,max}} / N_{\mathrm{lopll}} = 67.5\,\mathrm{MHz} \end{aligned} \tag{5.5}$$

and, in addition, the signal-to-noise ratio (4.11) and the spurious-free dynamic range (4.12) close-to-carrier ($f_{\mathrm{ddfs}} \pm B_{\mathrm{lopll}}$, where B_{lopll} is the respective LO-PLL loop bandwidth) at

$$\begin{aligned} SNR_{\mathrm{ddfs}} &\geq 90\ \mathrm{dB} \\ SFDR_{\mathrm{ddfs}} &\geq 70\ \mathrm{dBc} \end{aligned} . \tag{5.6}$$

Hence, a commercially available DDFS-IC offering both a sampling-clock frequency of at least 150 MHz and according to (4.8) an amplitude resolution of at least 15 bit is required. Although modern DDFS-ICs, which exhibit sampling-clock capabilities up to 1 GHz, usually exceeds the demand on the sampling-clock frequency, their amplitude resolution is currently limited to 14 bits. Utilizing (4.8), this theoretically yields $SNR = 86.04\,\mathrm{dB}$, which falls below the critical lower bound specified in (5.6). Hence, the implementation of the DDFS had to be separated into two parts where the numerical controlled oscillator (NCO) core is implemented into FPGA and the digital-to-analog conversion is carried out by a separate high performance DAC. A DAC device offering an amplitude resolution of $d = 16\,\mathrm{bit}$, which theoretically yield $SNR = 98.08\,\mathrm{dB}$, and a sampling-clock capability up to 400 MHz was chosen.

Furthermore, separation of the DDFS topology allows advantageously for having impact on both the frequency resolution of the entire DDFS stage and the spurious performance of the NCO core. The frequency resolution of LO-PLL and thus the frequency resolution of the DDFS determine the overall frequency resolution of the RFISA synthesizer unit. Hence, adequate resolution of the phase accumulator in the NCO design is essential to provide not only a wide output frequency range of the synthesizer unit but also very fine frequency resolution. With the specified frequency resolution of $\Delta f_{\mathrm{o,min}} = 0.1\,\mathrm{Hz}$, the LO-PLL reference divider value of $R_{\mathrm{lopll}} = 1$, and the DDFS sampling-clock frequency of $f_{\mathrm{ddfsclk}} = 400\,\mathrm{MHz}$, rearranging of (3.8) yields a minimum phase accumulator resolution given by

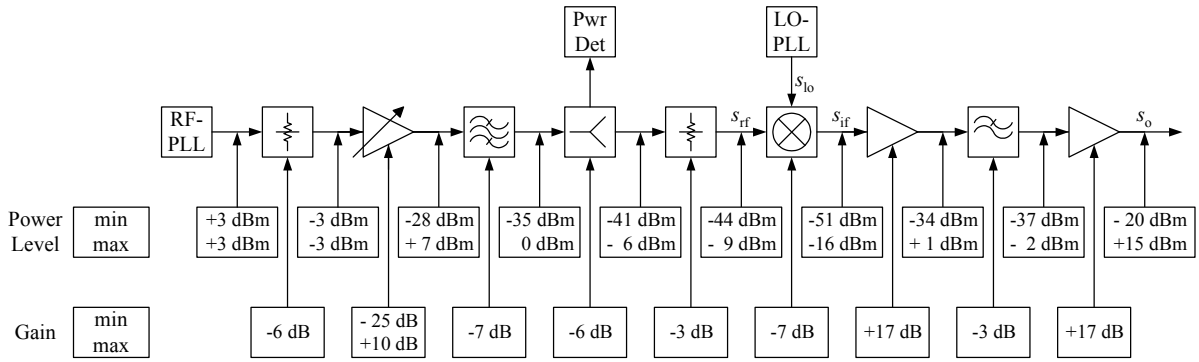

Figure 5-3 Power level estimation of the RFISA synthesizer unit.

$$r_{\min} = 37\,\text{bit}\,. \tag{5.7}$$

Finally, to meet the pretension for fast impedance spectrum analysis, the settling time of the RFISA synthesizer unit must significantly be less than the upper limit of the measurement period specified in section 1.4. The settling time is therefore specified at

$$t_{\text{set}} \leq 10\,\mu\text{s}\,. \tag{5.8}$$

The automatic level control (ALC) loop of the synthesizer unit was primarily employed to ensure that the power level of the sensor's excitation signal s_o is almost steady over the wide frequency tuning range. In addition, the level control loop allows also for an adjustable power level depending on the specific sensor and sensor interface electronics. Generally, ALC loops comprise a conventional feedback loop and are therefore subjected to the principles of the basic control theory. Hence, analog to phase locked loops, the settling time of the ALC loop is inversely proportional to the loop bandwidth. The loop bandwidth must be reduced to ensure sufficient ripple filtering and stability of the loop. Consequently, as shown in Figure 5-2 the ALC loop was embedded into the mixer's RF-input path, s_{rf}, in order to control the power level of the signal that is frequency down-converted. This allows an appropriate ALC loop design at the fixed, high frequency at 1.16 GHz. In order to specify the required VGA gain range, estimation of the power level of the gain and attenuator components in the RFISA synthesizer unit is essential. Apparently from Figure 5-3, setting the output power level of the RFISA synthesizer unit in the desired power range from -20 dBm to +15 dBm requires an adjustment of the VGA gain in the range of $-22\,\text{dB} \leq G_{\text{vga}} \leq +13\,\text{dB}$. The circuit design of the ALC loop is shwon in Appendix A3. Detailed description of the circuit configuration can be found in [169].

Based on the specifications given before, the configuration of the critical circuit designs for the DDFS, the PLLs, and the IF-OUT of the synthesizer will be described in the following.

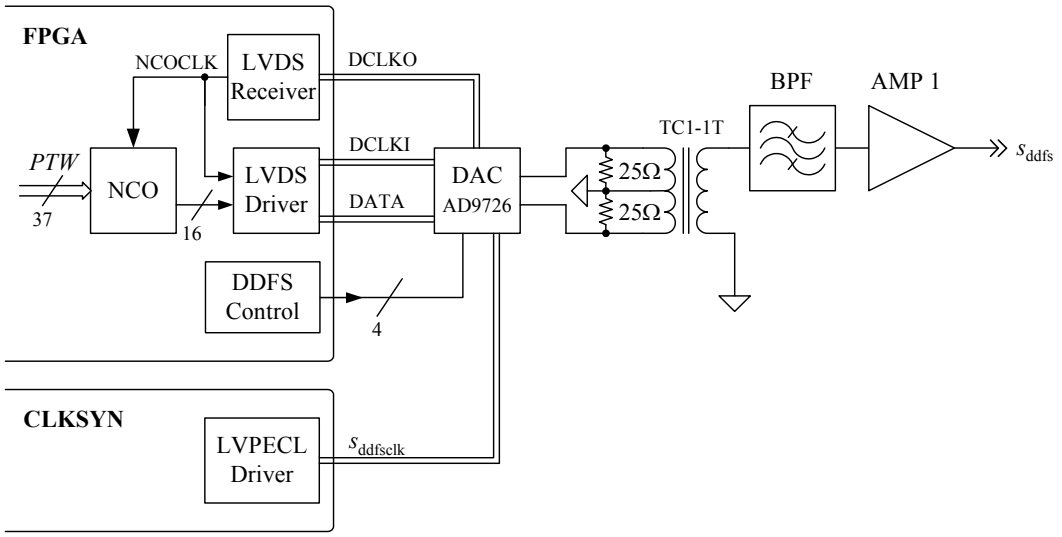

Figure 5-4 Analog signal conditioning of the direct digital frequency synthesizer stage.

5.2.1 Design of the DDFS stage

The design of the DDFS stage is depicted in Figure 5-4 and comprises the NCO core implemented in FPGA, the separate 16-bit DAC, the band-pass reconstruction filter (BPF), and the fixed gain amplifier (AMP 1). According to (5.6), the efforts of the DDFS circuit design were focused on a spurious-free-dynamic range of $SFDR_{\mathrm{ddfs}} \geq 70\,\mathrm{dBc}$ and a signal-to-noise ratio of $SNR_{\mathrm{ddfs}} \geq 90\,\mathrm{dB}$ within the close-to-carrier bandwidth of $\left| f_{\mathrm{ddfs}} \pm B_{\mathrm{lopll}} \right|$. The requirements must be met for all DDFS output signals, which will be generated in the specified tuning range of 36.25 MHz – 67.5 MHz.

The configuration of the NCO design depicted in Figure 3-4 is determined by the specified minimum resolution of the phase accumulator $r_{\mathrm{min}} = 37\,\mathrm{bit}$ according to (5.7) and the amplitude resolution of the employed DAC $d = 16\,\mathrm{bit}$. Latter also specifies the output amplitude resolution of the phase-to-waveform converter (PWC) in the NCO design. Obviously, the required values of r_{min} and d entail a PWC memory size of $2^r \times d$, which would consume too much logic resource for a practicable implementation of the NCO core into FPGA. Consequently, as described in section 4.1.2 truncation of the phase sequence $\theta[n]$, which is generated by the phase accumulator, is inevitable to maintain the memory capacity to a reasonable size. According to (4.9), $w \geq 18$ most significant bits out of all r phase word bits must be retained to keep the discrete phase truncation spurs lower than the background noise floor caused by the amplitude quantization. However, even if the quarter wave symmetry of the sinusoidal waveform is exploited to store only the sinusoidal waveform information of the first quadrant $[0, \pi/4)$ [134] [170] [171], an input data word size of $w = 18\,\mathrm{bit}$ would impose a memory size of $(2^w \times d)/4 = 1024$ KiBit. This consumes 79% of the total 1296 KiBit block memory resources of the employed Virtex™-4LX25 FPGA device (value is taken from data

sheet). Obviously, this is still too large for a reasonable FPGA implementation, in particular when high-speed clocking operation of the memory resources is required. Consequently, in order to reduce the PWC memory size further, it is necessary to decrease again the retaining bit width w along with the application of an adequate spur reduction technique.

For implementation in FPGA, two commonly used numerical techniques are offered by Xilinx, Inc., which allow for reduction of the power level of the discrete phase truncation spurs: phase dithering [106] [141] and error feed-forward Taylor series correction [172]. In principle, both techniques in different manner substitute memory storage for computational complexity and can therefore be applied to dramatically decrease the PWC memory size. For selection the target implementation design, the spectral output performance of the NCO core with phase dithering and with Taylor series correction were comparatively determined. For this purpose, system modeling based on Matlab/Simulink® from MathWorks, Inc., was applied to simulate and evaluate the spectral performance of the respective NCO implementation. By the aid of the DSP System Generator from Xilinx, Inc., the corresponding VHDL modules were translated into Matlab/Simulink® models, which allow for using the MathWorks model-based design environment Matlab/Simulink®.

The top-level design parameter for both NCO designs were specified with a phase accumulator word size of $r = 37\,\text{bit}$, a PWC output data word size of $d = 16\,\text{bit}$, and clock frequency of $f_{\text{ddfsclk}} = 400\,\text{MHz}$. Furthermore, the Discrete Fourier Transform (DFT) with Hann-Window were applied to compare the spectral performances of the NCO's discrete output sequence $x_{\text{nco}}[n]$. Since the desired number of frequencies given by (5.5) is large, it is inapplicably to simulate all of them. However as mentioned in section 4.1.2, for phase tuning words that have the same value of $\gcd(PTW, 2^b)$, the spurious spectrum due to all NCO's system nonlinearities can be generated from a permutation of a another spectrum. In order to sufficiently evaluate the worst-case spurious contamination within the bandwidth of $\left| f_{\text{ddfs}} \pm B_{\text{lopll}} \right|$, an odd phase tuning word were chosen to obtain the maximum number of spurs $P = 2^r$. An odd phase tuning word produce spurious signals as close as 2^{-r} to the carrier f_{ddfs}. Hence, only one simulation is needed in order to sufficiently determine the close-to-carrier spurious response of the particular NCO design. Using (3.4), $r = 37\,\text{bit}$, and $f_{\text{ddfsclk}} = 400\,\text{MHz}$, the chosen phase tuning word value of $PTW = 17176433527$ yields a NCO frequency of 49.99 MHz.

DFT computation plots for the wideband and narrowband spectral representation are shown in Figure 5-5. The wideband representation is regarded to the bandwidth of the band-pass reconstruction filter, which will be described afterwards, whereas the narrowband representation is regarded to the LO-PLL bandwidth B_{lopll} (see section 5.2.2). Principally, it is obvious from comparing the spectrum plots that both NCO implementations properly maintain the critical

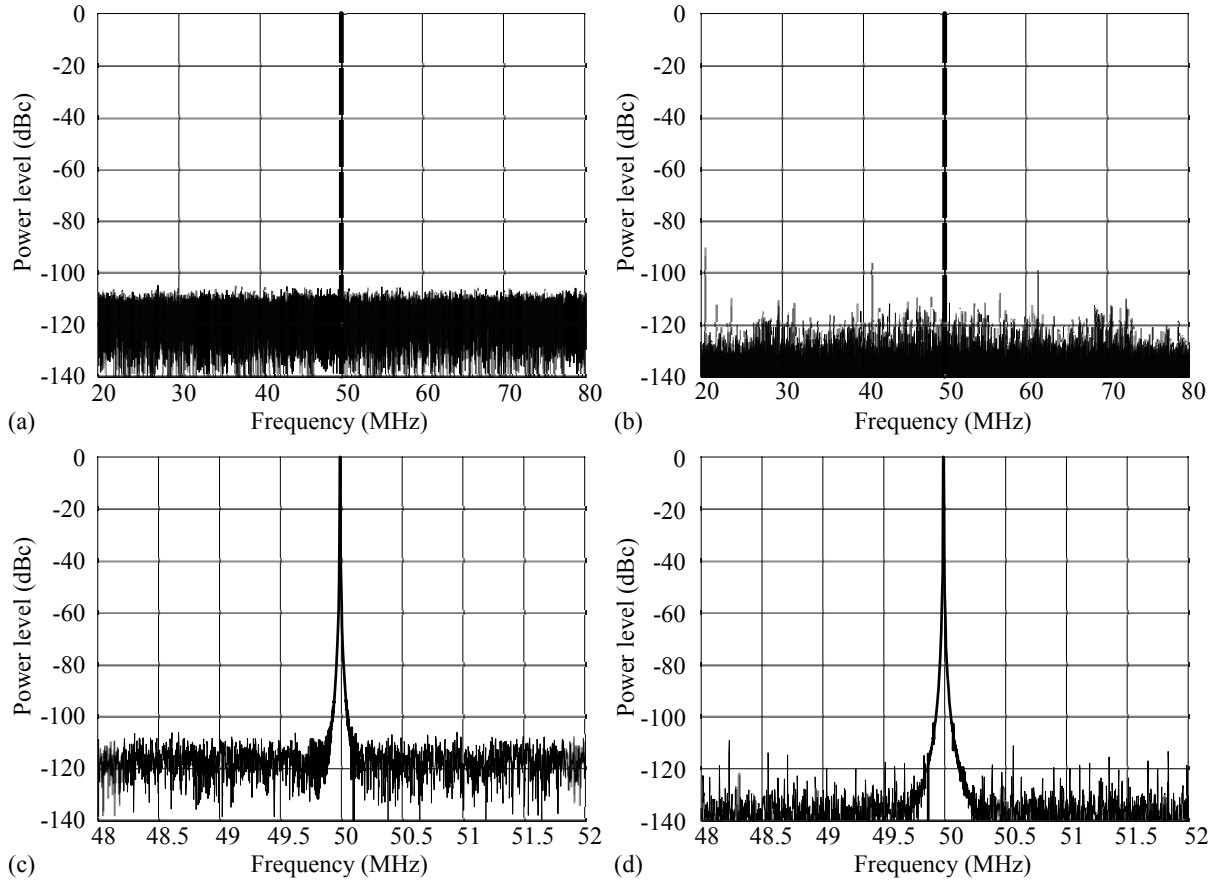

Figure 5-5 Output spectra of the sinusoidal waveform generated by the NCO. Plots (a) and (c) show the wideband and narrowband, respectively, spectral representation of the NCO implementation with phase dithering. Plots (b) and (d) show the wideband and narrowband, respectively, spectral representation of the NCO implementation with Taylor series correction.

SFDR bound (70 dBc). For the phase dithering method, this, however, is at the expense of an increased broadband noise floor because phase dithering spreads the energy of the phase truncation error sequence $e_{\mathrm{PQ}}[n]$ throughout the total Nyquist bandwidth. The NCO implementation with Taylor series correction reveals better background noise performance and, in particular, a better SFDR close to the carrier. However, this is at the expense of some discrete spurious signals that appear evidently. Nevertheless, the power level of these spurious signals is properly below the critical bound of 70 dBc. Hence, due to the better close-to-carrier SFDR performance a NCO design with Taylor series correction was eventually implemented.

As mentioned in 4.1.2, the spectral quality of the DDFS output signal is additionally affected by the performance of the high-speed DAC. It was therefore essential to choose a DAC that provide not only adequate resolution and sampling clock performance but also high linearity to minimize the contamination by distortion. Hence, a 16-bit DAC was chosen that additionally offers an on-chip calibration routine for enhanced dynamic (low-distortion) performance in

the desired frequency range. The on-chip calibration routine is controlled by DDFS Control block in the FPGA. In addition, the DAC uses low voltage differential signaling (LVDS) to perform the high-speed data connection to the FPGA and low-voltage positive emitter-coupled logic (LVPECL) for driving the DAC by the sampling clock, s_{dacclk}. Advantageously, both techniques are low voltage and differential and share therefore the benefits of reduced radiation of electromagnetic interferences caused by the high-speed data transfer. This protects the surrounding analog circuitry against high-frequency disturbances. Since a low-noise, low-jitter sampling clock is essential to achieve maximum performance of the entire DDFS design, the DAC sampling clock is generated by the LVPECL output stage of the clock distribution unit, which will be described in section 5.4. The analog output of the DAC consists of differential (balanced) current sources providing rejection of common-mode signals present on the DAC output. Hence, balanced-to-unbalanced conversion accomplished by the center-trapped transformer (TC1-1T) is required to couple between the balanced DAC output and the unbalanced AMP input.

The wideband fixed gain AMP 1 completes the DDFS stage and provide amplification of the output signal. This is required to drive the LO-PLL with an adequate signal level. The essential reconstruction filter is designed as eight-order elliptic band-pass filter with, in accordance to (5.5), a pass-band range of 25 – 75 MHz and adequate stop-band attenuation of at least -120 dB. Furthermore, in order to accommodate matched source and load impedances, the filter is designed with a characteristic impedance of $50\,\Omega$. The eight-order filter topology presents a reasonable compromise between high stop band attenuation, small transition bandwidth, and still low circuit complexity. Compared to equivalent Butterworth or Bessel filter designs, elliptic filters (also known as Cauer filters) provide steepest transition between pass-band and stop-band. Therefore, it allows for a compact filter design with a very small transition-band [173]. The schematic of the designed BPF and its corresponding frequency response are shown in Figure 5-6.

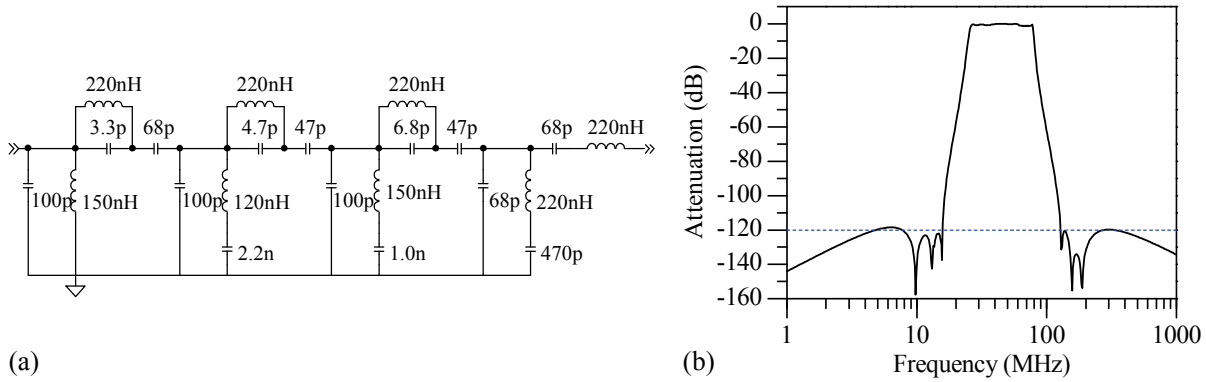

Figure 5-6 Representation of (a) the schematic and (b) the frequency response (semi-logarithmic plot) of the eight-order elliptic band-pass filter.

5.2.2 Design of the PLL stages

Design of the RF-PLL stage

The RF-PLL is attuned to the fixed frequency $f_{\mathrm{rfpll}} = 1.16\,\mathrm{GHz}$ and thus does not affect the settling time of the entire RFISA synthesizer unit. Hence, the loop could be designed to attain minimized phase noise and spurious contamination at the output frequency of the phase-locked RF-VCO. In reference to the explanations in section 4.1.1, the design of the loop filter is the most critical part of the RF-PLL stage in order to gain good spectral quality of the RF-PLL output frequency.

Figure 5-7 shows the schematic of the passive loop filter that is generally recommended in conventional charge-pump PLL applications [114] [128]. The filter components R_1 and C_1, which provide the current-to-voltage conversion, form a first-order low pass filter. They are essential to achieve the desired second-order PLL topology. The shunt capacitor C_0, which extends the loop filter to second order, is employed for additional ripple filtering. This is required to avoid overload of the VCO and to suppress spurious signals due to the ripple voltage generated by the instantaneous changes in the charge-pump current across R_1. Furthermore, for enhanced attenuation of the spurious signals due to the feedthrough of the phase detector frequency, a third low-pass filter section (R_2, C_2) was added, resulting in the third-order loop filter shown in Figure 5-7.

The values of the filter components must be carefully chosen with regard to the stability criterions of the second-order PLL model described in section 4.1.1. In order to maintain the stability criterions, the loop filter has to by approximated to first-order to comply with the requirements for a second-order PLL model. Taking into account Gardner's stability limit, the loop bandwidth have to be chosen at $\omega_{gc} \ll 2\pi \cdot f_{\mathrm{pd}} / 20$ in order to attain both adequate sta-

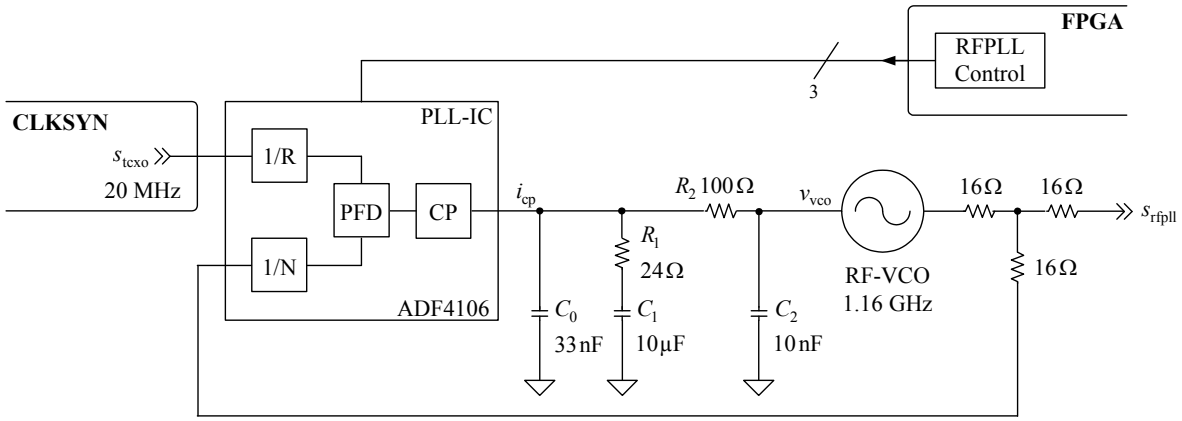

Figure 5-7 Circuit design of the RF-PLL stage.

bility margin and sufficient suppression of feedthrough spurs. Furthermore, it is essential to keep the loop bandwidth from interacting with the additional pole frequencies of the loop filter design. A comprehensive analysis of the requirements to attain first-order approximation of the loop filter design can be found in several textbook, e.g. [114] [115].

Provided that the phase noise of the VCO and the *N*-amplified phase noise of the TCXO predominate opposite to the other noise sources of the loop, the optimal loop bandwidth for a low noise PLL design is close to the frequency of intersection of the amplified phase-noise spectrum of the TCXO and the phase-noise spectrum of the free-running VCO [99]. Therefore, a RF-PLL loop bandwidth of $B_{\mathrm{rfpll}} = 10\,\mathrm{kHz}$ was chosen.

As mentioned in section 4.1.1, the amplitude of the feedthrough spurs are determined by the (trans-)impedance of the loop filter. Consequently, a decrease of the loop-filter impedance level is required. This implies a proportional increase of the nominal charge-pump current to maintain a constant value of the loop bandwidth B_{rfpll} specified before [132]. Hence, the nominal charge-pump current of the PLL-IC is set to its maximal value.

Finally, to avoid peaking in the transition-band of the loop transfer response, which amplifies the in-band noise, a high damping factor (large phase margin, respectively) of the loop transfer function is required. Hence, a phase margin of 81° is chosen to achieve sufficient flatness in the loop transfer response und, thus, to suppress VCO noise near the loop bandwidth. The characteristic loop parameters of the RF-PLL are summarized in Table 5-1.

Table 5-1 Design parameters of the LO-PLL and RF-PLL.

design parameter	RF-PLL	LO-PLL
output frequency	1.16 GHz	1.16 GHz–2.16 GHz
phase detector frequency	20 MHz (f_{tcxo})	36.25 MHz–67.5 MHz (f_{ddfs})
reference divider	1	1
feedback divider	58	32
in-band noise amplification	35 dB	30 dB
loop bandwidth	10 kHz	934 kHz–980 kHz
settling time	< 30 ms	< 5 us
phase margin	81°	51°

Design of the LO-PLL stage

The frequency sweep time of the RFISA synthesizer unit is primarily determined by the settling time of the LO-PLL stage. Hence, the LO-PLL had to be designed with regard to the capability of fast locking. It was therefore essential to maximize the loop bandwidth at least so wide that the settling time of the LO-PLL properly meet the specification in (5.8). Furthermore, since the LO-VCO requires a higher tuning voltage than the charge pump of the PLL-IC can supply, an active loop-filter topology is needed in order to tune the LO-VCO over the wide frequency range given in (5.2).

The schematic of the active loop filter design is shown in Figure 5-8. It also exhibits third-order topology and, thus, the filter design considerations described before can be adopted. Taking into account the lower bound of the DDFS tuning range in (5.5), the loop bandwidth of the LO-PLL is chosen at $B_{\mathrm{lopll}} = 1\mathrm{MHz}$. This is high enough to provide fast locking of the PLL and still low enough to properly meet Gardner's stability criterions. To achieve fast frequency settling of the LO-PLL, a low damping factor (low phase margin, respectively) of the loop transfer function is required (see section 4.1.1). Hence, a phase margin of 51° is chosen. Unfortunately, the tuning sensitivity of the LO-VCO considerably varies over its entire tuning range. Adjusting of the loop gain factor K is therefore required to maintain the loop bandwidth chosen. Depending on the specified tuning sensitivity for the settled VCO frequency, adjusting of K in (4.1) is accomplished by increasing or decreasing, respectively, the programmable nominal charge-pump current as shown in Figure 5-9.

The characteristic loop parameters of the LO-PLL designs are also summarized in Table 5-1. Simulation of the PLL behavior and calculation of the loop parameters and the particular filter components were done by the aid of the simulation software *ADIsimPLL*® from Analog Devices, Inc. The pertinent simulation results for the open loop gain and the settling time of the

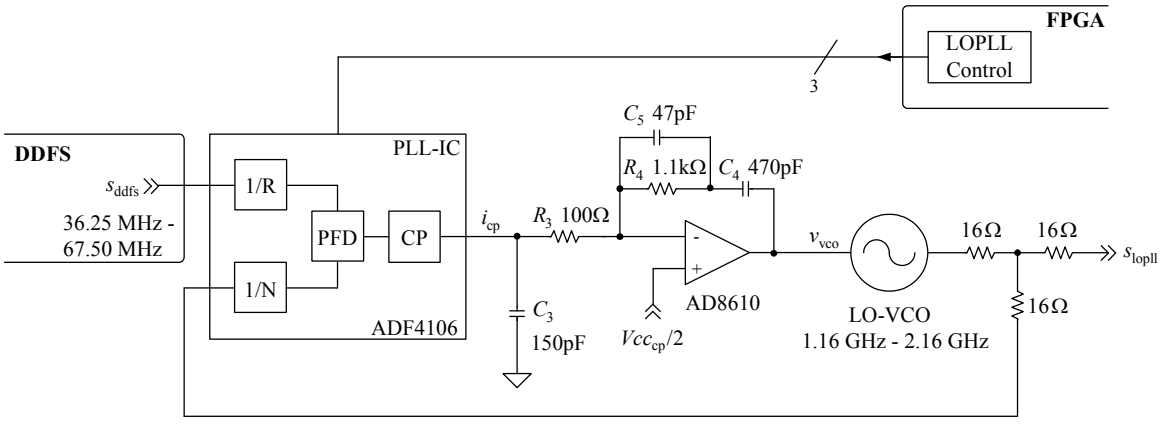

Figure 5-8 Circuit design of the LO-PLL stage.

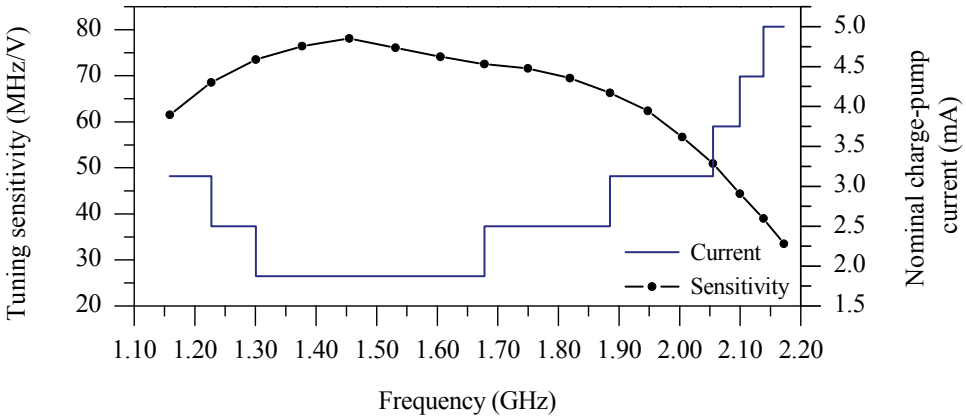

Figure 5-9 Tuning sensitivity of the wideband voltage controlled oscillator LO-VCO and adjusted nominal charge-pump current of the PLL-IC as function of the LO-PLL output frequency. (Tuning sensitivity is taken from data sheet)

RF-PLL and LO-PLL designs are shown in Appendix A4. Setting of the divider values and the nominal charge-pump current of the PLL-ICs is accomplished by the corresponding Control blocks in the FPGA

5.2.3 Design of the mixer stage

At the end of the signal chain of the RFISA synthesizer unit, the frequency down-conversion and the amplification of the output signal, which eventually stimulates the particular sensor device, is accomplished by the IF-output stage. The circuit design in Figure 5-2 is divided into the RF-signal path (s_{rf}), the LO-signal path (s_{lo}), and the IF-signal path (s_{if}). The RF-signal path comprises the variable-gain amplifier (VGA) and the self-designed band-pass filter (RF-BPF). The LO-signal path comprises the fixed-gain amplifier (AMP 2), the ceramic high-pass filter (LO-HPF) with cut-off frequncy at 880 MHz, and the ceramic low-pass filter (LO-LPF) with cut-off frequency at 2575 MHz. Finally, the IF-signal path comprises two fixed-gain amplifiers (AMP 3 – 4) and the self-designed output low-pass filter (IF-LPF).

The mixer device is a passive double-balanced diode mixer that inherently exhibits very good port-to-port isolation and spurious rejection. In principle, double-balanced mixers can be treated as LO-driven polarity reversing switch, connecting the signal, s_{rf}, applied at the RF-port to the IF-port but reversing its polarity every half cycle of the LO-signal, s_{lo}, [104]. The cascaded design of the LO-HPF and the LO-LPF yields a band-pass filter characteristic and is employed to minimize the contribution of wideband phase noise to the IF-output noise floor. For low distortion performance, the mixer requires a signal power of +13 dBm at the LO-port to switch the diodes fully on and off. Hence, the amplifier AMP 2, which provides a fixed gain of 18 dB, is employed in the LO-signal path to ensure a sufficient driver level by amplifying the output signal of the LO-PLL, s_{lo}. Furthermore, in order to gainfully emphas-

ize the benefits of the double-balanced diode mixer, perfect impedance matching at all mixer ports is essential to attain overall symmetric circuit design. Hence, resistive matching networks, each with a characteristic impedance of $Z_0 = 50\,\Omega$, are employed in both input signal paths of the mixer. At the output of the mixer, proper wideband $50\,\Omega$ termination is ensured by the amplifier (AMP 3), which offers a very good input VSWR (voltage standing wave ratio) of 1.2:1 up to a frequency of 4 GHz. Moreover, the amplifier provides a buffer stage not only to decouple the mixer output from undesired load variations due to the IF-filter's input impedance, which is not constant over the wide frequency range, but also to drive the IF-Filter sufficiently. The amplifier AMP 4 decouples the IF-Filter from the synthesizer output and performs the driving amplifier that stimulates the sensor eventually.

The RF-BPF and the IF-LPF are the most crucial elements in order to achieve the required frequency selection, transmitting the output frequency f_o while sufficiently rejecting other mixer products, which are caused by the inevitable non-linear mixing operation. Since the interaction of all of mixer products in (3.3) becomes much more extensive when the input signals consist of undesired harmonics, sufficient filter stages applied to the mixer's input and output signals were mandatory to attain high spectral quality of the IF-output signal. The RF-BPF, which is located before the mixer's RF-port, acts as image reject filter. It is employed to effectively minimize the noise bandwidth of the signal s_{rf} and to suppress the harmonics of the signal s_{rf}. Latter is required to avoid that mixer products originated from harmonics and spurs of the RF-PLL signal s_{rf} may down-convert within the pass-band of the IF-Filter. This would considerably impair the spectral performance of the output signal s_{if}. Hence, band-pass filtering of the signal s_{rf} minimizes the number of mixer products, which are originated from the term mf_{rf} in (3.3). Furthermore, a RF-BPF band-pass filter design that exhibits a steep roll-off characteristics and a very narrow pass-band proportional to its center frequency of f_{rf}=1.16 Ghz is required to achieve sufficient reduction of the broadband noise floor of the signal s_{rf}.

The IF-LPF output filter must pass the desired output frequency $f_o = f_{if} = f_{lo} - f_{rf}$ in (3.3) and sufficiently attenuate all mixer intermodulation products $f_{if} = nf_{lo} + f_{rf}$ in (3.3), provided that sufficient attenuation of the harmonics of f_{rf} is ensured. Assuming the minimum output frequency in (5.3), the first intermodulation product will occur at $f_{lo} + 10\,\text{kHz} \approx 1.16\,\text{Ghz}$. Furthermore, due to the mixer's non-perfect LO-to-IF port isolation in practice, the signal applied at the LO-port is only attenuated by at least $-20\,\text{dB}$ (value is taken from data sheet). This result in a LO-feedthrough, which appears in the output spectrum at 1.16 Ghz with a estimated power level of $+13\,\text{dBm} - 33\,\text{dB} = -20\,\text{dBm}$. Additionally, estimation of the minimum level of the IF-signal s_{if} with $-51\,\text{dBm}$ (as shown in Figure 5-3) and the specified maximimum spur level of $-40\,\text{dBc}$ (see section 1.4), yields a maximum LO-feedthrough level of $-91\,\text{dBm}$ at 1.16 Ghz. Consequently, $-71\,\text{dB}$ IF-filter attenuation at 1.16 Ghz is required.

Taking into account the desired IF-LPF filter pass-band width of $B_{if} = 1\,\text{GHz}$, a very steep roll-off characteristic in the range of $1.0\,\text{GHz} - 1.16\,\text{GHz}$ is essential. Unfortunately, adequate high-order filter designs that consists of lumped elements, such as inductors and capacitors, are not practicable at gigahertz frequencies because of both the significantly reduced quality factor and the wide spread of element values. Hence, to ensure optimum filter performance of the RF-BPF filter and the IF-LPF filter at gighertz frequencies, filter designs in microstrip geometry are mandatory.

The self-designed RF-BPF shown in Figure 5-10a is based on a microstrip combline filter structure with tapped-line input and output stages. Compared to other types of band-pass microstrip filter described in [174] [175], the combline structure beneficially offers structural compactness, allowing for a small-sized printed circuit board (PCB) implementation. In general, combline filters are based on a structure of coupled resonators. The resonators consist of line elements (1 to *n*), which are short-circuited at one end, with a lumped capacitance loaded between the other end of each resonator line element and ground. The lines 0 and *n*+1 are not resonators but simply part of impedance-transforming sections at the ends. In this type of filter, coupling between the resonators is achieved by way of fringing fields between the resonator lines. With the lumped capacitance present, the resonator lines can be less than quarter-wave long at resonance, and the coupling between resonators is predominantly magnetic [174]. The larger the loading capacitances, the shorter the resonance lines, resulting in a more compact design of the filter structure. When taking into account a free-space wavelength of electromagnetic waves of approximately 30 cm at 1 GHz, the advantage in terms of a compact PCB implementation of combline filters compared with those that are based on quarter-wave resonance is apparent. Figure 5-10a shows the original physical PCB dimensions of the RF-BPF combline filter. The filter geometry was pre-calculated by synthesis formulas suggested in [176] [177] and post-designed with the RF simulation software *Ansoft Designer*®

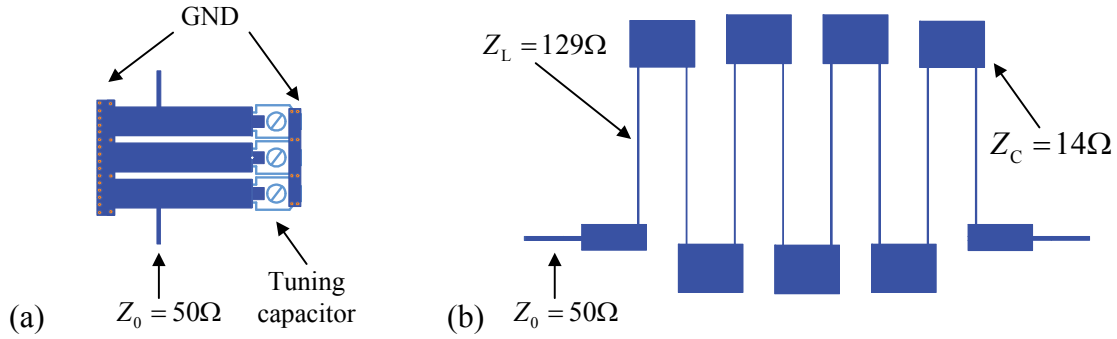

Figure 5-10 Layout in original physical dimensions of the microstrip filter geometry for (a) the fifth-order combline band-pass filter with tapped-line input and output and (b) the seventeenth-order stepped-impedance low-pass filter.

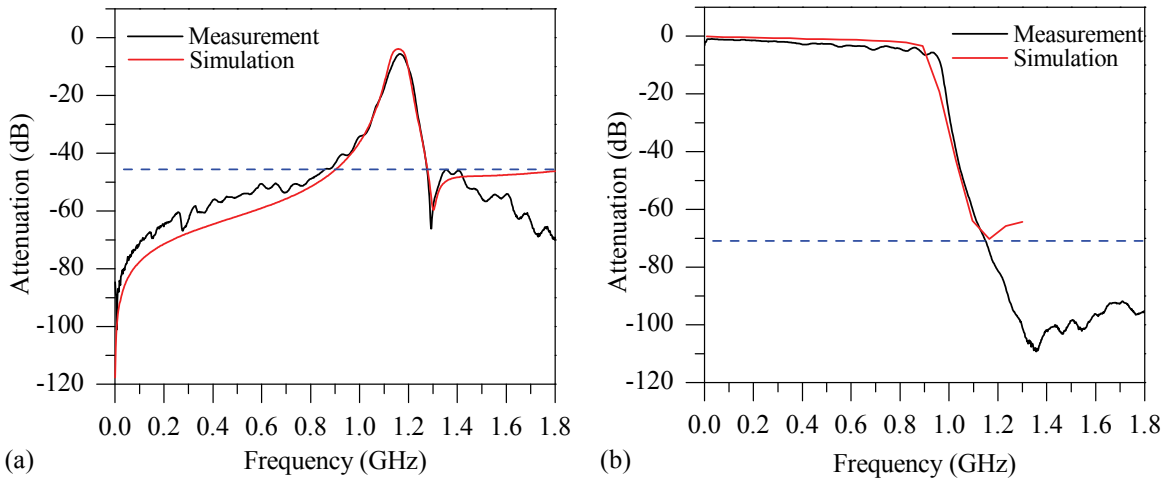

Figure 5-11 Measurement and 2D-field simulation results of the filter attenuation as a function of frequency for the microstrip filter structures designed as (a) tapped-line combline band-pass filter and (b) stepped-impedance low-pass filter.

from Ansoft Corporation. The RF-BPF is specified with center frequency at 1.16 GHz, a pass-band width of 1% (11.6 MHz), and characteristic impedance of Z_0=50 Ω. To allow for fine adjustment of the filter performance, variable high-frequency capacitors made of tuning screws are employed. Beside these top-level filter parameters, the design and the geometry of microstrip filter designs depend on the PCB substrate material used. Hence, a specific high frequency hydrocarbon material (RO4350) that features very low tolerance of the dielectric constant was chosen for manufacture of the PCB (see section 5.7). The tapped-lines at the input and output of the filter design match the resonators with the microstrip traces' Z_0=50 Ω characteristic impedance of the surrounding circuit design. Measurement and simulation results of the filter's frequency response are shown in Figure 5-11a. The measurement data were obtained using a Network Analyzer from Hewlett Packard, Inc., and reveal a stop-band attenuation of at least -40 dB and overall good agreement with the simulation results.

The original physical dimension of the IF-LPF is shown in Figure 5-10b. The structure is based on a stepped-impedance low-pass microstrip filter, using alternating sections of very high and very low characteristic impedance transmission lines. In general, the design of microstrip filters involves two steps. First, selection of an appropriate LC-prototype filter design in accordance to the required specifications (e.g. cut-off frequency, stop-band attenuation, roll-off characteristic). Second, realization of an appropriate microstrip structure that approximates the lumped-element prototype filter. The chosen prototype lumped-element filter shown in Figure 5-12 is a seventeenth-order low-pass filter with Chebyshev characteristics. It was designed with cut-off frequency at 1.0 Ghz, characteristic impedance of Z_0=50 Ω, and stop-band attenuation of 71 dB at 1.16 Ghz. In order to obtain the corresponding microstrip structure, the series inductors are replaced with high-impedance line sections, Z_L, and the shunt capacitors are replaced with low-impedance line sections, Z_C. Taking into account the

dieelectric constant of the RO4350 substrate material, the ratio between Z_L and Z_C is set to the highest and lowest characteristic impedance that could be practically fabricated on the PCB. Synthesis formulas for calculating the lengths of the lines with regard to the corresponding lumped elements in Figure 5-12 and the characteristic line impedances Z_L and Z_C can be found in [174]. Post-designing and simulation of the frequency response of the microstrip filter structure was again performed with the RF simulation software *Ansoft Designer*® from Ansoft Corporation. Results of the simulated and measured frequency response of the filter are shown in Figure 5-11b. The measured frequency response, which was obtained with a Network Analyzer from Hewlett Packard, Inc., reveals a stop-band attenuation of $\approx 70\,\mathrm{dB}$ at $1.16\,\mathrm{Ghz}$ and is in appropriate agreement with the specifications.

5.3 Analog front-end design of the digital vector voltmeter unit

In order to benefit gainfully from the direct-sampling technique introduced in section 4.2, the analog circuit design of the digital vector voltmeter unit must be minimized to reduce not only the hardware complexity but also the overall noise and distortion otherwise introduced by the amount of components. Due to the required wideband design of the analog signal conditioning in front of the analog-to-digital conversion, a sophisticated circuit design is mandatory to attain low-noise performance at frequencies up to 1 GHz. The analog front-end circuit design of the digital vector voltmeter is shown in Figure 5-13. It solely comprises a channel switch (CSW), an input low-pass filter (IN-LPF), a variable-gain stage (DVGS) digitally controlled, a differential amplifier (DAMP), an anti-aliasing filter (AF), a high-speed 12-bit analog-to-digital converter (ADC), and finally the FPGA. All components are listed in Appendix A1.

The channel switch is an absorptive SPDT (single-pole double-throw) switch featuring high channel isolation and high frequency operation. Advantageously of the absorptive switch, the input impedance of the port that is not switched is matched to $50\,\Omega$, allowing for maintaining matching to the characteristic impedance of the coax cable connected. The following amplifier (AMP 3) ensures proper wideband $50\,\Omega$ termination for the signal that is switched. Switch-

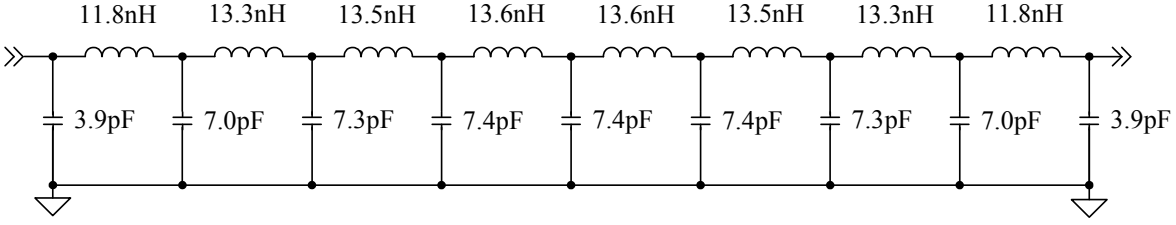

Figure 5-12 Schematic of the prototype lumped-element low-pass filter.

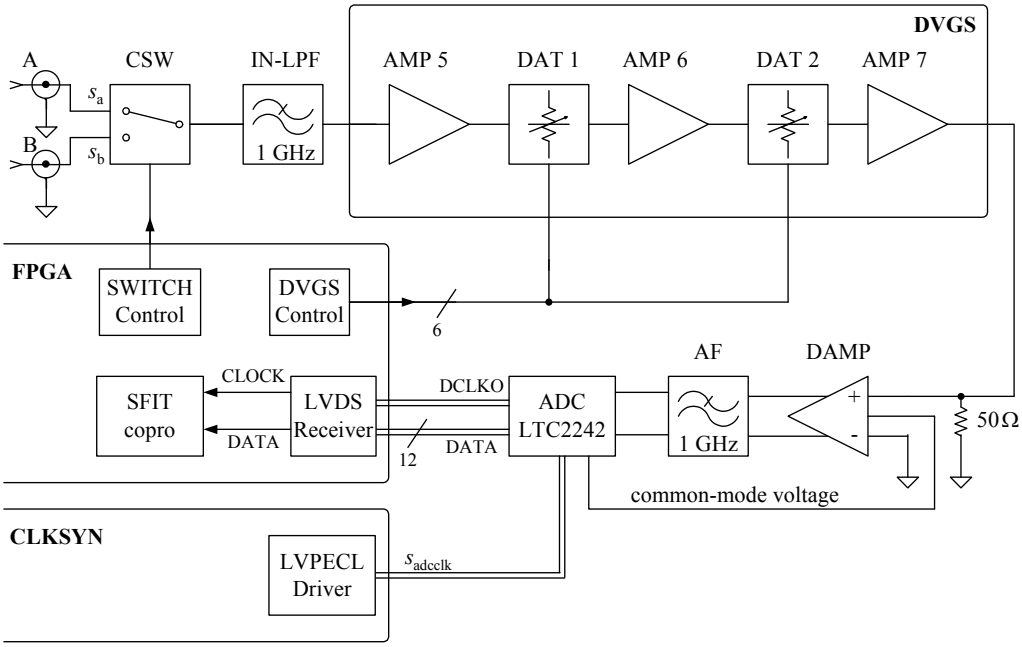

Figure 5-13 Basic circuit design of the analog front-end used in the digital voltmeter unit.

ing of the input signals s_a and s_b is accomplished at the earliest stage in the analog front-end to reduce the hardware complexity along the entire signal path significantly. This, moreover, allows for compensation of parasitic effects, which are introduced by the components or the board layout, because only a single signal path for the conditioning of both input signals is used. Disadvantageously, switching the input channels implies a successive analog-to-digital conversion of the input signals, delaying the data acquisition time of the RFISA electronics system. Hence, a high sampling frequency of the ADC is needed to avoid significant delays.

The ceramic low-pass filter (IN-LPF) offers a pass-band bandwidth of 1 GHz and a stop-band attenuation of -50 dB at 2 GHz. It is primarily employed in order to suppress high frequency interfering signals at the input of the RFISA electronics system and decrease the input noise floor. The following variable-gain stage, which is digitally controlled by the DVGS Control block in the FPGA, provides high amplification of weak input signals. This allows weak signals to be adjusted to an optimal amplitude level with respect to the resolution of the ADC. This is required to attain optimal SNR performance of the ADC (see section 4.2.2). Since no commercial IC for a digitally controlled variable gain amplifier offering an analog bandwidth up to 1 GHz was currently available, a cascaded amplifier-attenuator chain was designed to accomplish adjustment of the input amplification. The variable-gain stage comprises a cascading connection of three monolithic low noise, fixed gain amplifier (AMP 4 – AMP 6) providing an overall gain of $3 \cdot 18\,\mathrm{dB} = 54\,\mathrm{dB}$ and two passive 6-bit digital step attenuators (DAT1 and DAT2) providing an overall attenuation of $2(-31.5)\,\mathrm{dB} = -63\,\mathrm{dB}$. This results in a controllable gain range of $-9\,\mathrm{dB} \le G_{\mathrm{dvgs}} \le +54\,\mathrm{dB}$ adjustable in 0.5 dB increments. Alternating cascading of amplifier and attenuator devices protect for overloading of the fixed-gain amplifier. Since low noise and high linearity of the analog front-end is mandatory, the high gain,

low noise AMP 4 is employed at the earliest stage of the analog front-end in order to dominate the overall noise performance as suggested in section 4.2.2. Furthermore, the bandwidth and the output linearity of the variable-gain stage remains constant regardless of the gain/attenuation setting because only fixed-gain amplifiers are employed. Supposed that no amplifier overdrives, the variable-gain stage therefore provides a dynamic analog front-end design that maintains almost constant noise and distortion performance over the gain adjustment range. According to (4.15) and based upon the component values taken from the respective data sheets, the estimated noise figure of the analog front-end for the case $G_{\mathrm{dvgs}} = 54\,\mathrm{dB}$ is $\approx 80\,\mathrm{dB}$ at 1 GHz, and so that above the ADC's theoretical signal-to-noise ratio of the employed 12-bit ADC, given by $SQNR_{\mathrm{adc}} = 74\,\mathrm{dB}$ for $p = 12\,\mathrm{bit}$, $FSR = 0.7$ (see section 4.2.2).

Because of the applied direct-sampling technique, the switched input signals of the RFISA electronics are sampled at high frequencies and, thus, the ADC specified by its high frequency performance constitutes the major critical component of the analog front-end. Unfortunately, currently no commercial ADCs are available that offer high resolution, high sampling frequency, and high analog bandwidth at the same time [149] [151]. Since an analog bandwidth of the ADC of more than 1 GHz is essential for the direct-sampling technique, a 12-bit pipelined ADC offering a full power analog bandwidth of 1.2 GHz and a differential clocking capability up to 250 MHz is employed. As mentioned in section 4.2.4, undersampling is not crucial when the direct-sampling technique is applied at known signal frequency. Hence, in order to ensure low-jitter sampling-clock generation by the clock synthesizer unit, which will be described in section 5.4, a LVPECL sampling clock, s_{adcclck}, is synthesized that exhibits a frequency of $f_{\mathrm{adcclk}} = 200\,\mathrm{MHz}$. This is high enough to avoid significant delays of the data acquisition time due to the successive sampling process of the input signals. Driving the input of a high-speed ADC requires differential signaling to ensure high accuracy and low harmonic distortion levels. In contrast to the transformer based balanced-to-unbalanced conversion applied in the DDFS stage, a fully differential amplifier is employed to convert the single ended input signal into a differential signal. This is required because conventional transformers do not cover the necessary frequency range from 10 kHz to 1 GHz. The SFIT copro block in the FPGA represents the digital signal processing for the sine-wave fitting computation, which will be described in section 6.2.1.

Finally, the anti-aliasing filter between the differential amplifier and the ADC limits the noise bandwidth of the signal applied to the ADC and attenuates high-frequency distortion levels originated from the non-linearity of the amplifiers before. The self-designed differential anti-aliasing filter is based on a fifth-order low-pass filter topology with Chebyshev filter characteristic to ensure sharp roll off [173]. The filter is designed with a cutoff frequency of 1 GHz, a stop-band attenuation of $-30\,\mathrm{dB}$ at 2 GHz, and a characteristic impedance of $50\,\Omega$

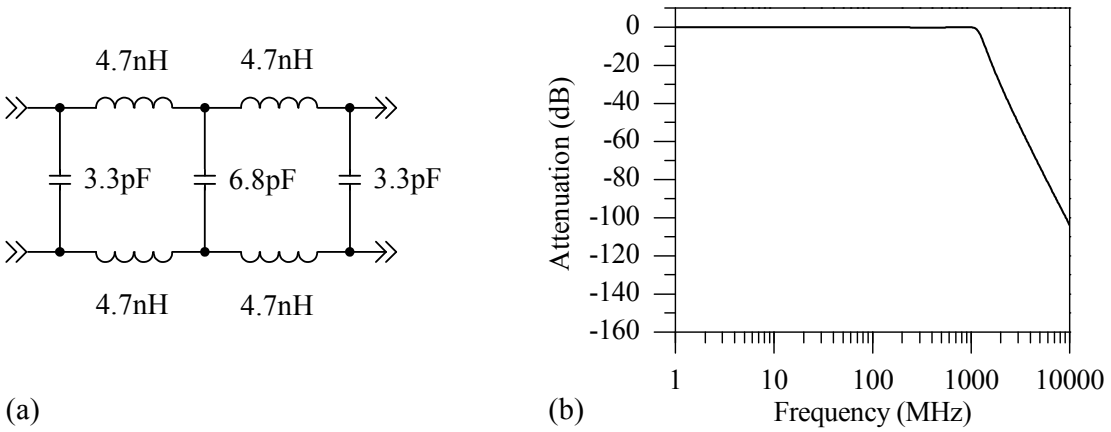

Figure 5-14 Representation of (a) the schematic and (b) the frequency response (semi-logarithm plot) of the differential fifth-order low-pass filter.

to ensure overall impedance matching. The schematic of the differential filter and its corresponding frequency response is shown in Figure 5-14.

5.4 Clock synthesizer unit

Generation of different reference clock signals is an essential part of the RFISA electronics. The key components of the RFISA electronics (PLL-ICs, DAC, ADC, and FPGA) require different clock frequencies as well as different clock levels, which must be derived from the 20 MHz system master clock (TCXO). Moreover, the spectral quality of the various reference signals has crucial impact on the performance of the entire RFISA electronics. As explained in Chapter 3 and Chapter 4, for one thing, the quality of the synthesized output frequency in coherent frequency synthesis is directly affected by the accuracy and spectral performance of the frequency reference, and for another thing, the conversion performance of the specific high-speed ADC and DAC devices is extremely sensitive to the quality of the sampling clock

In order to achieve high quality of the master clock and to generate multiple low-jitter sampling clocks from the given master clock, an enhanced clock distribution topology is designed. First, the master clock of the entire RFISA electronics is sourced from a high quality TCXO that offers a 20 MHz square-wave frequency reference with low phase noise and high frequency stability. Secondly, the high-speed, low-noise clock buffer (CLKBUF) is employed to reduce the fanout of the TCXO output signal, s_{tcxo}, and achieve a low-jitter clock distribution of the master clock to the specific sub-units of the RFISA electronics system. Third, a clock synthesizer IC (CLKSYN-IC) that provides multi-output clock generation and distribution function along with an on-chip phase-locked loop core is employed. All components are listed in Appendix A2.

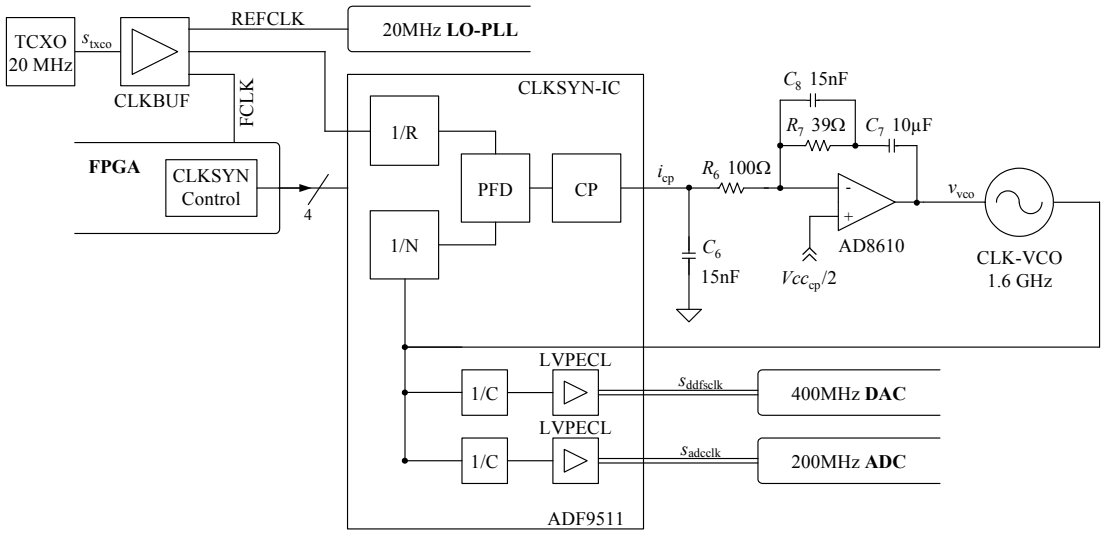

Figure 5-15 Circuitry of the clock synthesizer unit.

The CLKSYN-IC offers five independent clock outputs with LVDS or LVPECL output capability, each with individually programmable dividers (1/N). Furthermore, to accomplish the overall loop action, the phase-locked loop core requires solely few external components: the VCO and the components for the loop filter configuration. Beneficially, since the various output clocks are derived by a divide-by N operation of a phase-locked frequency, high-speed clock signals with low jitter and noise performance can be obtained. For the voltage controlled oscillator of the clock synthesizer (CLK-VCO) the same type of VCO as employed in the RF-PLL is used, but phase locked at higher frequency. The topology of the clock synthesizer unit along with the required output specifications is depicted in Figure 5-15. Controlling and configuration of the CLKSYN-IC is accomplished by CLKSYN Control block in the FPGA.

Since the frequency of the TCXO is exploited as reference, the phase locked loop is designed for a phase detector frequency at $f_{\mathrm{tcxo}} = f_{\mathrm{pd,clkpll}} = 20\,\mathrm{MHz}$ and a fixed output frequency at $f_{\mathrm{clkpll}} = 1.6\,\mathrm{GHz}$. This implies a reference-divider value of $R_{\mathrm{clkpll}} = 1$ and a feedback-divider value of $N_{\mathrm{clkpll}} = 80$. In order to generate the 400 MHz LVPECL sampling clock, s_{ddfsclk}, for the DAC employed in the DDFS stage and the 200 MHz LVPECL sampling clock, s_{adcclk}, for the ADC employed in the digital vector voltmeter unit, the corresponding clock dividers are set to a value of four and eight, respectively.

The phase locked loop and, in particular, the loop filter must be designed wit regard to low noise and spurious signal performance in order to synthesize low-jitter sampling clocks. The considerations of the loop filter design are identical to that of the RF-PLL loop filter design (see section 5.2.2) because $f_{\mathrm{pd,clkpll}} = f_{\mathrm{pd,rfpll}} = f_{\mathrm{tcxo}} = 20\,\mathrm{MHz}$ and the same key components as in the RF-PLL stage are employed. However, an active filter configuration must be chosen to supply the tuning voltage that is required to fix the frequency of the CLK-VCO at 1.6 GHz.

The active loop filter configuration is designed with a loop bandwidth of 10 kHz and a phase margin of 80°, which is equivalent to the loop parameter of the RF-PLL (see Table 5-1). The filter topology is the same as the active filter topology applied in the LO-PLL. Simulation of the loop behavior and calculation of the loop parameters and the particular filter components were performed with the software *ADIsimCLK*® from Analog Devices, Inc.

5.5 Processor unit

The processor unit of the RFISA electronics system depicted in Figure 5-16 provides the final computation of the impedance spectrum according to (2.2) and, with regard to the particular sensor application, the evaluation of the specific sensor data obtained from the analysis of the respective impedance spectra. It also supports various common peripheral interfaces for the data transfer to an external component, such as a personal computer or notebook (combined as host in the following), and for process controlling. Depending on the particular sensor application, extensive data computation may accrue in order to determine the specific parameters from the sensor response. However, in order to allow stand-alone operation of the RFISA electronics, external data computation on a host is not feasible. Hence, a powerful central processing unit (CPU) embedded into the RFISA electronics is needed.

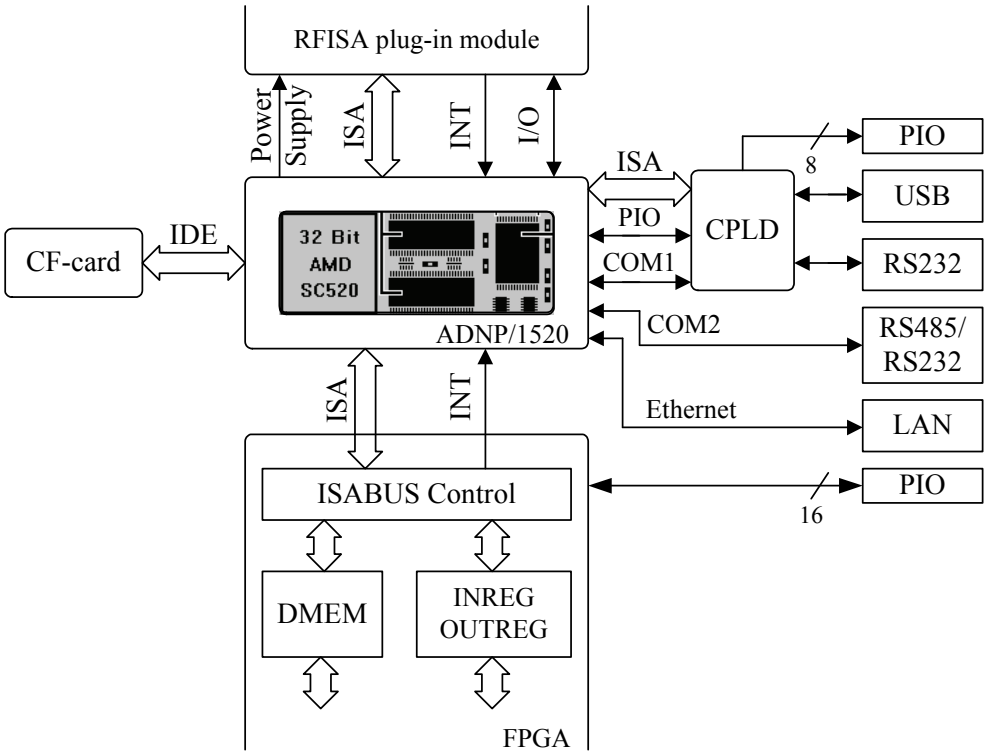

Figure 5-16 Functional block diagram of the processor unit.

The key component of the processor unit is the single-board computer ADNP/1520 from SSV Software Systems GmbH. The ADNP/1520 module provides an AMD 32-bit SC520 low power 586 CPU with 133 MHz clock speed and included hardware FPU (floating point unit), a complete set of PC/AT-compatible peripherals, a 16-bit ISA (industry standard architecture) expansion bus interface, and seven programmable interrupt (INT) inputs.

In addition to the powerful 32-bit CPU, the ADNP/1520 module offers on-board: 16 MByte FLASH memory for the Embedded-Linux operation system, 64 MByte SDRAM (synchronous dynamic random access memory) for storing data and specific application software, an IDE (integrated drive electronics) interface, two 16C550 UARTs (universal asynchronous receiver transmitter) providing two serial communication ports (COM1, COM2), and a LAN (local area network) controller providing a 10/100Mbps Ethernet interface. Due to the subminiature module dimension ($82\text{mm} \times 36\text{mm}$), a small-sized overall processor unit could be eventually realized.

The Ethernet interface allows advantageously for both high-speed data transfer of the measurement data to a directly connected host for data storing and installation of an embedded networking solution. Latter beneficially provides operation of the RFISA electronics by remote control and data transmission to distributed hosts. This allows spatial separation between the RFISA electronics system and the host in laboratory or industrial application. Furthermore, to connect the RFISA electronics system with a host via modern serial connections directly, the peripheral interfaces around the ADNP/1520 module have been extended with an additional USB (universal serial bus) interface. The USB interface is connected to COM1 by a XOR-operation[8] on the USB and RS232 port. The USB-xor-RS232 interface is controlled by the complex programmable logic device (CPLD) and the transfer of the serial data via USB is accomplished by the USB-RS232 converter FT232BM from Future Technology Devices International Limited.

Beside the optional data transfer of the measurement data, the USB-xor-RS232 interface is primarily used for debugging and configuration of the RFISA electronics. The COM2 port is extended to a RS232/RS485 multi-protocol interface to support both standards of serial connections for data transmission and process controlling. The IDE interface of the ADNP/1520 is utilized to allow connection of a CompactFlash (CF) memory card for recording sensor data in stand-alone operation of the RFISA electronics systems over large periods. The peripherals of the RFISA electronics is completed by several general-purpose programmable input/outputs (PIOs) controlled by the CPLD and the FPGA.

[8] The exclusive OR (symbolized XOR) operation describes a logical disjunction on two operands resulting in a value of true if only one of the operands is true.

The processor unit also provides the interface to the FPGA that contributes as external peripheral in the ISA address and data space of the ADNP/1520. For this purpose, the FPGA includes an ISABUS Control block, input and output register (INREG, OUTREG), and a data memory block (DMEM) to accomplish enhanced data exchange between FPGA and processor unit. Finally, in order to allow future expansion of the RFISA functionality (e.g. by a plug-in LCD module), an interface for a plug-in module is implemented, which provides the ISA bus interface, power supply, and programmable input/output ports (I/O).

5.6 Sensor interface unit

The sensor interface unit accomplishes the electrical and mechanical connection between the target sensor and the RFISA main electronics, well adapted to specific sensor application. In accordance to the principle of measurement described in section 2.1, the primary function of the sensor interface is to split the incoming synthesizer signal s_o into the stimulus signal, which is applied to sensor, and the reference signal s_a and response signal s_b, which are recorded by the RFISA main electronics. In order to provide individual and appropriate adaptation to the specific sensor and sensing application, the sensor interface unit is separated from the RFISA main electronics, thus allowing for small-sized interface boards connectable close to the particular sensor. The separation, moreover, makes sophisticated sensor probes for *in situ* impedance-spectroscopy measurements possible. To ensure optimum accuracy at high frequency, the input and output of the sensor interface are matched to the characteristic impedance ($Z_0 = 50\,\Omega$) of the coaxial cables that connect the RFISA main electronics with the separate interface electronics. In principle, any analog (passive or active) circuit configuration that is based on either RF current-voltage measurement methods or the RF transmission measurement methods can be adopted for the design of the sensor interface electronics. With regard to sensor applications that will be presented in section 7.3, four specific sensor-interface circuit designs were developed, each with the objective of a small-sized circuit layout to allow implementation in the particular sensor probe.

The passive non-transformer circuit design in Figure 5-17a is based on the non-grounded transmission measurement method. It consists of some resistors solely and features therefore very small-sized circuit layout, wide impedance measurement coverage, and broadband frequency operation because, in principle, not a frequency-dependent component is employed. It is primarily intended for BAW sensor applications and for testing the measurement accuracy of the RFISA electronics. Since BAW sensors exhibit a wide impedance range in the vicinity of the resonance (see Figure 2-5), the sensor device is embedded between resistive attenuators (ATTN). The attenuators are designed with a characteristic impedance of $Z_0 = 50\,\Omega$ and decouple the variations of the sensor impedance Z from the characteristic input/output impedance Z_0 of the sensor interface. This ensures overall impedance matching to the characteristic

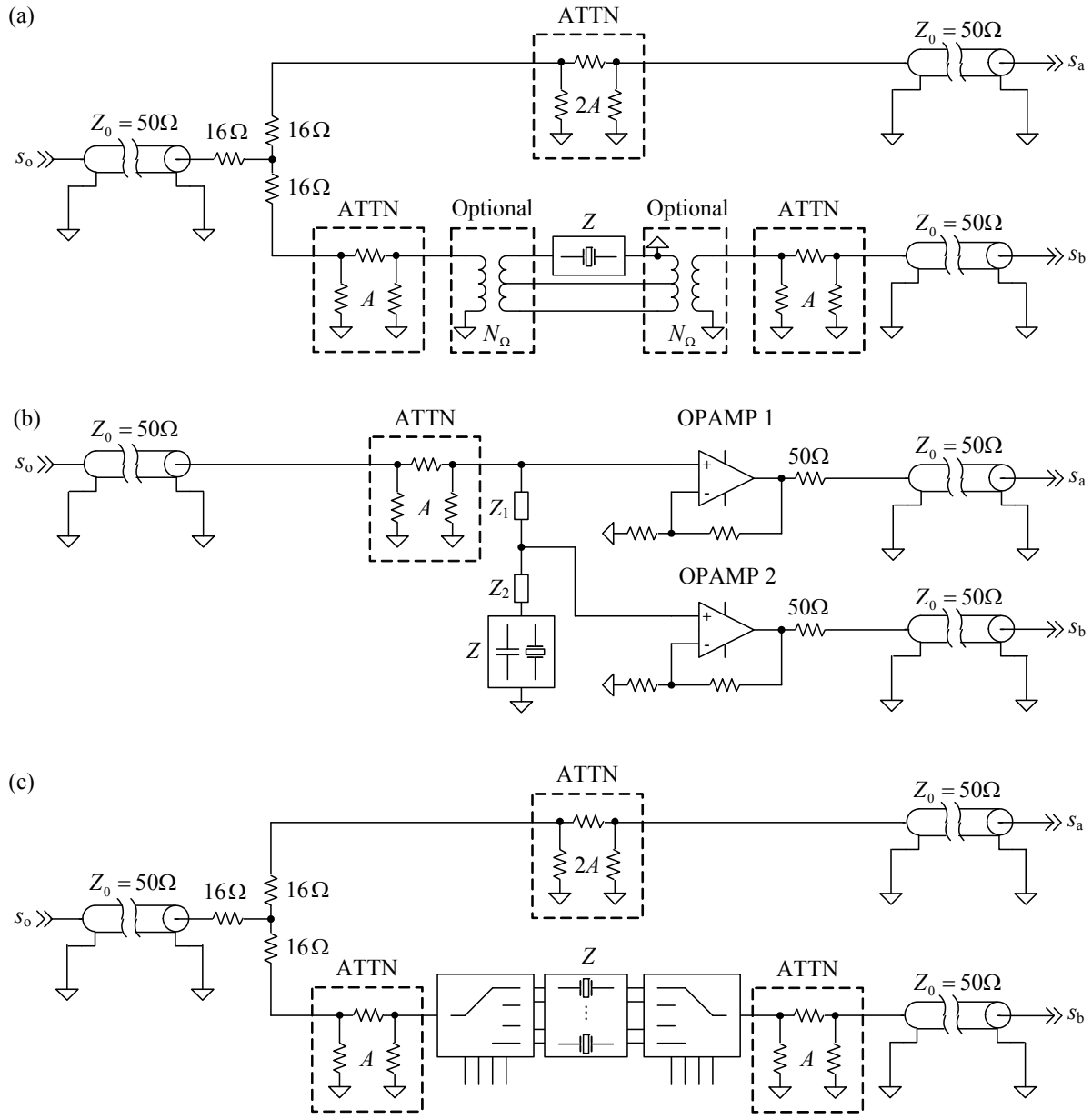

Figure 5-17 Circuit designs of the sensor interface unit for (a) passive transmission measurement method, (b) active voltage-divider measurement method, and (c) multiplexed transmission measurement method.

impedance of the coaxial cable and the RFISA electronics. The voltage ratio is given by $r(\mathrm{j}\omega) = k(\mathrm{j}\omega)\cdot\left(Z_0 / \left(2Z_0 + Z(\mathrm{j}\omega)\right)\right)$ where $k(\mathrm{j}\omega)$ describes the frequency-dependent network equivalent and have to be calibrated according to (2.3).

Proper decoupling of Z from Z_0, however, requires high attenuation factors, $A > -10\,\mathrm{dB}$, for the ATTN blocks. Hence, due to the weak output signals s_a and s_b that have to be recorded, sufficient noise reduction by the FPGA based sine-wave fitting computation is required to avoid deterioration of the measurement accuracy. The transmission measurement method with transformer circuit configuration allows for DC-grounded sensor measurements. Grounded

measurement is primarily required for in-liquid applications of TFE-TSM sensors in order to allow grounding the sensing electrode to keep the electric and dielectric boundary conditions constant [178]. The employed transformers, however, restricts the usable frequency range due to their frequency-dependent transfer characteristic.

The active circuit configuration in Figure 5-17b is based on the voltage divider principle of measurement and provides RF-grounded sensor measurement. It is intended for in-liquid application of both capacitive sensors applied for dielectric spectroscopy and TSM-BAW sensors. Specific adaptation to the particular sensor is achieved by proper choice of the series impedances ($Z_1(\mathrm{j}\omega)$ and $Z_2(\mathrm{j}\omega)$) in accordance to the predictable values of $Z(\mathrm{j}\omega)$. Although the active sensor interface configuration is able to provide signal amplification rather than attenuation, the required amplifier components (OPAMP 1 – 2) narrow the useable frequency range. Furthermore, the inevitable input impedance of OPAMP 2, which is parallel to the sensor impedance, adversely affects the measured sensor impedance. The choice of the particular OPAMP depends therefore on the frequency range and impedance range requirements of the specific sensor application. For the dielectric spectroscopy, the wideband (500 MHz) FET-input (field effect transistor input) operational amplifier OPA656 from Texas Instruments, Inc., which features a very low input capacitance inherently, was chosen to minimize the impact on the measured impedance of the capacitive sensor. With the assumption of $Z(\mathrm{j}\omega) >> Z_2(\mathrm{j}\omega)$, which is the general case because $Z_2(\omega)$ is only employed to allow appropriate short-circuit calibration measurement, the voltage divider ratio is given by $r(\mathrm{j}\omega) = Z(\mathrm{j}\omega) / \left(Z_1(\mathrm{j}\omega) + Z(\mathrm{j}\omega)\right)$.

With the example of impedance spectroscopy on a unloaded quartz crystal resonator (QCR), it is apparent from Figure 5-18 that both principles of measurement suffer from variations of the measurement sensitivity due to the non-linear relation between $Z(\mathrm{j}\omega)$ and $r(\mathrm{j}\omega)$. Basically, the sensitivity of the voltage-divider configuration is high for $Z(\mathrm{j}\omega)$ close to $Z_1(\mathrm{j}\omega)$ and degrades as the gradient of the voltage-divider ratio levels off for higher impedances, causing deterioration of the impedance measurement accuracy. Adaptation of the series impedance $Z_1(\mathrm{j}\omega)$ with respect to the highest predictable sensor impedance is therefore mandatory to spread the impedance range that is measurable with adequate sensitivity. However, this is attained at the expense of weaker signal levels that have to be measured in the lower impedance range. Thus, the active voltage-divider sensor interface is well suitable for applications that require grounded sensor application with a high sensitivity in a narrow impedance measurement range. As the result of the attenuator's characteristic impedance of $Z_0 = 50\,\Omega$, the sensitivity of the transmission principle of measurement levels off for $Z(\omega) < 50\,\Omega$ but exhibits an appropriate sensitivity over a broad impedance-measurement range. As shown in Figure 5-18, improving the sensitivity for lower impedance values can be obtained by application of transformers with suitable transformer impedance ratio, N_Ω.

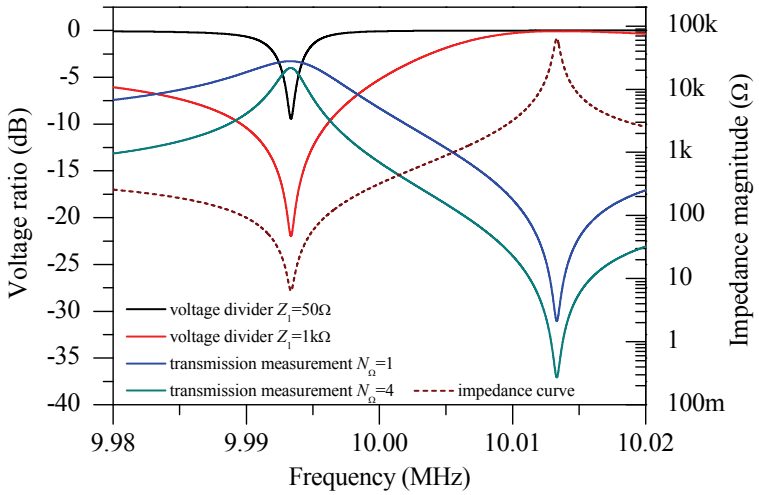

Figure 5-18 Voltage divider and transmission principle of measurement in dependence on the quartz crystal resonator's impedance magnitude as a function of frequency for various circuit configurations.

In principle, additional multiplexer plug-in boards can easily extend all three sensor interface units for the application of multi-sensor arrangements. Figure 5-17c shows the developed transmission sensor interface unit with on-board multiplexer, which is intended for a langasite BAW gas sensor array for high temperature applications (see section 7.3.1).

Integration of sensor interface circuitry into a sensor cell for in-liquid applications of 5 MHz QCR devices is shown in Figure 5-19. The sensor interface circuitry is based on the transmission measurement method. The cell has a cavity for 5 MHz QCR devices with 25.4 mm diameter. Inside the cavity, two Pogo® pins provide electrical connection to the QCR's electrodes. The Pogo® pins are internally connected to the printed circuit board of the transmission circuitry. On top (sensing) side, an O–ring is used between the probe housing and the crystal retainer to seal the QCR electrodes from the liquid media.

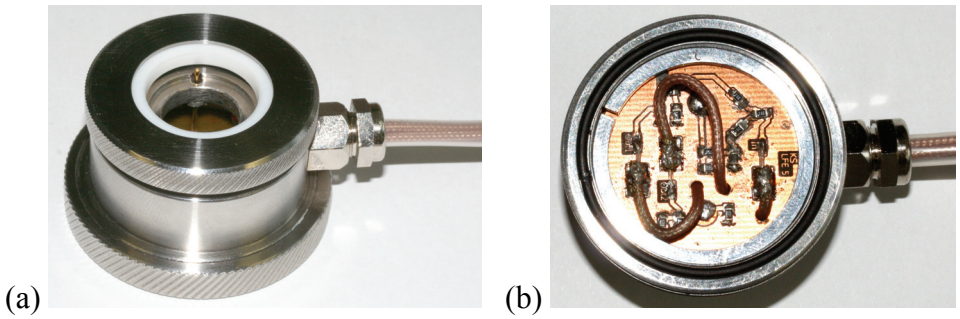

Figure 5-19 Sensor cell for 5 MHz quartz crystal resonators. (a) top view onto the sensor cell (b) bottom view onto the integrated sensor interface circuitry

5.7 Layout and assembling

Operation of the RFISA electronics at high and very high frequencies requires not only sufficient design strategy and component choice (as explained in the sections before) but also sophisticated printed circuit board (PCB) layout and assembling. Taking into account harmonics of the various RF/Gigahertz signals synthesized, frequencies far within the Gigahertz-range may occur. Moreover, the noise floor, spur performance, and jitter performance of the employed mixed/analog circuits (ADC-IC, DAC-IC, CLKSYN-IC) is greatly influenced by not only the high-frequency characteristic of the components chosen but also by corruptions of the power supply and, eventually, the circuit board layout.

In order to avoid deterioration of the overall performance (measurement accuracy) of the RFISA electronics, in the first instance the well-known fundamental standards for RF circuit/board designs (e.g. sophisticated power supply de-coupling, star grounding of the separated (solid) digital and analog ground planes, proper component placement, and sufficient floor planning [179], [180]) were strictly adhered. For the lumped elements employed for the various discrete LC-filter designs, specific high-frequency components with high self-resonant frequency and high quality factor were chosen. In order to reduce the parasitic effects and, moreover, to save board area consumption due to the large total number of components required for the overall operation of he RFISA electronics, all lumped components were chosen in 0603 small-sized package ($1.6\text{mm} \times 0.8\text{mm} \times 0.7\text{mm}$), which allows a reasonable compromise between small size and soldering manageability.

Furthermore, to ensure compliance to the specifications for differential signaling (LVPECL, LVDS) and proper overall impedance matching to the RFISA electronics' system impedance, all high-frequency (analog) and high-speed (digital) signal traces are designed as single-ended or edge-coupled differential microstrip transmission traces (shown in Figure 5-20a) with a characteristic impedance of $Z_0 = 50\,\Omega$ and $Z_{0,\text{diff}} = 100\,\Omega$, respectively. Latter are required for LVDS and LVPECL signal/clock traces. In general, a microstrip transmission line is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground (GND) or power plane. The structure's dimensions (trace width, W, trace thickness, T, substrate material width, H, and gap, S, between differential traces) along with the dielectric material properties determine Z_0, providing therefore a trace-controlled impedance on the PCB. A reasonable approximation for calculation of the corresponding trace impedances is given in [179] and listed in Appendix A1.

Due to the high-integration of the various DC, RF, and pure digital or mixed analog/digital components (low- or high-speed clocked) and the high-density of single-ended and differential traces (analog and digital), a six-layer PCB structure (shown in Figure 5-20b) is used to

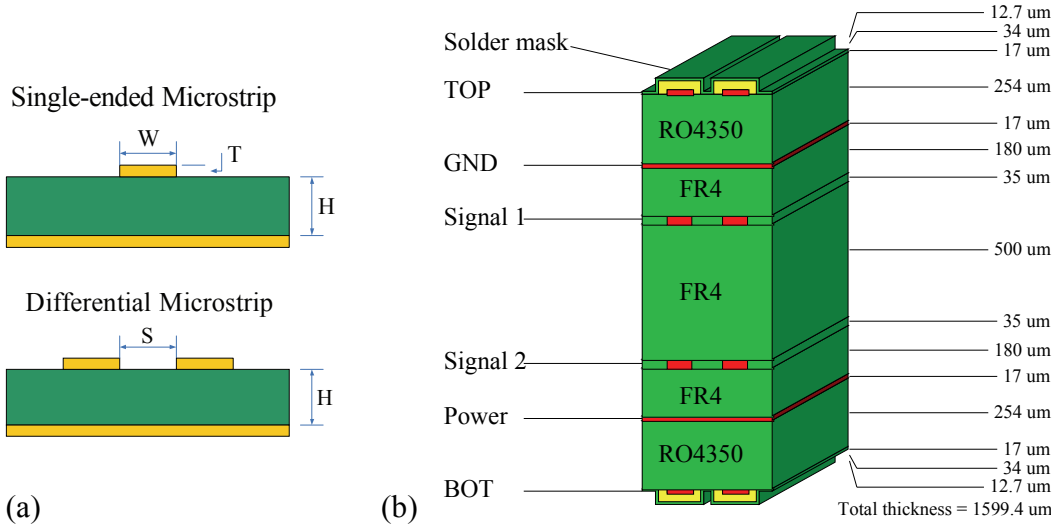

Figure 5-20 Representation of (a) the structures for single-ended and edge-coupled differential microstrip traces, and (b) the board layer stack-up.

ensure proper board layout, to allow for designing dedicated solid ground and power planes, and to choice an appropriate PCB layer stack-up. This also gave the opportunity for isolation between the various sections of the board in order to reduce undesired coupling. For the inner PCB layers, the standard, low-cost FR4 substrate material was chosen. As listed in Table 5-2, the specified electrical properties of FR4, however, exhibit large tolerances and vary with the frequency notably [181]. In order to ensure stable electrical properties over a broad frequency range, especially at frequencies far within the gigahertz range, the special high-frequency material RO4350 was chosen for the top and bottom layer to provide a stable dielectric constant. This is needed to ensure maintaining of the specified frequency characteristic of the designed microstrip filters and the characteristic impedance of the microstrip transmission traces. The substrate thickness of the RO4350 layer was chosen at 254 µm to obtain a microstrip trace width of $W = 0.52\,\text{mm}$, which is in acceptable agreement with the pad size of most components employed. Further remarks to the PCB layout can be found in [169].

Table 5-2 Dielectric constant and dissipation factor for different PCB materials[9].

PCB material	dielectric constant	dissipation factor
FR-4 (glass reinforced epoxy)	4.1 – 5.3	0.002 – 0.02
RO4350 (glass reinforced hydrocarbon)	3.48 ± 0.05	0.0031 @2.5 GHz

[9] Data obtained from printed circuit board vendor ANDUS ELECTRONIC GmbH.

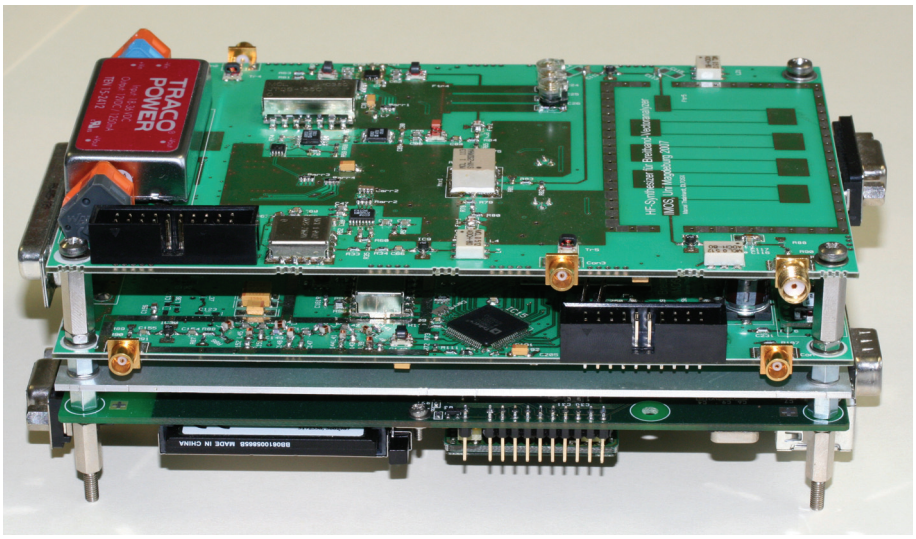

Figure 5-21 Photograph of the electronics system with top view of the synthesizer board. The geometry of the stepped-impedance low-pass filter is to be seen on the right side. The combline band-pass filter is to be seen on the upper edge.

As the final result, the entire RFISA electronics system could be assembled on three europrint size PCBs (160 mm × 100 mm × 60 mm) mounted on top of each other, as shown in Figure 5-21. In contrast to commercial benchtop instruments, this allows for a very compact overall measurement setup for impedance spectrum analysis. Assembling on different PCBs provides functional partitioning of the various units of the RFISA electronics system in order to reduce coupling between parts with high-speed digital electronics, RF/microwave analog electronics, and noise-sensitive DC analog electronics. Board interconnections are made by RG-178 coax cables for the high frequency analog signals and parallel board-to-board stacking connectors for the low-speed digital control signals and the power supply distribution. In order to prevent crosstalk between the boards, additional metal plates for shielding are employed. The metal plates are placed between the bottom sides of the printed circuit boards whereas all RF signals are routed on top side. Detailed photographs of the single printed circuit boards are shown in Appendix A5, and the seperate units are labled.

5.8 Summary of the electronics system

The content of this chapter was focused on the detailed hardware description of the RFISA electronics system. The final circuit design was primarily dictated by the electronic components that were presently available because they had imposed the most constraints on it. With regard to the specifications defined in section 1.4 and the conclusions presented in Chapter 4, a compact electronics (160 mm × 100 mm × 60 mm) was developed, which allows for a portable and stand-alone operation of RF impedance spectrum analysis for *in situ* sensor applications.

A RF sine-wave synthesizer unit was designed, which meets the requirements on compact circuitry (single PCB), high output frequency range (10 kHz – 1 GHz), fine frequency resolution (1 mHz), fast settling time (<10 µs), and output level adjustment (-20 dBm – 15 dBm). To achieve also highest possible spectral quality of the RF output signals synthesized, microstrip filters based on comb-line band-pass and stepped-impedance low-pass geometries were designed to effectively reduce the noise and spurs contamination. To ensure excellent close-to-carrier spectral quality of the output signal, the DDFS circuitry driving the frequency-tunable PLL was separated into the numerical controlled oscillator with Taylor series correction implemented in FPGA and the high-speed high-resolution DAC.

A specific high-frequency PCB substrate material (RO4350) and an appropriate PCB layer stack-up were chosen to make a high-density PCB layout possible and ensure adequate high-frequency performance of the microstrip structures far within the GHz-range. The designed clock synthesizer unit provides enhanced distribution of various high-frequency clock signals with low-jitter performance. The application of the direct-sampling technique has considerably reduced the circuit complexity. The employment of a high-speed ADC with 200 MHz sampling clock avoids noticeable time delays, which otherwise appear due to the successive sampling process of the input signals, and provides fast sensor data acquisition of the RFISA electronics.

Furthermore, with the development of a cascaded amplifier-attenuator chain employed in the analog-front of the direct-sampling digital vector voltmeter unit, weak input signals can adequately be amplified to attain optimum performance of the analog-to-digital conversion (maximum amplification: 54 dB). Beside various common communication and peripheral interfaces, the developed processor unit provides sufficient computing power for extensive data, sensor data computation, and on-board data storing (CF-card) over large periods in stand-alone operation of the RFISA electronics.

Finally, different small-sized sensor interface units installable in specific sensor probes were developed, which provide appropriate adaptation of the measurement sensitivity according to the predictable sensor impedance range, and, in addition, grounded or non-grounded sensor measurements. Separation of the sensor interface unit from the RFISA main electronics had allowed for individual adaptation to the specific sensor application without the need to redesign the overall RFISA electronics.

Chapter 6
Digital system design

An overview of the digital system design implementation in FPGA is given in this chapter. The topic is focused on the concept description of the high-speed digital signal processing, which is required to achieve real-time data computation at the speed of the sampling clock. A complete description of implementation details, in particular for controlling the autarkic measurement task and the electronic components of the analog circuit design, is not provided, as it would extend the scope of this work. A modified processing for the sine-wave fitting is presented, which allows for combined fixed-point and floating-point real-time computation of the complex algorithm by FPGA hardware instead of usually applied digital signal processor.

6.1 FPGA on-chip system architecture and main control

The digital system design of the RFISA electronics is separated into the software-programmable processor implementation (PRO unit, see section 5.5) and the hardware-programmable FPGA implementation. The task of the FPGA is to operate as autarkic frond-end coprocessor of the direct-sampling digital vector voltmeter unit and measuring controller of the entire RFISA electronics system. Due to the autarkic operation, the resources of the processor unit are simultaneously devoted to accomplish higher-level data computation (e.g. sensor data evaluation), off-board process control, or host communication tasks. Opposed to dedicated digital signal processors, a FPGA based DSP system was chosen because modern FPGA devices support both high-speed DSP implementation for real-time data processing of the recorded signals $s_{\mathrm{a,b}}[n]$ and parallel processing tasks to carry out measuring control and data processing simultaneously. The employed Virtex$^{\mathrm{TM}}$-4LX25-10 FPGA device from Xilinx, Inc., offers high integration of logic cells (24192 cells), 48 embedded Xtreme-DSP slices operating fully-pipelined at speeds up to 400 MHz (each Xtreme-DSP slice contains one dedicated 18×18 multiplier, an adder, and an 48-bit accumulator), and 448 programmable user input/outputs supporting single-ended (e.g. LVTTL, LVCMOS) and differential (LVDS) input/output standards.

The on-chip FPGA system architecture is depicted in Figure 6-1. In addition to the various control blocks introduced in Chapter 5, the FPGA system architecture includes the MAIN block for controlling and timing the overall measuring tasks. The SYN block controls the ana-

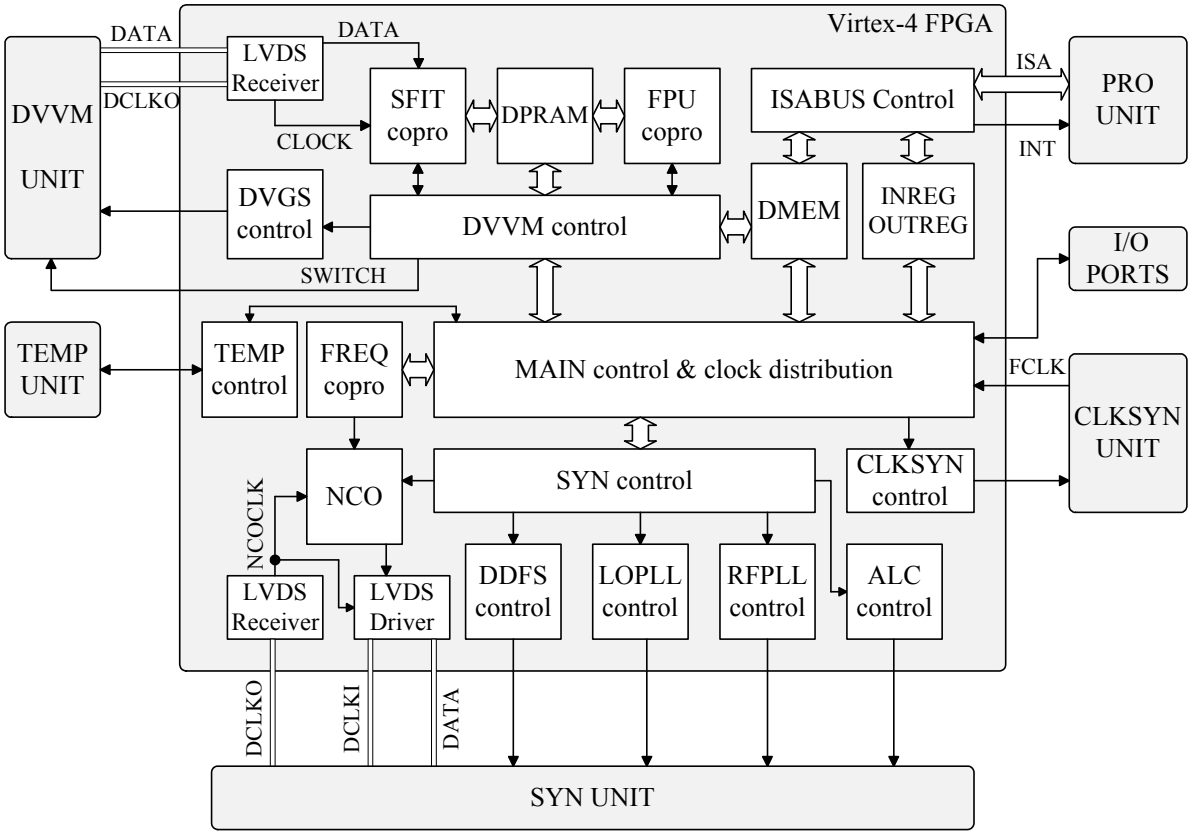

Figure 6-1 Overview of the FPGA on-chip system architecture.

log components of the synthesizer unit and the operation of the numerical controlled oscillator (NCO). The DVVM block is implemented for controlling the analog components and tasks of the digital vector voltmeter unit. The frequency coprocessor (FREQcopro) in Figure 6-1 computes the frequency sweep by updating the current DDFS phase tuning word PTW . Updating the current frequency can be accomplished by either linear frequency sweeps or logarithm frequency sweeps. Latter is required to provide adequate frequency distribution in broadband impedance spectroscopy applications. The SFITcopro block represents the fixed-point coprocessor implementation for the real-time computation of the vector coefficients of the sine-wave fitting (see section 6.2.1). The FPUcopro block represents the floating-point coprocessor implementation to compute the matrix of the sine-wave fitting (see section 6.2.2). Finally, an autarkic on-chip signal averaging operation is implemented to support enhanced noise reduction along with the capability of fast data acquisition .Controlled by the MAIN block, all blocks are implemented in parallelism operation to provide high overall data throughput. This allows fast overall system operation in order to attain short measurement periods.

The main measuring sequence is shown in Figure 6-2. In order to reduce the resource usage of high-speed Xtreme-DSP slices, computation of the sine-wave fitting is subdivided into two consecutive tasks, where sample-free computations are accomplished during the waiting time window of the overall measuring sequence.

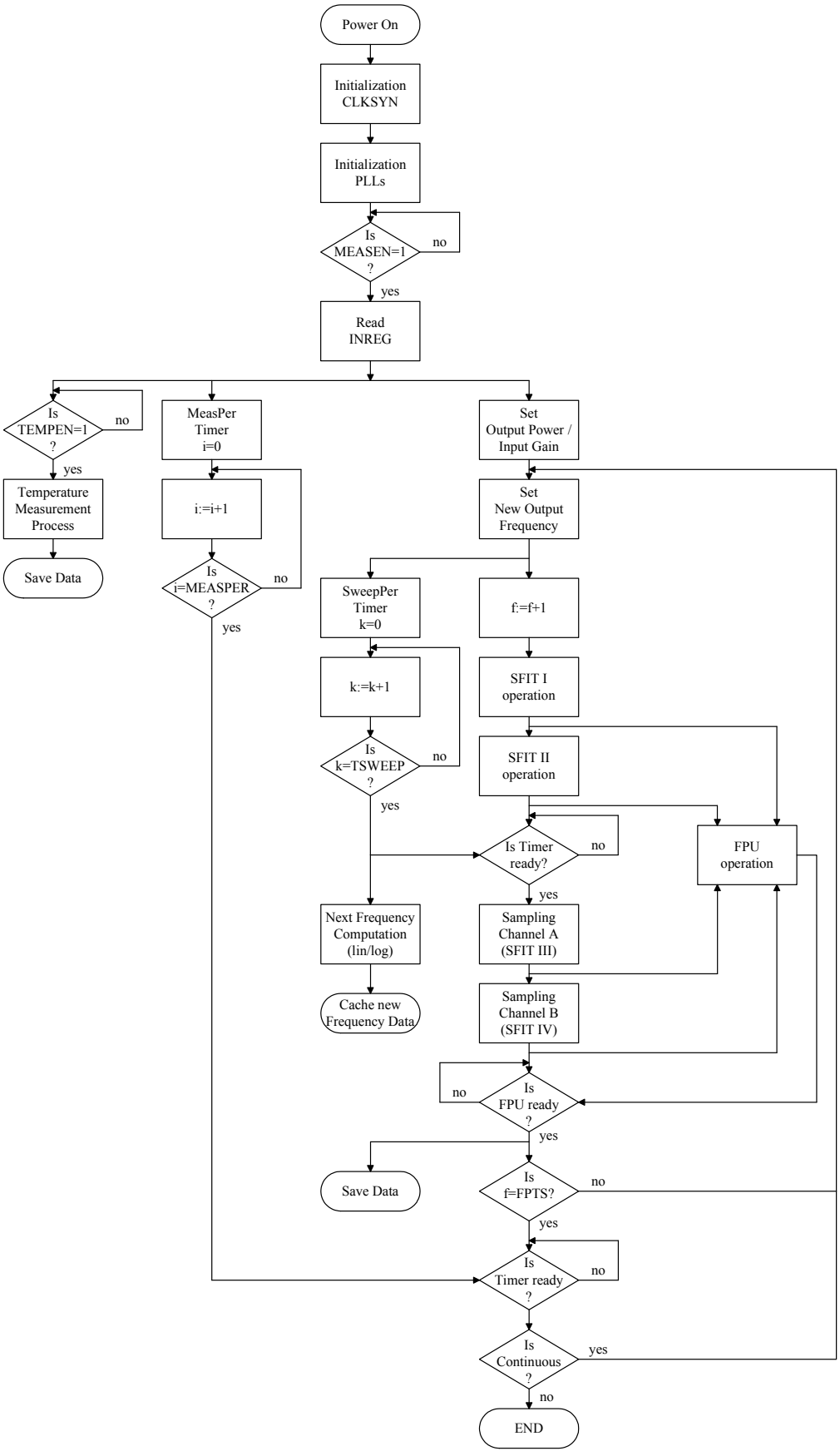

Figure 6-2 Simplified flowchart of the main control measuring sequence.

Flexible time adjustment of the measuring sequence is realized by controlling the frequency sweep period, t_{sweep}, which defines the time between setting the new frequency and recording the input signal s_{a}, and by controlling the measuring sequence period t_{measper}. Latter allows constant time pattern between continuous measurements of impedance spectra in stand-alone operation of the RFISA electronics system. In a accordance to the settling time of the LO-PLL stage (see section 0), the frequency sweep period is determined by $t_{\text{sweep}} \geq 5\,\mu\text{s}$.

Settings of the measuring sequence are specified by the data structure that is written into the input registers (INREG). The data structure includes:

- start frequency (FSTART),
- incremental frequency (FINC),
- number of frequency points (FPTS)
- linear/logarithm sweep frequency mode (LINLOG),
- source power of the SYN unit (SPWR),
- input gain of the DVVM unit (IGAIN),
- frequency sweep period (TSWEEP),
- measuring sequence period (MEASPER),
- number of sample points (SPTS),
- number of averages (NAVG),
- setting of the 15 auxiliary I/O ports (AUX),
- temperature enable (TEMPEN),
- measurement enable (MEASEN).

Controlled by an interrupt request the computed vector parameters of the recorded signals, which are cached into the data memory (DMEM), the corresponding frequencies and the measured temperature data are read by the processor unit in blocks after 512 frequencies. Access to the DMEM and the input/output control registers (INREG/OUTREG) is accomplished by the processor unit via the ISA-BUS. To allow for enhanced data transfer between FPGA and processor unit, the FPGA constitutes an external memory device in the ISA address and data space of the ADNP/1520.

The 20 MHz master clock (FCLK) drives most of the blocks depicted in Figure 6-1. The blocks computing the sine-wave fitting operations (SFITcopro, DPRAM, FPUcopro) are clocked by the high-speed data-output clock of the ADC (200 MHz) as well as a low speed (50 MHz) clock-aligned derivative from it. The NCO block, which produces the discrete sinusoidal waveform $x_{\text{nco}}[n]$ loading the digital-to-analog converter of the DDFS stage, is clocked by the DAC's high-speed data-output clock (400 MHz). All high-speed clocks or their derivatives are properly conditioned by dedicated on-chip digital clock management (DCM) circuits in the FPGA.

6.2 Digital signal processing

The FPGA application as autarkic frond-end coprocessor of the digital vector voltmeter unit (DDVM) aims to co-implement high-speed data acquisition functionality and digital signal processing (DSP) functionality. The data acquisition functionality is required for recording the sampled signals $s_{\mathrm{a,b}}[n]$ at the speed of the sampling clock. The DSP functionality is required for parameter estimation of the recorded signals by computing the three-parameter sine-wave fitting (SFIT) method.

In contrast to software computation using a low-cost data acquisition board as reported in [38] or a digital signal processor as reported in [39], a complete FPGA computation of the DSP routines was preferred because FPGAs provides high level of parallelism. This allows for real-time computation of the three-parameter SFIT at the speed of the ADC's sampling clock ($f_{\mathrm{adcclk}} = 200\,\mathrm{MHz}$) and makes the delay due to the sequential sampling of s_{a} and s_{b} insignificantly. Furthermore, since a flexible, large number of sample points J is desired in order to reduce the noise sensitivity of the SFIT method, this approach avoids the need for resource-rich FPGA memory implementation for storing the incoming samples $s_{\mathrm{a,b}}[n]$. Thus, a flexible DSP performance even with large values of J is provided. Particularly, with regard to the weak output signals of the sensor interface unites introduced in section 5.6 and the significantly decreased signal-to-noise ratio at high frequencies due to the applied direct-sampling technique (see section 4.2), the capability to operate with a flexible, large number of total sample points became essential. However, to avoid resource-rich FPGA implementation for determination the closed form least-square solution (4.19), the computation effort for the best-fit approach (4.18) had to be simplified.

In order to obtain minimum error for the solution in form of (4.18), the partial derivatives with respect to the target parameters being fit to zero

$$\frac{\partial \varepsilon}{\partial A_{\mathrm{a,b}}} = 0 = -2\sum_{n=1}^{J}\left[\cos\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right)\cdot\left(s_{\mathrm{a,b}}[n] - A_{\mathrm{a,b}}\cos\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) - B_{\mathrm{a,b}}\sin\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) - G_{\mathrm{a,b}}\right)\right] \quad (6.1)$$

$$\frac{\partial \varepsilon}{\partial B_{\mathrm{a,b}}} = 0 = -2\sum_{n=1}^{J}\left[\sin\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right)\cdot\left(s_{\mathrm{a,b}}[n] - A_{\mathrm{a,b}}\cos\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) - B_{\mathrm{a,b}}\sin\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) - G_{\mathrm{a,b}}\right)\right] \quad (6.2)$$

$$\frac{\partial \varepsilon}{\partial G_{\mathrm{a,b}}} = 0 = -2\sum_{n=1}^{J}\left(s_{\mathrm{a,b}}[n] - A_{\mathrm{a,b}}\cos\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) - B_{\mathrm{a,b}}\sin\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) - G_{\mathrm{a,b}}\right) \quad (6.3)$$

yield the linear system of equations (6.4) that must be solved.

$$\begin{pmatrix} A_{\mathrm{a,b}} \\ B_{\mathrm{a,b}} \\ G_{\mathrm{a,b}} \end{pmatrix} = \mathbf{D}^{-1} \cdot \begin{pmatrix} YC_{\mathrm{a,b}} \\ YS_{\mathrm{a,b}} \\ Y_{\mathrm{a,b}} \end{pmatrix} = \begin{pmatrix} CQ & SC & C \\ SC & SQ & S \\ C & S & J \end{pmatrix}^{-1} \cdot \begin{pmatrix} YC_{\mathrm{a,b}} \\ YS_{\mathrm{a,b}} \\ Y_{\mathrm{a,b}} \end{pmatrix} \tag{6.4}$$

where

$$S = \sum_{n=1}^{J} \left[\sin\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) \right] \tag{6.5}$$

$$C = \sum_{n=1}^{J} \left[\cos\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) \right] \tag{6.6}$$

$$SQ = \sum_{n=1}^{J} \left[\sin^2\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) \right] \tag{6.7}$$

$$CQ = \sum_{n=1}^{J} \left[\cos^2\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) \right] \tag{6.8}$$

$$SC = \sum_{n=1}^{J} \left[\sin\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) \cdot \cos\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) \right] \tag{6.9}$$

$$Y_{\mathrm{a,b}} = \sum_{n=1}^{J} \left[s_{\mathrm{a,b}}[n] \right] \tag{6.10}$$

$$YS_{\mathrm{a,b}} = \sum_{n=1}^{J} \left[s_{\mathrm{a,b}}[n] \cdot \sin\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) \right] \tag{6.11}$$

$$YC_{\mathrm{a,b}} = \sum_{n=1}^{J} \left[s_{\mathrm{a,b}}[n] \cdot \cos\left(2\pi f_{\mathrm{o}} n t_{\mathrm{s}}\right) \right] \tag{6.12}$$

Calculation of the inverse matrix $\mathbf{D}^{-1}$ yields

$$\mathbf{D}^{-1} = \frac{1}{|\mathbf{D}|} \cdot \begin{pmatrix} -SQ \cdot J + S^2 & SC \cdot J - S \cdot C & SQ \cdot C - SC \cdot S \\ SC \cdot J - S \cdot C & -CQ \cdot J + C^2 & -C \cdot SC + CQ \cdot S \\ SQ \cdot C - SC \cdot S & -C \cdot SC + CQ \cdot S & SC^2 - SQ \cdot CQ \end{pmatrix} = \frac{1}{|\mathbf{D}|} \cdot \begin{pmatrix} c_{11} & c_{12} & c_{13} \\ c_{21} & c_{22} & c_{23} \\ c_{31} & c_{32} & c_{33} \end{pmatrix} \tag{6.13}$$

where $|\mathbf{D}| = SC^2 \cdot J - 2 \cdot SC \cdot S \cdot C - SQ \cdot CQ \cdot J + SQ \cdot C^2 + CQ \cdot S^2$ is the determinant of $\mathbf{D}$. Furthermore, from (6.13) it is obviously that $c_{12} = c_{21}$. With insertion of (6.13) into (6.4), the target fitting parameters $A_{\mathrm{a,b}}$ and $B_{\mathrm{a,b}}$ can be obtained from (6.14) and (6.15), respectively.

$$A_{\mathrm{a,b}} = \frac{1}{|\mathbf{D}|} \cdot \left(c_{11} \cdot YC_{\mathrm{a,b}} + c_{12} \cdot YS_{\mathrm{a,b}} + c_{13} \cdot Y_{\mathrm{a,b}} \right) \tag{6.14}$$

$$B_{\mathrm{a,b}} = \frac{1}{|\mathbf{D}|} \cdot \left(c_{12} \cdot YC_{\mathrm{a,b}} + c_{22} \cdot YS_{\mathrm{a,b}} + c_{23} \cdot Y_{\mathrm{a,b}} \right) \tag{6.15}$$

Since $|\mathbf{D}|$ is only a scaling factor dependent on the instantaneous frequency f_o and independent of the content of the data record $s_{a,b}[n]$, it will be canceled out by computation the vector voltage ratio $r(j\omega) = V_a(j\omega)/V_b(j\omega)$ in (2.2). Hence, it is not needed to determine $|\mathbf{D}|$, simplifying the implementation of DSP routines into the FPGA hardware as well. Computation of $A_{a,b}$ and $B_{a,b}$ without $|\mathbf{D}|$ is consecutively executed for both recorded signals at the instantaneous frequency f_o. The required operation are accomplished by specific DSP routines implemented into the FPGA blocks: SFITcopro that computes the coefficients (6.5) – (6.12) and FPUcopro that sequentially computes the intermediate data to determine the matrix elements ($c_{11}, c_{12}, c_{13}, c_{22}, c_{23}$) in (6.13). Finally, the FPUcopro also solves (6.14) and (6.15). The obtained parameter values of $A_{a,b}$ and $B_{a,b}$ along with the respective frequency values are stored into the DMEM in Figure 6-1. Computation of the complex voltage ratio

$$r(j\omega) = \frac{B_a(\omega) + jA_a(\omega)}{B_b(\omega) + jA_b(\omega)} = |r(\omega)| \angle \phi(\omega) \tag{6.16}$$

and, finally, the complex impedance $Z(j\omega)$ without calibration data according to (2.2) or with calibration data according to (2.3) is executed by software routines in the processor unit of the RFISA electronics system.

The FPGA implementation of the SFITcopro and FPUcopro blocks is described in the following sections. In order to provide a large number of total sample points *J* without delaying the overall measuring sequence, the design efforts of the corresponding DSP implementations were concentrated on high-speed clocking capability and high data throughput. High-speed clocking and high date throughput could be realized by extensive utilization of parallel DSP operations and well-designed allocation of a sequential data flow. Computation of the eleven coefficients (6.5) – (6.12) (taking into consideration that (6.10) – (6.12) must be computed for both sampled input signals) involves ordinary multiply-accumulate operations, which can gainfully be implemented into specific FPGA logic recourses. The total number of multiply-accumulate cycles depends on the value of *J*. With the derivation described before, computation of (6.14) and (6.15) requires fifteen intermediate calculations to determine the required five matrix elements ($c_{11}, c_{12}, c_{13}, c_{22}, c_{23}$) in (6.13) and lastly ten calculation steps to solve (6.14) and (6.15), giving a fixed total number of operations of twenty-five.

Prerequisite for application the three-parameter sine-wave fitting is the exact knowledge of the frequency value f_o of the instantaneous signal being fitted. To ensure exact frequency knowledge two techniques are applied. First, as described in section 5.4, the RF-PLL reference signal and the ADC/DAC sampling clock signals are derived from a single 20 MHz system master clock in the clock synthesizer unit of the RFISA electronics system. This ensures that frequency fluctuations of the master clock affect all signals in the same manner. Second,

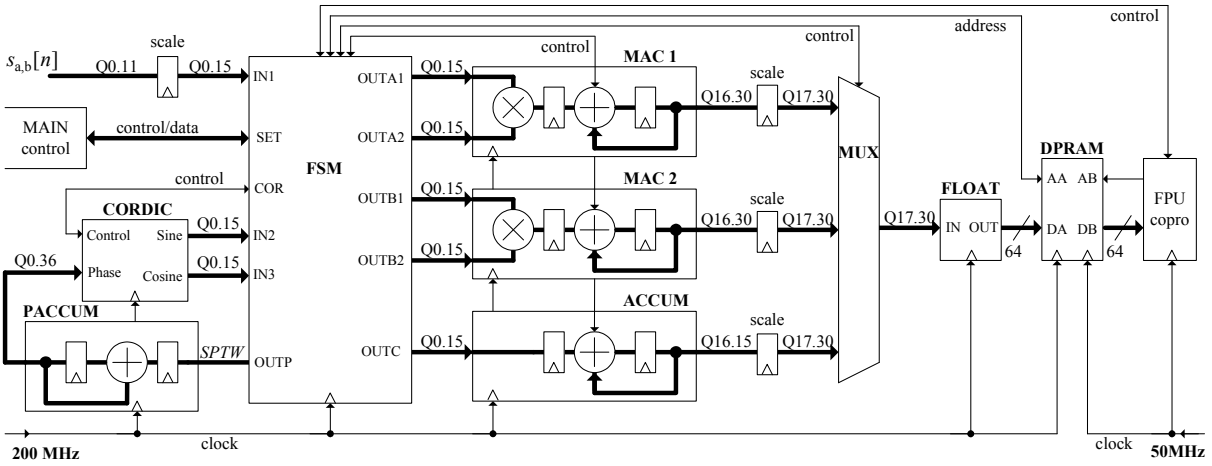

Figure 6-3 Block diagram of the fixed-point sine-wave fitting coprocessor design.

in order to avoid divergences due to the finite numerical precision by FPGA computations, the implemented FREQcopro computes not only the frequency sweep but also the sine-fit phase tuning word, $SPTW$, from the instantaneous DDFS phase tuning word PTW. This ensures proper derivation of the $SPTW$ from the PTW. The sine-fit phase tuning word is the binary representation of the instantaneous stimulus frequency f_o with respect to the sampling frequency f_{adcclk}, given by

$$SPTW = (PTW - OTW) \cdot r_{clk} \cdot N_{lopll} \tag{6.17}$$

where OTW is the binary representation of the minimum DDFS output frequency $f_{ddfs,min}$ in (5.5), $r_{clk} = f_{ddfsclk} / f_{adcclk} = 2$ the ratio between the DAC and ADC sampling clock, and N_{lopll} the LO-PLL feedback divider value (5.4). Since the values of the clock ratio r_{clk} and the feedback divider N_{lopll} are chosen to a power-of-two, the required multiply operation can be replaced by simple shift operation.

6.2.1 Sine-wave fitting coprocessor

The block diagram of the SFITcopro unit is shown in Figure 6-3. The efforts of the SFITcopro implementation were focused on an optimized balance between high-speed operation performance and reasonable utilization of the FPGA resources. The finite state machine (FSM) controls the timing and the data flow of the SFIT processing sequence and interacts with the higher-level MAIN control block in Figure 6-1. The 37-bit accumulator (PACCUM) produces the phase stream that addresses the CORIDC processor that computes the digital sine and cosine waveform stream. Two dedicated Xtreme DSP slices (MAC 1 – 2) perform in parallelism the multiply-accumulate operation and one ACCUM block accomplishes the accumulator operation. The results for the coefficients are formed after *N* operations and the FLOAT block

converts the respective coefficient data from the fixed-point integer representation to the double format (64 bits) floating-point representation. Finally, the calculated coefficients are stored in a dual-port random access memory (DPRAM) before the operations of the FPUcopro start. The DPRAM is randomly accessible at Port A from the SFITcopro storing the eleven coefficient data. At Port B, the FPUcopro reads the coefficient data for the floating-point operations.

The CORDIC (COordinate Rotation DIgital Computer [182]) is a specific hardware-efficient iterative algorithm using only shift and add operation to perform various trigonometric and vector transformation operations, such as computation of the sine and cosine values or the polar-to-rectangular bidirectional transformation of an input vector. A comprehensive description for the iterative operation of the CORDIC algorithm can be found in e.g. [148] [182]. In principle, there are a number of configurations to implement the CORDIC algorithm into FPGA. The complexity depends on the clocking speed versus area tradeoff. Hence, in order to gain a logic implementation optimized for both speed and area, a parameterizable logic core offered from Xilinx, Inc., is employed.

As mentioned in section 6.1, computation of the eleven coefficients at each frequency is subdivided into four processing steps (SFIT I – IV, see Table 6-1). This allows multiple utilization of logic blocks, which significantly reduces the resource requirements. The SFITcopro in autarkic operation accomplishes sequential processing of step SFIT I – II and SFIT III – IV. The start for executing the entry processing steps I and III is controlled by the higher-level MAIN control sequence depicted in Figure 6-2. At each processing step the MAC 1 – 2 and ACCUM operations are carried out in parallelism. Since autarkic processing of the SFIT I and II steps is accomplished during the essential waiting time window t_{sweep} of the overall measuring sequence, the sequential operation does not significantly delay the measurement period per frequency. The SFIT III and VI processing steps comprise the successive sampling processes of signal s_{a} and s_{b}.

Table 6-1 Processing steps of the sine-wave fitting computation.

operation	SFIT I	SFIT II	SFIT III	SFIT IV
MAC 1	$\sum \mathrm{sine} \times \mathrm{sine} = \mathrm{SQ}$	$\sum \mathrm{sine} \times \mathrm{cosine} = \mathrm{SC}$	$\sum \mathrm{s_a} \times \mathrm{sine} = YS_{\mathrm{a}}$	$\sum \mathrm{s_b} \times \mathrm{sine} = YS_{\mathrm{b}}$
MAC 2	$\sum \mathrm{cosine} \times \mathrm{cosine} = \mathrm{CQ}$	—	$\sum \mathrm{s_a} \times \mathrm{cosine} = YC_{\mathrm{a}}$	$\sum \mathrm{s_b} \times \mathrm{cosine} = YC_{\mathrm{b}}$
SUM	$\sum \mathrm{sine} = S$	$\sum \mathrm{cosine} = C$	$\sum \mathrm{s_a} = Y_{\mathrm{a}}$	$\sum \mathrm{s_b} = Y_{\mathrm{b}}$

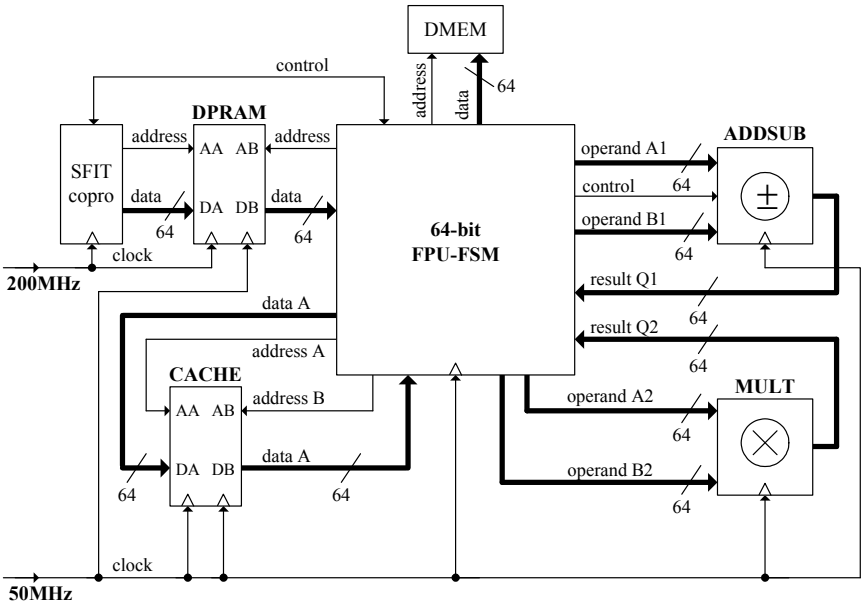

Figure 6-4 Block diagram of the floating-point coprocessor design.

The various fixed-point operands in Figure 6-3 are represented by the two's complement fractional Q*x*.*y* notation. In this notation *x* represents the bits for integer portion and *y* the bits for fractional portion; the total number of bits is 1+*x*+*y* including the sign bit in the most significant bit position. According to the ADC resolution, the input samples $s_{a,b}[n]$ are represented by a data word size of 12 bit. The word size of the number of sample points is specified with 16 bit, allowing for $J = 2^{16} = 65536$ accumulations in order to provide enhanced noise suppression by the sine-wave fitting method.

With a careful circuit hardware description in VHDL (Very-High-Speed Integrated Circuits Hardware Description Language) to implement the DSP functionalities into the FPGA, extensive use of pipelining for time-critical sections, and specific adaptation to the internal Virtex^{TM}-4LX25 structure to gainfully benefit from the dedicated hardware recourses, it was attained to operate the sine-wave fitting coprocessor with non-truncated data word sizes at the high speed of the ADC's sampling clock ($f_{adcclk} = 200\,\text{MHz}$). This allows real-time processing of the incoming samples $s_{a,b}[n]$ to compute the corresponding coefficients (6.10), (6.11), and (6.12).

6.2.2 Floating-point coprocessor

The FPUcopro design in Figure 6-4 aims to sequentially compute the twenty-five intermediate calculations in double format (64 bits) floating-point operations to solve (6.14) and (6.15). For this purpose, an ADDSUB block performing floating-point addition/subtraction operations and a MULT block performing floating-point multiplication operations are designed. The finite state machine (FPU-FSM) in autarkic operation executes the control sequence for

processing and timing the sequential data flow of the operands and the floating-point computation tasks. Intermediate results are cached into the CACHE dual-port memory block. Interaction with the higher level finite state machine of the SFITcopro is accomplishes via some control lines. Due to the hardware complexity of FPUcopro design, the operation clock frequency is set at 50 MHz and derived from the ADC's sampling clock (200 MHz) by using a dedicated DCM core in the FPGA. For the floating-point arithmetic operations, highly optimized IP (intellectual property) cores offered from Xilinx, Inc., are employed to combine speed and efficient resources usage.

Memory access and computation of the intermediate calculations is executed in a specific operation sequence in order to produce high data throughput. The operation sequence allows in parallelism multiplication and addition/subtraction operations applied to the stored coefficient data or the cached intermediate results. The operation sequence for computation the intermediate results for the matrix elements in (6.13) starts when the SFIT I processing step in section 6.2.1 is finished and ends when the SFIT III processing step (sampling of signal s_{a}) is completed. Then, the second computation sequence starts to solve (6.14) and (6.15) for s_{a}. When sampling of signal s_{b} is completed, the third computation sequence starts to solve (6.14) and (6.15) for s_{b}. As described before, determining of $|\mathbf{D}|$ is not needed. Finally, computed values for $A_{\mathrm{a,b}}$ and $B_{\mathrm{a,b}}$ will be stored in the output data memory DMEM in Figure 6-1.

Due to the almost parallel processing of the SFITcopro and FPUcopro operation sequences and with a reasonable assumption of $J \geq 512$ total number of samples, the latency due to pipeline processing and channel switching are negligible. Thus in accordance to the processing steps listed in Table 6-1, the total computation time for the sine-wave fitting can reasonably be approximated by

$$t_{\mathrm{sfit}} \approx 4 \cdot J \cdot t_{\mathrm{s}} \quad \text{for } J \geq 512 \tag{6.18}$$

where $t_{\mathrm{s}} = 1/f_{\mathrm{adcclk}} = 5\ \mathrm{ns}$ is the sampling time with regard to sampling frequency $f_{\mathrm{adcclk}} = 200\ \mathrm{MHz}$. Taking into consideration the total record time ($2 \cdot J \cdot t_{\mathrm{s}}$) for sampling both signals (s_{a} and s_{b}) and the essential waiting time window ($t_{\mathrm{sweep}} \geq 5\,\mu\mathrm{s}$), the implemented high-speed parallel DSP sequences allow large data word sizes to attain high computation precision and do not significantly delay the total measuring sequence. Note, the general case $J \geq 512$ also ensures $t_{\mathrm{sweep}} \geq 5\,\mu\mathrm{s}$ due to the sequential execution of the processing steps SFIT I and SFIT II in Table 6-1. The total processing time, t_{proc}, for the measuring sequence depicted in Figure 6-2 with $J \geq 512$ depends on the chosen sweep time t_{sweep} and is given by

$$\begin{aligned} t_{\mathrm{proc}} &= 4 \cdot J \cdot t_{\mathrm{s}} + t_{\mathrm{seq}} && \text{for } t_{\mathrm{sweep}} < t_{\mathrm{sfit}}/2 \\ t_{\mathrm{proc}} &= t_{\mathrm{sweep}} + 2 \cdot J \cdot t_{\mathrm{s}} + t_{\mathrm{seq}} && \text{for } t_{\mathrm{sweep}} > t_{\mathrm{sfit}}/2 \end{aligned} \tag{6.19}$$

where $t_{seq} = 2.5\,\mu s$ specifies the overall time of the intermediate procedures in Figure 6-2, which are clocked by the 20 MHz RFISA master clock. For the case $t_{sweep} < 2 \cdot J \cdot t_s$, $J = 2^{15}$ samples per recorded signal can be taken without exceeding the specified maximum processing time (1 ms per frequency of the entire spectrum, see section 1.4). This maintains fast data acquisition of the RFISA electronics system even with a large total number of samples per signal and thus allows for sufficient noise suppression by the sine-wave fitting method. Furthermore, when t_{sweep} is set in the order of the maximum settling time of the synthesizer stage (5 µs), the total processing time per frequency can reasonably by estimated by $t_{proc} \approx t_{sfit}$, when $J > 512$. Hence, change between very fast data acquisition and enhanced noise suppression due to the averaging process of the sine-wave fitting can easily be done by scaling *J*.

6.3 Summary of the digital system design

The topic of the previous chapter was focused on the primary parts of the digital system design implementation in FPGA. The main task of the FPGA is the autarkic operation as frond-end coprocessor for the direct-sampling vector voltmeter unit and measuring controller of the entire RFISA electronics system. Latter allows for continuous data acquisition without interruption by the processor unit. This gives the RFISA processor unit time resources for parallel processing of higher-level sensor data computation and host communication tasks. The combined fixed-point and floating-point DSP implementation of a modified sine-wave fitting in FPGA hardware provides real-time computation of the vector components (real and imaginary part) of the recorded signals at the high-speed ADC sampling clock. With the extensive application of parallel DSP operations and a well-designed allocation of a sequential data flow, a high data throughput with large data word sizes is achieved. Latter is required to ensure high numerical precession for the sine-wave fitting to be computed by the finite DSP implementation. Thus, in spite of the sequential sampling process of the input signals to be recorded and the essential waiting time due to the settling time of the RFISA synthesizer unit, fast data acquisition is achieved, even when a large number of sample points for better noise suppression is chosen.

When the frequency sweep time is set in the order of the synthesizer's settling time, adjustment of the total number of sample points allows for either enhanced noise suppression with many sample points or very fast measurements with fewer sample points. The minimum (complete) data processing time for one frequency per spectrum is 12.74 µs and the maximum data processing time is approximately 1.3 ms. In comparison to commercial benchtop instruments, very fast data acquisition can be achieved to establish impedance spectroscopy in the application of real-time kinetic analysis with quartz crystal resonators [47] or resonant sensor arrays (see section 7.3.1).

Chapter 7
Measurement results

The following measurement have been done to prove the applicability of the developed electronics system. The first measurements have been focused on the evaluation of the spectral performance of the synthesizer output signal in comparison with the expected values for the maximum power level of spurs and harmonics. The impedance measurement accuracy has been proved with a quartz crystal resonator. A comparsion of the impedance spectra measured with the electronics system and a standard benchtop instrument as reference has given information about the attainable measurement precision. The application of the electronics system for narrowband impedance spectroscopy on acoustic microsensors has been tested with a langasite bulk acoustic wave resonator for high temperature in situ sensor applications and with a lateral field excited quartz crystal resonator for in-liquid sensor applications. The broadband impedance measurement performance has been proven with a capacitive sensor probe for dielectric spectroscopy.

7.1 Noise and spurious performance of the synthesizer unit

The aim of section 5.2 was to present the developed hybrid synthesizer design, which results from a reasonable compromise between the desired minimized circuitry, the electronic components that were presently available, and the efforts to achieve low noise and spurs contamination at the output frequency. With regard to the standards specified in [48], the requirements on the noise and spurious performance of the synthesizer output signal were defined in section 1.4. They include a minimum sideband attenuation of –60 dBc in the range of ±10% to the carrier frequency (narrowband spectral performance) and a usual spur and harmonic attenuation of –40 dBc (wideband spectral performance). In accordance to the conclusions presented in section 4.1.4, several design efforts were described in section 5.2 to reduce the close-to-carrier noise and spurs contamination originated from the wideband DDFS-driven LO-PLL stage. Furthermore, different filter geometries in microstrip technique were employed to reduce the broadband noise and harmonic contamination caused by the mixer operation. Hence, the noise and spurious performance of the RFISA synthesizer unit was verified on the two critical signals: (a) at the output of the DDFS stage and (b) at the synthesizer' IF-output. For this purpose, the respective signal spectra were measured using the benchtop Spectrum Analyzer 4396A from Agilent, Inc.

As mentioned in section 5.2.1, determination of the spectral performance for all output signals generated by the wideband-tunable DDFS stage is not feasible. Hence, in accordance to the simulated output spectra of the numerical controlled oscillator in section 5.2.1, the same odd phase tuning word was chosen for verification the spurious performance of the DDFS stage. Figure 7-1 shows output specta of the DDFS output signal ($f_{\mathrm{ddfs}} = 49.99$ MHz, output power level 6 dBm) in comparison with the output spectra of the signal generated by a commercial Arbitrary Function Generator (AFG2020) from Tektronix, Inc. The the narrowband spectral representation ($f_{\mathrm{ddfs}} \pm B_{\mathrm{lopll}}$) is related to the loop bandwidth of the LO-PLL ($B_{\mathrm{lopll}} = 1\,\mathrm{MHz}$) whereas the wideband spectral representation is related to the bandwidth of the DDFS band-pass reconstruction filter (25 MHz – 75 MHz).

It is obvious from the spectrum plots in Figure 7-1a-b that the critical design specifications $SNR_{\mathrm{ddfs}} \geq 90\,\mathrm{dB}$ and $SFDR_{\mathrm{ddfs}} \geq 70\,\mathrm{dBc}$ in the range of $f_{\mathrm{ddfs}} \pm B_{\mathrm{lopll}}$ are properly met. Taking into account the chosen resolution bandwidth, *RBW*, of the Spectrum Analyzer[10] (labeled in the corresponding plot legends), the normalized broadband noise floor in Figure 7-1a is lower than -100 dBc/Hz. As labeled in Figure 7-1a, the power level of the sole sideband spurs is -83 dBc in the range of $f_{\mathrm{ddfs}} \pm 750\,\mathrm{kHz}$. These are good conditions in order to ensure the required spectral quality within the loop bandwidth $B_{\mathrm{lopll}} = 1\,\mathrm{MHz}$ of the DDFS-driven LO-PLL stage. The spectrum plot over the bandwidth of the DDFS band-pass reconstruction filter in Figure 7-1b shows also good spectral quality of the DDFS output signal, where the dominant spurious sidebands has a power level of –64 dBc in the range of $f_{\mathrm{ddfs}} \pm 10\,\mathrm{MHz}$.

In contrast, the spectrum plots of the AFG2020 (Figure 7-1c-d) reveal a considerably poorer quality of the synthesized output signal. Evidently, a large number of close-to-carrier spurious signals appear, impairing the spectral quality of the output signal significantly. Furthermore, some spurious magniudes exceed the critical limit of –70 dBc. The high-level spurious signals are spreaded out across the entire frequency range in the wideband plot in Figure 7-1d.

The spectral performance of the synthesizer IF-output signal, which eventually stimulates the particular sensor, is shown in Figure 7-2 for different frequencies in the range of 9.995 MHz to 889.775 MHz. The spectra of the output signal in the vicinity of $\pm 10\%$ to the respective carrier frequency f_{o} (narrowband performance) and over a range from 1 MHz to 1.8 GHz (wideband performance) are represented. The upper measurement bound was determined by the frequency limitation of the used Spectrum Anaylzer. The carrier was adjusted to a constant power level of 10 dBm and the measured power levels are referenced to the carrier power level. It is evident from the spectral representations that the requirements on the spectral quality of the synthesizer's output signal for all synthesized low-frequency and high-frequency signals are adequately met.

[10] *P* (dB/Hz) = (measured value in dB) – 10log(*RBW* of spectrum analyzer)

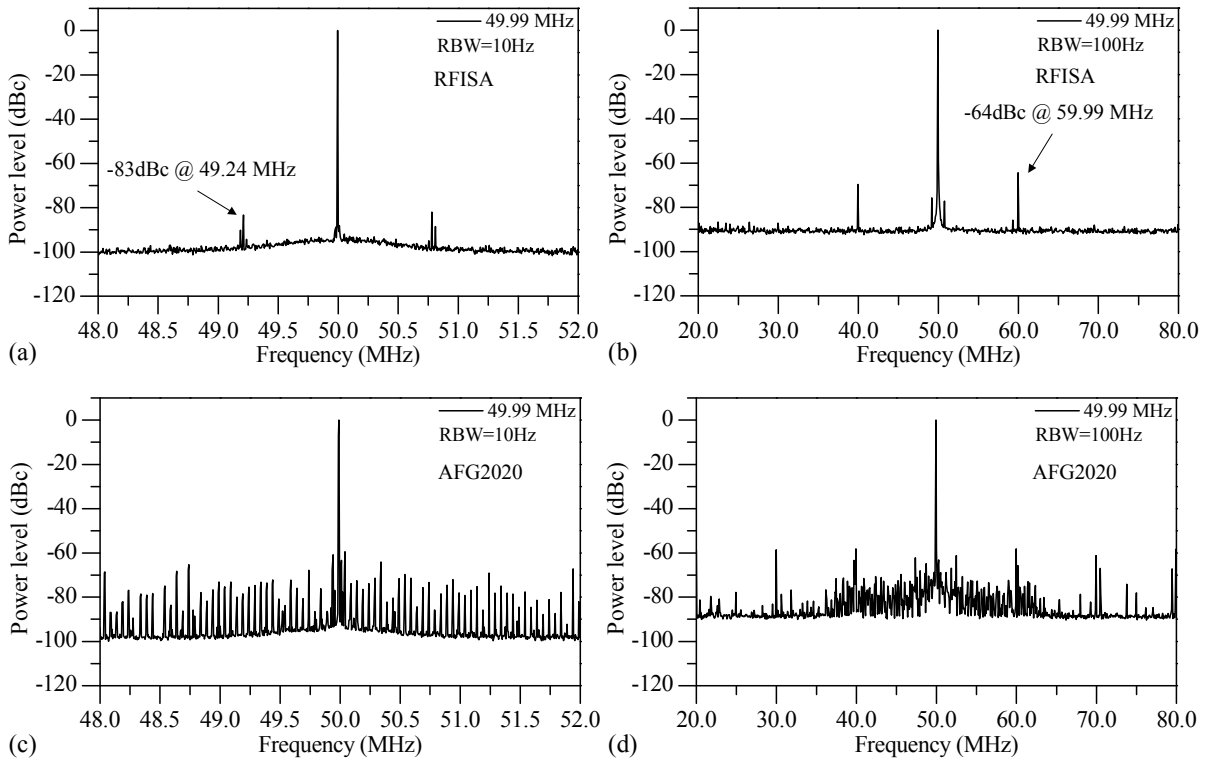

Figure 7-1 Output spectra of the RFISA direct digital frequency synthesizer and the reference synthesizer AFG2020 for a signal frequency of 49.99 MHz. Plots (a) and (b) show the narrowband and wideband, respectively, spectral representation of the RFISA direct digital frequency synthesizer output signal. Plots (c) and (d) show the narrowband and wideband, respectively, spectral representation of the reference synthesizer output signal.

The power level of harmonics, where the second ha rmonic is always the strongest (labeled in the corresponding wideband plots), is maximum -40 dBc and the power level of the spurious sidebands (labeled in the corresponding narrowband plots) is maximum –70 dBc. A very low close-to-carrier background noise floor is also evident in Figure 7-2a.

Furthermore, it is obvious from Figure 7-2b that the power level of the otherwise powerful sum product of the mixer operation (9.995 MHz + 1.16 GHz) is sufficiently attenuated (-65 dB). The normalized broadband noise floor is at least lower than –100 dBc/Hz. However, permanent spurious signal in the range from 50 MHz to 600 MHz are apparent in the wideband plots. They are independent of the certain carrier frequency. Further measurements have shown that the majority of these spurious signals are originated from spurious signals of the LO-PLL stage. Due to the mixer operation, spurious signals from the LO-PLL are down-converted into the IF-Filter's 1 GHz pass-band bandwidth and cannot be filtered out by the IF-Filter. Nevertheless, the power level of the permanent spurious signal is below the critical limit of –60 dBc.

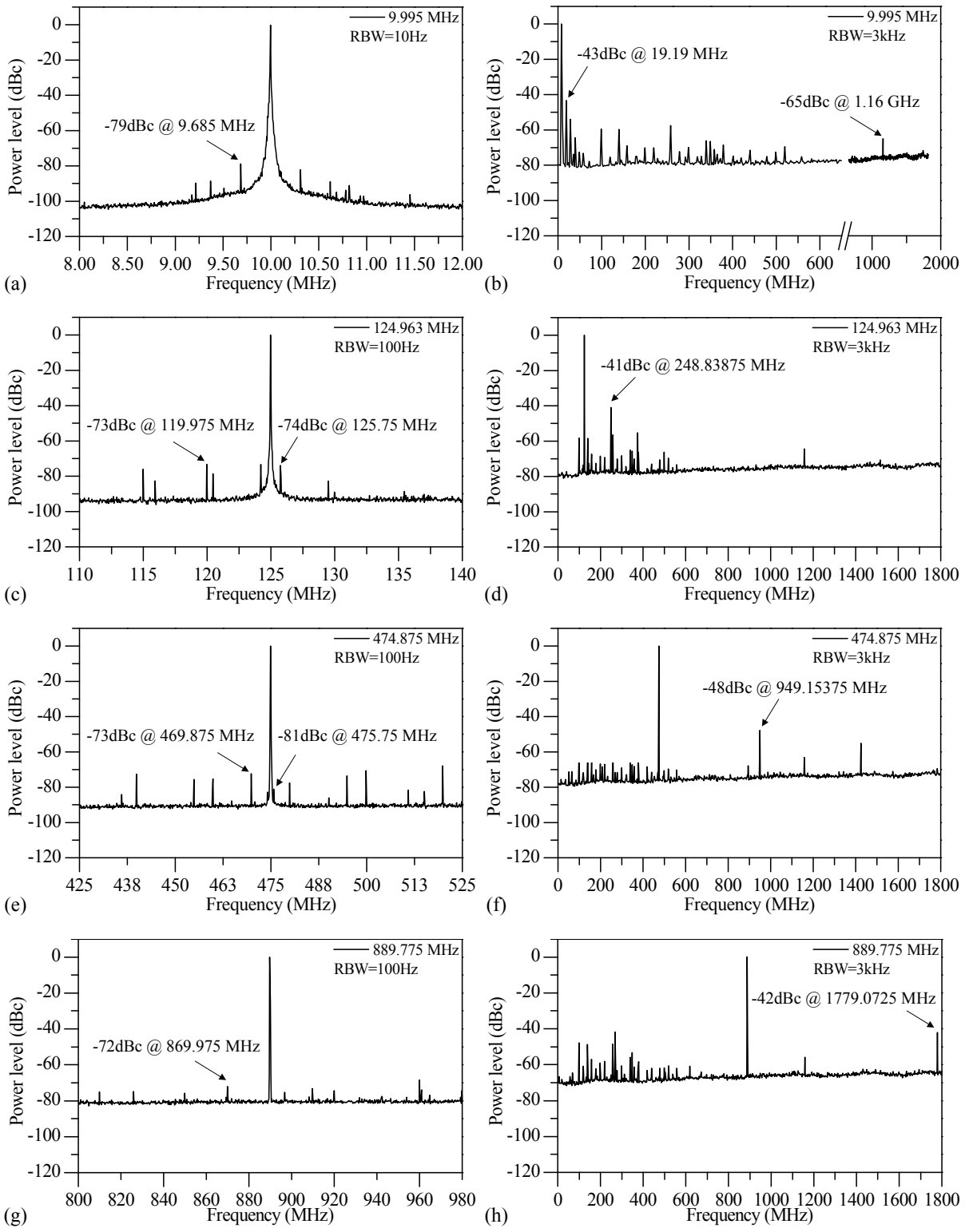

Figure 7-2 Noise and spurs performance of the synthesizer's output signal for various frequencies. The frequency of the desired carrier and the resolution bandwidth (RBW) of the spectrum analyzer are labeled in the plot legend. The plots on the left side show the narrowband spectral performance in the range of ±10% of the carrier. The plots on the right side show the wideband spectral performance.

A summarization of the noise and spurious performance of the RFISA sysnthesizer unit is listed in Table 7-1.

Table 7-1 Noise and spurious performance of the RFISA synthesizer unit.

parameter	maximum power level
spurious sideband	–70 dBc
harmonics	–40 dBc
mixer products	–65 dBc
broadband noise floor	–100 dBc/Hz

7.2 Impedance measurement precision

A comparison of the impedance spectra measured with the RFISA electronics system and the reference benchtop instrument HP4395A from Hewlett Packard, Inc., had allowed for evaluating the attainable impedance measurement precision. The comparison was performed for narrowband impedance spectroscopy on a commercial 5 MHz quartz crystal resonator (QCR) device. The reference benchtop instrument HP4395A is a combined impedance-network-spectrum analyzer. The impedance spectra were measured uisng the passive transmission-measurement sensor interface (see Figure 5-17a), which was applied to the RFISA electronics system and the HP4395A. The QCR device as load condition was chosen with regard to the sensor applications, which will be presented in section 7.3.1 and section 7.3.2, in order to estimate the measurement precision for determination of resonant impedance spectra. Moreover, the measurement of an unloaded QCR device in the vicinity of its resonance and antiresonance had allowed for evaluation the measurement precision in a wide impedance range, from low ohms up to few megaohms, with a single impedance spectrum measurement.

The narrowband impedance spectrum measurements were performed at the fundamental resonance (5 MHz) and the third overtone resonance (15 MHz) and the impedance data were determined according to (2.3) after calibration. As shown in Figure 7-3, the impedance magnitude and phase data obtained using the RFISA electronics properly fit with the data obtained using the reference instrument for both the low-impedance resonance and the high-impedance antiresonance. The relative error of the RFISA impedance magnitude data referenced to the HP4395A data for a single-shoot measurement is presented in Figure 7-4a. The magenta and blue curves show the impedance-magnitude tolerance curve of the HP4395A at 5 MHz and 15 MHz, respectively, for a single-shoot measurement in dependence on the measured impedance magnitude. The equation was taken from operation manual and is listed in Appendix A1.

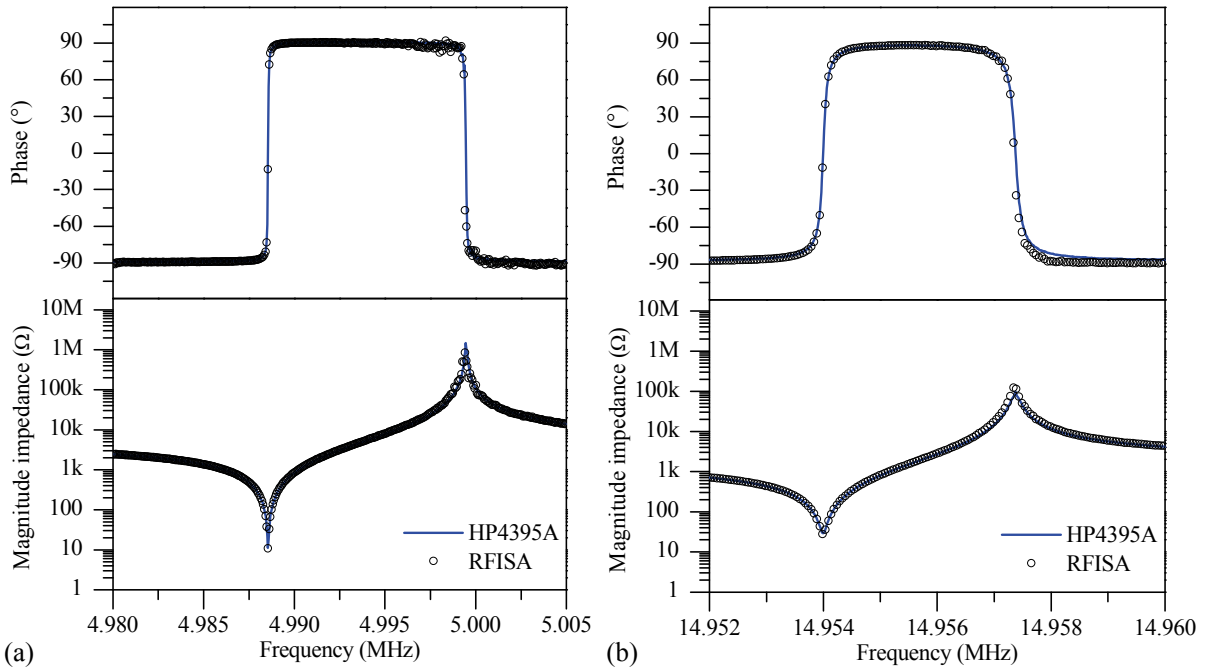

Figure 7-3 Impedance spectrum (magnitude and phase) of a 5 MHz QCR device measured with the RFISA electronics system and a benchtop instrument (HP4395A) for (a) the fundamental mode and (b) the third overtone.

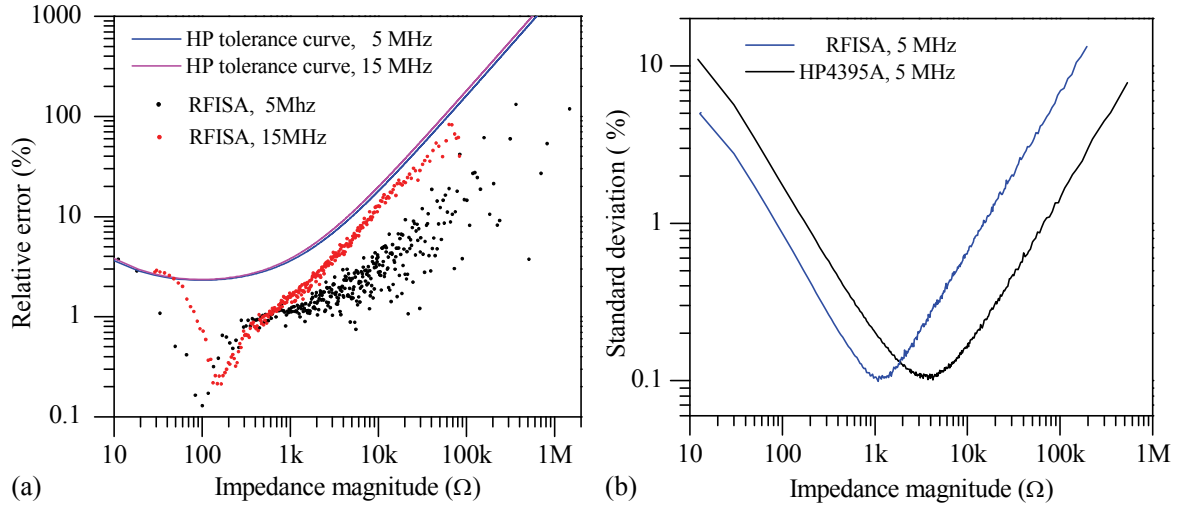

Figure 7-4 Divergence of the measured impedance magnitude values from the data obtained using the benchtop instrument HP4395A for a 5 MHz QCR device. Plot (a) shows the relative error (referenced to the HP4395A data) and the HP4395A's tolerance curves as a function of the impedance magnitude for a single-shoot impedance-spectrum measurement. Plot (b) shows the experimental standard deviation of the measured data as a function of the impedance magnitude for 1000 measurements in comparison to the HP4395A.

As expected, the relative error between RFISA and HP4395A is minimal (lower than 1%) in the low and middle impedance range and increases significantly up to 100% with increasing magnitude values at very high impedance values, but remains under the tolerance curve of the reference instrument for both frequency ranges (5 MHz and 15 MHz).

In order to evaluate the measurement repeatability in comparison to the HP4395A (respectively the noise performance of the electronics), 1000 consecutive 5 MHz-QCR impedance-spectrum measurements were recorded and the experimental standard deviation were computed for each impedance magnitude measured. As shown in Figure 7-4b, the measurement repeatability (noise performance) of the RFISA electronics system and the HP4395A benchtop instrument are sufficiently comparable because no significant differences for the curve progression and the minimum and maximum levels occur. For the middle-impedance measurement range (100 Ω – 1 kΩ), the experimental standard deviation is sufficiently under 1%. The divergence of the minimum experimental standard deviation in accordance to the respective impedance magnitude value is caused by overall measurement sensitivity of the particular instrument. Since the HP4395A benchtop instrument is primarily intended for a very wide impedance measurement range, its measurement sensitivity is properly adapted to the middle of the measurable impedance range. For high impedance magnitude values, the RFISA electronics system reveals a larger measurement uncertainty compared to the HP4395A, but it is still below 10%. However, the curve shift of the experimental standard deviation to lower impedance values for the RFISA electronics system is advantageously in the application for determination resonant impedance spectra. This is the crucial impedance range (minimum impedance magnitude) of the entire spectrum for examination the frequency response of bulk acoustic wave (BAW) sensor devices (see section 2.2.2). Finally, in order to evaluate the divergence of the specific resonance parameter of the unloaded QCR device, the averaged impedance spectra of both instruments were fitted in accordance to [63] and the crucial parameter series resonant frequency and resistance were extracted. The comparison (listed in Table 7-2) shows good agreement between the RFISA electronics system and the HP4395A benchtop instrument.

Table 7-2 Comparison of average measurement results for series resonant frequency and resistance of a 5 MHz QCR device. Relative errors are referenced to HP4395A.

instrument	f_0 (MHz)	relative error frequency (%)	R_0 (Ω)	relative error resistance (%)
RFISA	4.988608509	0.0007	10.969	0.68
HP4395A	4.988574237	—	11.044	—

Summarizing, there is no indication that the benchtop instrument HP4395A offers significant more precision than the developed RFISA electronics system. Especially in the neighborhood of the resonance frequency (minimum impedance magnitude), which is the crucial measurement range for determination the frequency response of the particular BAW sensor device, the RFISA exhibits good accordance with the benchtop instruments and reveals an adequate accuracy and noise performance of the measurement results. Obviously from Figure 7-4b, the optimum impedance measurement range of the RFISA electronics system is determined between $100\ \Omega - 10\ \mathrm{k}\Omega$, which is in accordance with the impedance spectrum measurement range of heavy loaded BAW sensor devices for in-liquid or high temperature applications presented in the following sections.

7.3 Examples of application

The primarily intended application field of the portable RFISA electronics system is the characterization of medium (liquid or gas) properties by measuring the impedance spectrum of an appropriate sensor. Selected *in situ* process and laboratory applications of the RFISA electronics system for bulk acoustic wave (BAW) resonators operating in liquid or gas media and for a capacitive sensor probe applicable for in-liquid dielectric spectroscopy will be presented in the following.

7.3.1 Langasite BAW gas sensor for high temperature applications

In cooperation with Richter *et al.,* a gas sensor system has been developed that allows for high-temperature detection of small amounts of carbon monoxide in hydrogen-rich atmospheres [183]. The sensor system is based on the RFISA electronics in combination with an array of high temperature stable langasite BAW resonators to establish *in situ* process monitoring in fuel cell reformers, combustors, or gas firing stage. Distinction of carbon monoxide (CO) and hydrogen (H_2) at high temperature is needed for example to prevent catalyst poisoning of proton exchange membrane (PEM) fuel cells after reforming of natural gas to syngas or methanol. Suppression of the unwanted CO by-product can thereby be achieved by monitoring and controlling the reforming process in the first reforming step at about 600°C–700°C. In principle, the langasite BAW sensors vibrate in thickness shear mode (TSM) at a resonant frequency of 5 MHz (fundamental) and act as classical microbalance described in section 2.2.1. Unfortunately, their operation at high temperatures is accompanied by not only a significant damping (as shown Figure 7-5a) but also a strong dependence of the resonant frequency on temperature. Latter therefore necessitates a temperature compensation for the obtained resonant frequency shift by measuring the more damped third overtone resonant frequency (15 MHz) in addition [56]. Both conditions require the employment of the portable

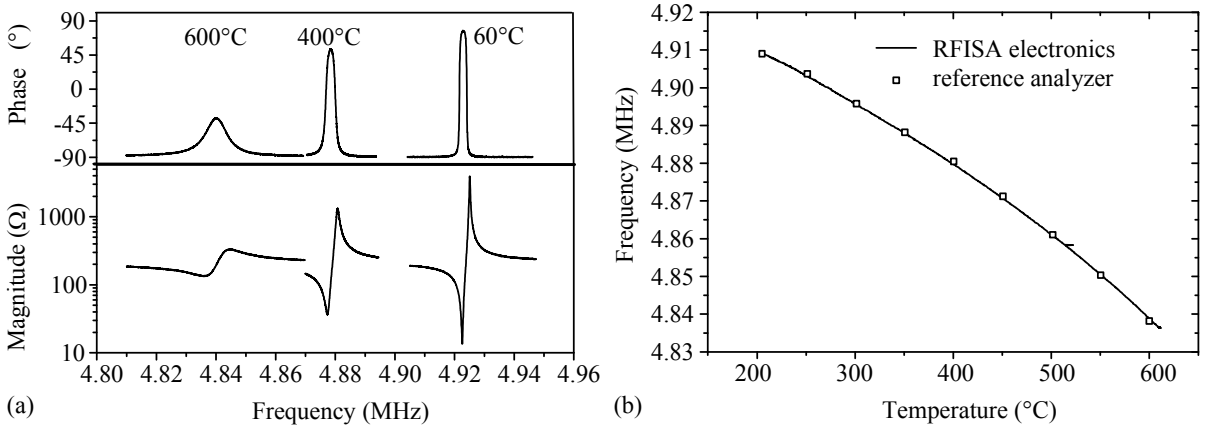

Figure 7-5 Representation of the measured (a) resonant spectra of a langasite resonator at different temperatures and (b) the temperature dependent frequency shift measured with the RFISA electronics compared to a commercial network analyzer.

RFISA electronics system in order to properly obtain the resonator‘s frequency response using impedance spectrum analysis.

Application of the developed stand-alone gas sensor system for *in situ* distinction of CO and H_2 at high temperature in the particular application is demonstrated in several publications e.g. in [183] [184] [185]. A short overview of some results will be given in the following. In accordance to the explanations in section 2.2.2 and with application of (2.3) after calibration, the resonance behavior of the langasite resonators were investigated by monitoring the impedance spectra $Z_{\mathrm{el}}(\mathrm{j}\omega)$ in the vicinity of the resonance at the fundamental mode and the third overtone. The measured data were then converted into the admittance form $Y_{\mathrm{el}}(\mathrm{j}\omega)$ and the resonant frequencies f_{res} were determined and tracked by the center frequency of a fitted function near the maximum of the conductance spectra $G_{\mathrm{el}}(\omega)$.

The temperature dependent resonant frequency shifts of a langasite resonator were measured and compared with results of a commercial network analyzer (HP 5110A from Hewlett Packard, Inc.). As shown in Figure 7-5, the resonance shifted to lower frequencies with increasing temperature. The RFISA electronics system allows for proper determination of the resonant frequency at high temperatures and exhibits no significant differences in comparison with the benchtop instrument (Figure 7-5b). Hence, in spite of the resonant spectra being highly damped and broadened due to increasing electric losses at high temperatures (Figure 7-5a), determination of the resonant frequency remains possible. For the application as gas sensor, the langasite resonators have been coated with different metal oxide based sensing film materials such as CeO_2 (cerium oxide) or TiO_2 (titanium dioxide) by Richter *et al.* and tested by the measurement of gas atmosphere dependent resonant frequency shifts. Figure 7-6 shows the measurement results for a langasite resonator that was coated with a TiO_{2-x} film acting as an oxygen partial pressure dependent mass load. The coated resonator was exposed to gas

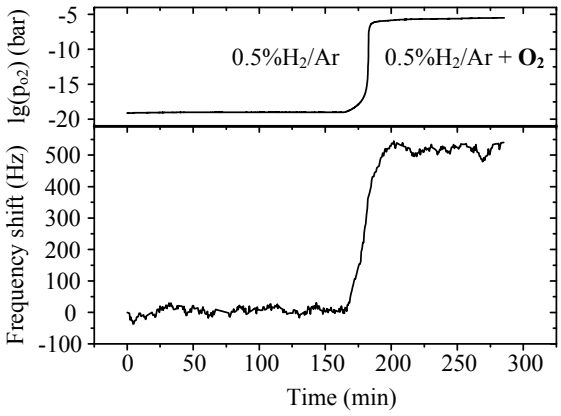

Figure 7-6 Temperature compensated frequency shift of a TiO_{2-x} -coated langasite resonator by variation of the oxygen partial pressure at a temperature of 600°C.

changes at a nominal temperature of 600°C and the resonant spectra were analyzed in the vicinity of the fundamental mode and the third overtone to obtain the temperature compensated resonant frequency shift. Changes in oxygen partial pressure are expected to cause changes of the electrical and mechanical properties upon partial reduction or oxidation of the TiO_{2-x} film. A significant shift of the resonant frequency due to change of atmosphere from 0.5% H_2/Ar to content of additional oxygen by variation of the oxygen partial pressure could be measured.

In order to distinguish between the sensor‘s frequency response related to conductivity property changes of the sensing film layer and related to mechanical property changes of the sensing film layer, two different electrode and sensing film layouts were designed by Richter *et al.*, resulting in a so called microbalance and conductivity measurement mode of the langasite resonator. A detailed description of the resonator preparation and the corresponding sensor effects can be found in [12] [56]. Figure 7-7 shows by the example of langasite resonators coated with a CeO_2 sensor film the dependence of the temperature compensated resonant frequency from the oxygen partial pressure for different gas mixtures. The resonators are operated at the different modes and exhibit different curve progressions. Furthermore, both resonators exhibit a different response to the CO and H_2 containing gas mixtures, which can be ascribed to different effects taking place in the electrical and mechanical properties of the CeO_2 layer. The variation of the frequency in conductivity mode is thereby significant larger than in the microbalance mode. As shown in Figure 7-7c, combining both measurement results leads to a significant improvement of the sensor selectivity for distinction of CO and H_2 at high temperatures, independent from the oxygen partial pressure.

Application of an appropriate gas sensor array that includes langasite resonators operating in the two measurement modes and coated with different sensing films allows for simultaneous measurements of both sensing effects by a single data acquisition technique. Hence, a high sensitivity for distinction between CO and H_2 at high temperatures can be achieved.

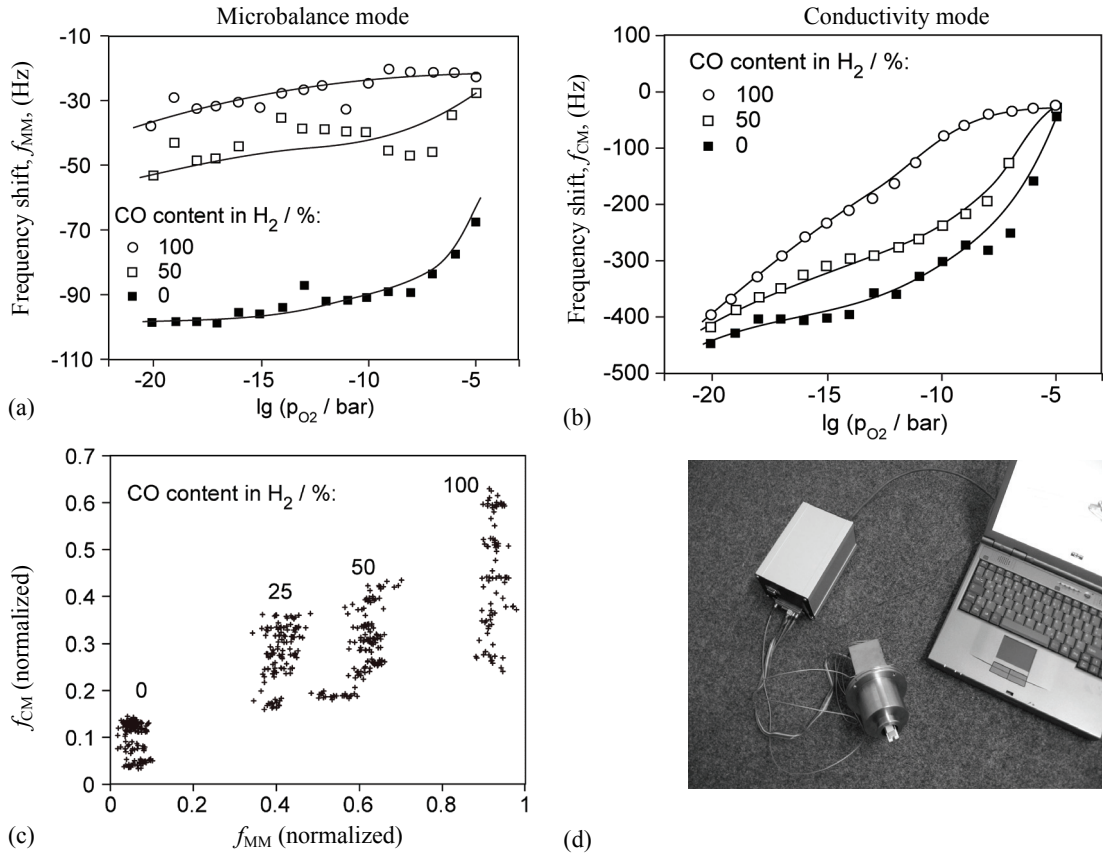

Figure 7-7 Temperature compensated frequency shifts of CeO_2-coated langasite resonators at 600°C in (a) microbalance mode and (b) conductivity mode at different gas composition containing a 0.25 % H_2/CO mixture in argon. Plot (c) shows the normalized frequencies by combining both measurement results. The Photograph in (c) shows the components of the portable sensor system comprising the RFISA electronics system and the high temperature sensor probe. [183]

For this purpose, the RFISA electronics system in combination with the multiplexed sensor interface unit based on the transmission method (see Figure 5-17c) was employed and a sensitivity of 2 % CO in H_2 was obtained and presented in [185]. Thus, the portable employment of the gas sensor system (Figure 7-7d) for in situ detection of small amounts of carbon monoxide at high temperatures in the target process application could successfully be demonstrated. Beneficially, due to fast data-acquisition capability of the developed RFISA electronics, the sensor array, which comprises six langasite resonators, can completely be analyzed at the corresponding fundamental and the third overtone resonance in less than 1.4 s, when 300 frequencies and a reasonable number of sampling points ($J < 2^{14}$) are taken for one impedance spectrum to be measured. This high data acquisition rate maintains almost continuous monitoring of the individual sensors included in the array and reduces the influence of unstable system conditions (e.g. temperature) on the array's overall sensor response.

7.3.2 Quartz LFE-TSM resonator for in-liquid sensor applications

As mentioned in section 2.2.1, lateral field excited (LFE) AT-cut quartz resonator (QCR) vibrating in thickness shear mode (TSM) show an increased sensitivity to both mechanical (mass, density, viscoelasticity) and electrical (conductivity, permittivity) property changes of an adjacent media or a coated sensor film layer. Since this has introduced new applications for (bio-)chemical in-liquid QCR sensors as demonstrated in [15] [16] [17] [73] recently, the developed RFISA electronics was tested in the application of a portable measuring setup (Figure 7-8b) for investigation of lateral field excited liquid acoustic wave sensors.

The used LFE-TSM resonators were prepared by the sensor group of Professor Dr. J. Vetelino at the Laboratory of Surface Science and Technology at the University of Maine (Orono, Maine, USA). The piezoelectric substrate consists of a 5 MHz AT-cut quartz crystal blank having a diameter of 25.4 mm. Semi-circled electrodes were sputtered onto one (reference) side of the quartz blank and separated by a gap having a width of 1 mm (Figure 7-8a). Further details about fabrication the LFE resonator can be found in [14]. The LFE resonators was placed in a standard crystal holder from Maxtek, Inc., which provides spring pin contact to RF source and ground potential for the electrodes at the reference surface, and the crystal holder was connected to the RFISA's sensor interface comprising in the grounded transformer circuit configuration shown in Figure 5-17a. The bare (sensing) surface was exposed to different liquid environments in order to measure the LFE-TSM resonator's impedance spectrum depending on liquid electrical property changes. Again, after calibration with (2.3), the shift of the crucial resonance parameters, namely the shift of the series resonance frequency Δf and resistance ΔR, were tracked by the center frequency of a fitted polynomial function near the maximum of the respective conductance spectra $G_{\mathrm{el}}(\omega)$.

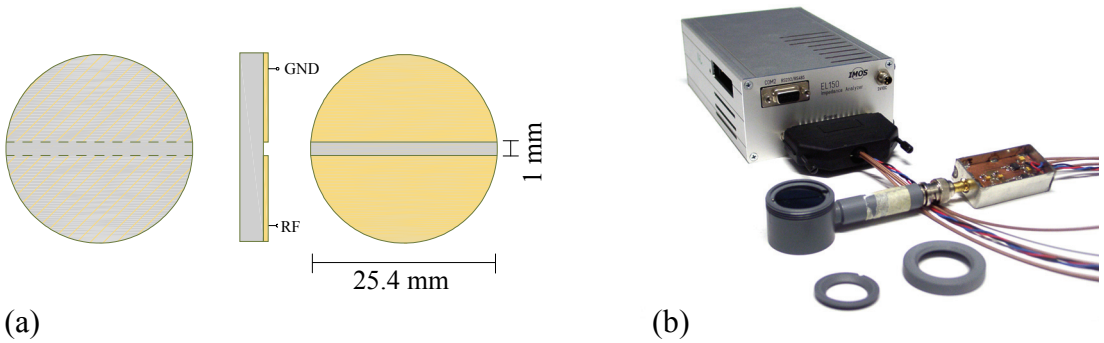

Figure 7-8 Representation of (a) the electrode layout of a 5 MHz LFE quartz crystal resonator (left: bare sensing surface; right: reference surface with electrodes) and (b) the portable measuring setup comprising the RFISA electronics and the crystal holder from Maxtek, Inc.

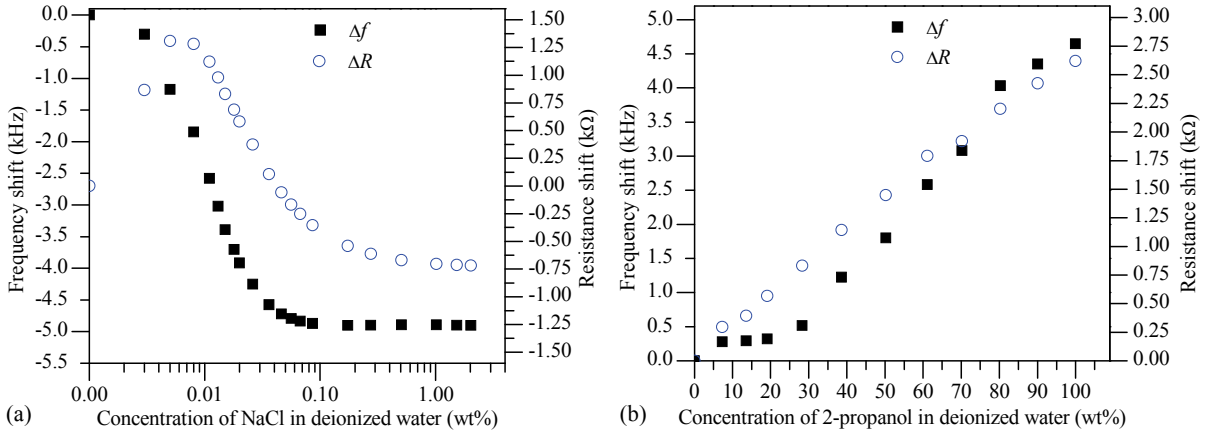

Figure 7-9 Frequency and resistance shift of a 5 MHz LFE-TSM quartz resonator as a function of (a) NaCl concentration in deionized water (semi-logarithm plot) and (b) 2-propanol in deionized water. (Referenced to deionized water).

The influence of polar, high-conductive liquids on the resonator‘s frequency response was investigated by applying different electrolytic solutions that consisted of different amounts of NaCl dissolved in deionized water. The obtained frequency and resistance shift, referenced to deionized water, as a function of the NaCl concentration are shown in Figure 7-9a and reveal the high sensitivity of the LFE-TSM resonator to liquid electrical property changes. The resonant frequency initially decreases upon exposure to NaCl solutions and starts to saturate for a NaCl concentration of about 0.05 % by weight (wt%). The influence of the liquid’s permittivity on the resonator‘s frequency response was studied by exposing the bare surface of the LFE-TSM resonator to different 2-propanol solutions. By mixing different volumes of 2-propanol into deionized water concentrations from 0 wt% up to 100 wt% 2-propanol were prepared, resulting in a decreasing permittivity of the solutions. The obtained frequency and resistance shift, again referenced to deionized water, as a function of the 2-propanol concentration are shown in Figure 7-9b. It is shown that as the 2-propanol concentration increases, which involves a decreasing permittivity level of the solution, the resonant frequency of the LFE-TSM resonator significantly increases. Opposed to the influence of varying liquid’s conductive levels, no saturation effect occurs. For both cases, the obtained frequency shift results measured with the RFISA electronics are comparable to the results reported in [14]. Since the resonator’s frequency and resistance response are influenced by both the liquid mechanical and electrical loading effects, the extraordinary frequency shift in both cases do not coincide with the theoretical values known from the standard quartz crystal microbalance theory, which primarily describes the mechanical influence of the adjacent medium [14] [72]. Thus, investigation of the impedance spectrum is required to provide better insight into the piezoelectric excitation and transduction mechanism of the LFE acoustic device under various electric property conditions at the quartz-medium interface and, thus, to interpret the frequency response.

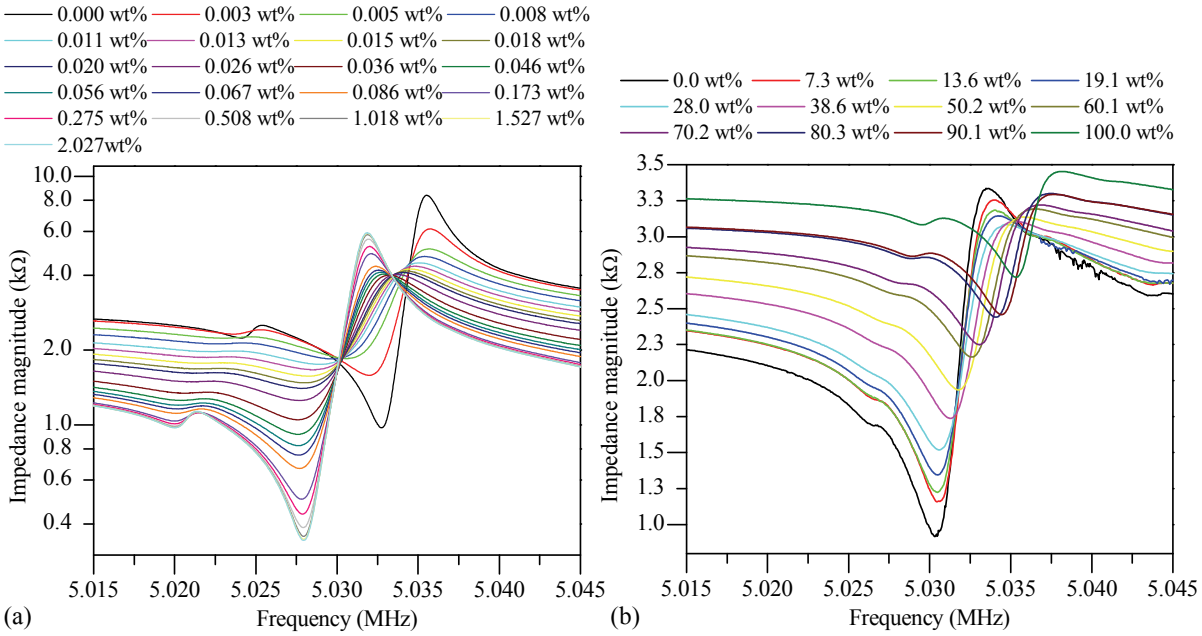

Figure 7-10 Impedance magnitude of a 5 MHz LFE-TSM quartz resonator as a function of frequency for (a) different NaCl concentrations in deionized water (in logarithm magnitude scale) and (b) different 2-propanol concentrations in deionized water.

The measured impedance magnitude spectra depending on varied concentration of NaCl and 2-porpanal are shown in Figure 7-10. Obviously, the electrical properties of the adjacent liquid medium significantly influence the frequency response of the LFE-TSM resonator not only in the vicinity of the series (mechanical) resonance but also outside the mechanical resonance. The minimum of the impedance magnitude in Figure 7-10a initially increases up to a NaCl concentration of approximately 0.01 wt%, decreases then and begins to saturate at approximately 1.5 wt%, which is above the concentration at which the resonant frequency in Figure 7-9a begins to saturate. Furthermore, a significant decrease of the impedance magnitude outside the mechanical resonance is also observed. With decreasing permittivity level of the solution, a noticeable increase of the impedance magnitude outside the mechanical resonance combined with a strong compression of the entire spectrum is revealed in Figure 7-10b.

In summary, from the results shown in Figure 7-10 one can conclude that changes of the electrical property (conductivity or permittivity) of the adjacent liquid medium in contact to the bare LFE-TSM resonator surface considerably affect the distribution of the excitation electric field in the piezoelectric substrate. Opposed to thickness field excited (TFE-) TSM resonators, this results in a significant change of the entire LFE-TSM resonator's impedance spectrum in the vicinity of the resonance frequency. In order to improve the understanding of the altered piezoelectric excitation and transduction mechanism influenced by the electric properties of the adjacent medium, Hempel *et al.* have comprehensively been investigated the impedance spectrum of LFE-TSM resonators with the application of the RFISA electronics system. Ex-

perimental results and conclusions can be found in [71] [72] [73]. In principle, it is pointed out that the high sensitivity of LFE-TSM devices is attributed to a combined acuosto-electric sensing effect opposed to the principal acoustic sensing effect of TFE-TSM devices.

7.3.3 Broadband dielectric spectroscopy on liquids

As introduced in section 1.3, a forerunner electrical impedance spectrum analyzer electronics (ELISA150) with a frequency range up to 150 MHz was developed in teamwork with Doerner [43] [45]. In combination with Doerner's capacitive sensor probe [46], various applications of in-liquid dielectric spectroscopy were successfully demonstrated in the past years. The combination was tested in process automation application for monitoring the methanol concentration in the liquid feed of a direct methanol fuell cell (DMFC). With the portable analyzer electronics it has been possible to establish *in situ* determination of the methanol concentration by measuring the perimittivity spectra of the liquid feed [84]. The results showed good reproducibility and accuracy of the acquired dielectric constant, which had led to a measurement precision of the methanol concentration better than 0.2 wt%. Recently, inline determination of micellar concentration and size in colloidal dispersion with anionic surfactant as disperse phase was demonstrated by Doerner in [85]. By application of the ELISA150 electronics in combination with the capacitive sensor probe, he presented a correlation of the measured dielectric loss spectra with the particle size distribution of the disperse phase. Currently, after advanced adaptation of the ELISA150 electronics in order to provide also determination of the liquid's sound velocity, Doerner presented in [186] a novel capacitive sensor probe that allows for combined acoustic-dielectric measurements. By analysis of the acoustic and dielectric properties, an extension of the measurement range could be achieved.

Since the ELISA150 electronics is limited to a maximum frequency of 150 MHz, the developed RFISA electronics system was tested for the application of in-liquid dielectric spectroscopy at higher frequencies. With regard to the measurements that have been presented in [46] [187], various dipole liquids were used for measuring the corresponding spectra of the complex dielectric permittivity. The measurement results for the dielectric permittivity and the dielectric loss, which were obtained from the measured raw data using the calibration method introduced in [84], are shown in Figure 7-11. As reference liquids for calibration of the capacitive sensor probe and the RFISA electronics system deionized water as high-permittivity reference and octane as low-permittivity reference were preferred. The measurement process was constantly tempered at 20 C. To allow for evaluation of the measurement results, the calculated frequency-dependent values of the complex dielectric permittivity are also presented in the figure. The data were calculated using the equations suggested in [188]. The respective equations are listed in Appendix A1.

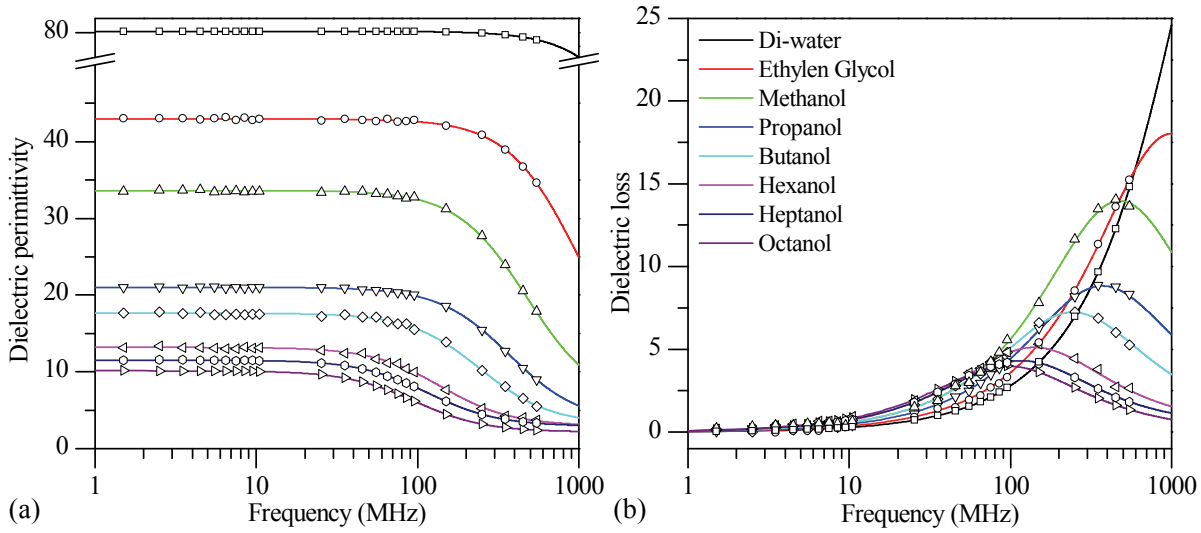

Figure 7-11 Calibrated spectra of (a) dielectric permittivity and (b) dielectric loss for various liquids at a temperature of 20°C. Calibration liquids are deionized water (Di-water) as high-permittivity reference and octanol as low-permittivity reference. Solid lines represent the calculated frequency-dependent characteristics.

From Figure 7-11 it is evident that the respective dipole relaxations up to a frequency of approximately 550 MHz could be tracked. The results for the measured dipole relaxation in the frequency range from 1 MHz to 550 MHz are in good agreement with the theoretically expected data.The limitation of measurements up to a maximum frequency of 550 MHz is caused by the bandwidth limitation of the active analog components employed in the sensor interface unit. The sensor interface unit is placed within the capacitive sensor probe and based on the active voltage-divider circuit configuration introduced in section 5.6. The second limitation of the frequency range arises from geometry of the capacitive sensor probe. For measurements above 500 MHz a redesign of the capacitive sensor probe with regard to optimized electromagnetic field distribution is needed.

7.4 Discussion

Evaluation of the noise and spurious performance of the RFISA synthesizer output has verfiefied a good signal quality. Due to the design efforts described in section 5.2, the synthesizer specifications are very well met. Test measurements with defined impedance load conditions have confirmed a good measurement precision, which is comparable to that using a standard benchtop instrument. There is no indication that the benchtop instrument offers significant more precision than the developed RFISA electronics system. Applications of the RFISA electronics system for impedance spectroscopy on various acoustic microsensors and a capacitive sensor probe for in-liquid dielectric spectroscopy up to 550 MHz have been successfully demonstrated. For higher frequency applications, further test measurements are required.

Chapter 8
Summary and prospects

The application of modern sensor devices requires appropriate measurement methods and sophisticated electronic instruments in order to precisely determine the sensor response with regard to the target parameters of a medium under study. The impedance spectrum of the sensor provides multiple information that allows for conclusions about the design of the particular sensor device, the sensor-medium interaction, or for advanced modeling. For this purpose, the analysis of the sensor's impedance spectrum is well established for characterization of the particular sensor device in laboratory applications. Presently, however, impedance spectroscopy at very high frequencies has only been applicable with standard benchtop instruments, covering a broad frequency and impedance measurement range. They are well suited for stationary (laboratory) sensor application rather than for a portable, *in situ* measurement setup. The present work introduces a novel electronics system that provides wideband high-frequency impedance spectrum analysis for portable *in situ* sensor applications. In contrast to bulky benchtop instruments, the electronics system allows for a compact, stand-alone *in situ* measurement setup for laboratory as well as industrial sensor applications and very fast data acquisition.

The electronics system is primarily intended for sensor applications of acoustic microsensors and capacitive sensor probes, but, in general, it can be versatility applied to any appropriate sensor that transduces electrical or non-electrical (such as acoustic) signals into an electrical impedance. The representatives for resonant sensor applications (narrowband impedance spectroscopy) and capacitive sensor applications (wideband impedance spectroscopy) were chosen because they specify in different manner the measurement requirements on the frequency and impedance coverage for a versatile employment of the electronics system.

With regard to the main objective of minimizing circuit design, a single-board hybrid synthesizer architecture combining various analog and digital synthesis techniques was developed, which meets the requirements on broad frequency coverage (10 kHz–1 GHz) with arbitrary fine frequency resolution (<1 Hz), fast frequency settling, and good spectral quality of the output signal. It combines the frequency multiplication properties of two phase locked loops (PLL) that operate in the gigahertz range, the fast hopping and fine tuning capability of a direct digital frequency synthesizer (DDFS) that tunes the frequency-tunable PLL, and the frequency translation property of a mixer that down-converts the high-frequency PLL signals to the low-frequency intermediate output signal. In order to ensure excellent close-to-carrier

spectral quality of the output signal, the DDFS circuitry driving the frequency-tunable PLL was separated into the numerical controlled oscillator with Taylor series correction implemented in field-programmable gate array (FPGA) and the high-speed high-resolution digital-to-analog converter. This was essential because no commercial DDFS integrated circuit was presently available that complies with the specified requirements on amplitude resolution and clocking speed in order to attain the required output spectral quality. To maintain sufficient reduction and attenuation of the mixer's sum products far within the gigahertz range, microstrip filters based on a tapped-line combline band-pass filter geometry and a stepped-impedance low-pass filter geometry were designed.

Significant reduction of the total circuit design as well as fast sensor data acquisition were achieved by utilizing a direct-sampling technique, which analog-to-digital converts the high-frequency measurement signals without decisive analog signal conditioning. Since the overall measurement precision primarily depends on the signal-to-noise ratio of the directly sampled signals, a sine-wave fitting algorithm for extracting the crucial signal parameters (amplitude and phase) is applied. Because coherent sampling of the input signal is not practicable, it was concluded that the sine-wave fitting method provides the most flexibility for changing easily between either very fast data acquisitions or very precise measurements by simple adjustment of the total number of sample points, without the need for modification of the particular digital signal processing implementation. To emphasize fast data acquisition, the parallel processing capability of FPGA was exploited to provide real-time computation of the sine-wave fitting at speed of the sampling clock. Therefore, a modified processing of the sine-wave fitting was developed, which allows for combined fixed-point and floating-point computation of the complex algorithm by FPGA hardware instead of usually applied digital signal processor hardware. A powerful processor unit was developed, which provide sufficient computation power and data storage capacity for stand-alone operation of the electronics system. The
autarkic FPGA operation as frond-end coprocessor for the sine-wave fitting and controller for the overall measurement task gives the processor unit time-resources for parallel processing of higher-level sensor data computation and host communication tasks.

For specific adaptation of the electronics system to the particular sensor and sensing application, the sensor interface was separated from the main electronics system. This allows placing the interface electronics in the particular sensor probe physically close to sensor device and avoids the need to redesign the entire electronics system when adapting to other sensor devices is required. Different small-sized sensor interface electronics were developed, which provide passive or active and grounded or non-grounded circuit configurations.

Applications of the electronics system for narrowband impedance spectroscopy on various bulk acoustic wave sensors vibrating in thickness shear mode and a capacitive sensor probe for broadband in-liquid dielectric spectroscopy were successfully demonstrated. Evaluation of the measurement precision with well-defined impedance load conditions confirmed a measurement precision, which is comparable to that using a standard benchtop instrument. No indication that the benchtop instrument offers significantly more precision than the developed electronics system was obtained.

Based on the results it was demonstrated by this thesis that the portable electronics system provides an appropriate alternative for *in situ* sensor applications by replacing commercial benchtop instruments in laboratory and industrial applications. Three points of interest are recommended for continuing the work:

- The proposed principle of impedance measurement does not allow for direct determination of the impedance value because a calibration computation is mandatory to mathematically relate the measured voltage ratio with the desired impedance value. For accurate impedance determination, this calibration must be done not only over the complete frequency range but also in accordance with the specific sensor probe and conditions of the measurement environment (e.g. thermal effects). Hence, for successful stand-alone employment in industrial applications, performance tests of the calibration computation in terms of robustness of the measurement results under rough environmental conditions or even modification of the principle of impedance measurement to prevent a calibration computation must be investigated.
- Due to the operation in the gigahertz range, the influence of electromagnetic interferences emitted as well as received from the electronics system on the measurement performance must be systematically analyzed and improved. For employment in industrial applications, the compliance with the standards for electromagnetic compatibility must be verified.
- The sine-wave fitting algorithm best fit the recorded measurement signal with a sine function by determining the function parameter that minimize the least square error between the recorded measurement signal and the generic sine-wave model. Since the recorded measurement signal is strongly related to the particular sensor device, evalution of the least square error may allow for advanced information about the sensor device. In particular in process automation application, this can provide additional information about e.g. sensor aging and variations of the environmental or process conditions.

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Appendix

A.1 Additional equations

Microstrip transmission line impedance:

In accordance to the synthesis formulas given in [179], the characteristic impedances of a single-ended and edge-coupled differential microstrip transmission trace are given by

$$Z_0 = \left(\frac{87}{\sqrt{\varepsilon_r + 1.41}} \right) \ln\left(\frac{5.98 \cdot H}{0.8 \cdot W + T} \right) \quad \text{valid for } 0.1 < W/H < 2.0 \tag{A.1}$$

and

$$Z_{0,\text{diff}} = Z_0 \cdot \left(1 - 0.48 \cdot e^{-0.96 \cdot S/H}\right), \tag{A.2}$$

respectively, where W is the trace width, T the thickness, H the substrate material width, and S the gap between differential traces.

Impedance measurement accuracy of the HP 4395A Network Analyzer from Hewlett Packard, Inc.: [189]

- Impedance magnitude accuracy:

$$Z_a = A + \left(B / |Z_m| + C \cdot |Z_m| \right) \cdot 100 \ \ [\%] \tag{A.3}$$

where $|Z_m|$ is the impedance magnitude measured,

$$A = 2\%, \tag{A.4}$$

$$B = 150 + 2\pi f \cdot 0.3 \ \ [\text{m}\Omega], \tag{A.5}$$

and

$$C = 15 + 2\pi f \cdot 3 \cdot 10^{-2} \ \ [\mu\mathrm{S}]. \tag{A.6}$$

- Phase accuracy:

$$\varphi_{\mathrm{a}} = \sin^{-1}(Z_{\mathrm{a}}/100) \tag{A.7}$$

Functional relation of the complex dielectric permittivity as a function of frequency and temperature for various liquids, as suggested in [188]:

- Propanol:

$$\varepsilon(f,T) = 2.2 + \frac{(23.41 - 0.12T) - 3.5}{1 + \mathrm{j}\left(2\pi f 10^{-12}\right)\cdot(581 - 7.5T)} + \frac{3.5 - 2.2}{1 + \mathrm{j}\left(2\pi f 10^{-12}\right)\cdot(26.1 - 0.21T)} \tag{A.8}$$

- Butanol:

$$\varepsilon(f,T) = 2.22 + \frac{(19.93 - 0.115T) - 3.25}{1 + \mathrm{j}\left(2\pi f 10^{-12}\right)\cdot(903.3 - 12.4T)} + \frac{3.25 - 2.22}{1 + \mathrm{j}\left(2\pi f 10^{-12}\right)\cdot(31.8 - 0.248T)} \tag{A.9}$$

- Hexanol:

$$\varepsilon(f,T) = 2.19 + \frac{(15.04 - 0.093T) - 3.0}{1 + \mathrm{j}\left(2\pi f 10^{-12}\right)\cdot(1624 - 24.2T)} + \frac{3.0 - 2.19}{1 + \mathrm{j}\left(2\pi f 10^{-12}\right)\cdot(37.4 - 0.335T)} \tag{A.10}$$

- Heptanol:

$$\varepsilon(f,T) = 2.17 + \frac{(13.19 - 0.083T) - 2.95}{1 + \mathrm{j}\left(2\pi f 10^{-12}\right)\cdot(1965 - 29.7T)} + \frac{2.95 - 2.17}{1 + \mathrm{j}\left(2\pi f 10^{-12}\right)\cdot(41.7 - 0.38T)} \tag{A.11}$$

- Octanol:

$$\varepsilon(f,T) = 2.17 + \frac{(11.67 - 0.077T) - 2.17}{1 + \mathrm{j}\left(2\pi f 10^{-12}\right)\cdot(2397 - 37.1T)} \tag{A.12}$$

- Ethylen glycol:

$$\varepsilon(f,T) = 3.95 + \frac{(47.8 - 0.242T) - 7.55}{1 + \mathrm{j}\left(2\pi f 10^{-12}\right)\cdot(265.5 - 5.19T)} + \frac{7.55 - 3.95}{1 + \mathrm{j}\left(2\pi f 10^{-12}\right)\cdot(23.5 - 0.43T)} \tag{A.13}$$

A.2 Key components of the RFISA electronics systems

Table A-1 Listing of components and their specification.

component	part number	main specification
RF-VCO voltage controlled oscillator	JTOS-1550 (Mini-Circuits, Inc.)	tuning range: 1150 MHz – 1550 MHz tuning voltage: 2 V – 16 V phase noise @ 1 MHz offset: -141 dBc/Hz output power: 7.0 dBm
LO-VCO voltage controlled oscillator	ROS-2160W (Mini-Circuits, Inc.)	tuning range: 1160 MHz – 2160 MHz tuning voltage: 1 V – 18 V phase noise @ 1 MHz offset: -137 dBc/Hz output power: 5.0 dBm
PLL-IC PLL frequency synthesizer chip	ADF4106 (Analog Devices, Inc.)	frequency range: 500 MHz – 6000 MHz phase detector frequency (max): 104 MHz phase noise floor: -219 dBc/Hz nominal charge-pump current (max): 5 mA
MIX frequency mixer	SYM-25DMHW (Mini-Circuits, Inc.)	frequency range: 40 MHz – 2500 MHz LO-power level: +13 dBm conversion loss: 6.6 dB
VGA variable gain amplifier	ADL5330 (Analog Devices, Inc.)	frequency range: 10 MHz – 3000 MHz gain range @ 900 MHz: (-34 dB) – (+22 dB) noise figure @900 MHz: 9 dB
AMP 1 – 3 fixed gain amplifier	ERA51-SM (Mini-Circuits, Inc.)	frequency range: DC – 4000 MHz fixed gain: 18 dB noise figure: 4.1 dB
DAC digital-to-analog converter	AD9726 (Analog Devices, Inc.)	sampling clock (max): 400 MHz resolution: 16 Bits phase noise floor @ 70 MHz: -160 dBm/Hz SFDR @ 70 MHz: 68 dBc
LO-HF ceramic high-pass filter	HFCN880 (Mini-Circuits, Inc.)	loss > 3 dB: 880 MHz loss > 20 dB: 640 MHz loss >40 dB: 500 MHz
LO-LF ceramic low-pass filter	LFCN2250 (Mini-Circuits, Inc.)	loss > 3 dB: 2575 MHz loss > 20 dB: 2900 MHz loss >30 dB: 3000 MHz

TCXO temperature compen- sated crystal oscillator	CFPT-9000 (C-MAC, Inc.)	frequency: 20 MHz phase noise floor: -145 dBc/Hz
CLKSYN-IC clock distribution IC with on-chip PLL	AD9511 (Analog Devices, Inc.)	frequency range: 1600 MHz phase detector frequency (max): 100 MHz phase noise floor: -218 dBc/Hz nominal charge-pump current (max): 4.8 mA clock outputs: 3x LVPECL (max. 1.2 GHz) 2x LVDS (max. 800 MHz)
PwrDet-IC true rms-responding power detector	AD8362 (Analog Devices, Inc.)	conversion frequency range: 50 Hz–2.7 GHz input dynamic range: -52 dBm – +8 dBm linear-in-decibels output, scaled: 50 mV/dB
DAT 1 – 2 6-bit digital step attenuator	DAT-31R5 Mini-Circuits, Inc.	frequency range: DC – 2400 MHz attenuation range: 0.5 dB – 31.5 dB attenuation step: 0.5 dB
ADC analog-to-digital converter	LTC2242-12 (Linear Technology, Inc.)	sample clock (max): 250 MHz full power bandwidth: 1200 MHz resolution: 12 Bits aperture jitter: 95 fs
DAMP fully differential amplifier	AD8351 (Analog Devices, Inc.)	frequency range: DC – 3000 MHz slew rate: 13000 V/µs input noise: 2.7 $nV/\sqrt{Hz}$
IN-LPF	LFCN1000	loss > 3 dB: 1300 MHz loss > 20 dB: 1550 MHz loss > 30 dB: 1900 MHz

A.3 Circuit design of the autoamtic level control loop

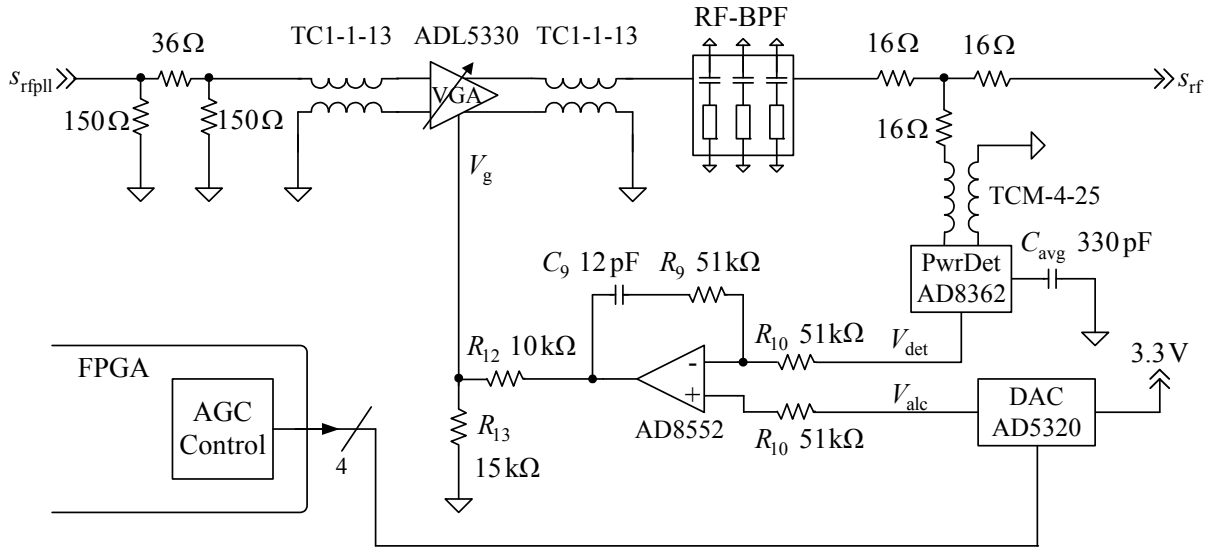


Figure A-1 Circuitry of the automatic level control loop.

A.4 Simulation results

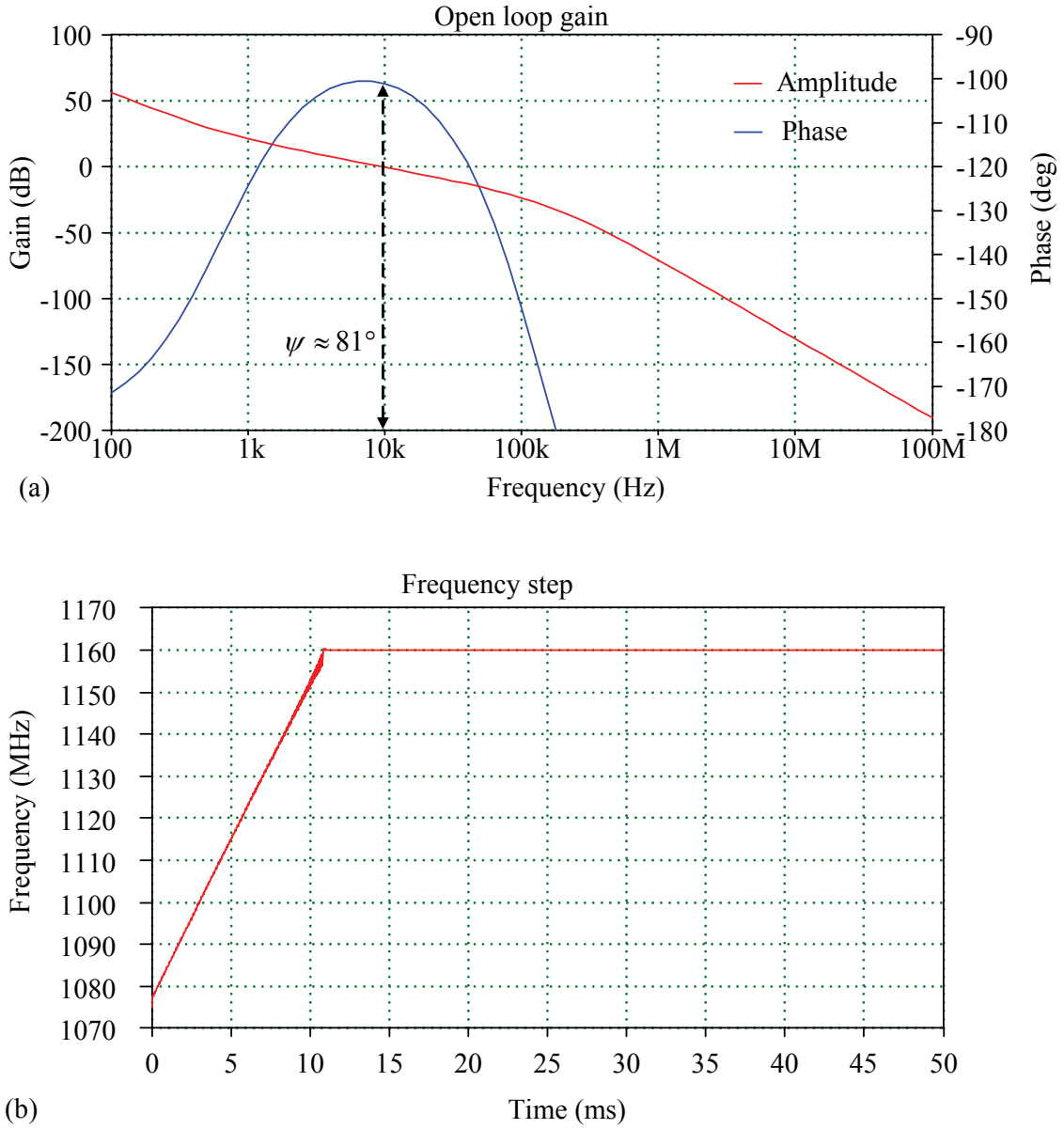
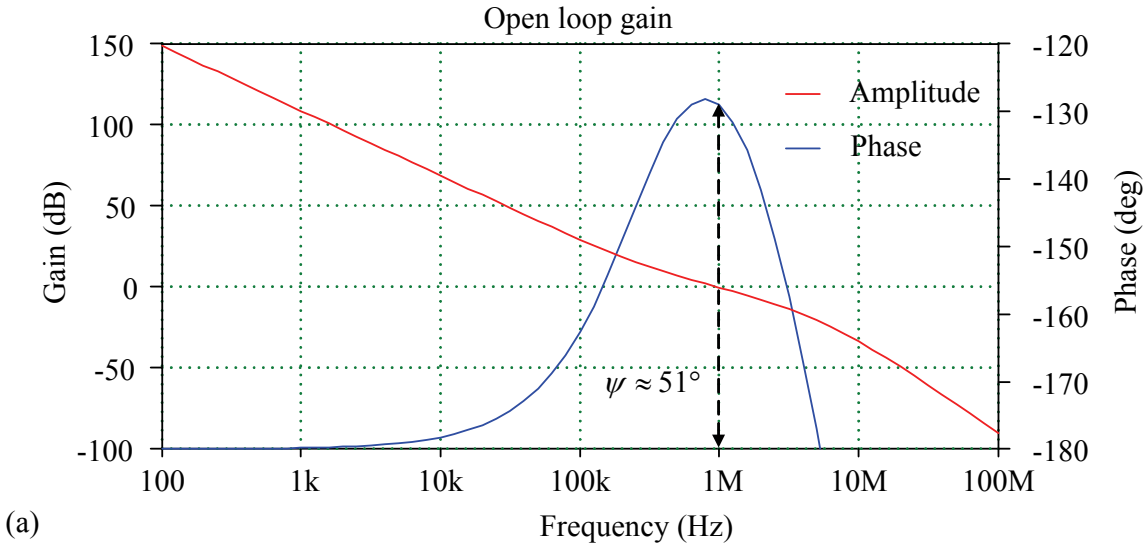
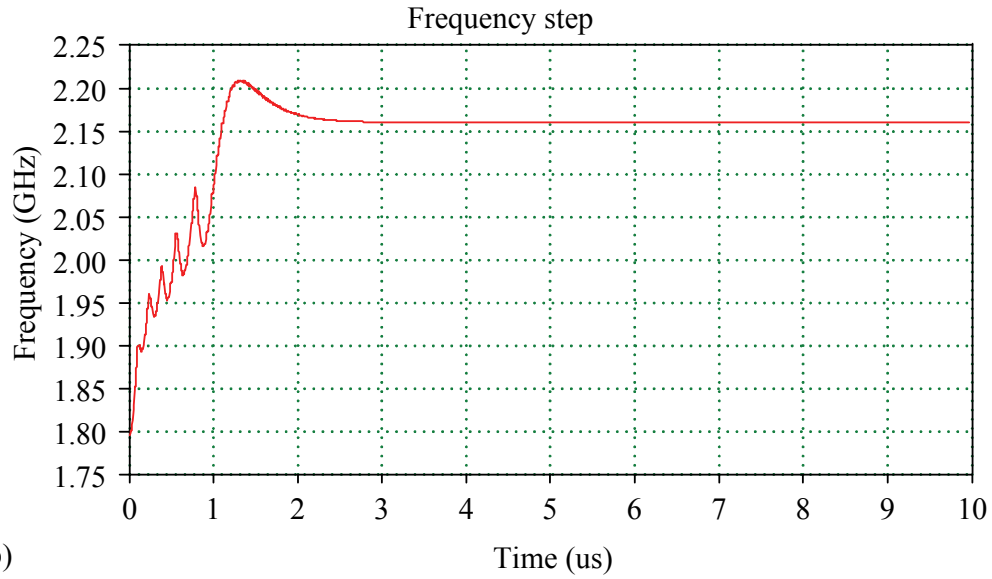


Figure A-2 ADsimPLL simulation results of the RF-PLL stage: (a) open loop gain and phase as a function of frequency and (b) settling time of the loop for a applied frequency step.



(a)



(b)

Figure A-3 ADsimPLL simulation results of the LO-PLL stage: (a) open loop gain and phase as a function of frequency and (b) settling time of the loop for a applied frequency step.

A.5 Photograph of the electronics system

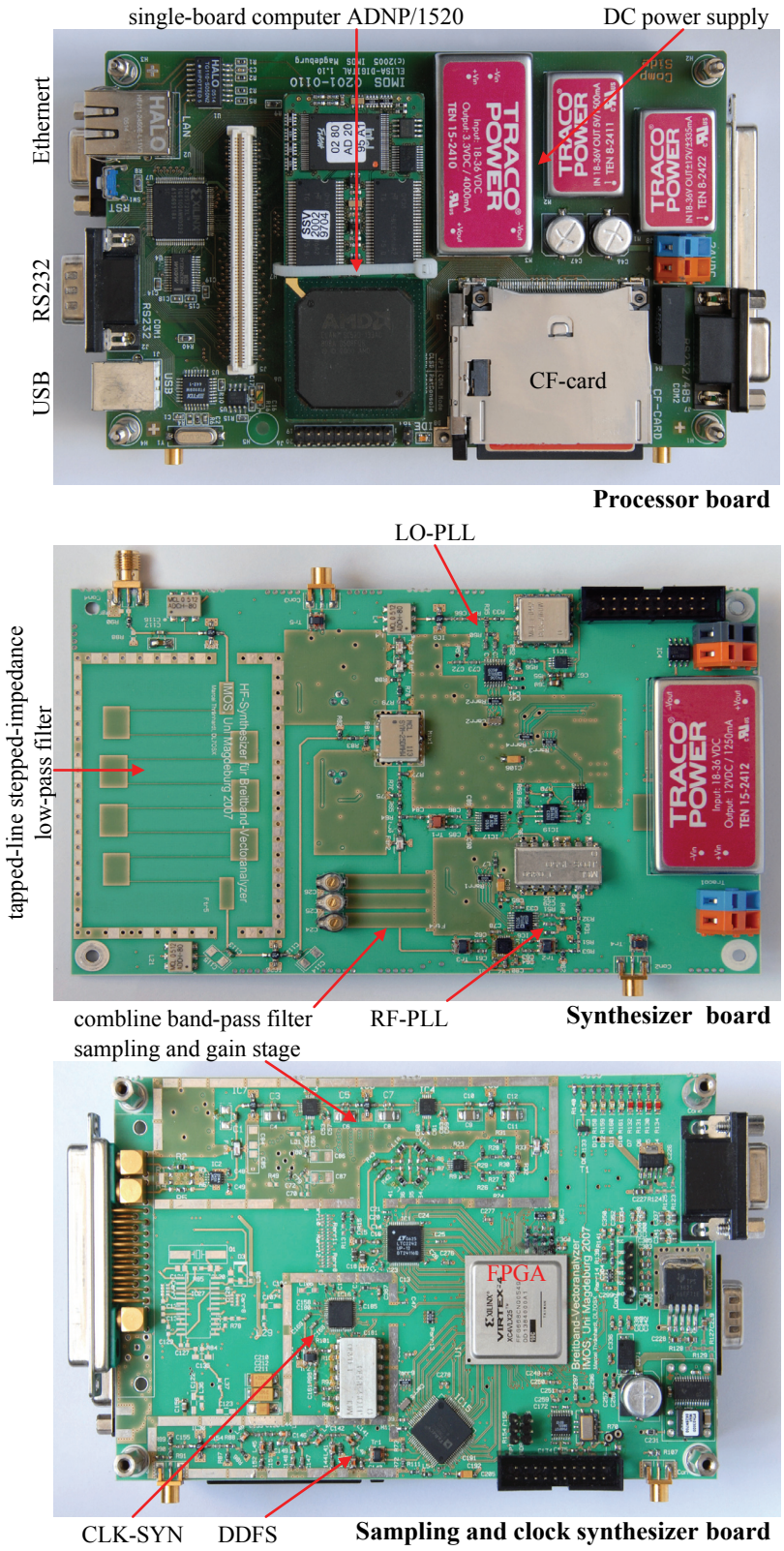


Figure A-4 Photographs of the electronics system.

Curriculum vitae

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Citizenship	Germany

Education

1984 – 1990	Polytechnical school “Am Regenstein”, Blankenburg
1990 – 1996	Secondary school “Am Thie”, Blankenburg

Alternative service

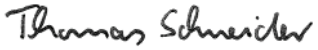
1996 – 1997	Hospital Wernigerode

Studies

1997 – 2003	Electrical engineering at Otto-von-Guericke-Universität Magdeburg
03/2003	Degree, Thesis: “Direct-Sampling-Technique for the impedance spectroscopy“

Experience

09/2001 – 01/2002	Internship at Siemens/VDO AG in Schwalbach/Taunus
since 2003	Research assistant at Otto-von-Guericke-Universität Magdeburg, Institute of Micro– and Sensor Systems, working on the BMBF research topic “Selective gas sensor for high temperature applications up to 900°C” and the AIF research topic “Resonant sensor for in-situ analysis of flue gas”



Benzingerode, July 02, 2008