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Chapter I

INTRODUCTION

Novel electronic applications often require high quality single crystalline layers on appropriate substrates. Various methods such as heteroepitaxial growth by molecular beam epitaxy or metalorganic chemical vapour deposition yield devices with a high concentration of threading dislocations when involving materials with different lattice constants such as silicon and gallium arsenide.

Wafer bonding is an attractive, flexible choice for the fabrication of such single crystalline layers on top of substrates in terms of doping profiles, surface orientation, crystallographic alignment and lattice mismatch [1]. The phenomenon of adhesion between two smooth and clean surfaces by means of van der Waals forces was observed and investigated more than one century ago. However, it was not until the mid eighties of the last century that researches from IBM and Toshiba introduced the hydrophilic and hydrophobic bonding between silicon wafers for electronic applications [2], [3]. In their approach the initial low bonding strength had to be increased to the fracture energy of the bulk material by high temperature annealing steps. In many situations a high bonding energy is desired directly after room temperature bonding, and this could be achieved after appropriate surface activation and bonding in an ultra-high vacuum (UHV) environment. Using this approach which was termed ultra-high vacuum bonding, high fracture energies could be achieved upon joining at room temperature by covalent bonding [4]. However, except for a few material combinations that have been shown to work very well, the aforementioned technique remains a challenge due to different surface chemistries specific to each material. Particularly, when bonding silicon to gallium arsenide at room temperature, low fracture energies were reported necessitating high temperature annealing before further processing could be carried out. In order to overcome the problem of different thermal expansion coefficients, heteroepitaxial growth of silicon and gallium arsenide on different substrates in combination with wafer bonding were used, as in the case of silicon-on-sapphire bonded to gallium arsenide [5] and gallium arsenide-on-germanium bonded to silicon [6]. Nevertheless, such approaches tend to be tedious and expensive. To our knowledge, no direct bonding of silicon to gallium arsenide without intermediate layers on a large scale was reported up to date.

It is within the scope of the present work to demonstrate that smooth, oxide-free interfaces can be obtained by UHV bonding of silicon to gallium arsenide at room temperature. Electrical and structural investigations were carried out in order to demonstrate the suitability of such interfaces for device fabrication.

Since most applications require uniform layers in the micron and sub-micron thickness range on appropriate substrates, it is necessary to develop a method that would allow reducing the device thickness effectively, without sacrificing the whole wafer. Chemo-mechanical polishing and selective etching techniques are obviously not the best choice in this respect, both being time consuming, expensive and cumbersome. Layer transfer by means of implantation induced splitting combined with wafer bonding is already a well-established procedure for producing silicon-on-insulator wafers [7]. Nevertheless, it always involves an intermediate oxide layer which makes this approach unsuitable for applications requiring electrically conductive interfaces.

In the present work a novel layer transfer approach based on ion implantation, surface activation by photons in the ultra-violet range and UHV bonding is proposed and implemented for the transfer of ultra-thin single crystalline silicon and GaAs layers onto silicon substrates.

Although UHV bonded interfaces are oxide-free, the current flow across the interfaces can still be hindered to some degree by the presence of a grain boundary formed during bonding. Previous investigations have shown that the Si-Si bonding process causes a potential barrier at the fused interface, particularly important in lowly doped substrates [8]. However, up to now little attention has been paid to the electrical properties of bipolar interfaces produced by UHV bonding, especially those involving dissimilar materials.

The dissertation consists of five chapters. Following the introduction, Chapter II deals with the basic concepts of wafer bonding, ion implantation and layer splitting. An overview of the defects present in crystalline semiconductors is presented, with emphasis on grain boundaries. The anti-serial Schottky barrier model used to describe the thermionic emission over the unipolar grain boundary barrier [9] is briefly discussed, followed by a description of the drift-diffusion model augmented to include interface traps, which was used to model bipolar interfaces.

Chapter III is dedicated to the experimental work performed in this dissertation. The complete process flow including ion implantation, cleaning, surface activation, UHV bonding and sample preparation is described. An overview of investigation techniques is also given.

Chapter IV focuses on results and discussions. The electrical properties are investigated by means of temperature-dependent current-voltage measurements and deep-level transient spectroscopy. The results are correlated with numerical simulations of the fabricated devices in order to understand the physical processes governing the electrical transport across bonded interfaces between identical and dissimilar materials. The layer transfer of Si and GaAs layers onto silicon substrates using the proposed approach is shown to work very well, yielding devices with good structural and electrical properties.

Finally, a summary of the work is given in Chapter V.

Chapter II

THEORETICAL CONSIDERATIONS

2.1. Wafer bonding

2.1.1. Introduction

When two clean and smooth solid surfaces are joined together at room temperature (RT) so that the distance between them is of the order of the interatomic spacing, they adhere spontaneously to each other without external forces or glue. Once the bonding is initiated, it propagates by itself across the whole interface. This phenomenon, although not necessarily involving wafer-shaped materials, is often referred to as wafer bonding, direct wafer bonding, fusion bonding or surface activated bonding [1].

The attraction originates either in weak interactions (van der Waals forces, hydrogen bonds) or strong ones (ionic, covalent or metallic bonds) depending on the chemistry of the surfaces involved and on the ambient conditions. The bonding achieved by weak interactions is reversible and necessitates subsequent thermal treatment to increase the bonding energy.

Wafer bonding can be implemented to virtually any material, provided that the requirements regarding surface cleanliness, smoothness, and flatness are met. Introduced first to semiconductor industry during the 80's for silicon-silicon bonding [2], [3], wafer bonding has received increasing attention ever since.

The following discussion focuses on theoretical and practical aspects of semiconductor wafer bonding.

2.1.2. Surface preparation

Wafer bonding is very sensitive to cleanliness and smoothness, because the initial interactions that mediate the attraction are weak and short-ranged in nature. For this reason, the first step is always to ensure that the surfaces meet the mechanical and chemical requirements.

When exposed to air, silicon readily develops a thin SiO_2 layer (typically 2-5 nm thick), which passivates the unsatisfied dangling bonds (DB) present in a large number on the surface. Thus, as-delivered silicon wafers are always covered with a native oxide on top of which typically undesirable contaminants are present, reflecting the processing history of the sample: water, ionic compounds, polar and non-polar organics from processing liquids or from the air. The latter render the wafer surface hydrophobic (water repellant) and should be first removed during the cleaning process, since the cleaning mixtures are polar and would be repelled from the surface as well. It is recommended to perform the cleaning in a controlled dust-free atmosphere, preferably in a cleanroom. Additionally, ultrapure DI (deionised) water and semiconductor grade chemicals are to be used in order to avoid contamination during the chemical treatment itself. The chemicals used in the semiconductor industry are able to remove dust particles and contaminants without degrading the surface quality of the wafers too much.

First, the RCA1 solution (also termed 'basic piranha') is used for the removal of organics. This solution consists of a mixture of NH_4OH:H_2O_2:H_2O=1:1:5 and becomes effective when heated above 60°C. To increase its efficiency, it is usually combined with immersion in an ultrasonic bath. If gross contamination is suspected, an 'acid piranha' (H_2SO_4:H_2O_2=3:1) cleaning step can be performed before RCA1 in order to support further removal of organic contaminants [2].

In a second step, the RCA2 solution (HCl:H_2O_2:H_2O=1:1:6) is used to remove most metallic contamination, except for Au and Pt [10]. Again, the solution must be heated above 60°C in order to initiate the reaction. Between these steps the wafers are thoroughly rinsed with DI water. At this stage, the wafers are contamination-free and protected by a thin layer of SiO_2.

Depending on the desired properties of the bonded structures (that is, yielding electrically insulating or conducting interfaces), the bonding can be done with SiO_2 at the interface or after oxide removal.

2.1.3. Hydrophilic bonding

The SiO_2 layer that covers the wafer surface after cleaning is terminated by OH groups, forming the so-called silanol groups (Si-OH) which render the silicon surface hydrophilic [11]. As a consequence, water molecules will be chemisorbed on the surface via hydrogen bonds. The water excess is removed by spin-drying in a turbulence-free microcleanroom [12] or by pure nitrogen blowing [13]. After this step the wafers are joined together and small pressure is applied in order to initiate the bonding, which is caused by hydrogen bonds between remaining water molecules (Fig. 2.1). Not only these water molecules mediate the initial bonding, but they fill in the gap between non-perfectly mating surfaces, bridging distances as large as 1 nm [14].

The fracture surface energy (bonding energy) between the wafers is in the range of 100-150 mJ/m^2 directly after RT bonding, and increases above 200 mJ/m^2 after long-term storage in air [15], partly due to additional silanol groups formation (as a result of water reaction with the surfaces), and partly due to the slow diffusion of water molecules out of the interface. Slightly above RT, a small fraction of silanol groups will be close enough to bond directly with each other. Further, silanol groups condensate leading to covalent Si-O-Si bonds formation (siloxane) [16], thus increasing the overall bonding energy:

$$\text{Si-OH} + \text{OH-Si} \rightarrow \text{Si-O-Si} + H_2O \qquad (2.1)$$

This is a very slow process at RT, and leads to the formation of additional water molecules. Moreover, (2.1) is reversible, which means that the interfacial water causes further silanol group formation, weakening the bonding energy. For this reason, the bonding energy tends to saturate at relatively low values. In order to accelerate the process and to increase the bonding strength, thermal annealing needs to be performed.

Below 110°C the bonding energy is similar to RT. Between 110°C and 200°C more and more hydrogen bonds between adjacent silanol groups are converted into covalent siloxane bonds depicted by the red lines in Fig. 2.1, and the interface energy increases rapidly up to 1200 mJ/m^2.

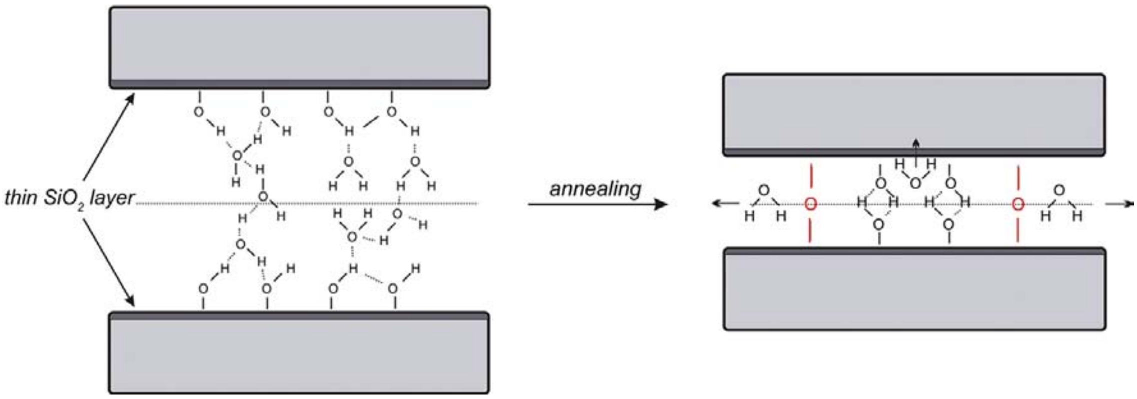

Figure 2.1: Interface morphology upon RT hydrophilic bonding (left) and after annealing (right).

Further temperature increase up to 700-800°C yields no change in the bonding energy [17], due to the saturation behaviour of the above described mechanism. That is, no further bonding energy increase is possible after all available silanol bonds are converted to siloxane bonds, the limitation being given by the actual contact area between mating surfaces. Since these surfaces are not atomically flat, microgaps are expected to form at the unbonded areas.

At 800°C, the SiO_2 becomes viscous and starts filling the microgaps. As a result, the bonding energy increases to 2000-2500 mJ/m^2 [18]. If the annealing temperature exceeds 1000°C, the native oxide layer at the interface disintegrates into islands leading to Si-Si covalent bonding and the interface loses its insulating properties, provided the SiO_2 layer is reasonably thin and the oxygen concentration in bulk silicon is low [2].

2.1.4. Hydrophobic bonding

Hydrophobic (i.e. ‘water repellent’) surfaces result when the native oxide is etched away using hydrogen fluoride [19] or buffered ammonium fluoride [20] solutions, for Si(100) and Si(111) surfaces, respectively. The dissolution of SiO_2 by HF is depicted in the following reaction:

$$SiO_2 + 4HF \rightarrow SiF_4 + 2H_2O \qquad (2.2)$$

After oxide removal, the dangling bonds of the surface atoms are passivated by hydrogen and only to a small extent by fluorine atoms. This occurs because of the strong polar character of the Si-F bonds which in turn causes bond polarization of the Si-Si back-bonds. HF molecules, having a highly polar character as well, attack these back-bonds resulting in the release of stable SiF_x species [21]. The Si-H bonds are quite stable in air (up to a few hours). However, hydrophobic surfaces are very prone to hydrocarbon contamination; therefore bonding should be performed very quickly without water rinse which would cause partial re-hydrophilisation due to the conversion of Si-F bonds to Si-OH bonds.

Once the wafers are joined, the adhesion is caused by van der Waals forces between hydrogen atoms, as depicted in Fig. 2.2. The initial fracture strength in the case of hydrophobic bonding takes values between 20 and 30 mJ/m^2 (lower than those corresponding to hydrophilic bonding), and remains low up to 300-400°C annealing temperature when the hydrogen and HF molecules start to dissociate from the silicon surface and to diffuse along the interface, allowing covalent bond formation depicted by the red lines in Fig. 2.2 [1]. Thus, energies as high as 2000 mJ/m^2 can be reached after annealing at 700°C.

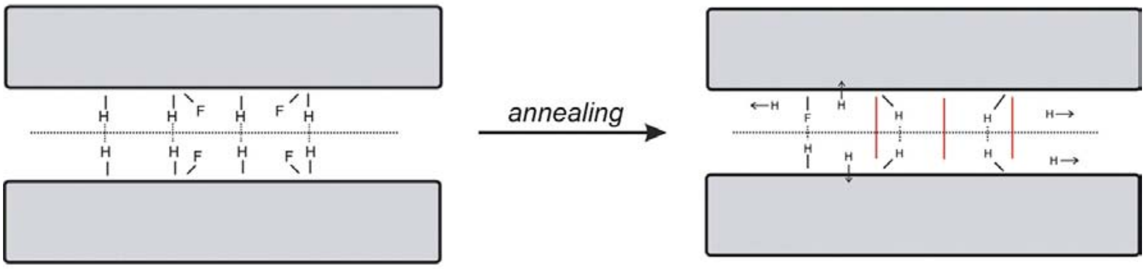

Figure 2.2: Interface morphology upon RT hydrophobic bonding (left) and after annealing (right).

As in the case of hydrophilic bonding, the bonding energy is limited by the actual contact area between mating surfaces. At temperatures higher than 700°C, silicon atoms start to flow along the interface filling the microcavities originating in the initial wafer roughness. A number of workers identified bubbles and voids at the interface [22], [23], formed by impurity agglomerates and gas trapping (hydrogen, fluorine, and nitrogen).

2.1.5. UHV bonding

Both hydrophilic and hydrophobic bonding exhibit low initial fracture energy and high temperature annealing steps are required to obtain strong bonding, which might not be sensible in many situations, especially when dealing with dissimilar materials. For this reason, new ways of achieving strong bonding upon joining at RT have been thoroughly investigated.

One possible solution is ultrahigh-vacuum (UHV) bonding [4], which can be regarded as a modified hydrophobic bonding performed in an ultrahigh-vacuum environment (pressure less than 10^{-9} mbar). The procedure of producing hydrophobic surfaces has already been outlined, so we can easily imagine a bonding experiment in which two such surfaces are joined together.

Without subsequent annealing, the bonding energy is low and the wafers can be separated at any time, e. g. in UHV. Assuming a flat Si(100) surface, the two DBs on each surface atom are hydrogen terminated, leading to a Si(100)-(1x1):H structure (neglecting the small amount of fluorine). Upon annealing to about 500°C the hydrogen is desorbed from the separated surfaces in UHV, leaving two DB per atom, i. e. about 10^{15} DB/cm^2.

The energy of the free surfaces is very high in this case (ca. 2.25 J/m^2, ref. [24]), and a (2x1) reconstruction is adopted via formation of Si-Si dimers which give a more stable configuration with only one DB per surface atom. For Si(111) surfaces, a (7x7) reconstruction is favoured [25]. The energy of a reconstructed Si-Si bond is still higher than that of an undisturbed bond because of the strong bending. For sufficiently small separation between surfaces, the electronic surface states overlap and an ‘adhesive avalanche’ occurs via reconstruction breaking and covalent bonding as predicted by molecular dynamics simulations for Si(111)-(1x1) [26] and Si(100)-(2x1) [27]. The schematic drawing in Fig. 2.3 shows the sequence of heating and cooling before room temperature bonding in UHV. The red lines represent direct Si-Si bonds.

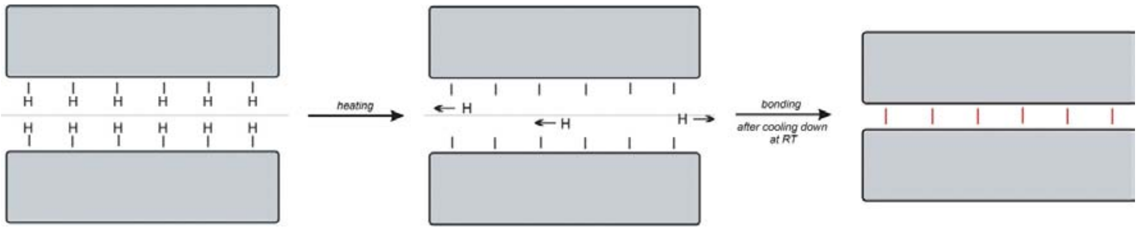

Figure 2.3: UHV bonding at RT after hydrogen desorption.

The energy released during the bonding process is spent to re-arrange surface atoms. Even if the two wafers are bonded in such a manner that their crystallographic orientations are perfectly aligned, the interface doesn’t resemble a perfect structure due to incomplete bonding arising from atomic steps and fast energy dissipation. In real cases there is always a tilt (ψ) related to the surface miscut and a twist (θ) between the bonded wafers, which makes the re-arrangement less perfect, resembling a grain boundary at the bonded interface. The atoms at the transition between the two crystals have different arrangements than in the bulk material, with important consequences on the electrical properties. In either case, the bonding energy is above 2 J/m^2 directly after RT bonding [8]. No further annealing treatment is required. However, at high temperatures one can expect a re-arrangement of the interface atoms into more relaxed configurations.

In summary, not only does UHV bonding ensure high fracture strength without annealing, but the voids observed after hydrophobic bonding caused by trapped gas atoms and surface steps can be avoided to a large degree. Based on the high driving force associated with UHV bonding, local imperfections can be bonded by mechanical distortion. The approach was extended to crystals with different surface orientation and also to dissimilar materials [28], [29] becoming a very attractive choice for materials integration.

2.2. Layer transfer by ion implantation and wafer bonding

The transfer of single crystalline layers onto various substrates plays a major role for materials integration. Hydrophilic wafer bonding followed by implantation induced splitting is already established for producing silicon-on-insulator (SOI) wafers and offers many advantages over traditional methods such as polishing/etching techniques. This process has been termed “Smart-Cut” by Bruel [7] who also patented it. The patent was later on licensed exclusively to the commercial silicon-on-insulator supplier SOITEC in France. Its versatility has been demonstrated by extending the approach to a variety of other material combinations, such as silicon on poly-SiC [30], GaAs [31] and InP [32]. In the following, the general features of layer transfer will be discussed.

2.2.1. Basics of implantation

Ion implantation is a process by which energetic ions are introduced into a target in order to change its mechanical and electrical properties. Due to its unique characteristics such as accurate control of depth and dose, it has experienced rapid development for semiconductor industry as an alternative method for doping. Here, the particularities of ion implantation when applied to layer transfer will be outlined.

Upon entering a semiconductor material, the energetic ions lose energy by two stopping mechanisms [33]. The first is by energy transfer to the target nuclei, which causes deflection of the former and dislodging of the latter from their original sites. This process defines a *nuclear stopping* which results in structural damages of the semiconductor, such as point and line defects.

A second mechanism is by the inelastic collision of the ion with both bound and free electrons in the target. Energy is lost by means of transient generation of electron-hole pairs and ionization of the target atoms without inducing displacement. This process gives the *electronic stopping*. The energy loss per unit distance (*dE/dx*) is related to the corresponding stopping power *S* via the following equation:

$$S_{e,n} = -\frac{1}{N}\left(\frac{dE}{dx}\right)_{e,n} \tag{2.3}$$

where *N* is the density of target atoms in the semiconductor and the subscripts “e”, “n” denote electronic and nuclear stopping, respectively.

In order to establish which mechanism prevails a number of physical parameters have to be considered, including the masses and the atomic numbers of both the incident ion and the target material, the energy *E* of the incident ion, the density of the target, the crystal orientation with respect to the beam, and the lattice structure of the target. For moderate energies (50-500 keV) implants of H and He in Si and GaAs, most of the energy is lost through electronic stopping given by:

$$S_e = kE^{1/2} \tag{2.4}$$

where *k* is a function of ion-target combination [34].

Once S_n and S_e are known, one can calculate the range R given by the distance travelled by the ion before coming to rest. It is actually the projection of this range along the direction of the incident ion (projected range) that bears more significance in semiconductor technology, together with its standard deviation along the same direction (straggle). The implantation profile is usually non-Gaussian and higher-order statistics are required to describe its shape [34].

If the incident beam is aligned to a major crystallographic axis the ions travel a considerable distance through the lattice with minor energy loss, by a process known as channelling. This process is reflected in an increased penetration depth without considerable lattice disorder [35], but the range depends critically on the degree of alignment and the ion dose. Such an effect is avoided by tilting the wafer by an angle of about 7-10° away from any low index direction.

2.2.2. Hydrogen in silicon and gallium arsenide

The role of hydrogen in semiconductors, particularly in silicon has been investigated over the last two decades due to its ability to passivate the electrical activity of defects [36].

Upon entering a semiconductor hydrogen generates displacement damage in the form of interstitials, vacancies and complexes. Given a sufficiently high dose ($>1.8\text{x}10^{16}$ cm^{-2}), these point defects agglomerate along [100] and [111] planes, generating free inner surfaces, i.e. finite areas with a high number of broken bonds called platelets [37]. Already present in high concentrations, H is quickly trapped at these surfaces passivating the broken bonds [38]. It has been estimated that only about 1/8 of the implanted H is contained in the platelets, while most of H atoms are trapped by other defects like vacancy agglomerates and dislocation loops [37].

During annealing the trapped H dissociates from complexes and diffuses into the platelets forming H_2 molecules. Thus, the platelets expand into micro-cracks while the density of interstitials, vacancies and complexes decreases [39]. The pressure inside the micro-cracks increases to such values that expansion in lateral direction occurs via an Ostwald ripening process [40]. As soon as the micro-cracks join together in the same plane, material exfoliation occurs locally.

In order to understand the evolution of defects upon annealing, it is required to know the preferred lattice sites for hydrogen and possible migration paths in silicon. Van de Walle et al. [41] determined that the bond-centered site is favourable for the neutral and positively charged hydrogen, while the tetrahedral interstitial site is preferred by the negatively charged hydrogen in n-type silicon. In addition, Chang et al. [42] postulated the existence of two diatomic complexes, H_2 and H_2^* respectively. H_2 is formed by two hydrogen atoms occupying two adjacent tetrahedral interstitial sites oriented in the [100] direction and H_2^* contains one center-bonded hydrogen and one interstitial hydrogen. It is generally accepted that hydrogen exists in silicon in the form of H^+ (center-bonded), H^- (tetrahedral interstitial), H_2, H_2^*, B-H (boron doped silicon) and P-H (phosphorus doped silicon).

In GaAs, hydrogen produces very little damage up to a dose of 10^{16} cm^{-2} [43]. Few studies have been performed in order to understand the nature of defects in GaAs and their evolution during annealing [34], [44]. It has been shown that the implantation temperature must fall within an interval specific to each selection of energy and dose in order to induce blistering [26]. Radu [45] found that for doses ranging from 3 to 5x10^{16} cm^{-2} and energies of 130 keV blistering occurs directly during implantation if the temperature exceeds 100°C.

Neethling et al. [46] performed TEM investigations and proposed a theoretical model which predicts that for low doses (5x10^{15} cm^{-2}) only 1.9% of the hydrogen is trapped in the platelets developing a pressure of about 1 GPa, which corresponds to a density of 4x10^{22} cm^{-3}, i.e. 1-2 H atoms per vacancy.

2.2.3. Helium in silicon and gallium arsenide

Helium in semiconductors was studied before the development of the Smart-Cut process. Gas bubbles and micro-cracks were observed upon implantation starting in early 1980's [47], [48]. Having a lower solubility than H in silicon, He forms vacancy-related complexes and bubbles, depending on implantation parameters [49]. During annealing the bubbles grow and He diffuses out leading to void formation, provided that the dose is larger than 1x10^{16} cm^{-2}. For doses lower than 5x10^{15} cm^{-2} He vacancy clusters are formed but they dissociate below 250°C preventing bubble formation [50]. At intermediate doses, some He atoms remain trapped after annealing forming a low density of voids, but the density is not high enough to cause blistering/exfoliation.

The mechanism of exfoliation in He implanted GaAs is less clear, partly because it received less attention compared to H implantation. However, data about defect formation upon implantation exist for both (100) [51] and (111) oriented GaAs [52]. In case of (100) GaAs, TEM investigations depict a combined dislocation-bubble microstructure localized near the end-region of the damaged layer which seems to be responsible for surface flaking. Implanted and annealed (111) GaAs feature extended He platelets lying in (111) planes which grow until splitting occurs. Large area exfoliation instead of blistering was reported for RT implantation [45], favoured by the high density of small micro-cracks (with diameter much smaller than the depth where they are located) present in the implanted material. On the other hand, blisters were observed in the as-implanted sample when the implantation was performed above 100°C.

2.2.4. Blistering and splitting

So far the effects of ion implantation followed by thermal annealing have been outlined. The microscopic defects created during implantation are essential for micro-crack formation and later blistering/exfoliation.

Experimentally it has been found that for a specific set of implantation parameters and for a specific ion-target combination the surface blistering occurs only with a proper combination of annealing temperature and time. More exactly, for a specific annealing temperature surface blisters form only if the time has reached a critical value, termed blistering time (t_b). Tong et al. [53] found that t_b has an exponential dependence on the annealing temperature:

$$t_b \propto e^{\frac{E_a}{kT}} \qquad (2.5)$$

where *k* is Boltzmann's constant, *T* is the absolute temperature and E_a is the effective activation energy of the process. Fig. 2.4 features the dependence of the blistering time on the annealing temperature for H_2^+ implanted Si(100) according to [54].

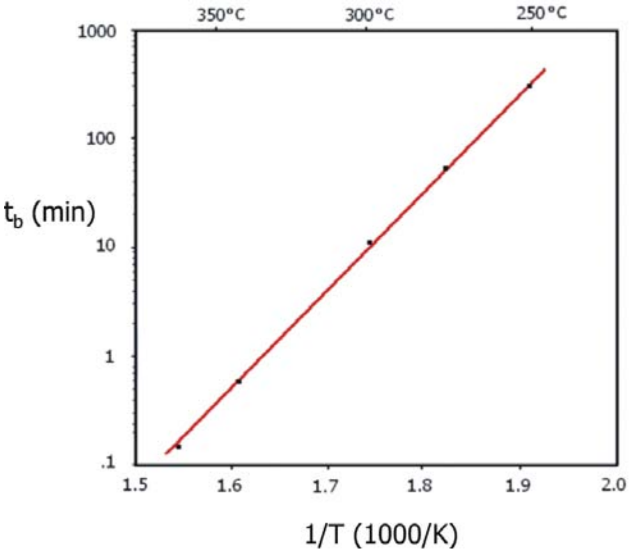

Figure 2.4: Blistering time vs. annealing temperature according to [54] (H_2^+ implantation, 135 keV, $5x10^{16}$ ions/cm^2).

In order to achieve layer transfer instead of blistering, the implanted wafer is stiffened by means of bonding to a handle wafer. Upon annealing, layer transfer occurs via large area splitting, provided that the bonding energy (at the required splitting temperature) in higher than the fracture energy of the implanted layer. Experimentally it was determined that the time required for splitting is about ten times larger than the blistering time [55], the latter being often used for estimate purposes. The layer transfer approach is summarized in Fig. 2.5.

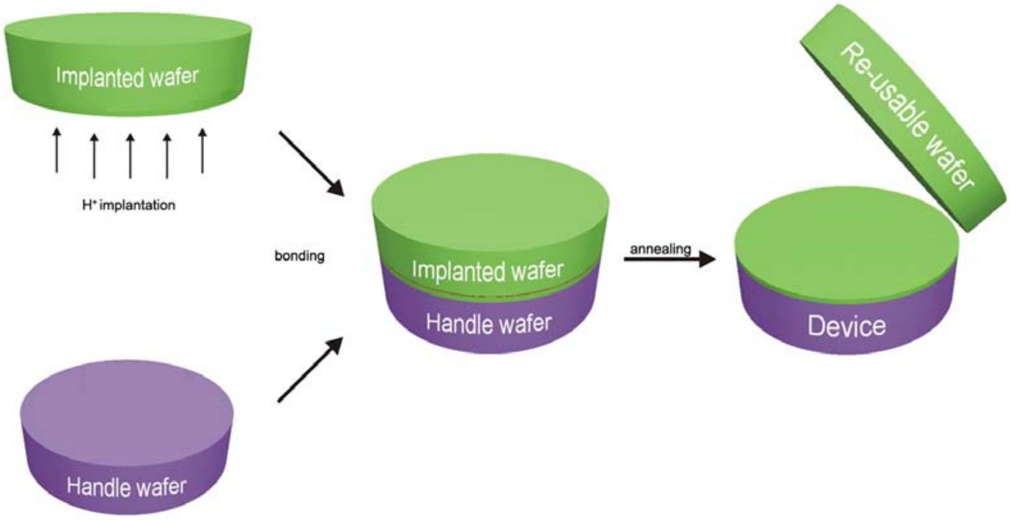
Implanted wafer
H⁺ implantation
bonding
Handle wafer
Implanted wafer
Handle wafer
annealing
Re-usable wafer
Device

Figure 2.5: Layer transfer by ion implantation, wafer bonding and anneal induced splitting.

2.3. Defects in crystalline semiconductors

Any crystalline imperfection where the atoms do not have a perfectly periodic arrangement on the lattice sites represents a defect. Defects always exist in semiconductor materials. They can be unintentionally introduced at any stage of the process flow from crystal growth to metal contacting. Undesired in most situations, defects can degrade the performance of semiconductor devices in a number of ways. They can be electrically or optically active and might become more important than dopants in determining the material properties.

According to their dimensionality the defects are usually classified in the following way:

- 0-dimensional defects, also called point defects. They include intrinsic point defects (vacancies and self-interstitials) and extrinsic point defects (impurities).
- 1-dimensional defects represented by all kinds of dislocations.
- 2-dimensional defects (planar defects) which include stacking faults, grain boundaries and phase boundaries.
- 3-dimensional defects, namely precipitates (usually involving foreign atoms), voids (agglomeration of vacancies in three-dimensional form) and special cases like stacking fault tetrahedra and dislocation clusters.

In the following, an overview of defects in silicon will be given, with emphasis on those types of defects introduced during wafer bonding.

2.3.1. Point defects

Point defects are localized defects of atomic dimensions occurring in an otherwise perfect crystal lattice. As already mentioned, they include intrinsic point defects (involving only atoms of the host lattice) and extrinsic defects (involving foreign atoms, i. e. impurities).

The simplest imaginable intrinsic point defect is the vacancy, which occurs whenever an atoms leaves its lattice site due to thermal fluctuations or vapour pressure of the species surrounding the material. In the event that the atom migrates to the crystal surface, we have the so-called Schottky defect whose energy of formation is 2.6 eV in the case of silicon. A single vacancy is created by breaking of four covalent bonds whereas two neighbouring vacancies require only six bonds to be broken. Due to this reason, di-vacancies can form as well, with higher probability than pairs of individual vacancies.

The second type of intrinsic point defect is the interstitial (or, more exactly, the self-interstitial), which occurs when an atom becomes located in one of the many interstitial positions within the crystal structure. The energy of formation of this defect in silicon is around 1.1 eV. An atom leaving its regular site has now an additional possibility – that is, ending up in an interstitial position. Thus, a Frenkel defect is created, having an energy of formation of about 9 eV.

In compound semiconductors e.g. GaAs, interstitials and vacancies can be encountered in two ways, involving either gallium or arsenic atoms. Moreover, a gallium atom has the additional possibility to take the position normally occupied by an arsenic atom (and vice-versa), thus generating an antisite defect.

The concentration of intrinsic point defects depends on their energy of formation and on the temperature. Taking into account only the possibility to form Frenkel defects, their equilibrium concentration at RT is given by [56] as follows:

$$n = Ne^{-\frac{E_f}{2kT}} \tag{2.6}$$

where N is the total number of atoms in a crystal of unit volume (roughly 5×10^{22} cm^{-3} for silicon), E_f is the energy of formation of a Frenkel defect (≈9 eV), k is the Boltzmann's constant and T is the absolute temperature. The factor 2 in the denominator of the exponent appears because the formation of a Frenkel defect requires an interstitial and a vacancy to form independently.

The extrinsic point defects (also called chemical point defects) are represented by impurities, either deliberately introduced (for doping purposes or in the case of fast switching devices) or inadvertently as contamination during processing. They can occupy either lattice sites (substitutional impurities) or interstitial sites (interstitial impurities). In many cases, the former are electrically active while the latter are inactive. Among impurities which are electrically active, donors and acceptors which have energy levels within 3kT of the conduction and valence band edges, respectively, are referred to as shallow impurities, while those with energy levels outside this range are referred to as deep, i. e. levels lying in the interval (E_c-0.1 eV)… (E_v+0.1 eV). They have the special (and most of the time undesired) property of reducing the minority carrier lifetime through the generation-recombination (G-R) mechanism. For this reason they are also called G-R centers, trapping centers or simply traps.

Shallow impurities are well known for their doping properties. Using the effective mass theory their ionization energies are found to be 0.04-0.07 eV away from the corresponding band edges. Their ionization probability depends on the concentration and on the temperature; at RT they are fully ionized for low and moderate concentrations. They are not within the scope of this work, therefore the term “defects” will only refer to deep levels henceforth.

The effective mass theory does not apply in the case of deep impurities because their electronic wave functions are more highly localized than for shallow impurities [57]. In order to illustrate the general character of deep levels in semiconductors, consider a monovalent impurity introduced into a substitutional site. Such an atom, in the neutral state, has only one attached electron which provides covalent bonding with its neighbouring lattice atoms. As soon as electrons are attached to it, it is successively transferred to a more and more negatively charged state, giving rise to as many as three acceptor levels. Additionally, the atom can lose an electron and be promoted to a positive (donor) charge state. However, in most cases only a few of these levels are identifiable due to the fact that the addition/extraction of electrons leads to such a decrease/increase of energy until the corresponding energy level eventually moves beyond the bandgap.

The concentration of these impurities depends on their availability and their solid solubility in the semiconductor material. The latter depends upon the position of the Fermi level in the semiconductor, i. e. the background doping level and type.

A special category of point defects is represented by *complexes*, which can result from the following interactions between point defects:

- intrinsic-intrinsic
- extrinsic-extrinsic
- intrinsic-extrinsic

Some of the most commonly observed complexes are those that involve association between oppositely charged donors and acceptors. When the donor and the acceptor are both singly charged, the quasi-chemical equation that describes the complex formation would be:

$$D^{+} + A^{-} = (DA)^{0} \tag{2.7}$$

This neutral complex can then be ionized by donating an electron to the conduction band or accepting a hole from the valence band. The ionization energy would be:

$$E_i = E_g + \frac{q^2}{4\pi\varepsilon}\left(\frac{1}{r_{da}} - \frac{1}{2r_d} - \frac{1}{2r_a}\right) \tag{2.8}$$

where r_d and r_a are the orbital radii of the electron in the ground state of the isolated donor and the hole in the ground state of the isolated acceptor, respectively and r_{da} is the donor-acceptor separation [58]. ε represents the absolute permittivity and q is the elementary charge. When

$$r_{da} < \frac{2r_d r_a}{r_d + r_a} \tag{2.9}$$

the ionization energy of the pair is greater than the energy gap. That is, the donor and acceptor energy levels are removed from the energy gap as the two ions are brought together. Since the Bohr radii of electrons and holes around isolated hydrogenic donors and acceptors are typically large, the formation of a complex will generally remove states from the forbidden band. There are, however, situations when a complex might be electrically active such as:

- when one of the ions is doubly charged. In this case the deeper second ionization state can remain in the forbidden gap.
- when the ionization energy of one or both of the ions is large. In this case the orbital radius of the electron or hole will be small and it might be difficult for the complex to fulfil the inequality (2.9).

In summary, both intrinsic and extrinsic point defect concentrations can be maintained in principle low enough to ensure a negligible influence on device characteristics. The use of prime quality wafers combined with semiconductor grade chemicals and a cleanroom environment would suffice, since today's silicon can be grown with metallic impurities concentrations of less than 10^{10} cm^{-3}. However, subsequent processing steps such as ion implantation, high temperature annealing, and metal contacting tend to introduce higher concentrations.

In wafer bonding, point defects might become important because they can be easily incorporated at the bonded interface. Moreover, point defects might as well play a role when interacting with dislocations.

2.3.2. Dislocations

Dislocations are one-dimensional defects which can extend throughout large regions of the crystal generating a geometric fault of the lattice. It occurs when the crystal is subjected to stresses in excess of the elastic limit. They are characterized by a core region with a diameter in the nm range, where the crystal symmetry is broken and a far-field region where an elastic field changes slowly in space. If the dislocation has dangling bonds, it can be viewed as a linear array of acceptors that scatter mobile carriers. The dangling bonds can also attract impurities and interstitials or act as an internal source and sink for vacancies. Due to the many-electron nature of the dislocations, they might have a quasi-continuous spectrum of electronic states in the bandgap [59].

Since the dislocations are one-dimensional defects, the lattice is disturbed (only) along the dislocation line. Thus, a first element to describe the dislocation at any point is the line vector $\vec{l}$. In order to describe the state of slip that generates a dislocation or has been generated by a dislocation, a second element, called Burgers vector $\vec{b}$ is introduced. It specifies the direction and distance by which atoms in one plane have moved with respect to atoms in another plane. Alternatively, the Burgers vector is defined as a closure failure arising in a cycle in the perfect material surrounding the dislocation. The slip (glide) plane is a plane along which the dislocation can move under applied stresses, and it is determined by the line and Burgers vectors.

Although the nature of dislocations is quite complex, they are usually composed of combinations of two basic types, namely the screw dislocation and the edge dislocation which will be briefly discussed in the following. A simple cubic lattice will be considered. For a detailed analysis the reader is referred to textbooks [60], [61].

Fig. 2.6 depicts the schematic representation of a screw and an edge dislocation.

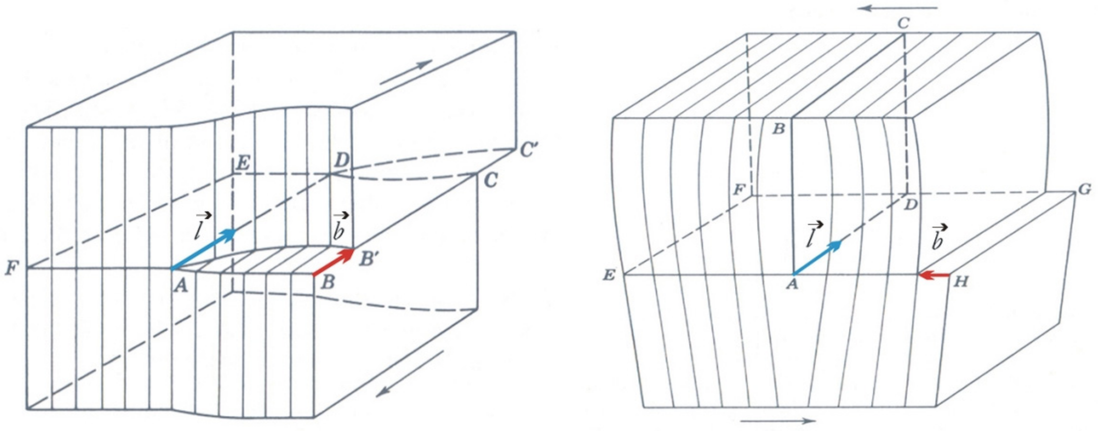

Figure 2.6: Schematic representation of a screw (left) and edge (right) dislocation.

In the first case, consider an imaginary cut in the crystal along the plane ABCD that ends on the line AD. Applying sufficiently high shear stresses on the two halves of the crystal separated by the plane ABCD, will cause them to shift by one atomic spacing. Thus, a screw dislocation is created along the line AD which marks the boundary in the plane ECBF which divides the perfect crystal from the imperfect. The line and Burgers vectors are parallel, so there is no well defined slip plane, i. e. the screw dislocation can move, in principle, in any plane. The screw dislocation doesn’t have dangling bonds but perturbs the lattice by a spiral rearrangement of bonds around its axis. Consequently, it only shifts the band edges locally without introducing deep levels in the band gap of silicon. Using elasticity theory one can get an approximate formula for the strain energy associated with a screw dislocation:

$$E_{screw} = \frac{Gb^2 l}{4\pi} \ln\left(\frac{R}{r}\right) \tag{2.10}$$

where G is the shear modulus, b is the magnitude of the Burgers vector, l represents the dislocation length, r is the core radius and R is an undetermined external radius corresponding to the distance at which strain fields of the dislocations cancel each other (typically 10^5 atom spacings). With a value of the ratio R/r of about 10^4, this energy is roughly estimated to 10-19 eV/atom length, quite high compared to the energy of formation of a point defect.

Fig. 2.6b shows how an edge dislocation can be constructed by inserting an extra half-plane of atoms, ABCD in a regular lattice. Most of the distortion will be concentrated around the line AD. An edge dislocation is created by applying a shearing force along the face of the crystal parallel to a major crystallographic plane, high enough to cause plastic deformation and move the upper half of the crystal. As observed, the Burgers vector is perpendicular to the line vector determining a glide plane on which the dislocation can move. The strain energy associated with an edge dislocation is

$$E_{edge} = \frac{Gb^2 l}{4\pi(1-\nu)} \ln\left(\frac{R}{r}\right) \tag{2.11}$$

where ν is the Poisson ratio (about 0.3 for Si and GaAs). Thus, it is approximately 60% larger than that for a screw dislocation, with important consequences on the direction that real dislocations like to assume. Two dangling bonds are present in each atomic plane along the direction of the axis; therefore a continuum of states can be expected in the band gap if no reconstruction occurs.

Due to the high energy of formation for both screw and edge dislocations, they cannot be thermally generated like point defects and thus their equilibrium concentration is negligible. They can move relatively easy by slip (along the glide plane) or climb (outside the glide plane with the help of point defects). Provided that dislocations can move within the crystal, they might come close enough to interact, tending to attract or repulse each other depending on whether their resulting strain field is smaller or larger than the individual strain fields, respectively. Thus they can create knots (point where at least three dislocations meet) and networks. The real dislocations encountered in a semiconductor material usually are mixed, having both screw and edge character. They will tend to be straight meanwhile trying to have as large screw component as possible because the total energy is proportional to both the dislocation length and the Burgers vector according to (2.10) and (2.11). If enough energy is provided to the crystal, dislocations can also multiply forming closed loops.

Dislocations cannot end inside the crystal, but only at a surface, an internal surface or interface (e.g. grain boundary), a dislocation knot or on itself (forming a closed loop).

So far only perfect dislocations in a simple cubic lattice were considered. In fcc (face centered cubic) lattices dislocations have an additional option to lower their energy, by splitting into partials (dislocations having Burgers vectors smaller than a translation vector of the lattice) accompanied by stacking fault formation. The sphalerite structure (to which both Si and GaAs belong), has two atoms in the base of the crystal. Consequently, the extra lattice plane defining an edge dislocation may come in two modifications called “glide” and “shuffle” set, because it might end in two distinct atomic positions. The dislocations of the two sets have different core structures and dangling bond configurations. A partial belonging to the glide set has dangling bonds that can disappear upon reconstruction, while the one belonging to the shuffle set doesn’t have this property [62]. For silicon, the glide set seems to prevail, while for GaAs the situation is less clear. Upon reconstruction the core atoms form bonds pair-wise and states are removed from the band gap [63]. The same effect is expected when the dangling bonds are passivated with hydrogen atoms.

High quality single crystalline silicon comes nowadays (almost) dislocation free, while GaAs is somewhat poorer in this respect with values up to 5000 dislocations/cm^2 (which can be considered still a low value). For this reason dislocations don’t represent a problem by themselves, provided that the core is reconstructed. However, if there is an increased content of both point defects and dislocations, the former might interact with the strain field of the latter, often leading to segregation of metallic impurities around the dislocation core.

In summary, if there is to be any electrical activity associated with dislocations, it must be determined by point defects or by the interplay of point defect levels and dislocation states.

2.3.3. Grain boundaries

A grain boundary is a two-dimensional defect, defined as a thin layer of atomic dimensions in a crystalline material corresponding to the transition from one crystallographic orientation to another. A grain boundary extends over the whole bonded interface and governs the electrical activity of the interface. In the following, a rather intuitive description of the grain boundaries will be given in order to emphasize the main structural features.

Imagine a diamond structure in a <110> projection, where a cut along a [111] plane has been made such as to separate the crystal in two parts (Fig. 2.7, left).

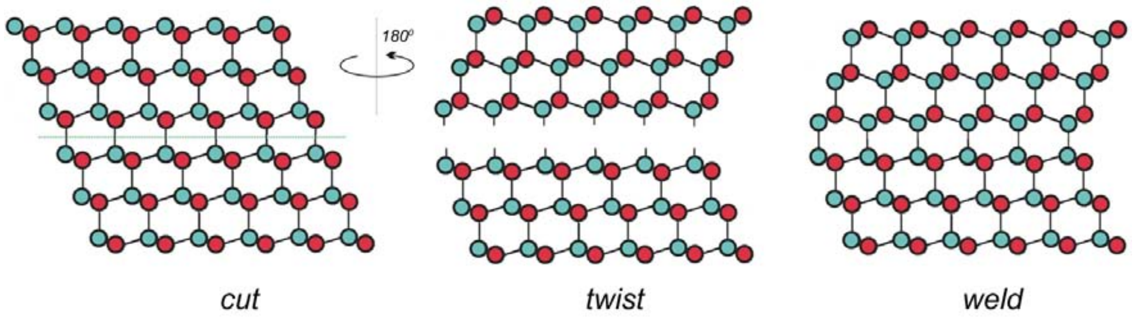

Figure 2.7: Formation of a twin boundary.

If the upper part is rotated by 180° around an axis perpendicular to the cut plane (Fig. 2.7, center) and then welded to the lower part again (Fig. 2.7, right), we obtain a structure that preserves the coherence of the lattice, therefore being termed as (coherent) twist boundary. We call it twist because the boundary was formed only by a twist operation. In a similar manner, the upper part can be tilted clockwise by a proper angle (70.53° around the <110> axis), and welded to the lower part after the necessary material removal, generating a (coherent) tilt boundary. The structure obtained in this way is identical to the previous one, and because of the mirror symmetry of the crystal along the cut/weld plane it is usually termed as twin boundary. The energy associated with a twin boundary (i. e. the energy spent in order to form one unit area of twin boundary) is quite low, since this structure preserves both the bond length and angle, and all dangling bonds find partners upon welding.

If the same exercise would be repeated using different twist (and tilt) angles, one observes that the two parts of the crystal won't fit with the same accuracy: a small number of bonds will directly find partners, some other bonds will be distorted while many bonds remain unsatisfied. Consequently, an increase in energy is expected to occur. Thus the twin boundary is a special case of a grain boundary, having the highest symmetry and the lowest possible energy. An important parameter that changes continuously upon twist and/or tilt of the two grains is the degree of coincidence (overlapping) between the lattices sites of the two crystals. This is described in terms of a coincidence site lattice (CSL) which shows that there are preferred orientations between grains that lead to high number of coincidence lattice points. Generally, low energy configurations correspond to a high number of CSL points [64], [65].

Of special interest are the small-angle grain boundaries formed when the grains have small misorientations with respect to those of a low energy configuration. In this case the grain boundary may decrease its energy by introducing grain boundary dislocations so that the dislocation free parts are now in a precise CSL orientation and the misalignment is taken up by the grain boundary dislocations. These grain boundary dislocations have the same properties as individual and separated dislocations, i. e. they posses strain and stress fields, energy, they can interact and form networks but they are generally confined to the boundary (except for the case when they split into partials). Additionally, their Burgers vectors take values belonging to the set of all possible displacement vectors which preserve the CSL.

Of course, upon bonding the wafers cannot be perfectly aligned. If we additionally consider the tilt associated with the wafer miscut, the steps and the possible foreign atoms at the wafer surface, we end up with a quite complicated grain boundary that posses energy, yields a high number of dangling (and distorted) bonds and consequently might have a quasi-continuous distribution of deep levels in the band gap by the same token as dislocations.

The determination of a dislocation structure needed to transform a near-coincidence boundary into a true coincidence boundary is a difficult task. There are two extreme cases where the misalignment is resolved in a simple manner: for a pure tilt boundary (by a sequence of edge dislocations) and for a pure twist boundary (by a network of screw dislocations). Fig. 2.8 depicts how edge dislocations can accommodate the misfit relative to a low energy orientation.

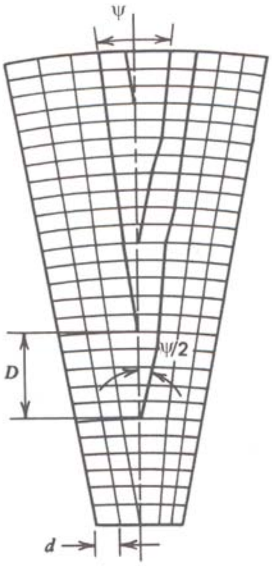

Figure 2.8: Model of a low-angle grain boundary.

If *d* is the atomic spacing, the distance between dislocations is given by:

$$D = \frac{d}{2\sin\left(\frac{\psi}{2}\right)} \approx \frac{d}{\psi} \tag{2.12}$$

where ψ is the tilt angle between the grains. The approximation in (2.12) holds only for small tilt angles (ψ expressed in radians). For $\psi \leq 1°$, the term lineage boundary is used, denoting a negligible loss of coherence. For $1° \leq \psi \leq 5°$ a low-angle grain boundary forms, preserving only partially the lattice coherence.

The electronic properties of a low-angle grain boundary can be perceived also by looking at the situation in a different way. It is well known that a freshly cleaved semiconductor surface exhibits a high number of deep-lying levels throughout the energy gap, due to the presence of unsaturated covalent bonds that are acceptor-like in character [66]. In an internal surface (or interface), many of these bonds are terminated by a partial coherence of the lattice, leading to a reduction in the density of deep levels. Thus, the less dangling bonds the less space charge around the grain boundary.

2.4. Electrical characterization of bonded interfaces

First, the properties of the bonded interfaces in thermal equilibrium are described. Afterwards, the steady state condition in case of both unipolar and bipolar current flow is discussed in terms of a voltage dependent barrier height. The electrical conductivity is explained using the well-known thermionic emission theory. In the last part of this section, an overview of the drift-diffusion model extended to incorporate deep levels is given.

2.4.1. Grain boundary barrier in thermal equilibrium

As outlined in the previous section, the bonding process causes a continuum of interface states in the band gap of silicon. These states can be either acceptor-like, i. e. causing a negative interface charge in the ionized state, or donor-like, causing a positive interface charge in the ionized state. For charge neutrality, the interface charge is compensated by a complementary space charge at both sides of the interface. Generally, the interface causes both a potential barrier and superficial distribution of recombination centers.

Taylor et al. [9] observed that grain boundaries in germanium bicrystals behave like a rectifying element in blocking direction. They developed the model of anti-serial Schottky barrier (or double-Schottky barrier) used extensively in the literature since then to describe the properties of grain boundaries [67], [68], [69], [70], [71], [72], [73], [74].

In the following, an acceptor-like grain boundary in n-type silicon will be assumed. For simplicity, the full depletion approximation will be used, which asserts that the depletion region created by the interface charge does not contain mobile charges.

According to Fig. 2.9, the relation between the interface charge Q_S and the equilibrium depletion width x_{d0} is:

$$Q_S = -2qN_D^+ x_{d0} \tag{2.13}$$

The corresponding electrical field strength $\vec{E}$ and the electrostatic potential ψ at the interface are evaluated using the Poisson equation:

$$\Delta\psi = -\frac{\rho}{\varepsilon} \tag{2.14}$$

which gives:

$$E_{\max} = E(0) = \frac{qN_D^+ x_{d0}}{\varepsilon}$$
$$\psi_{\max} = \psi(0) = \Phi_B = \frac{qN_D^+ x_{d0}^2}{2\varepsilon} \tag{2.15}$$

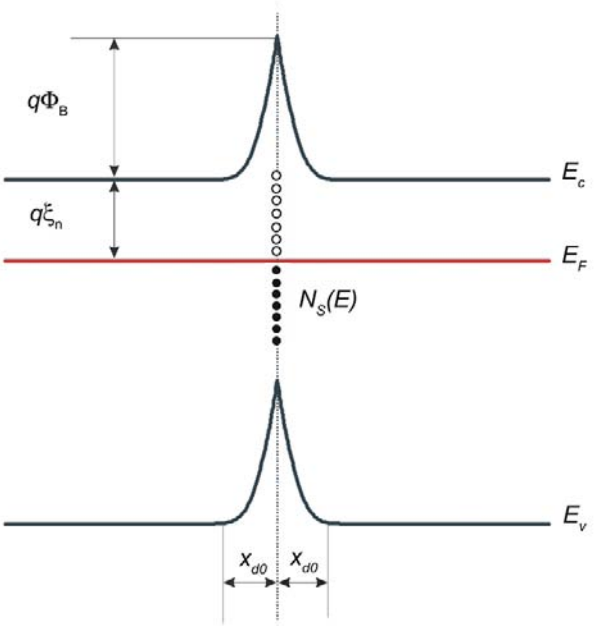

Figure 2.9: Grain-boundary barrier in thermal equilibrium.

Considering a more general situation when Q_S is represented by both donor and acceptor type levels, we have:

$$Q_S = q(N_{SD}^+ - N_{SA}^-) \tag{2.16}$$

where N_{SD}^+ represents the amount of ionized donors and N_{SA}^- the amount of ionized acceptors. In order to relate these quantities with the total available donor and acceptor states one can use the Fermi-Dirac distribution function:

$$f(E) = \frac{1}{1 - e^{\frac{E-E_F}{kT}}} \tag{2.17}$$

Thus the interface charge becomes:

$$Q_S = q\int_{E_{v,s}}^{E_{c,s}} N_{SD}(E)\left[1 - f(E)\right]dE - q\int_{E_{v,s}}^{E_{c,s}} N_{SA}(E)f(E)dE \tag{2.18}$$

The subscript “s” refers to the positions of valence and conduction band edges at the interface. One can see that the trap occupation strongly depends on the relative position of the Fermi level in the band gap. For levels situated several *kT* below the Fermi level, all states are filled with electrons whereas trap levels several *kT* above the Fermi levels are free. Consequently, acceptor type levels are negatively charged for $E_T \ll E_F$ and neutral for $E_T \gg E_F$. Similarly, donor type traps are neutral for $E_T \ll E_F$ and positively charged for $E_T \gg E_F$.

Depending on the types and densities of the interface traps, the grain boundary can cause:

- depletion layers, when $E_F - E_{i,s} > 0$
- inversion layers, when $E_F - E_{i,s} < 0$
- accumulation layers, when $E_F - E_{i,s} < E_F - E_{i,b}$ (E_i denotes the intrinsic Fermi level and the subscripts "b" and "s" refer to bulk and interface values, respectively)

2.4.2. Unipolar current through the interface

The current flow above the potential barrier is modelled using the thermionic emission theory [75]. Thus, only carriers having energy greater than ($E_C + \Phi_B$) can contribute to the current. In thermal equilibrium, the barrier height that carriers need to overcome is identical for both sides of the grain boundary, yielding zero current.

As soon as a potential difference *U* is applied across the barrier, the energy bands on the right hand side of the grain boundary are lowered compared to the left exactly by this amount as depicted in Fig. 2.10.

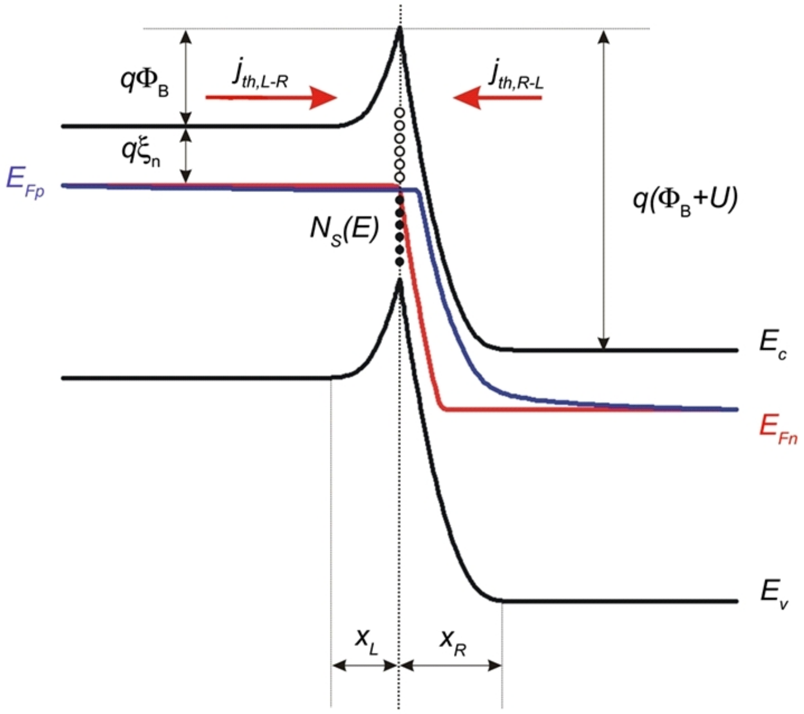

Figure 2.10: Barrier height and trap occupancy in the unipolar case.

The Fermi level splits into the quasi-Fermi levels (QFL) for holes and electrons, E_{Fn} and E_{Fp}, respectively, while the carrier densities outside the depletion region remain at their equilibrium values.

The thermally emitted current is given by the difference between the current components flowing into the interface from either side of the grain boundary:

$$\begin{aligned} J_{th,L\rightarrow R} &= -A_n^* T^2 e^{-\frac{q(\xi_n+\Phi_B)}{kT}} \\ J_{th,R\rightarrow L} &= -A_n^* T^2 e^{-\frac{q(\xi_n+\Phi_B+U)}{kT}} \end{aligned} \tag{2.19}$$

Thus:

$$J_{th,n} = J_{th,R\rightarrow L} - J_{th,L\rightarrow R} = A_n^* T^2 e^{-\frac{q(\xi_n+\Phi_B)}{kT}}\left(1-e^{-\frac{qU}{kT}}\right) \tag{2.20}$$

The Richardson constant for electrons A_n^* is given by:

$$A_n^* = \frac{4\pi q m_n^* k^2}{h^3} \tag{2.21}$$

where m_n^* is the effective mass of electrons in the crystal, h is Planck's constant and ξ_n is the demarcation between the conduction band edge in the bulk and the QFL for electrons. Since m_n^* depends on the wavevector $\vec{k}$, A_n^* depends on the crystallographic orientation to some degree.

The current increase is accompanied by a decrease of the potential barrier Φ_B. Consequently, the depletion width at the left of the grain boundary decreases, while the depletion width at the right increases according to:

$$\begin{aligned} x_L &= \sqrt{\frac{2\varepsilon}{qN_D^+}\Phi_B} \\ x_R &= \sqrt{\frac{2\varepsilon}{qN_D^+}\left(\Phi_B+U\right)} \end{aligned} \tag{2.22}$$

Due to the decreasing potential barrier height, the QFL for electrons approaches the conduction band edge, leading to an additional occupation of interface states:

$$\Delta Q_S = -q\int_{E_F}^{E_{Fn}} N_S(E)f(E)dE \tag{2.23}$$

For this reason, the maximum voltage drop at the interface corresponding to a collapse of the barrier can reach values as high as 100 V in the case of unipolar current flow for moderate doping levels.

2.4.3. Bipolar current through the interface

In the case of a bipolar current, both electrons and holes are involved in the transport process. The position of the associated QFLs is given by [76]:

$$
\begin{aligned}
n &= n_i e^{\frac{E_{Fn}-E_i}{kT}} \\
p &= n_i e^{\frac{E_i-E_{Fp}}{kT}}
\end{aligned}
\tag{2.24}
$$

An increasing electron concentration is accompanied by a rise of the QFL for electrons towards the conduction band edge, and an increasing hole concentration causes a rise of the QFL for holes towards the valence band edge (the direction of energy increase for holes is opposite to that of electrons). As a consequence, the trap occupancy will no longer be given solely by the position of the E_F and QFL for electrons. Fig. 2.11 depicts the situation in the case of bipolar current flow, where the trap occupancy changes according to the position of both QFLs.

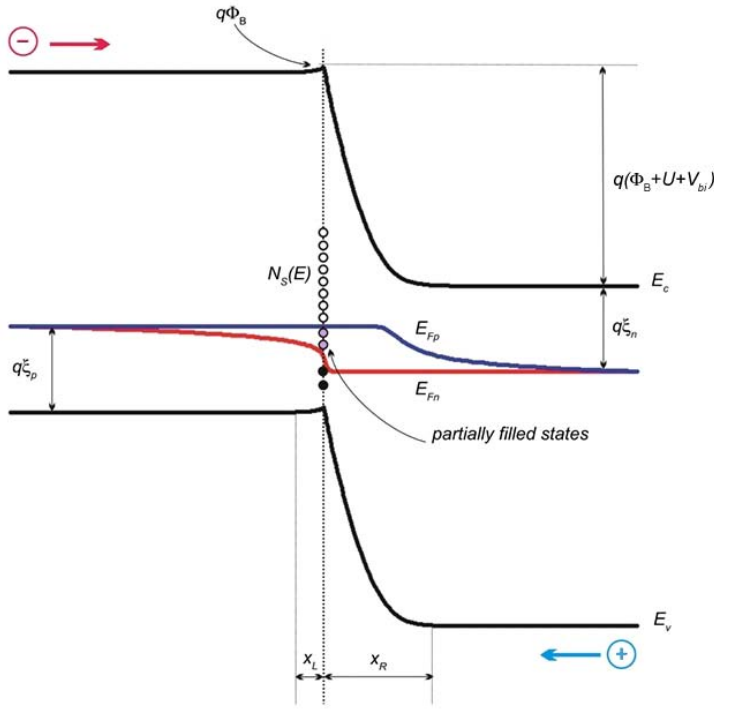

Figure 2.11: Barrier height and trap occupancy in the bipolar case.

In order to predict the trap occupancy, two simplifying hypotheses are made:

- no interaction between different trap levels is considered.
- the emission of electrons into the conduction band is neglected for trap energies lower than E_{Fp} and the emission of holes into the valence band for energies higher than E_{Fn}, respectively.

According to [77] the occupation probability in the case of a bipolar current can be approximated to:

$$f(E) = \begin{cases} 1 & for \quad E < E_{Fp} \\ \dfrac{R_{th} n}{p + R_{th} n} & for \quad E_{Fp} < E < E_{Fn} \\ 0 & for \quad E > E_{Fn} \end{cases} \tag{2.25}$$

where R_{th} is the ratio between the capture coefficients of electrons c_n and holes c_p, respectively. Equation (2.25) tells us that the occupation probability decreases between E_{Fn} and E_{Fp}, leading to a decrease of the absolute total value of the interface charge:

$$\Delta Q_S = q \int_{E_{Fp}}^{E_{Fn}} N_S(E)\left[1 - f(E)\right] dE \tag{2.26}$$

In contrast to the unipolar case, the decreasing potential barrier is accompanied by a decrease of the negative interface charge when applying a potential difference *U* across the interface.

Recalling (2.20) which describes the current flow across the interface in the case of unipolar transport, an extra contribution of holes thermionic current is added in a similar fashion:

$$J_{th,p} = A_p^* T^2 e^{-\frac{q\xi_p}{kT}} \left(1 - e^{-\frac{qU}{kT}}\right) \tag{2.27}$$

where $\xi_p = E_{Fp} - E_{v,b}$ is the effective barrier for holes. For low injection conditions in an isotype junction (same type of doping in both sides of the interface), $\xi_p > \xi_n$ and the overall current is a pure electron current.

2.4.4. Generation-recombination statistics at traps

The above derived formulas for transport at bonded interfaces rely on the full depletion approximation, which gives inaccurate results in some cases. Moreover, the current across the interface as given by (2.20) depends on the barrier height Φ_B which in turn depends on the trap density (and occupancy) at the interface. By using the drift-diffusion model coupled with equations describing the charge conservation at traps, one can obtain a set of six coupled partial differential equations which can be numerically solved to give accurate simulation of bonded interfaces. This model covers almost anything except for tunnelling and impact ionization, provided that the necessary boundary conditions are given.

First, the generation-recombination process involving a trap and the conduction and valence bands will be briefly described. With a single trapping level E_T close to the middle of the bandgap (Fig. 2.12), four processes can occur.

In a first step, the trap can capture an electron from the conduction band at a rate given by:

$$r_c = \sigma_n v_{th,n} n N_T (1-f) \tag{2.28}$$

which depends on the capture cross-section for electrons σ_n, the thermal velocity of the electrons in the crystal $v_{th,n}$, the number of available traps N_T and the trap occupancy by the (presently unknown) distribution function f. The reverse process is called electron emission, given by:

$$g_c = e_n N_T f \tag{2.29}$$

e_n being the emission coefficient for electrons.

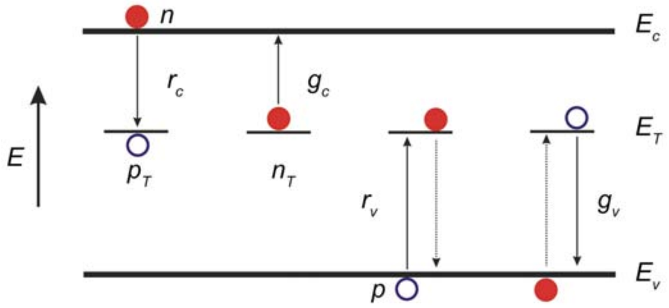

Figure 2.12: Capture and emission processes between the level E_T and the conduction and valence bands.

In a similar manner the fall of a trapped electron to the valence band (viewed as a hole capture from the valence band) is described:

$$r_v = \sigma_p v_{th,p} p N_T f \tag{2.30}$$

with σ_p and $v_{th,p}$ analogously defined as the capture cross-section for holes and the thermal velocity of holes, respectively. The reverse electron excitation from the valence band to the trapping level (viewed as a hole emission to the valence band) is described by the following equation:

$$g_v = e_p N_T (1-f) \tag{2.31}$$

e_p being the emission coefficient for electrons.

The difference between the captured and emitted electrons gives the net electron recombination rate. The net hole recombination rate is defined similarly:

$$\begin{aligned} U_n &= r_c - g_c \\ U_p &= r_v - g_v \end{aligned} \tag{2.32}$$

Finally, we are in a position to describe the trap occupancy in time (charge conservation):

$$\frac{\partial n_T}{\partial t} = U_n - U_p \tag{2.33}$$

We add the continuity equations for electrons and holes:

$$\begin{cases} \dfrac{\partial n}{\partial t} = \dfrac{1}{q}\nabla J_n - U_n \\ \dfrac{\partial p}{\partial t} = -\dfrac{1}{q}\nabla J_p - U_p \end{cases} \tag{2.34}$$

where J_n, J_p are the total electron and hole current densities (summing drift and diffusion components):

$$\begin{aligned} J_n &= q\mu_n n + qD_n \nabla n \\ J_p &= q\mu_p p - qD_p \nabla p \end{aligned} \tag{2.35}$$

μ_n and μ_p represent the electron and hole mobilities and D_n, D_p the diffusion coefficients for electrons and holes, respectively. The Poisson equation is needed for overall charge balance:

$$\Delta\psi = -\frac{q}{\varepsilon}\left(p - n + N_D^+ - N_A^- + n_T\right) \tag{2.36}$$

The term n_T accounts for charged traps in the volume of the semiconductor.

Although the system of equations (2.33)-(2.36) can only be solved numerically, the trap occupancy can be obtained in an analytical form for particular cases. In steady state $U_n=U_p$, i. e. the trap occupancy doesn't change any more with time. Moreover, in thermal equilibrium each emission process is balanced by the corresponding capture process. Then a crucial assumption (not necessarily valid in all cases) is made: the capture and emission coefficients in non-equilibrium remain equal to their equilibrium values $e_n \approx e_{n0}$, $e_p \approx e_{p0}$, $c_n \approx c_{n0}$, $c_p \approx c_{p0}$ [58], [78]. Letting $v_{th,n}=v_{th,p}=v_{th}$, we have:

$$e_n = \sigma_n v_{th} n_0 \frac{1-f_0}{f_0} = \sigma_n v_{th} n_t \tag{2.37}$$

f_0 denoting the thermal equilibrium Fermi-Dirac distribution as given in (2.17) and

$$n_t = n_i e^{\frac{E_T - E_i}{kT}} \tag{2.38}$$

which is the concentration of electrons that would be in the conduction band if $E_F=E_T$. In a similar fashion:

$$e_p = \sigma_p v_{th} p_0 \frac{f_0}{1-f_0} = \sigma_p v_{th} p_t \ , \qquad p_t = n_i e^{\frac{E_i - E_T}{kT}} \tag{2.39}$$

The non-equilibrium distribution function f can now be obtained recalling the steady-state condition, with the result:

$$f = \frac{\sigma_n n + \sigma_p p_t}{\sigma_n (n + n_t) + \sigma_p (p + p_t)} \tag{2.40}$$

The steady-state net recombination rate can be calculated:

$$U_n = U_p = U = \frac{\sigma_n \sigma_p v_{th} N_T (np - n_i^2)}{\sigma_n (n + n_t) + \sigma_p (p + p_t)} \tag{2.41}$$

this is the well-known Shockley-Read-Hall (SRH) formula for band-to-impurity recombination [79]. With additional definitions,

$$\frac{1}{\tau_{p0}} = \sigma_p v_{th} N_T \qquad \text{and} \qquad \frac{1}{\tau_{n0}} = \sigma_n v_{th} N_T \tag{2.42}$$

(2.41) becomes

$$U = \frac{np - n_i^2}{\tau_{p0}(n + n_t) + \tau_{n0}(p + p_t)} \tag{2.43}$$

For $\tau_{n0}=\tau_{p0}=\tau$, the expression for the net G-R rate can be further simplified:

$$U = \frac{np - n_i^2}{n + p + 2n_i \cosh\left(\frac{E_i - E_T}{kT}\right)} \frac{1}{\tau} \tag{2.44}$$

This tells us that the recombination efficiency increases as the trap level lies closer to the intrinsic Fermi level E_i. Therefore, midgap traps are very efficient G-R centers while shallower traps usually contribute to the band shift via traping-detraping mechanism involving only one type of carriers.

In the case of surface/interface traps, a surface recombination velocity is defined analogously to the minority carrier lifetimes given by (2.42) as:

$$S_{n,p} = N_S \sigma_{n,p} v_{th} \tag{2.45}$$

Chapter III

EXPERIMENTS

3.1. Materials used in the experimental study

According to the theoretical investigations presented in the previous chapter, the bonding process causes both a potential barrier and G-R centers at the interface with important consequences for the electrical properties of the fabricated devices. The impact of the interface on the current-voltage characteristics should be more pronounced in unipolar devices since in that case the occupation of interface states increases when the device is biased, opposite to the bipolar case. Impurities and material imperfections can further influence the properties of the devices.

The objective of this work is the investigation of the steady-state and transient electrical behaviour of unipolar and bipolar devices fabricated by UHV bonding. Special attention has been given to the possibility of combining ion implantation with UHV bonding in order to induce transfer of ultra-thin layers onto silicon substrates. High quality single-crystalline Si and GaAs wafers mainly (100) oriented were used to fabricate homo- and heterojunctions. The wafer diameter was 100 mm in all cases and the thickness was 525 μm ± 25 μm and 625 μm ± 25 μm for Si and GaAs wafers, respectively. The doping of the Si wafers was in the range 10^{14}-10^{18} cm^{-3} for both n and p-type wafers. The GaAs wafers were n-type doped, in the range 10^{17}-10^{18} cm^{-3}.

The implantations were performed by the company Implant Sciences located in USA. In all cases, the implantation was performed at RT using a 7° tilt of the beam with respect to a direction perpendicular to the wafer surface (see Section 2.2.1, Chapter II). Different energies and doses listed in Table 3.1 were used in order to determine the optimal conditions for achieving large-scale transfer.

Implanted species	Energy (keV)	Dose (x10^{16} ions/cm^2)	Target	
			Material	Doping (cm^{-3})
H_2^+	30	1.5	(111)Si	3x10^{14} (n)
H_2^+	30	1.5	(100)Si	1x10^{15} (p)
H_2^+	30	1.8	(100)Si	1x10^{15} (p)
H_2^+	130	5	(100)Si	4x10^{17} (p)
H_2^+	130	5	(111)Si	6x10^{14} (n)
He^+	60	3	(100)GaAs	5x10^{17} (n)
He^+	60	5	(100)GaAs	5x10^{17} (n)

Table 3.1: Implantation conditions for layer transfer experiments.

The Si wafers were capped before implantation with a thermally grown SiO_2 layer (thickness around 50 nm) for protection. The GaAs wafers had no protection except for their native oxides.

3.2. Wafer cleaning

3.2.1. Cleaning of silicon surfaces

In the case of silicon, the cleaning sequence follows the steps described in Section 2.1.2, Chapter II. The procedure was carried out in a conventional chemical lab (in a fume hood) using high purity quartz jars (for RCA1 and RCA2) and Teflon vessels (for HF dipping). The wafers were handled using Teflon tweezers and holders. VLSI (very large scale integration) grade chemicals were used together with ultrapure DI-water (resistivity 18 MΩcm) with TOC content (total organic contaminants) of 5-10 ppb. A particle filter at the nozzle of the purifying system ensures that the DI-water is free of particles larger than 0.22 μm.

The whole handling equipment was cleaned with RCA1 before coming in contact with the wafers, in order to remove dust particles and organic contamination. After thorough water rinse, the wafers undergo RCA1 and RCA2 cleaning for 10-15 min at 75-80°C. Since implanted wafers frequently exhibit a layer with dark-brown colour (probably due to implantation induced polymerisation of the contaminants present in the implanter chamber), additional H_2SO_4:H_2O_2 cleaning in an ultrasonic bath is performed before RCA1.

Hydrophilic bonding was performed only for training purposes and it is not within the scope of this work. Therefore, RCA cleaning was followed by HF dipping in order to remove the native (or thermally grown) oxide. Typical HF concentrations in H_2O of 2-5% and dipping times of 0.5-2 min were sufficient to completely remove the oxide without Si etching. Since the cleaning/handling was not performed in a cleanroom, it was essential to minimize as much as possible the exposure time of the hydrophobic surfaces before pre-bonding. The microcleanroom setup used for hydrophilic bonding [12] required the wafers to be dipped in succession (one after another) and introduced relatively long delays during which surfaces got contaminated. Therefore, another approach was used in order to decrease the delay to 5-10 sec. A T-shaped Teflon holder was designed in such a way to keep two wafers face to face during dipping using a pair of spacers. As soon as the wafers were taken off the solution, the spacers were removed and the wafers were pressed against each other in order to initiate the bonding. The bonding quality still showed some unavoidable scattering; sometimes the pre-bonding could not be achieved at all. Nevertheless, in this way the hydrophobic surfaces could be quickly protected before being transferred to the UHV assembly.

3.2.2. Cleaning of gallium arsenide surfaces

When cleaning GaAs surfaces, difficulties arise due to the partially ionic character of the Ga-As bonding which reflects in a lower stability of GaAs compared to Si. Because of this, GaAs surfaces are prone to decomposition upon wet chemical cleaning. Trials to remove native oxides and contamination using standard RCA cleaning result in roughness that renders the wafer inappropriate for bonding. Moreover, GaAs does not have a well defined native oxide, the composition and thickness varying as a function of storage conditions and initial surface treatment. It is generally accepted that As_2O_x (with x=1, 3 and 5), Ga_2O_3 and $GaAsO_4$ can be found in different proportions on GaAs surfaces [1], [80], [81].

The standard method used to remove organics [82] relies on the ability of organic solvents such as trichloroethylene, acetone and ethanol to dissolve hydrocarbons. However, water rinse with ultrasonic waves, needed as a final step, can roughen the surface to some degree. For this reason, an approach based on ozone cleaning was used instead [83]. The wafers were exposed to ultra-violet radiation generated by a 172 nm Xe_2 lamp in low oxygen pressure. Contamination removal is accompanied by an increase of the oxide thickness with exposure time: As_2O_5 and Ga_2O_3 grow linearly as a function of time, while As_2O_3 grows logarithmically [84].

A decrease of the treatment time from 60 minutes to 1-2 minutes could be achieved using only O_2 gas; thus O^- radicals were involved in the cleaning process along with O_3, since they appear to be more reactive to organic contaminants than ozone itself. On the other hand, it is well known that O_2 molecules absorb strongly electromagnetic radiation with wavelengths between 130 and 175 nm [85]. By letting the absorption length be of the same order of magnitude as the distance of the UV lamp to the wafer, the O^- radicals near the wafer surface had a chance to react with adsorbed organic molecules. This was achieved by adjusting the O_2 pressure to 20 mbar, adding N_2 up to atmospheric pressure since the UV lamp did not work at very low pressures. These settings ensure an absorption length of ca. 10 cm, equal to the distance of the lamp to the wafer.

After UV/O_3 degreasing, the wafers were transferred to the UHV assembly.

3.3. Bonding procedure

3.3.1. The UHV system

All bonding experiments were performed using the UHV assembly developed by A. Plössl and H. Stenzel. The system is designed for 100 mm wafers. It consists of several vacuum chambers with various functionalities connected to a main transfer chamber, which contains a mechanism used to move the wafers from one chamber to another.

Once the wafers were cleaned and pre-bonded, they were transferred to the UHV assembly and processed in a few steps. First, the wafer pairs were inserted in a so-called load-lock chamber which was used as a buffer between ambient atmosphere and UHV. After the pressure reached a sufficiently low value ($<10^{-8}$ mbar) the flange interconnecting the load-lock and the next chamber was opened. The wafer pairs were transferred into the splitting chamber where they were separated using four disk-shaped knives. Afterwards, the wafers could be transferred to any of the chambers via the main transfer. A small turning chamber allows 180° rotation of the wafers (from ‘face up’ to ‘face down' and vice-versa) followed usually by hydrogen desorption inside the heating chamber which could withstand temperatures up to 750°C. The wafers were maintained in a storage chamber which is endowed with a low-energy electron diffraction (LEED) system. Different layers (Au, Pt, Dy, Fe, Co) could be deposited onto wafer surfaces with the help of four small e^--beam sources and one large e^--beam unit. The processing of GaAs wafers (heating, atomic H bombardment) was performed in a separate chamber where also UV laser photodesorption experiments were done. Finally, a bonding chamber encloses a special mechanism which allowed bonding with a twist accuracy of ±1°. The bonding chamber is also endowed with a small heater for intermediate temperatures (as high as 400°C).

The pressure in all chambers is maintained below 1×10^{-10} mbar using a combination of turbo-molecular and ion-getter pumps. The partial pressure during experiments inside the GaAs chamber and the heating chamber is monitored by two quadrupole mass spectrometers (QMS) connected to a PC.

3.3.2. Silicon-silicon bonding

As discussed in Section 2.1.5 Chapter II, the RT covalent bonding requires activation of the surfaces by hydrogen desorption. This was done inside the heating chamber by heating to about 500°C at a rate of 5K/min followed by natural cooling to RT. Afterwards the wafers were transferred to the bonding chamber, where they were placed horizontally on top of each other, face to face, at a distance of about 5 mm. A mechanism operated by a lever releases the upper wafer causing it to fall on the lower one. The RT bonding occurred instantaneously as the wafers join together.

In order to study the influence of the bonding temperature on the electrical properties of the interfaces, the wafers were heated to about 200-250°C before bonding, using high power lamps placed outside the bonding chamber, the heat propagating inside through a 100 mm viewport.

The standard thermal desorption procedure could not be applied to implanted wafers, since the implantation induced splitting/blistering is a thermally activated process (Section 2.2.4, Chapter II). The conditions used for standard thermal desorption would destroy the surface quality due to onset of blistering, rendering it unbondable. Instead, a photothermal desorption approach was used by means of short laser pulses [86]. A KrF excimer laser having a wavelength of 248 nm and pulse width of 20 ns yielded energy densities between 60 and 1500 mJ/cm^2, corresponding to focused and unfocused conditions, respectively. The beam was supplied to the vacuum chamber via a quartz viewport under 45° incidence. Both single-shot and multi-pulse regimes were used (pulse frequency 1-10 Hz). After photothermal desorption, the implanted wafer was bonded to a handle wafer whose surface was activated as described in Section 2.1.5, Chapter II. After bonding, annealing experiments were performed in order to induce splitting following the process flow described in Fig. 2.5, Chapter II.

3.3.3. Silicon-gallium arsenide bonding

Due to reasons already outlined, GaAs surfaces were still covered with a thin oxide layer upon entering the UHV assembly.
Therefore, in order to achieve direct covalent boding of Si to GaAs the oxide has to be removed first.

The possibility of oxide removal by pure thermal means was initially studied since it was known that most of the oxide species present on the surface are quite volatile, leaving the surface at temperatures lower than 400°C, except for Ga_2O_3 which requires about 570°C to evaporate [81], [87]. Since this temperature is close to the range where GaAs undergoes decomposition due to massive arsenic evaporation, an alternative approach based on low energy atomic H bombardment was investigated [88], [89]. The atomic hydrogen beam was produced by feeding molecular hydrogen through a tantalum capillary heated by electron bombardment to 1800 - 2100 K. According to [90], this temperature is sufficient to achieve nearly total H_2 dissociation under relevant working pressures ($1x10^{-6}$ mbar inside the chamber and higher in the capillary). The wafers were heated during bombardment to temperatures of 300-600°C using exposure times between five minutes and one hour.

After oxide removal, the GaAs wafers were transferred into the bonding chamber and bonded at RT to silicon wafers whose surfaces were activated according to the procedure described in Section 2.1.5, Chapter II. The bonding procedure follows the process flow described in Fig. 3.1.

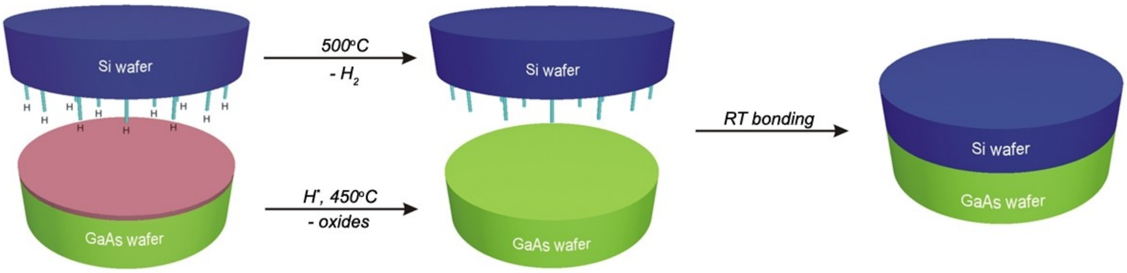

Figure 3.1: Schematic representation of the Si-GaAs RT bonding

For implanted GaAs wafers the oxide removal was attempted using the same photothermal desorption approach by means of excimer laser pulses. In order to avoid blistering and/or material ablation during laser irradiation, the energy density was kept to lower values compared to the case of silicon, i. e. 60-120 mJ/cm^2. Both single-shot and multi-pulse regimes were used.

3.4. Annealing experiments

When the temperature of a semiconductor material is increased sufficiently, it is expected that atoms start to move in the crystal lattice. This is particularly important at grain boundaries, where migration and interdiffusion could lead to a more relaxed interface. In implanted specimens, annealing can partially heal the implantation damage.

Si-Si interfaces were annealed at 1000°C in H_2 atmosphere (pressure 1 bar). The annealing was done in a quartz furnace for 5 hours. A temperature ramp of 30 K/min was used during heating and cooling.

For Si-GaAs interfaces, two kinds of annealing experiments were performed. In the case of Si-GaAs samples prepared by bonding, the GaAs layer had to be partially etched from 600 μm to about 20 μm using a H_2SO_4:H_2O_2:H_2O=8:1:1 mixture. The layer thickness was further reduced from 20 to 5 μm using chemo-mechanical polishing (CMP) with Syton. This was done in order to allow the samples to withstand the stress related to the difference in thermal expansion coefficients of the two materials. The samples were enclosed in a quartz ampoule after the air was evacuated to a pressure of $1x10^{-5}$ mbar. To ensure an arsenic overpressure during annealing, a large piece of GaAs was placed on top of the Si-GaAs sample before sealing the ampoule. The samples were heated to 850°C for 30 min using a temperature ramp of 10K/min.

In the case of Si-GaAs samples prepared by layer splitting, the thinning down step was not necessary, since the thickness of the transferred GaAs layer was in the range 0.4-0.6 μm. The annealing was performed in a quartz furnace at 850°C for 30 min in H_2 atmosphere (pressure 1 bar) using a temperature ramp of 10 K/min.

3.5. Investigation of the bonding quality

The first and most used investigation tool for analysis of bonding interfaces is the transmission infrared imaging. Apart of being straightforward and quick, it allows the inspection of a whole wafer pair in one step. It can be applied to both pre-bonded and UHV bonded pairs and relies on the property of silicon (and other semiconductors) of being transparent to infrared light. As a consequence, a first limiting factor is given by the fact that the band gap of the investigated semiconductor must be higher than the photon energy of the incident light. Silicon is transparent to wavelengths between 1200 and 1800 nm [91], provided that the doping level doesn't exceed 10^{19} cm^{-3}.

The system consists of an infrared light source and a CCD camera. The pair to be investigated is introduced between the source and the camera allowing the detection of the transmitted light and the storage of the resulting image.

The method is attractive especially for pre-bonded wafers in order to estimate the amount of macroscopic particles trapped at the interface, since they will clearly appear surrounded by dark areas as depicted in Fig. 3.2 (left). Light interference at unbonded areas produces fringes which appear as dark rings in the transmitted beam (Fig. 3.2, right). The features of these interference fringes allow the determination of the local separation between the wafers [92]. It is possible to combine the infrared imaging method with the double cantilever beam test [93], in order to estimate the bonding energy between the wafers. In this method, a blade of thickness *2h* is inserted at the bonded interface so as to debond an area of crack length *c*. At equilibrium, the elastic strain energy in the bended wafers equals the work of adhesion *W* required to form two new surfaces through the extension of the crack:

$$W = \frac{3Eh^2d^3}{4c^4} \tag{3.1}$$

with d being the wafer thickness and E denoting Young's modulus in the direction of the crack propagation.

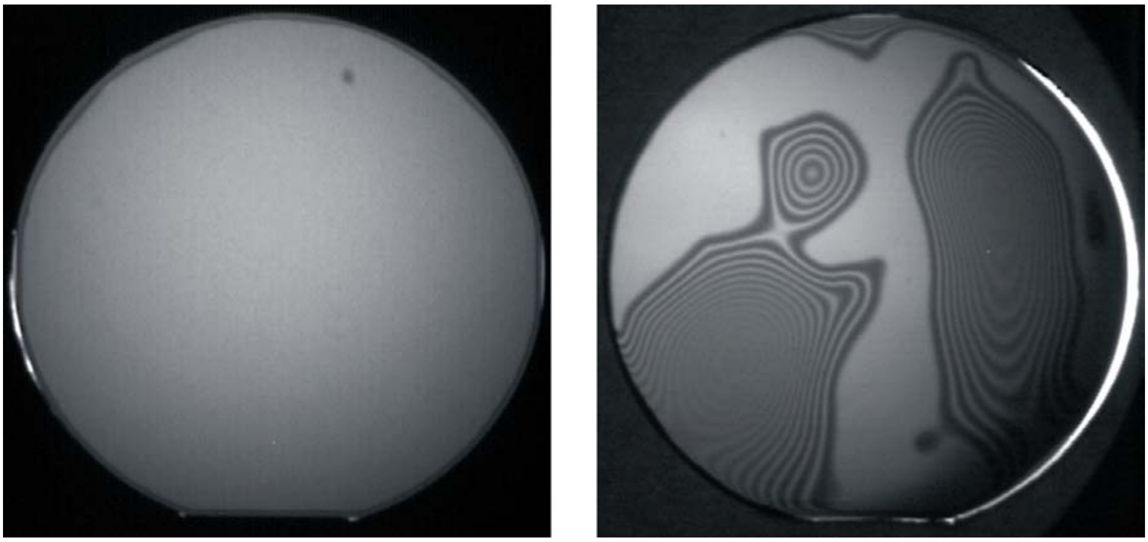

Figure 3.2: Infrared transmission image of a nearly-perfect bonded interface (left) and an interface featuring large unbonded areas (right).

Due to its simplicity and low demands, the infrared imaging is still very popular and was also used in this study to investigate bonded pairs at different processing stages. However, details smaller than 1 mm cannot be properly visualised with this method. An improved lateral resolution can be achieved using scanning acoustic microscopy [94], which in turn requires higher bonding energies to ensure stability of the wafer pair when immersed in the liquid required for transmitting the ultrasounds to the bonded wafer pair.

3.6. Electrical characterization

3.6.1. Sample contacting

After bonding the wafer pairs were transferred to the platinum chamber and/or to the e^--beam chamber for contacting. Ohmic contacts were prepared by e^--beam evaporation of Pt (on p-type substrates) and Sb (on n-type substrates) followed by Al deposition done in an external unit. Pt reacts with Si forming Pt_2Si which exhibits a low Schottky barrier height on p-type Si [95]. Sb is a doping element for Si and increases locally the substrate doping, creating an Al-Si tunnelling contact. Unfortunately Sb is quite volatile, developing a vapour pressure of 10^{-8} mbar at 280°C and can contaminate the e^--beam chamber. For this reason it was subsequently replaced with Dy which develops the same vapour pressure at 625°C and forms a silicide with low barrier on n-type silicon [96].

For GaAs substrates, Sn/Al and Ge/Au/Al tunnelling and alloyed contacts were prepared.

In some cases the ohmic contacts could not be prepared directly after bonding because the wafer pairs needed to be removed from the UHV assembly and undergo different processing steps (e. g. splitting experiments). After a quick cleaning step meant to remove particles and contaminants (a H_2SO_4:H_2O_2=3:1 mixture for Si-Si samples and acetone/ethanol/DI-water for Si-GaAs samples) the native oxides were removed by HF and HCl dip for Si and GaAs substrates, respectively. The samples were mounted on a disk shaped holder and were transferred to UHV where the metallization was done as described in the previous paragraph.

The quality of the contacts was influenced to a high degree by the surface cleanliness right before metallization and by the substrate doping.

3.6.2. Lock-in Thermography

Lock-in Thermography is a technique which allows a fast mapping of the current crossing the interface in terms of thermoelectric responses coming from different regions of the interface when a periodic current is applied to the bonded wafer pair. This type of excitation generates a broad spectrum of thermal wave frequencies having different penetration depth (proportional to the wavelength) and phase angle. Higher Fourier components are damped away, only the fundamental frequency being dominant and giving a thermoelectric signal.

The heat radiated by the wafer pair was detected at each 5 ms by a highly sensitive infrared camera endowed with an InSb sensor, being correlated with a sine and cosine wave synchronised to the exciting voltage signal. Thus it was possible to determine the amplitude and phase image of the heat distribution across the bonding interface [97]. The depth of the detected heat signal can be determined using the phase image. The frequency of the applied voltage must be tuned to make sure that the signal comes from the bonded interface and not from the ohmic contacts.

Typical DC voltages up to 1 V were applied to the samples (both forward and reverse in case of diodes). The current source was switched on and off by the lock-in electronics with frequencies of 3-30 Hz. In order to ensure the uniformity of the electrical contact, the metalized wafer surfaces were covered with a thin nickel foil and were enclosed into a black cover which was evacuated using a vacuum pump. Thus, contact discontinuities due to air bubbles were avoided. Typical heat amplitudes up to 5 mK were generated at the bonded interfaces. The brighter the amplitude image, the higher the current densities flowing across the interfaces.

3.6.3. Current-Voltage measurements

Current-voltage (I-V) measurements were performed using the four-point probe technique [78]. For this purpose, 3x1 mm^2 rectangular shaped samples were cut after metallization according to Fig. 3.3.

In order to arrange the four contacts, two channels 200 μm deep were cut on both sides of the bonded interface using a diamond wire saw. The samples were mounted on a transistor holder so as to have the four contacts pointing sideways. A thin dielectric plate was glued on top of the transistor holder before mounting the sample in order to avoid a short-circuit between the contacts. The connection between the holder pins and the sample has been done using silver paste and thin copper wires.

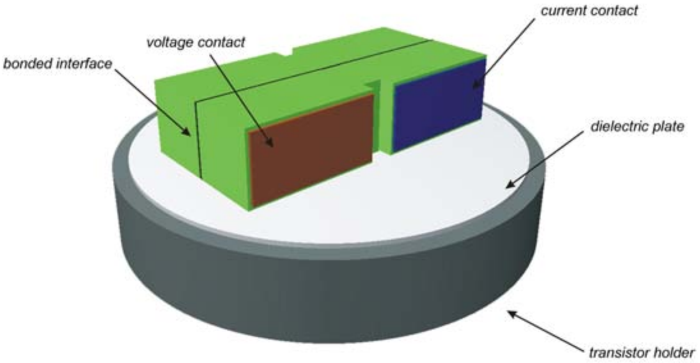

Figure 3.3: Sample configuration for four-point measurements.

Two contacts on each side of the interface were used to carry the current provided by a HP modular DC source. The voltage drop was measured at the other two contacts using a Keithley 2000 multimeter. In this way the effect of the contact resistance was minimized, only the interface being measured.

The transistor holder was mounted inside a copper block belonging to a nitrogen cooled cryostat. Using a computer controlled heating unit, measurements between 77 K and 370 K were possible. Typical voltages ranging from -0.5V to 0.5V were applied during measurements, but higher values were also possible.

In the case of samples prepared by layer transfer, only a two-point probe setup was used for simplicity. The contacting was done using a mask where 0.1 mm diameter holes were cut using a CO_2 laser. The metallization was done according to the method described in Section 3.6.1. The sample mounting was similar to the four-point setup, each contact being used both as a current and voltage probe.

3.6.4. DLTS

Deep level transient spectroscopy (DLTS) was introduced by Lang in 1974 [98] as a novel, highly sensitive method for the study of deep levels in semiconductors. Since then many extensions such as Double-Correlation DLTS (D-DLTS) [99], Constant-Capacitance DLTS (CC-DLTS) [100], Lock-in DLTS [101], Optical DLTS [102] and Laplace DLTS [103] have been introduced. The conventional DLTS technique and the experimental procedure will be discussed here. For an extensive study, the reader should refer to [78], [104] instead.

The principle of DLTS is to perturb the trap occupancy by changing the value of the reverse bias applied to a Schottky diode or p-n junction. The trap concentration N_T and the activation energy of the defect E_A are related to the capacitance variation with time. By varying the filling pulse width, one can also study the capture process.

In order to point out the correspondence between the capacitance transient and the properties of the trap, we recall the equation describing the trap occupancy n_T as a function of time (2.33) as:

$$\frac{\partial n_T}{\partial t} = (c_n n + e_p)(N_T - n_T) - n_T(e_n + c_p p) \tag{3.2}$$

Consider a Schottky diode on an n-type substrate in thermal equilibrium. Assuming an acceptor-like level of density N_T positioned at E_T in the band gap, the dominant process will be the capture of electrons from the conduction band and $n_T \approx N_T$, provided that $n >> p$, $c_n >> c_p$ and $E_T < E_F$.

As soon as the device is biased to a value $-V_R$ electrons will be emitted from traps situated above the Fermi level. Equation (3.2) can be simplified leading to the following solution for n_T:

$$n_T(t) = n_T(0)e^{-e_n t} \approx N_T e^{-e_n t} \tag{3.3}$$

which states that all the trap occupancy follows an exponential decay, going to zero after sufficiently long time. If the device is pulsed between $-V_R$ and a value $-V_P$ ($-V_R < -V_P$), the traps will be filled again with electrons according to:

$$n_T(t) = N_T - [N_T - n_T(0)]e^{-c_n n t_f} \tag{3.4}$$

with t_f being the capture or filling time. For long times, all traps will be filled again with majority carriers as in the initial state. Therefore, by pulsing the device repetitively between $-V_R$ and $-V_P$ one can successively charge/discharge the traps, the magnitude of the charge depending on the total available traps N_T, on their emission/capture probabilities e_n, c_n and on the filling time t_f.

The charge variation associated with the change of the trap occupancy leads to a variation of the device capacitance defined as:

$$C = \frac{dQ}{dV} = \frac{\varepsilon A}{W} \tag{3.5}$$

Q being the fixed charge in the depletion region and W the width of the depletion region. The time-dependent junction capacitance is:

$$C(t) = \sqrt{\frac{\varepsilon A \rho(t)}{2(V_{bi} - V_a)}} = \sqrt{\frac{q\varepsilon A(N_D^+ - n_T(t))}{2(V_{bi} - V_a)}} \tag{3.6}$$

where A is the device area, U is the applied voltage, V_{bi} is the built-in potential, V_a represents the applied bias and $\rho(t)$ is the total charge density inside the depletion region. Relating the capacitance $C(t)$ to the reverse-bias capacitance (at $-V_R$) of the device without deep-levels C_0 we have:

$$C(t) = C_0\sqrt{1-\frac{n_T(t)}{N_D^+}} \approx C_0\left(1-\frac{n_T(t)}{2N_D^+}\right) \tag{3.7}$$

For majority carrier emission from traps the capacitance transient becomes:

$$C(t) = C_0\left(1-\frac{n_T(0)}{2N_D^+}e^{-e_n t}\right) \tag{3.8}$$

Therefore, the capacitance follows an exponential decay with the same time constant $\tau_e=1/e_n$ as the trap occupancy does.

The standard DLTS (also called boxcar DLTS) uses a rate window in which the transient is measured. Following a bias pulse, the transient is measured at times t_1 and t_2. Since the transient is temperature dependent, both the sample temperature and the rate window are varied during the experiment. The variation of $C(t_1)$-$C(t_2)$ with temperature is sampled as shown in Fig. 3.4.

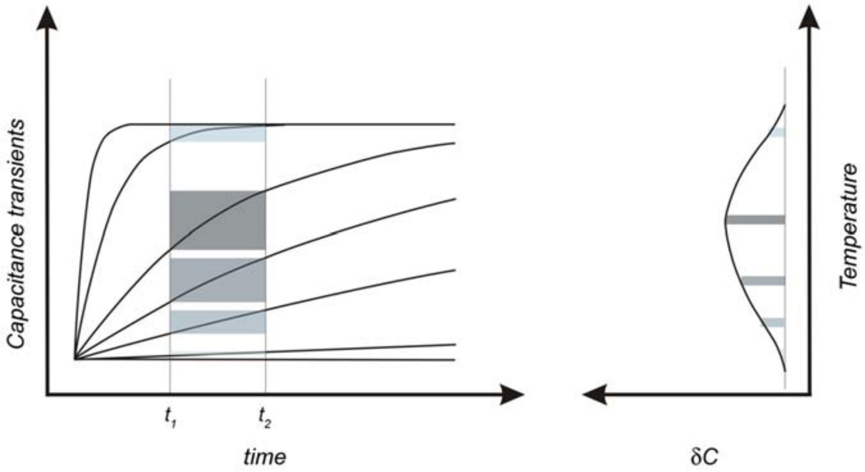

Figure 3.4: Capacitance transients and the corresponding DLTS spectrum.

There is no difference between the capacitance at the two sampling times for very slow or very fast transients, corresponding to low and high temperatures. A difference signal is generated when the time constant τ_e is on the order of (t_2-t_1), and the capacitance difference passes through a maximum giving the DLTS peak. The capacitance difference is expressed as:

$$\delta C = C(t_1)-C(t_2) = \frac{C_0 n_T(0)}{2N_D^+}\left(e^{-\frac{t_2}{\tau_e}} - e^{-\frac{t_1}{\tau_e}}\right) \tag{3.9}$$

In order to determine the value of τ_e for which δC attains a maximum, one has to differentiate δC with respect to τ_e and set the results equal to zero which gives:

$$\tau_{e,\max} = \frac{t_2 - t_1}{\ln\left(\frac{t_2}{t_1}\right)} \tag{3.10}$$

By measuring a series of capacitance transients at different temperatures for a given t_1, t_2 pair, one value of τ_e corresponding to a particular temperature is generated, giving one point on a $ln(\tau_e T^2)$ vs. $1/T$ plot. Repeating the measurement sequence for different t_1 and t_2 a series of points are obtained to generate an Arrhenius plot, which leads to the determination of E_T.

The total trap concentration can be determined from δC setting $t_1=0$ and $t_2=\infty$ in (3.9):

$$N_T = 2N_D^+ \frac{\delta C}{C_0} \tag{3.11}$$

In this work, conventional DLTS measurements were carried out by scanning the temperature between 77 K and 300 K and recording both the capacitance transients and DLTS spectra. The sample preparation and mounting was similar to the procedure described in Section 3.6.1.

The DLTS apparatus at MPI Halle was developed by Dr. O. Breitenstein. The samples were connected to a preamplifier which fed the signal to a C-meter that allows the compensation of the basic capacitance C as well as the conductance G, provided that the capacitance doesn't exceed 500 pF and the resistance is greater than 500 Ω. A sensitivity of 0.5 pF/V was used for all measurements. In the standard operating mode an rf signal (1 MHz) of 100 mV pk-pk (30 mV rms) was applied for the rf capacitance measurement giving a sensitivity of 10^{-4} pF. An additional setting of 1 V pk-pk allowed sensitivities as high as 10^{-5} pF to be attained. The reverse bias and pulse bias could be set between 0 and 15 V.

The capacitance transients were recorded and later processed to calculate the DLTS signal $\delta C=C(t_1)-C(t_2)$ corresponding to eight different rate windows between 1 s^{-1} and 10^4 s^{-1}. Each capacitance transient corresponding to eight values of the filling pulse between 10 μs and 100 ms was recorded, generating an 8x8 matrix of DLTS spectra per measured temperature.

3.7. TEM investigations

The bonded interfaces were examined with the help of transmission electron microscopy (TEM). At MPI Halle two transmission electron microscopes were used: a Philips CM 20 Twin having an accelerating voltage of 200 kV and a high resolution Jeol 4010 with an accelerating voltage of 400 kV. The bonded interfaces were examined in cross-section and in the 25° cut plan-view [105].

For the preparation of the latter, the wafer is sawed in such a way that the bonded interface and the cut form an angle of 25° as depicted in Fig. 3.5. This mode is called plan-view because during the investigation the sample is tilted with 25°, a normal projection of the interface being imaged.

The cross-section samples were prepared by cutting small pieces from the wafer pairs (5x5 mm^2 large) and stabilizing them on 1.5 mm thick silicon pieces. A diamond wire saw was used in order to cut 500 µm thick slices perpendicularly to the interface.

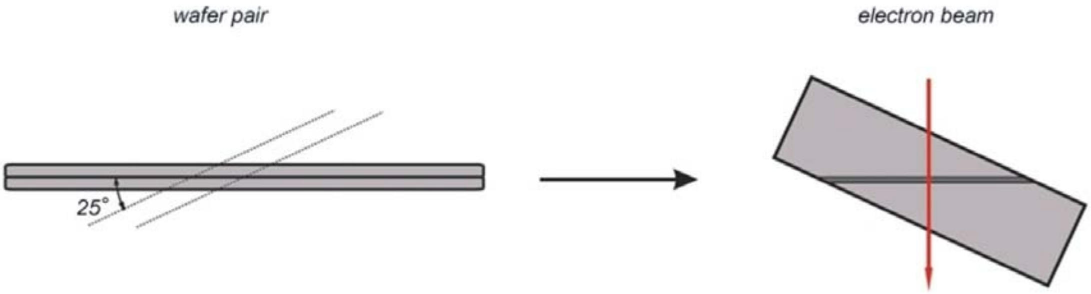

Figure 3.5: Cutting and TEM investigation of a 25° sample.

After gluing with two component epoxy, the slices were bored using a 3 mm ultrasonic drill and underwent polishing/grinding until the thickness reached ca. 10 µm. In the last step, the central part of the sample was further thinned down using a 4 kV PIPS (Precision Ion Polishing System), until a small hole appeared. According to [8], only samples having bonding energies higher than 800 mJ/m^2 can withstand the preparation.

3.8. LEED investigations

In order to study the structure of wafer surfaces at different processing stages, a low-energy electron diffraction (LEED) technique was used [106], [107]. The LEED system consists of three main components: an electron gun, a sample holder and a detector. The electrons were thermally emitted from a LaB_6 cathode (which has a low work function) and were accelerated by a variable voltage to energies between 10 and 200 eV. A system of electrostatic lenses within the gun formed an almost parallel beam which was directed onto the wafer under normal incidence.

The low-energy electrons provided by the electron gun have wavelengths comparable to the atomic spacing on the crystal surface (ca. one Angstrom). Therefore, they may diffract from the surface atoms, i. e. they are elastically back-scattered. Since the cross section for scattering of low-energy electrons is very large, an incident electron beam attenuates within the top few surface layers. These elastically and inelastically scattered electrons propagate in a field-free region between the sample and a transparent metallic grid. Before entering a detector the elastically scattered (i.e. diffracted) electrons have to be separated from the ones that have been inelastically scattered. This is done by a retarding field analyzer which consists of several hemispherical grids. The last grid is followed by a fluorescent screen onto which the diffracted electrons are once again accelerated by a voltage of 5 kV. Beams appear on the screen as fluorescing spots, and the arrangement of beam spots forms the LEED pattern. This pattern caused by diffraction is an image of the surface reciprocal-lattice.

Chapter IV

RESULTS AND DISCUSSIONS

4.1. Silicon-silicon interfaces

The understanding of physical phenomena governing the electrical transport through bonded interfaces is a key step towards further development and device fabrication. Particularly important for providing good quality interfaces is to ensure clean handling and proper surface activation before bonding.

In the following, the results on the electrical properties of Si-Si interfaces obtained by UHV bonding will be presented and discussed. The possibility of combining wafer bonding with implantation induced splitting will be investigated afterwards.

4.1.1. Silicon-silicon interfaces obtained by UHV bonding

As discussed in Chapter II the bonding process causes both a potential barrier and recombination-generation centers at the fused interface. Since the physical transition between the two crystals is embedded in the active area of the junction, it is expected that any process changing the surface properties before bonding will affect the electrical properties of the interfaces.

The wafers underwent various treatments listed in Table 4.1:

Experiment	Hydrogen desorption temperature (°C)	Bonding temperature (°C)	Final treatment
A	500	20	-
B	500	200	-
C	660	200	-
D	660	20	Annealed to 1000°C for 10h

Table 4.1: Wafer treatment before and after bonding.

Although successful surface activation can be achieved upon heating to about 450-500°C, a prolonged heating at elevated temperatures has been found to flatten the surface. The (100)-(2x1):H surface undergoes a clean two-domain (2x1) reconstruction by heating at 500°C (Fig. 4.1a) and remains stable when the temperature is further increased to 660°C (Fig. 4.1b). The sharpening of the diffraction spots indicates a higher degree of ordering of the surface induced by the higher processing temperature. A (111) surface appears almost unreconstructed after heating to 500°C as seen in Fig. 4.1c. Weaker intermediate spots are an evidence of some small domain (7x7) reconstruction, observed more clearly after heating to 660°C (Fig 4.1d) as the intermediate spots get sharper and brighter. Again, the effect is ascribed to a better ordering of the surface.

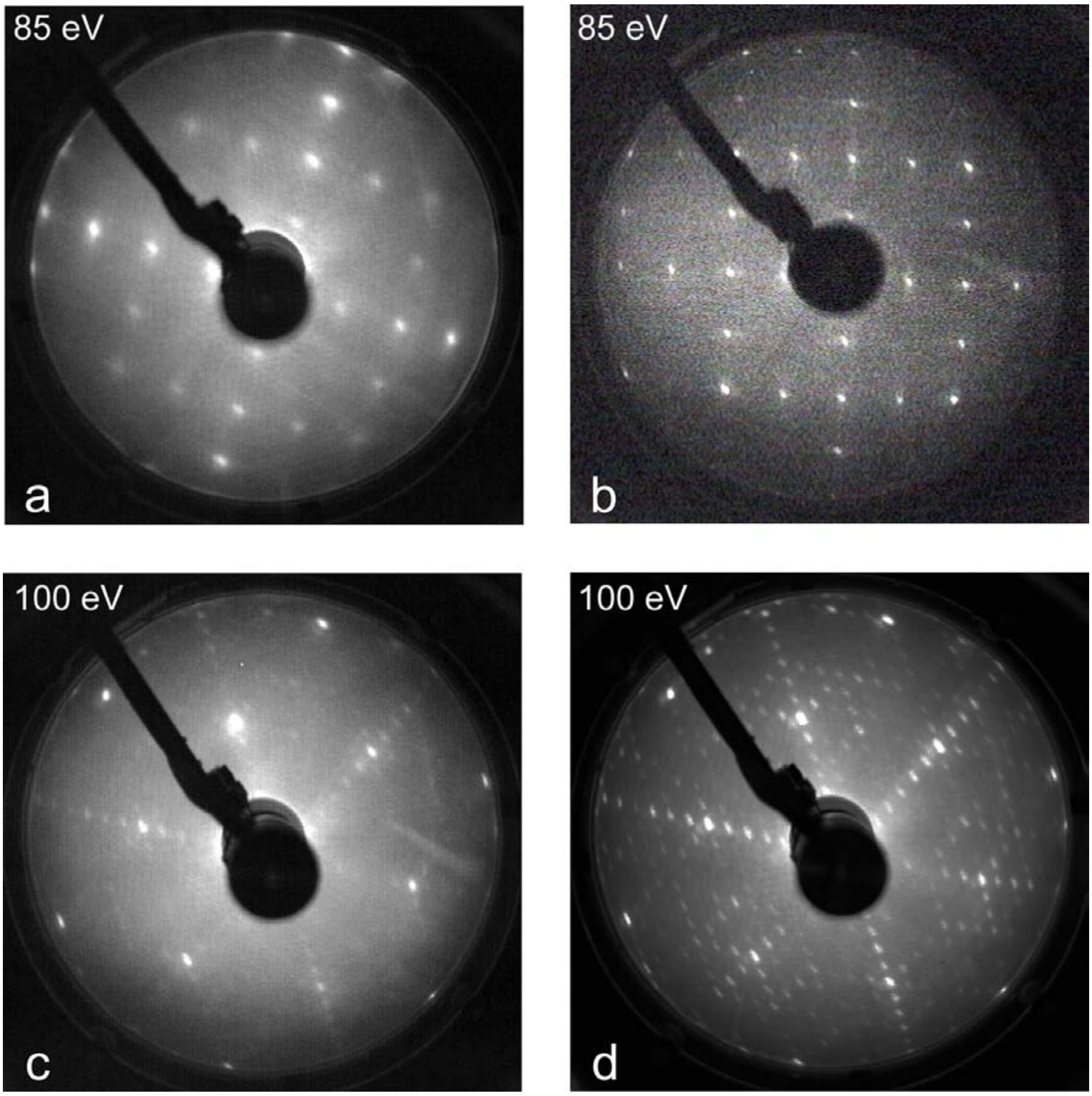

Figure 4.1: LEED images of Si surface reconstruction after heating (see text for details).

4.1.1.1. Electrical characterization of p-p and n-n interfaces

The preparation of isotype homojunctions (n-n or p-p) allows investigating the unipolar current flow across the bonded interfaces. Fig. 4.2 depicts several I-V characteristics measured at 260 K for different p-p homojunctions ($N_A = 10^{15}$ cm^{-3}) prepared according to the conditions listed in Table 4.1. As expected, the current density is relatively low in the case of room temperature bonded samples, as a consequence of the potential barrier that builds up at the interface. The current density increases when bonding is performed at elevated temperatures (200°C, experiment B).

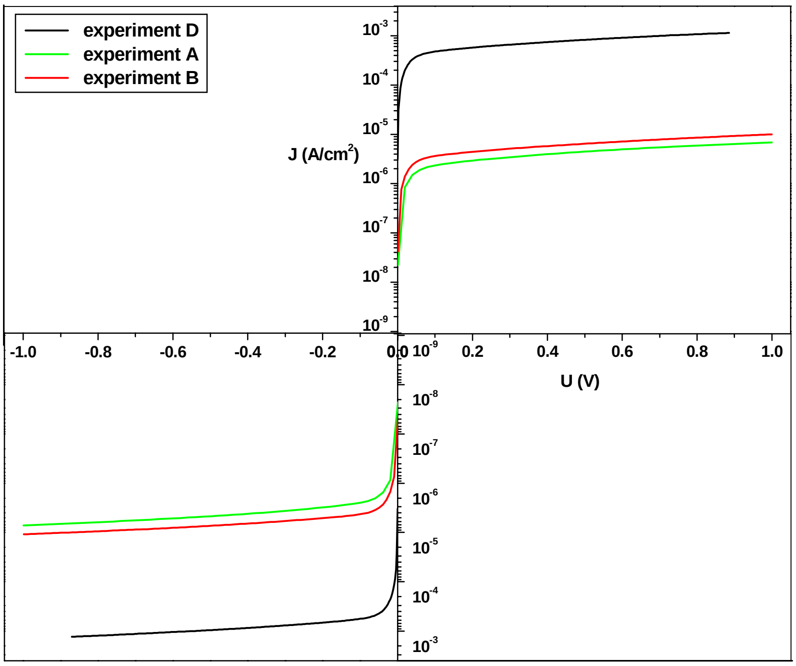

Figure 4.2: I-V characteristics of p-p interfaces (preparation according to Table 4.1).

As discussed in Section 2.1.5 Chapter II, the energy released during bonding is spent in order to rearrange the interface atoms. Provided that the atoms are more mobile (as a consequence of the thermal vibrational energy added by heating), a more efficient rearrangement is possible. Thus, more dangling bonds find partners upon bonding, leading to a decrease of the density of states at the interface.

The most significant improvement of the I-V characteristics occurs upon high temperature annealing (experiment D) due to long-range diffusion of atoms across the bonded interface which tend to arrange in more relaxed configurations.

The equation describing the thermionic emission over the potential barrier derived in Section 2.4.2, Chapter II is:

$$J_{th,p} = A_p^* T^2 e^{-\frac{q(\xi_p+\Phi_B)}{kT}} \left(1 - e^{-\frac{qU}{kT}}\right) \tag{4.1}$$

The subscript “p” denotes a hole current. When small voltages are applied to the bonded interface (less than ± 5 mV) it is possible to relate the current density to the potential barrier that holes need to overcome. Provided that $qU \ll kT$, the following approximation holds:

$$1-e^{-\frac{qU}{kT}} \cong \frac{qU}{kT} \tag{4.2}$$

Using (4.2) and dividing (4.1) by U, the following relation is obtained:

$$\ln\left(\frac{G}{T}\right) = \ln(G_0) - \frac{q(\xi_p + \Phi_B)}{kT} \tag{4.3}$$

where G denotes the conductance and $G_0 = q\mathrm{A}_p^*/k$. A $ln(G/T)$ vs $(1/T)$ plot allows to determine the barrier height without knowing the effective Richardson constant for holes A_p^*.

The slope of the small-signal conductance plot in Fig. 4.3 gives the potential barrier dependence on temperature for different bonded interfaces. One can distinguish a high temperature range for which the potential barrier is almost constant. The lines indicate the data points used to fit the effective barrier height $\Phi_{B,eff} = \xi_p + \Phi_B$ values listed in Table 4.2.

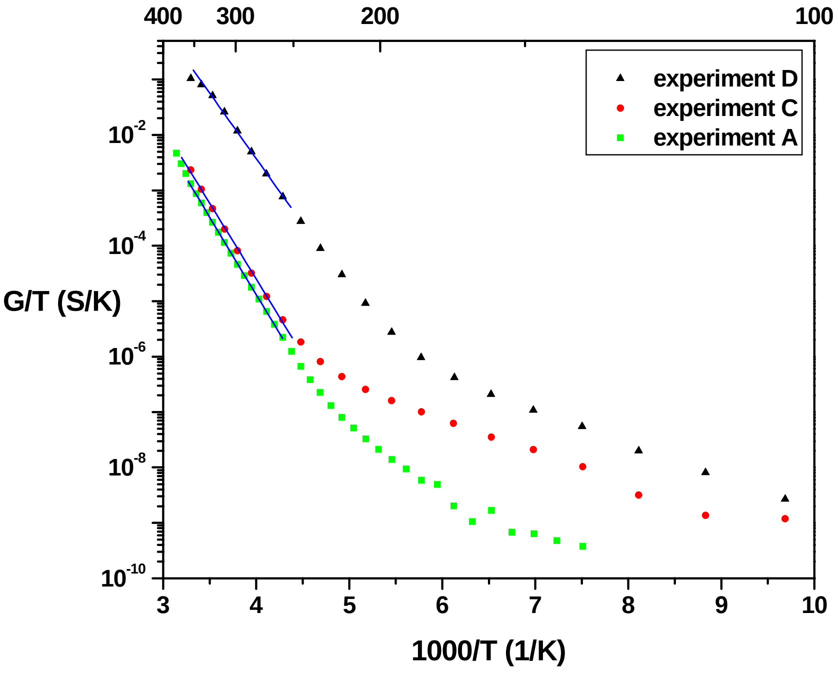

Figure 4.3: Arrhenius plot of the conductance.

When the temperature is lowered the Fermi level approaches the corresponding band edge (valence band in the case of p-doped substrates and conduction band in case of n-doped substrates) leading to a decrease of ξ_p (ξ_n). Consequently, the trap occupancy increases, as described by the grain boundary theory. Additional occupation of interface states increases in turn the barrier height Φ_B, so that the effective barrier height $\Phi_{B,eff}$ remains almost constant over a wide temperature range. The situation is depicted in Fig. 4.4 for a p-p interface (doping $N_A = 2\text{x}10^{15}$ cm^{-3}, experiment A). The effective barrier height was obtained by fitting the *G/T* vs. *1/T* data points (Fig. 4.3) to a straight line. The Fermi level position ξ_p was calculated for different temperatures in order to estimate the actual barrier height Φ_B. The aforementioned algorithm of extracting the barrier height does not account for surface leakage currents. For this reason, the conductance plotted in Fig. 4.3 is not solely given by thermionic emission at low temperatures, since the defective native oxide on the surface creates low resistivity paths through which carriers can readily flow. Therefore the calculated barrier height is an apparent barrier at low temperatures, corresponding to the case when the measured current would be a pure thermionic current.

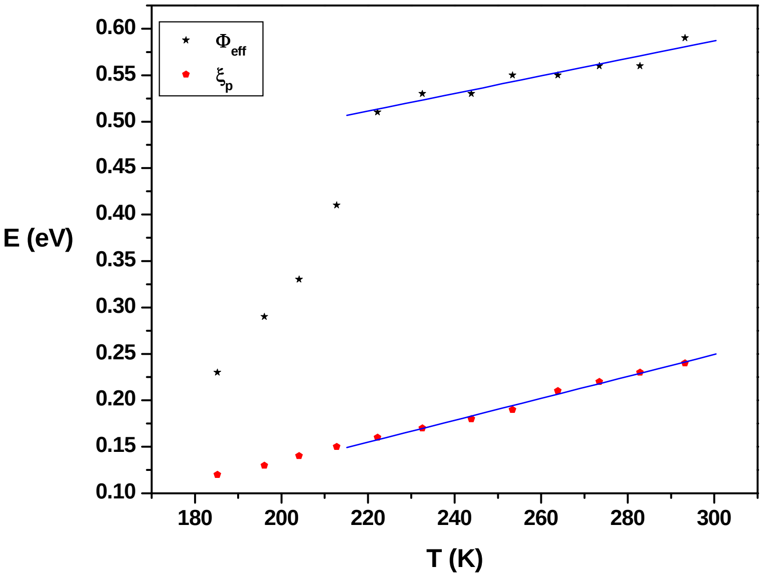

Figure 4.4: Variation of the Fermi level and the effective barrier height for a p-p interface (experiment A).

In order to correlate the barrier heights with the trap density, DLTS measurements were performed according to the procedure described in Section 3.6.4, Chapter III. A bias pulse of 7 V was applied while the interface was repetitively biased with a filling pulse of 10 μs having an amplitude of 14 V. Seven DLTS spectra corresponding to different rate windows were acquired as seen in Fig. 4.5 (experiment C), leading to the determination of several parameters of interest which will be discussed in the following.

The capacitance given by (3.6) cannot be used in the context of bonded interfaces, since it implies a volumic charge density. Moreover, there is no built-in potential associated with a p-p or n-n homojunction, provided that the doping is identical at both sides of the interface. Instead, we relate the initial trap occupancy N_0 to the reverse-bias capacitance C_0 using the relationship:

$$N_0 = \frac{\varepsilon N_A}{C_0} \tag{4.4}$$

This formula will be derived later in the context of p-n junctions.

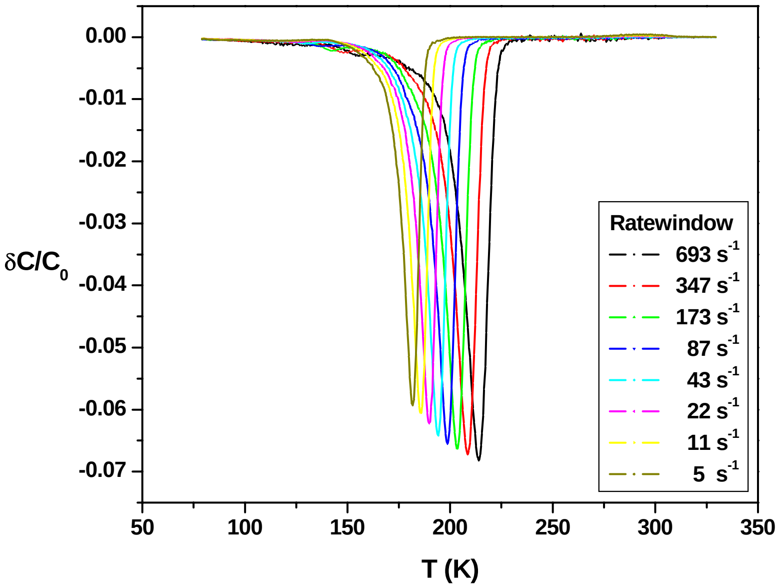

Figure 4.5: DLTS spectra of a p-p bonded interface (experiment C).

The initial trap occupancy N_0 is related to the number of states which remain occupied regardless of the bias regime. The capacitance transient δC (see (3.9)) gives the trap occupancy variation during the DLTS pulse, denoted by ΔN. The calculated values for N_0 and ΔN are listed in Table 4.2 together with the corresponding activation energies E_A.

Experiment	$\Phi_{B,eff}$ (eV)	N_0 (cm^{-2}) x10^{12}		ΔN (cm^{-2}) x10^{10}		E_A (eV)	
		Simulation	DLTS	Simulation	DLTS	Simulation	DLTS
A	0.55	1.6	-	50	-	0.47 (ΔN) 0.61 (N_0)	-
B	0.55	1.5	1.5	10	8.6	0.46 (ΔN) 0.61 (N_0)	0.46
C	0.54	1.2	1.2	5	5	0.47 (ΔN) 0.61 (N_0)	0.47
D	0.47	0.8	-	5	-	0.47 (ΔN) 0.61 (N_0)	-

Table 4.2: Parameters describing the electrical activity of p-p interfaces.

Numerical simulations of the bonded interfaces were performed using the software Wias-Tesca which is based on the drift diffusion model described by (2.33) - (2.36). In each case two levels were assumed in the bandgap, one responsible for the DLTS peak (i. e. the signal given by ΔN) and the other representing the permanently charged level N_0. The position of the first level was chosen to coincide with the activation energy determined with DLTS. The second level lies in the upper half of the bandgap, since it will be shown later that such levels are not chargeable by means of DLTS pulses (in case of a p-p interface). The values of N_0 and ΔN were chosen so as to achieve the best overlapping between simulated and measured current-voltage characteristics (see Fig. 4.2). By adjusting the position of the second level (corresponding to ΔN) it was possible to reach a consistency between the trap densities measured with DLTS and the simulated values.

In order to have a minimum number of free parameters, the activation energies were not changed from one simulation to another. The surface recombination velocities used for calculation were not listed here because of their negligible impact on the simulation output. As an example, different values for the recombination velocity were used to compute the room-temperature current-voltage relationship corresponding to experiment B, by keeping the trap concentration constant and varying the capture cross-sections. As seen in Fig. 4.6, a variation of the recombination velocity of three orders of magnitude results in a change of the current density only by a factor of 5 (at 1 V bias). The measured data was plotted along for reference.

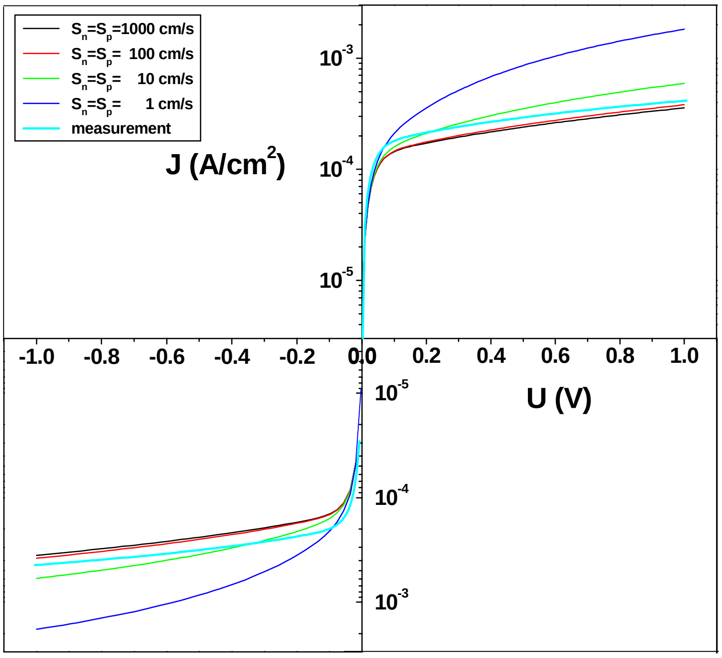

Figure 4.6: Influence of surface recombination velocities on the current-voltage characteristic (experiment B).

This can be explained taking into account the fact that the current is mainly given by thermionic emission, the recombination-generation processes having a smaller influence in the case of unipolar interfaces.

Numerical simulations were useful especially in those cases when a too conductive interface does not allow DLTS investigations to be performed (case D) or when electrically active defects cannot be detected (case A). In order to see when this occurs, we study the case of a grain boundary embedded in a p-p interface (Fig. 4.7) under equilibrium (left) and steady-state (right) conditions. The trap occupancy is given by the position of the Fermi level at the interface. Thus, traps situated in the energetic interval defined by the edge of the conduction band at the interface and the Fermi level will be neutral if acceptor-like or positively charged if donor-like. This interval is denoted by E_0 in Fig. 4.7.

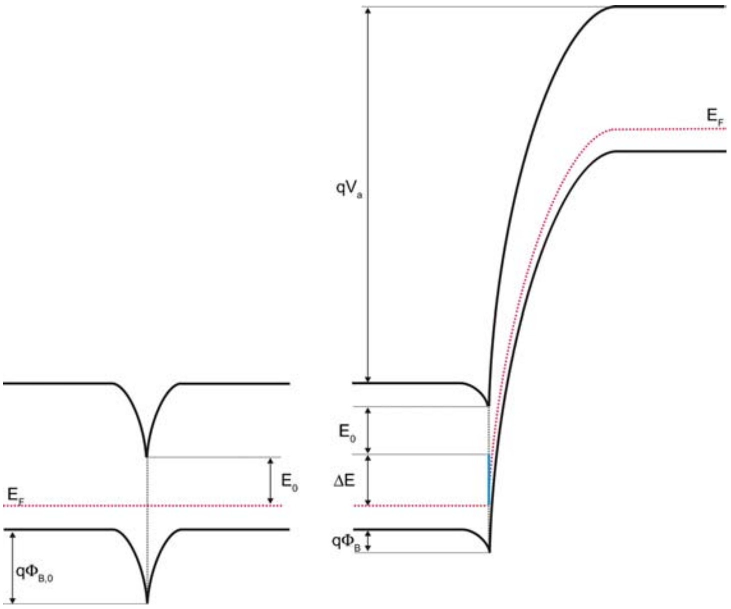

Figure 4.7: A p-p bonded interface in equilibrium (left) and under bias V_a (right).

When the bonded interface is biased, the barrier height decreases causing further occupation of interface states. Provided that the voltage is sufficiently high, all the states are occupied and the barrier eventually collapses. Since the effective barrier height is given by $\xi_p+\Phi_B$ and the quantity ξ_p remains constant, the decrease is done at the expense of Φ_B. Thus the Fermi level approaches the valence band edge at the interface, and carriers are subsequently emitted from traps lying in the interval ΔE marked in blue in Fig. 4.7.

The variation of ΔE with applied voltage was calculated in the case of a p-p junction (experiment C), the result being represented in Fig. 4.8. For low and moderate voltages there is almost no change in the Fermi level position due to the pinning at the interface. For example, only levels lying in an energetic interval of 0.05 eV (roughly $2kT$) can be charged/discharged with a 7 V filling pulse (the maximum value that our system can handle being 15 V). ΔE increases with applied voltage until the flatband condition is satisfied, i. e. when the potential barrier collapses. The jump occurring at 40 V is related to the event when all ΔN levels become occupied. The fact that such high bias values are needed to investigate traps should not be surprising. Broniatowski [108] investigated $\Sigma=25$ grain boundaries in p-type doped silicon bicrystals and found continuously distributed levels in the range (E_v+0.2 eV, E_v+0.6 eV) with densities on the order of 10^{12} cm^{-2} (N_A=8x10^{14} cm^{-3}) . He found that voltages as high as 100 V were required in order to investigate the traps lying in the respective energetic interval.

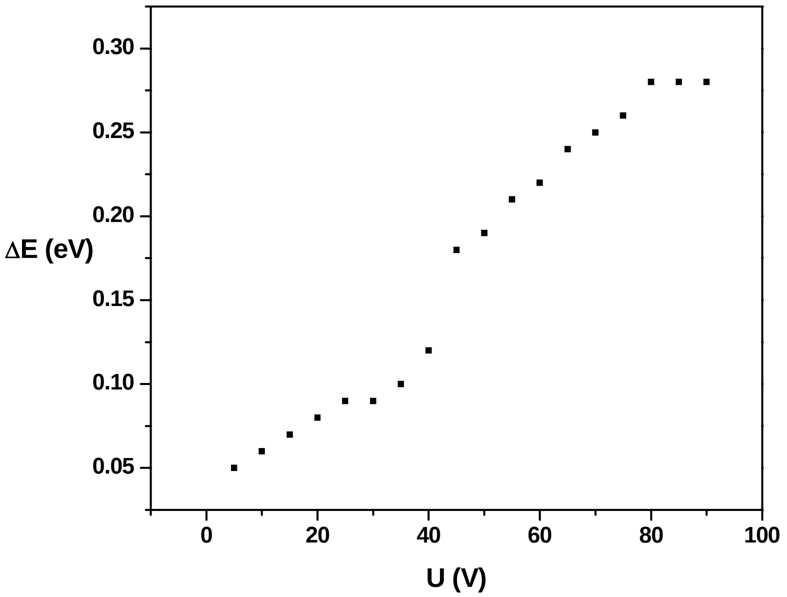

Fig. 4.8: Calculated Fermi level displacement as a function of the applied voltage (see text for details).

There is a good correspondence between the room temperature barrier height, the trap concentration and the interface resistivity. As expected, the initial trap occupancy decreases when bonding is done at elevated temperatures for reasons stated before. The electrical activity of the interface further decreases when one uses higher desorption temperatures, since it was already shown to yield a more ordered surface before bonding. The most significant change of the initial occupancy occurs when high temperature annealing is performed, as observed in earlier investigations [8].

Investigation of bulk (volume) traps with DLTS poses no problems since the depletion width can be varied relatively easily by applying low voltages, while in the case of interface trapped charge much higher biases are required. Even so, only traps in an interval smaller than half of the bandgap yield a DLTS signal. This limitation can be circumvented by producing p-n junctions since in this case the trap occupancy is determined by the position of both quasi-Fermi levels.

4.1.1.2. Electrical characterization of p-n interfaces

P-n junctions were successfully prepared and characterized by means of current voltage measurements. Fig. 4.9 depicts several temperature-dependent I-V curves corresponding to a p-n junction obtained by bonding (100) (left) and (111) (right) oriented wafers. The rectifying factor (defined as the ratio between the forward and the reverse current at a certain voltage) is remarkably good at low temperatures (10^5) and decreases to 10^3 at room temperature, as a result of the generation mechanisms which contribute to the reverse-bias current. The ideality factor is about 1.3 at 210 K and exhibits different behaviour for the two cases: increase with temperature for the (111) bonded interface and remains fairly constant for the (100) interface. The upward bending of the forward bias characteristic is an effect of the sample geometry. The four-point probe represented in Fig. 3.3 relies on the assumption that the interface resistance is much higher than the semiconductor bulk resistance, which is obviously not valid in forward regime. Above a certain bias, the apparent voltage drop across the junction is smaller than the real one, causing the current overshot observed in Fig. 4.9.

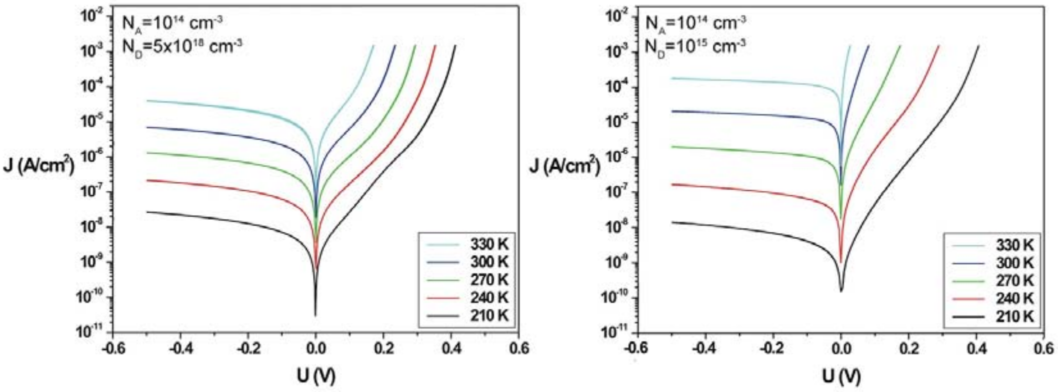

Figure 4.9: I-V characteristics of a (100) (left) and a (111) (right) p-n Si-Si junction.

In order to evaluate the electrical activity of the interfaces, DLTS investigations were performed as well. First, one has to relate the reverse-bias capacitance to the initial trap occupancy N_0 and the capacitance transient to the trap filling variation ΔN. As discussed in the previous paragraph, (3.6) needs to be changed to account for interface trapped charge and doping profile change at the interface.

The analysis of the space-charge region of a p-n junction proceeds in a similar manner to that given in textbooks [58], [75], the only difference being the boundary conditions imposed on the system. A continuous electrostatic potential is assumed at the interface:

$$\psi_p(0) = \psi_n(0) \tag{4.5}$$

The subscripts “n” and “p” denote the potential in the respective regions.

Due to the presence of charged traps, the electric flux density is no longer a continuous function:

$$\varepsilon \frac{d\psi_p(0)}{dx} \pm qN_S = \varepsilon \frac{d\psi_n(0)}{dx} \tag{4.6}$$

N_S being the interface trap density which will be assumed acceptor-like (the derivation in the case of donor-like traps is similar). The electric field at the edges of the depletion region is zero:

$$\frac{d\psi_p(-x_p)}{dx} = \frac{d\psi_n(x_n)}{dx} = 0 \tag{4.7}$$

where x_n and x_p denote the depletion width of the n and p regions, respectively. Under the full depletion assumption, the Poisson equation (2.36) becomes:

$$\begin{cases} \dfrac{d^2\psi_p(x)}{dx^2} = \dfrac{q}{\varepsilon} N_A \\ \dfrac{d^2\psi_n(x)}{dx^2} = -\dfrac{q}{\varepsilon} N_D \end{cases} \tag{4.8}$$

Integrating (4.8) once and using the boundary condition (4.7), one finds the electric field:

$$\begin{cases} \dfrac{d\psi_p(x)}{dx} = \dfrac{q}{\varepsilon} N_A\left(x_p + x\right) \\ \dfrac{d\psi_n(x)}{dx} = \dfrac{q}{\varepsilon} N_D\left(x_n - x\right) \end{cases} \tag{4.9}$$

Evaluating the electric fields at the interface (x=0) with boundary condition (4.6) we obtain:

$$N_A x_p + N_S = N_D x_n \tag{4.10}$$

This indicates that the net positive charge in the n side balances the net negative charge in the p side and the negative interface charge N_S. Setting the potential zero at the edge of the depletion region in the p side, (4.9) can be integrated again to obtain:

$$\begin{cases} \psi_p(x) = \dfrac{qN_A}{2\varepsilon}\left(x_p + x\right)^2 \\ \psi_n(x) = (V_{bi} - V_a) - \dfrac{qN_D}{2\varepsilon}\left(x_n - x\right)^2 \end{cases} \tag{4.11}$$

where V_a is the applied voltage and V_{bi} is the built-in potential of the p-n junction expressed as:

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{4.12}$$

n_i being the intrinsic concentration. Using (4.10) and (4.11) x_n and x_p can be determined. The net positive charge per unit area equals the net negative charge:

$$Q = qN_D x_n = -q\left(N_A x_p + N_S\right) \tag{4.13}$$

Taking the derivative of this charge with respect to the voltage allows one to obtain the capacitance per unit area of a p-n junction with interface traps:

$$C = \frac{dQ}{dV} = qN_D \frac{d}{dV_a}\left(x_n\right) = \varepsilon\sqrt{\frac{qN_A N_D}{2\varepsilon\left(N_A + N_D\right)\left(V_{bi} - V_a\right) - qN_S^2}} \tag{4.12}$$

Setting $N_S=0$ we arrive to the well-known capacitance formula of an ideal p-n junction. The presence of interface traps decreases the depletion width and increases the capacitance per unit area. By formally substituting N_D with $-N_A$ in (4.12) one obtains (4.4) used earlier in the context of p-p interfaces. Using (4.12) it is possible to calculate N_0 and ΔN from the DLTS peak. These values are given in Table 4.3 for (100) and (111) junctions.

Surface orientation	N_0 (cm^{-2}) x10^{11}	ΔN (cm^{-2}) x10^{11}	E_A (eV)	$S_{n,p}$ (cm/s)
(100)	69	0.46	0.18	S_n=190, S_p=180
(111)	0.55	1.1	0.51	S_n=S_p=360

Table 4.3: Parameters describing the electrical activity of p-n interfaces.

The initial trap occupancy N_0 is not negligible, indicating that also in the case of p-n junctions there are occupied states in reverse-bias. During the filling pulse a small number of states contribute to the DLTS peak, since the occupation probability decreases in the case of bipolar current flow according to (2.25). Thus, the DLTS peak gives only the net charge variation which is not necessarily proportional to the total number of states in the bandgap. Provided that an equal amount of donor and acceptor-like states with similar capture cross-sections would exist in the forbidden gap, they yield very small or no net charge variation during the filling pulse, which doesn't mean that no interface traps are present. For this reason the electrical activity of the interface cannot be unambiguously evaluated using a single investigation method. The surface recombination velocities used for calculations indicate a stronger recombination at the (111) surface.

In summary, both isotype and anisotype interfaces prepared by UHV bonding exhibit a relatively high concentration of defects at the bonding interface. The electrical transport can be controlled by a proper choice of surface orientation, doping profiles and processing steps before and after bonding.

4.1.2. Layer transfer of silicon layers onto silicon substrates

The possibility to combine UHV bonding with layer splitting would be an attractive choice for materials integration. New structures obtained by this approach would benefit from the advantages of wafer bonding and the flexibility offered by ion cutting in terms of doping, orientation and thickness of the transferred layers.

The following section focuses on the results obtained when transferring ultra-thin silicon layers onto silicon substrates.

4.1.2.1. Surface activation by UV photothermal desorption

Since the surface activation in case of implanted surfaces cannot be done by standard thermal desorption, the hydrogen removal from surfaces was accomplished with KrF laser pulses as described in Section 3.3.2, Chapter III.

The dependence of the bonding quality on the irradiation parameters was studied for both implanted and non-implanted H-terminated silicon wafers. During each experiment, the wafers underwent different treatments listed in Table 4.4. The time needed for a line-scan was about one minute in each case. Laser irradiation was followed by bonding to standard silicon wafers activated according to the standard procedure described in Section 3.3.2, Chapter III.

For reference, a H-terminated wafer was bonded to an ‘unpassivated wafer’ (experiment A).

Experiment	Estimated laser fluence (mJ/cm^2)	Maximum surface temperature (°C)	Bonding energy (mJ/m^2)
A	-	RT	150-200
B	60-150	260	150-300
C	200	340	300-700
D	600	980	1000-1300
E	700	1140	≈1500
F	800	1300	>2000
G	900	>1400	<1000
H	1500	>1440 (melting point)	-

Table 4.4: Conditions for photodesorption experiments.

For small laser fluences, the cleaning effect is negligible. Local increase of the bonding energy is possible due to release of weakly chemisorbed molecules present on the surface, such as water and residual contaminants. The surface undergoes a clear (1x1) reconstruction specific to the di-hydride configuration, with each DB of the surface atoms passivated by a hydrogen atom (Fig. 4.10).

With increasing laser fluence, the surface temperature increases accordingly and H starts leaving the surface. Free neighbouring dangling bonds form dimers (mono-hydride configuration) in order to minimize the surface energy, while most of the surface preserves the initial di-hydride configuration. Upon bonding, the few free bonds may find partners and bond covalently at room temperature increasing locally the fracture strength.

At 600 mJ/cm^2, rows of dimers already form on the surface as a result of increasing H desorption. The LEED pattern in Fig. 4.10 (right) has the signature of a (2x1) two-domain reconstruction, which is characteristic for (100) silicon. However, the bonding energy is still below the fracture strength of silicon, indicating that a mono-hydride (2x1) reconstruction together with a clean (2x1) reconstruction is responsible for the observed pattern. As soon as the surfaces approach each other, dimers become unstable and the reconstruction is readily broken leading to covalent bonding by means of the ‘adhesive avalanche’ mechanism discussed in Section 2.1.5, Chapter II. Thus, bonding energies of 1000 mJ/m^2 and higher can be reached, due to the higher number of covalent bonds per unit area. Some hydrogen atoms might still be present at the interface, hindering further formation of covalent bonds. When the laser fluence was increased again (experiment E), the surface temperature rise above 1100°C, and more H atoms desorbed from mono-hydride sites.

The highest bonding energy (>2000 mJ/m^2, determined by fracture tests) was achieved for fluences of about 800 mJ/cm^2. Since the estimated surface temperature is close to the melting point of silicon, it is expected that the beam has a flattening effect, which contributes to the increased bonding energy. Above this fluence, no notable increase of the bonding energy was observed. Instead, the bonding energy decreased abruptly due to the surface deterioration by local melting of silicon. Eventually, the ablation threshold is exceeded and atoms are massively removed from the surface, as confirmed by the crater-like features observed after irradiation.

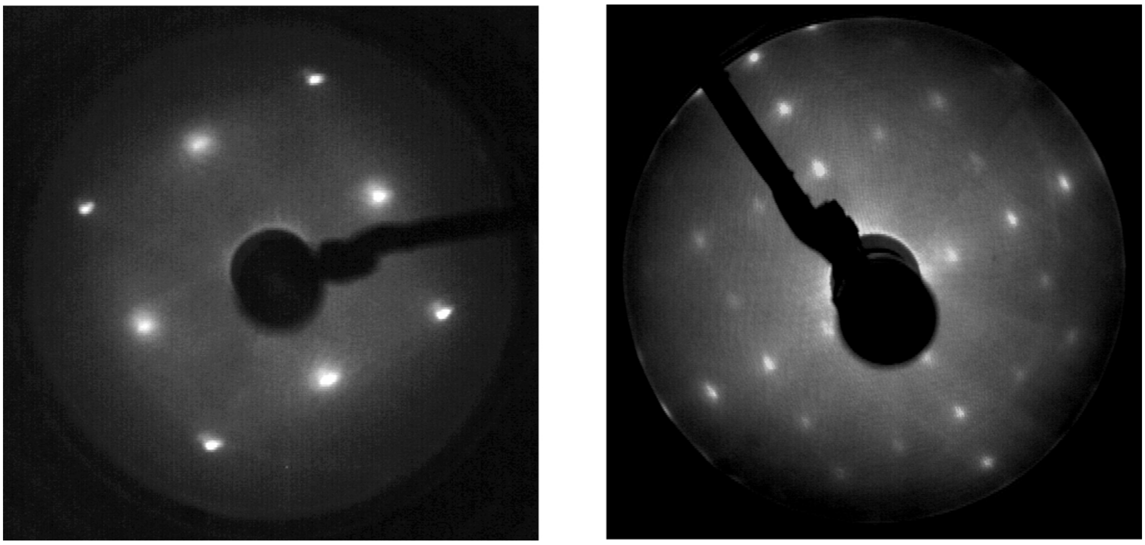

Figure 4.10: LEED image of a Si(100) surface after 150 mJ/cm^2 laser irradiation (left, electron energy 60 eV) and 600 mJ/cm^2 irradiation (right, electron energy 85 eV).

Although standard silicon wafers could be irradiated using fluences as high as 800 mJ/cm^2 in order to achieve high bonding energies, in the case of implanted wafers the blistering onset was observed around 700 mJ/cm^2. Therefore, the present experiments were limited to fluences of 600-650 mJ/cm^2 (a safety interval was ensured).

The temperatures listed in Table 4.4 were not actually measured, since it was impossible to monitor accurately such rapid temperature transients in the conditions imposed by the experiments. A theoretical estimation of the temperature profile within the wafer during (and after) the laser pulse was necessary since the onset of the blistering process should be avoided before bonding. Moreover, the wafer might have embedded structures that would be affected by prolonged heating at elevated temperatures. The temperature profile was obtained by solving the time-dependent partial differential equation describing the heat propagation within an isotropic solid [109]. In order to decrease the calculation time, a quasi-one-dimensional case was assumed since the wafer is almost a semi-infinite plane:

$$\rho c \frac{\partial T(x,t)}{\partial t} = \frac{\partial}{\partial x}\left(k \frac{\partial T(x,t)}{\partial x} \right) + Q(x,t) \tag{4.13}$$

The parameters ρ, c and k represent the density, the specific heat and the thermal conductivity of the material, respectively. The term $Q(x,t)$ contains all heat sources and sinks.

Once the laser beam impinges on the surface, it interacts with both surface and bulk atoms. A direct Si-H photochemical bond breaking is not possible since an electron would require at least 6-6.5 eV to be promoted from the Si-H σ bonding orbital to the unoccupied σ^* antibonding orbital, as demonstrated by electron-field emission from a scanning tunneling microscope (STM) tip for Si(111)-(1x1):H [110] and Si(100)-(2x1):H [111] surfaces. Moreover, theoretical calculations [112] and photochemical vs. photothermal desorption experiments done with F_2 (7.9 eV) and XeCl (4.0 eV) lasers [113] confirmed these findings. Since the incident photon energy is below the threshold of photochemical desorption, the hydrogen is removed by thermal excitation of Si-H bonds. That is, photons interact with the lattice producing direct optical excitations of electrons from filled states in the valence band to empty states in the conduction band. These hot electrons collide with the lattice atoms transferring energy to the phonons which increase the temperature and excite vibrationally the Si-H bonds. Plasma effects are negligible for the energy ranges used [114].

4.1.2.2. Modelling the laser source

The effect of the laser beam can be separated into a coordinate dependent term (related to the absorption length in the material) and a time dependent term (related to the pulse profile) [115], [116] in the following manner:

$$Q(x,t) = (1-R)I(t)\alpha e^{-x\alpha} \tag{4.14}$$

R is the reflectivity, $I(t)$ is the time-dependent laser intensity and α is the absorption coefficient in silicon.

The electromagnetic wave impinging on the wafer surface can be written as a linear combination of two waves, one with the electric vector polarized parallel to the plane of incidence (p-polarized), and one with the electric vector perpendicular to the plane of incidence (s-polarized) [117]. Since the polarization of the laser beam was not known, both reflectivities (corresponding to s and p waves) were calculated and an averaged value was used during the simulations. These reflectivities are:

$$R_{p,s} = \tilde{r}_{p,s}\tilde{r}^{*}_{p,s} \tag{4.15}$$

where $\tilde{r}_{p,s}$ and $\tilde{r}^{*}_{p,s}$ denote the complex Fresnel coefficients and their conjugates, respectively. In the general case of two dispersive media we have:

$$\begin{aligned} \tilde{r}_p &= \frac{\tilde{n}_1\cos\phi_0 - \tilde{n}_0\cos\tilde{\phi}_1}{\tilde{n}_1\cos\phi_0 + \tilde{n}_0\cos\tilde{\phi}_1} \\ \tilde{r}_s &= \frac{\tilde{n}_0\cos\phi_0 - \tilde{n}_1\cos\tilde{\phi}_1}{\tilde{n}_1\cos\phi_0 + \tilde{n}_1\cos\tilde{\phi}_1} \end{aligned} \tag{4.16}$$

The subscripts “0” and “1” denote the first (vacuum) and the second (silicon) medium of propagation, respectively. The evaluation of the Fresnel coefficients requires the refraction (transmission) angle $\tilde{\phi}_1$ and the complex refractive index $\tilde{n}$ to be known. The latter is given by:

$$\tilde{n}_{0,1}(\lambda) = n_{0,1}(\lambda) - ik_{0,1}(\lambda) \tag{4.17}$$

which contains a real part denoting propagation (given by the real refractive index *n*) and a complex part denoting losses (given by the extinction coefficient *k*). Both *n* and *k* are wavelength dependent parameters, except for the vacuum ($n = 1$, $k = 0$). Silicon has $n = 1.68$ and $k = 3.58$ for a 248 nm wavelength [118]. The extinction coefficient is related to the absorption coefficient by:

$$k(\lambda) = \frac{\lambda}{4\pi}\alpha(\lambda) \tag{4.18}$$

The refractive angle is related to the incidence angle via Snell’s law:

$$\tilde{n}_1\sin\tilde{\phi}_1 = \tilde{n}_0\sin\phi_0 \tag{4.19}$$

The calculated reflectivities for a wavelength of 248 nm and an incident angle of 45° were 0.56 and 0.75 for the p and s waves, respectively. In consequence, most of the beam will be reflected by the mirror-like surface of the wafer.

The time-dependent laser intensity was modelled using a piecewise function:

$$I(t) = \begin{cases} I_0\left(1 - e^{-\tau t}\right) & , t \le t_p \\ I_0 e^{-\tau\left(t - t_p\right)} & , otherwise \end{cases} \tag{4.20}$$

where I_0 is the maximum intensity (read at the front display panel of the apparatus in units of mJ/puls), τ is the time constant describing the intensity variation and t_p is the pulse width (20 ns). Once R, $I(t)$ and α were known, the source term $Q(x,t)$ in (4.13) was determined and plotted in Fig. 4.11. As can be seen, the penetration depth of the corresponding UV light is about 30 nm. The heat source quenches exponentially as the laser pulse ceases. Considering the thermal conductivity to be uniform in the material, (4.13) becomes:

$$\frac{\partial T(x,t)}{\partial t} = \frac{k}{\rho c}\frac{\partial^2 T(x,t)}{\partial x^2} + Q(x,t) \tag{4.21}$$

The following boundary conditions were used for numerical calculations:

$$\begin{aligned} &T(x,0) = T_0 \\ &T(w,t) = T_0 \\ &k\frac{\partial T(0,t)}{\partial x} = \sigma\varepsilon\left[T(0,t)^4 - T_0^4\right] \end{aligned} \tag{4.22}$$

which means:

- The wafer temperature is that of the surrounding environment (T_0) at the beginning of the laser pulse.
- At a depth corresponding to the wafer thickness w the temperature remains constant at $T_0 = 20°C$.
- There is a temperature gradient variation with time at the front surface as long as $T_{surface} > 20°C$.

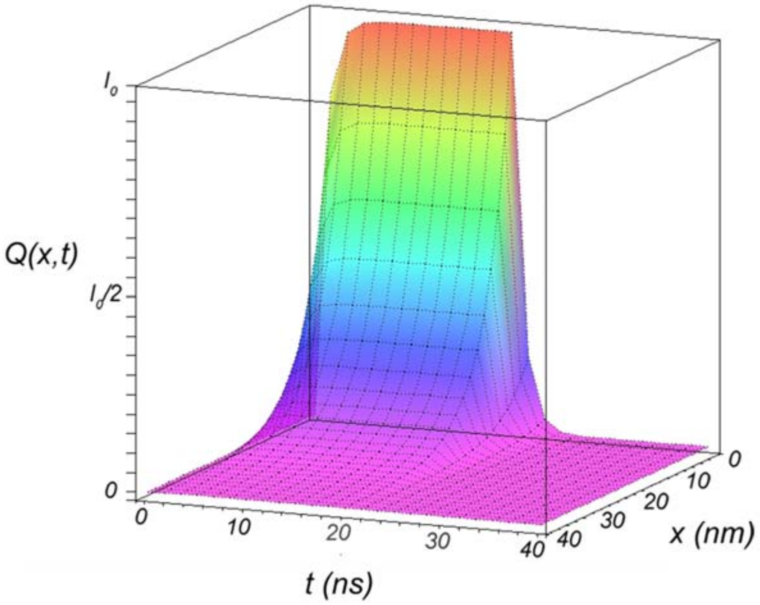

Figure 4.11: The heat source profile.

The solution of (4.13) is represented in Fig. 4.12 for a depth of 0-0.5 µm and a time range of 0-100 ns. As one can observe, at 0.5 µm below the surface (i. e. the implantation peak for most of our experiments) the temperature peaks after 20 ns reaching a value of 700°C (surface temperature was 980°C) and decreases to 250°C in 80 ns. Thus, the hydrogen is desorbed from the surface without blistering onset.

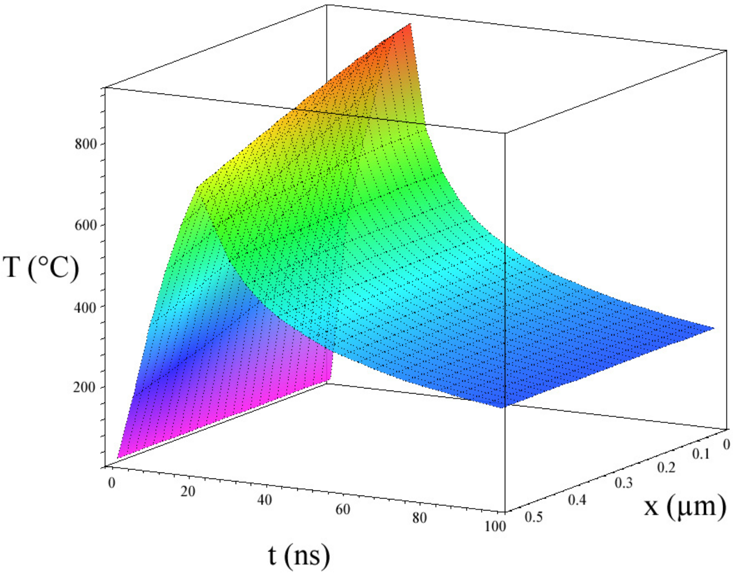

Figure 4.12: Heat flow inside the wafer.

4.1.2.3. Splitting

After RT bonding, the wafer pairs were annealed in order to achieve splitting. The annealing parameters were chosen according to the implantation parameters listed in Table 3.1, Chapter III. Once the splitting time corresponding to a certain temperature was reached, the transfer occurred instantaneously over large areas.

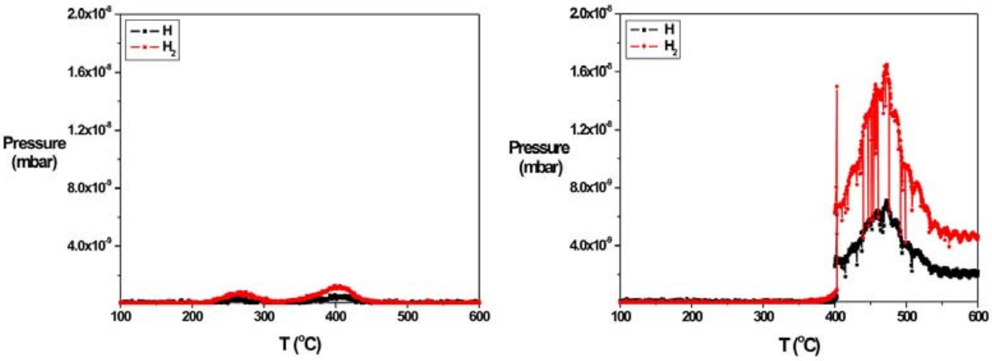

Figure 4.13: Quadrupol mass spectra of the hydrogen during standard thermal desorption (left) and layer splitting (right). A temperature ramp of 8 K/min was used.

Fig. 4.13 depicts the hydrogen release in the moment of splitting in comparison to the case of standard thermal desorption. One can see that the hydrogen released from the microcracks during splitting creates a much higher partial pressure than that produced during thermal desorption. The spike confirms the rapid release of gas in the splitting process.

4.1.2.4. Morphology of the transferred layer

Successful transfer of (100) and (111) Si layers having thicknesses between 0.2 and 0.6 μm was achieved (see Table 3.1, Chapter III) up to a percentage of more than 90% of the wafer area. The left image in Fig. 4.14 depicts only a few bubbles in an otherwise perfect layer. The Nomarsky mode micrograph on the right features the transition between a transferred and a non-transferred area at the rim of a bubble. The layer thickness was 0.5 μm in this case.

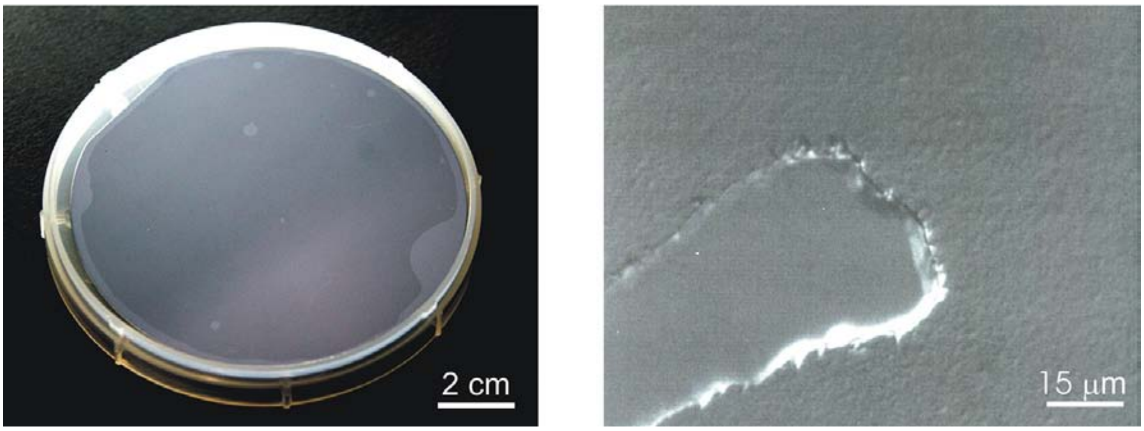

Figure 4.14: Image of the transferred layer over the whole wafer area (left) and detailed Nomarsky mode micrograph featuring a non-transferred area in the lower left part (right).

The roughness of the transferred layer was measured before and after annealing to 1000°C for 5 hours as seen in Fig. 4.15. AFM topographic images revealed a decrease of the mean roughness from 4.8 to 1.6 nm upon annealing in accordance with earlier findings [119] .

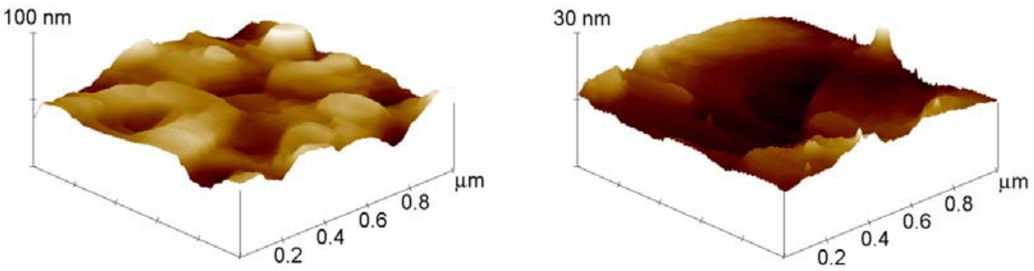

Figure 4.15: AFM morphology of the transferred layer before (left) and after (right) annealing.

In order to study the distribution of implantation generated defects in the transferred layer, TEM investigations were performed for as-transferred and annealed samples (Fig. 4.16). Towards the end of the implantation region one can see remaining platelets having the appearance of white stripes parallel to the bonded interface. During the post-bonding annealing (400 °C for 10 min) they grow without causing splitting due to the insufficient gas pressure contained inside them.

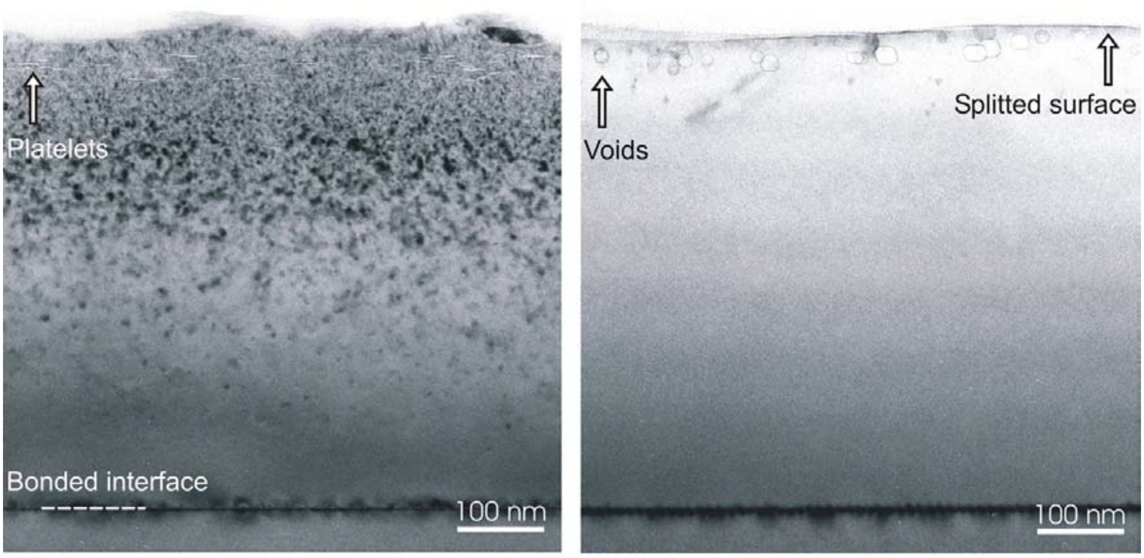

Figure 4.16: XTEM image of the as-transferred (left) and annealed (right) layer (H_2^+ implantation, dose 5x10^{16} cm^{-2}, energy 130 keV).

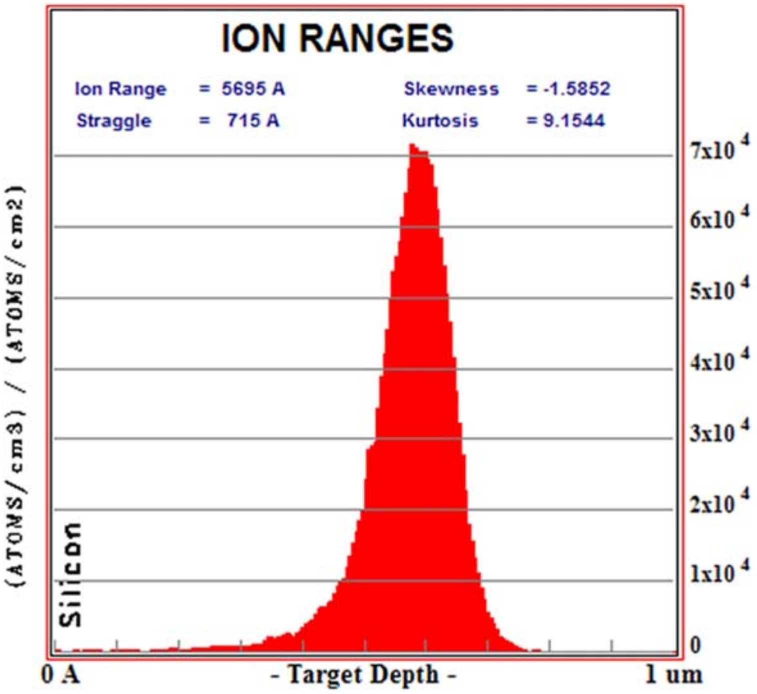

Figure 4.17: Calculated ion ranges and straggle of H_2^+ (130 keV) in Si.

The defects surviving the post-bonding annealing consist of point defect agglomerates and have a dark contrast (Fig. 4.16, left). Their distribution is related to the broadening of the implantation peak.

SRIM calculations of hydrogen ranges in silicon (Fig. 4.17) show the high range/straggle ratio of hydrogen in silicon, allowing ultra-thin layers to be transferred. An annealing step at 1000°C for 5 hours in H_2 atmosphere removed all the damage in the transferred layer, except for some faceted voids near the end of the implanted region originating in the platelets observed in the as-transferred layer (Fig. 4.16, right).

4.1.2.5. Structural investigations

As discussed in the previous section, the bonding strength after laser desorption and bonding was influenced to a high degree by the beam fluence. When using low fluences (e. g. 200 mJ/cm^2) the transfer was still possible, but the interface featured voids and gas bubbles upon annealing similar to the case of hydrophobic bonding [23]. Fig. 4.18 depicts a TEM cross-section image of a 170 nm transferred layer after RT bonding and 600°C annealing in order to achieve splitting. It should be noted that a higher annealing temperature was necessary in order to achieve splitting, because of the very low implantation dose used in this case (1.8x10^{16} cm^2).

By tilting the sample about 20° with respect to the edge-on position, two types of voids can be envisioned: larger voids near the end of the implantation region, having the same origin as those observed in Fig. 4.16 and smaller voids at the bonded interface. They contain hydrogen remaining on the surface after insufficient laser cleaning. Due to the small ion range it is also possible that some hydrogen diffusing out of the platelets migrates to the bonding interface during annealing accumulating there.

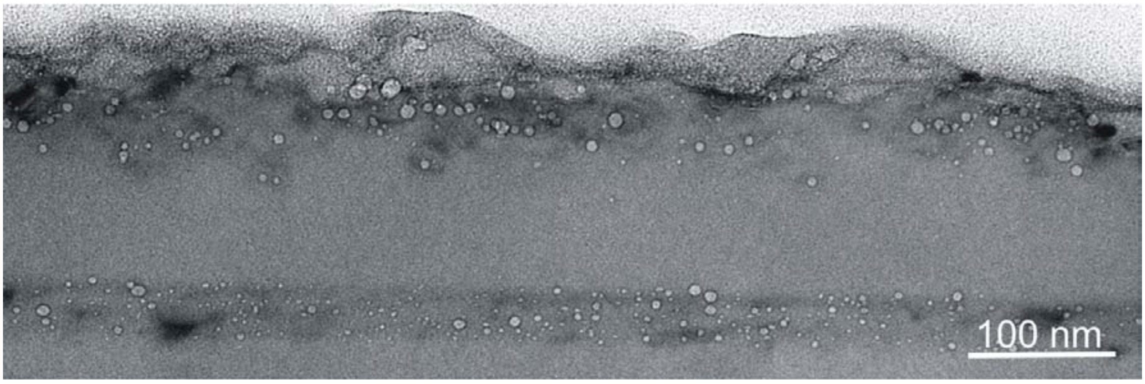

Figure 4.18: XTEM 20° tilt view of a bonded interface featuring voids.

For higher fluences (≈ 600 mJ/cm^2) voids were not observed neither in cross-section nor plan-view. There is, however, the possibility that voids having a size below the detection limit still exist at the bonded interface. High-resolution cross-section TEM images in Fig. 4.19 and 4.20 confirm that covalent bonding is achieved without the involvement of any intermediate layer for both (100) and (111) bonded interfaces.

In Fig. 4.19 two sets of (111) atomic planes can be observed, crossing the interface at an angle of 54.7° without any interruption. The bright spots with a periodicity of about 5 nm are given by the strain fields of the screw dislocation network which is directly observable in a plan-view image (Fig. 4.21). In the case of the (111) interface (Fig. 4.20), there is an overlapping effect of the lattice planes related to the large miscut of the bonded wafers (2.5-3°). Two sets of atomic planes are again observed: (111) planes parallel to the interface and $(\bar{1}11)$ planes inclined 70.5° with respect to the first set. Again, there is no evidence of an intermediate layer.

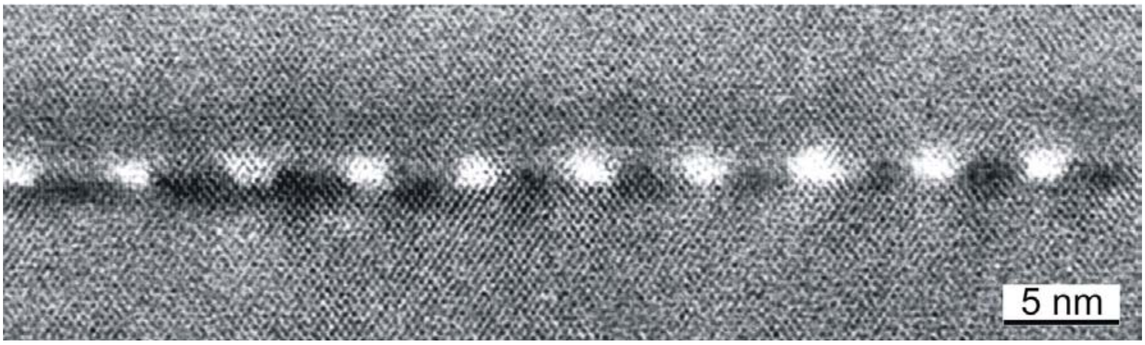

Figure 4.19: HRXTEM micrograph of a transferred (100) layer on a (100) substrate (viewing direction [110]).

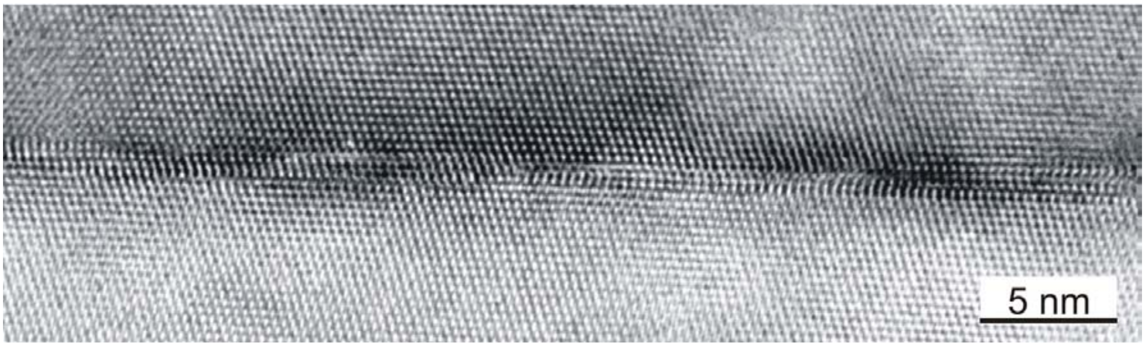

Figure 4.20: HRXTEM micrograph of a transferred (111) layer on a (111) substrate (viewing direction [110]).

As discussed in Section 2.3.3, Chapter II, the misorientation of a (100) twist boundary in fcc lattices is accommodated by a square network of screw dislocations having Burgers vectors ½$[110]$ and ½$[1\bar{1}0]$. The plan-view investigations (Fig. 4.21) showed that an almost perfect screw dislocation network establishes after heating at only 400°C (the temperature necessary for splitting in that case). Only very few closed defect circuits can be observed, originating in the interaction of some 60° dislocations accommodating a small tilt with the network of screw dislocations. Short interruptions of the dislocation lines are also observed, indicating that the interface might not be completely relaxed, since no further annealing was performed to this sample. A dislocation distance of 5 nm was found (correlated to the periodic strain observed in the cross-section image), corresponding to a twist angle of 4.4° between the bonded wafers.

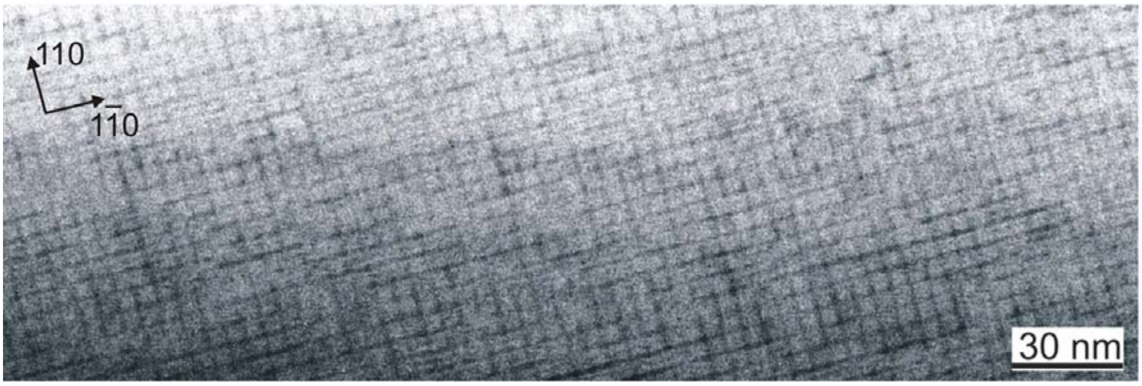

Figure 4.21: TEM plan-view image of a bonded Si (100) interface after splitting at 400°C.

Using this novel approach, it has been demonstrated that smooth, oxide-free interfaces can be obtained when transferring ultra-thin silicon layers onto (100) and (111) substrates. Both the transfer efficiency and the interface properties are strongly influenced by the laser fluence. For low values, the remaining hydrogen accumulates at the bonded interface upon annealing forming bubbles as in the case of hydrophobic bonding. High temperature annealing flattens the transferred layer and removes most of the implantation induced damage, except for voids situated near the end of the implantation range.

4.1.2.6. Electrical investigations

P-n junctions were prepared by transferring ultra-thin n-type layers on p-type substrates and vice-versa. Current voltage measurements performed on as-transferred and annealed (100) and (111) interfaces are shown in Fig. 4.22. The device structure is drawn schematically at the top of each I-V plot. The corresponding interfaces are those depicted in Fig. 4.20 and 4.19, respectively.

In both cases, the as-transferred samples are characterized by a poor rectifying behaviour, due to traps introduced at the interface by bonding and in the volume of the transferred layer by implantation. The latter also act as strong scattering centers. Various electrically active centers mainly related to vacancy-hydrogen complexes have already been reported in as-implanted silicon [56], [120], [121], [122] and they are removed by annealing to about 600°C.

In order to separate different contributions that alter the junction performance, high temperature annealing steps were performed since it was already shown to decrease the implantation damage (see Fig. 4.16). I-V characteristics show a decrease of the reverse-bias current by two orders of magnitude in both cases. Most of the generation-recombination (G-R) centers associated with implantation induced defects are removed and the rectifying behaviour is improved significantly.

For comparison, I-V characteristics were simulated using the drift-diffusion model implemented with Tesca. First, a reference characteristic was calculated by creating an ideal device: the n-type and the p-type regions were “artificially” brought together (without any electrical activity of the bonded interface). Bulk recombination lifetimes for electrons and holes of 10^{-6} s were used in both device regions.

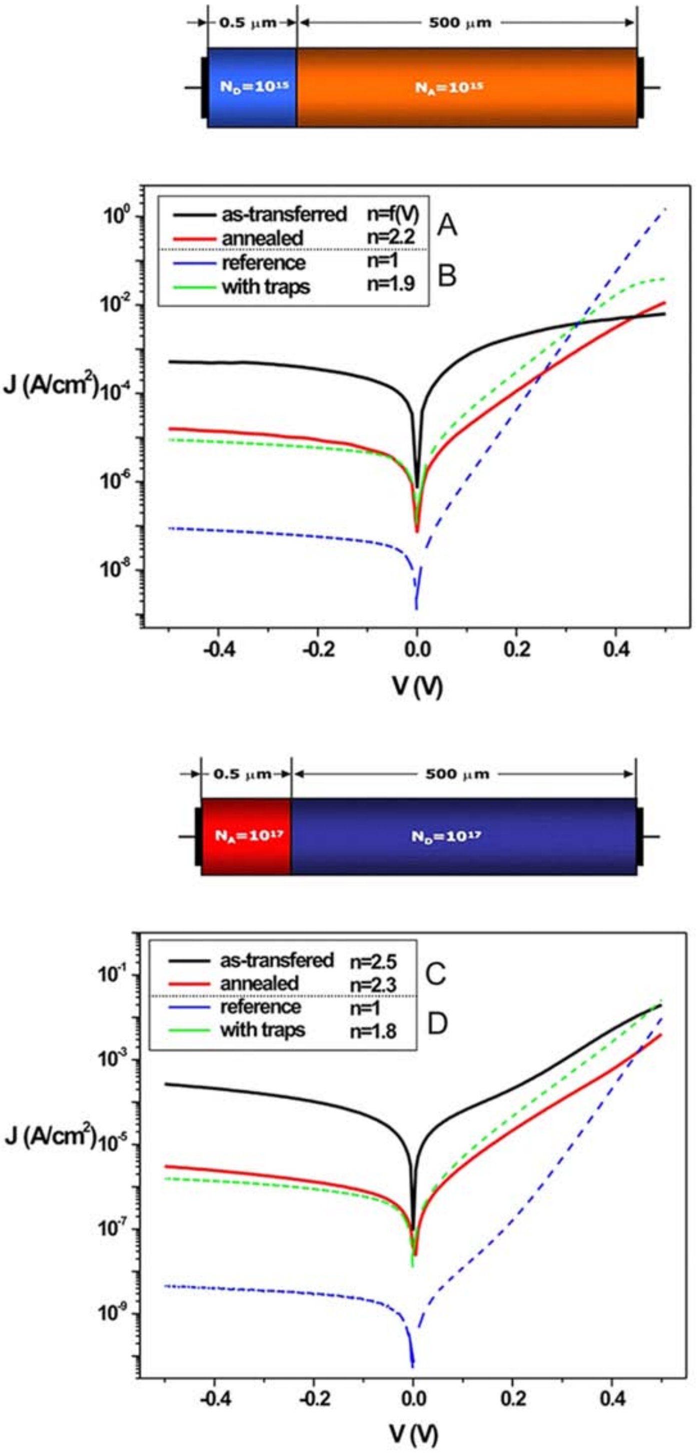

Figure 4.22: Device structure and I-V characteristics for (111) (up) and (100) (down) diodes made by layer transfer. A, C represent measured data and B, D simulation results.

The bonded interface was modelled using the parameters listed in Table 4.5. In both cases there is a good overlapping between the simulated and the measured data, indicating that the electrical activity of the interface can be correctly predicted. The relatively high trap concentration at the (111) interface is related to the large miscut of surfaces before bonding, which yields a high number of dangling and distorted bonds as described by the grain boundary theory (see Section 2.3.3, Chapter II). The surface recombination velocities are nevertheless reasonable, compared to an unpassivated Si surface (2×10^5 cm/s, ref. [123]). In the case of the (100) interface, both the trap density and the surface recombination velocities decrease to low values after annealing. Some dangling bonds might still be present at the interface, having an acceptor-like behaviour. For example, the recombination velocity for holes is only 15 cm/s, as compared to the lowest value reported for a silicon surface (0.25 cm/s) corresponding to a perfectly passivated surface [124].

Interface orientation	Trap density ($cm^{-2}eV^{-1}$)	Trap energy relative to E_i (eV)	Surface recombination velocities ($cm\cdot s^{-1}$)
111	5×10^{11}	-0.03..0	S_n=625, S_p=125
100	3×10^{11}	-0.03..0.03	S_n=150, S_p=15

Table 4.5: Model parameters.

The bulk recombination lifetimes reported in literature for as-implanted silicon are 10^{-9} s or less [56], i. e. three orders of magnitude lower than the values used here. Numerical simulations have been performed considering a lifetime of 10^{-9} s in the implanted region (not shown here), the calculated reverse-bias currents being about two orders of magnitude higher than the corresponding measured values. By repeating the simulation for different carrier lifetimes it was concluded that a lifetime recovery from 10^{-9} to 10^{-6} s occurs upon annealing.

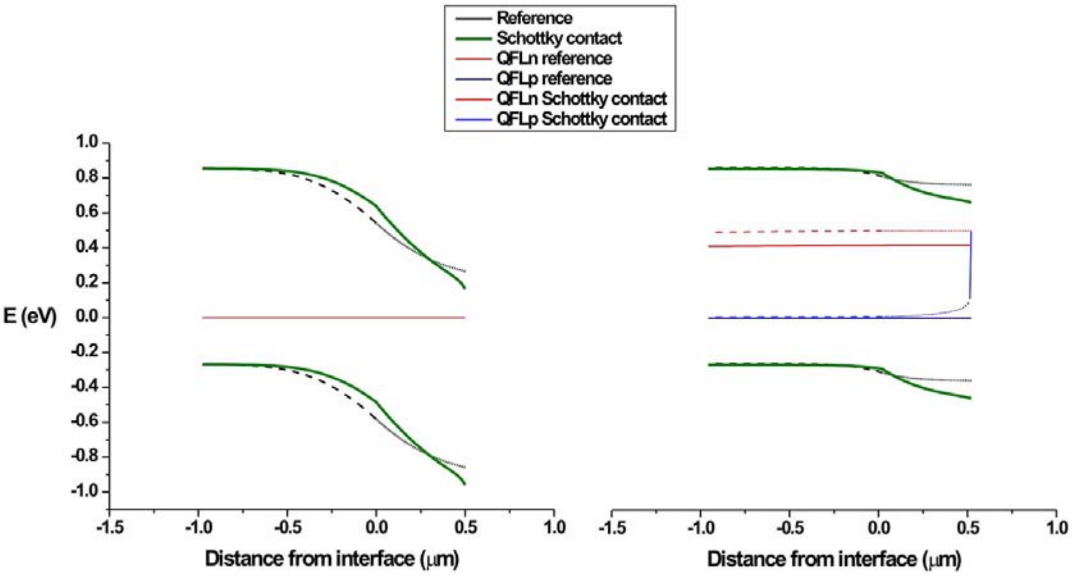

Figure 4.23: Band diagram of the bonded (111) interface when considering a Schottky contact at the n-doped surface: equilibrium (left) and 0.5 V forward bias (right).

The measured forward current is limited at higher bias values, in contrast to the ideal device curve. The effect is more pronounced in the case of the lowly-doped p-n junction, being related to the non-ideal Ohmic contact on the backside of the transferred layer, which acts as a Schottky barrier. Since the Debye length corresponding to a doping of 10^{15} cm^{-3} is several tenths of nanometers at RT, injected carriers cannot tunnel through the barrier; only those having sufficient energy to overcome the contact barrier contribute to the overall current.

The surface recombination seems not to be very important due to a low density of states at the metal-semiconductor interface. The real device simulation takes into account this effect, as depicted in Fig. 4.23.

The band bending corresponding to equilibrium and 0.5 V forward bias have been calculated to show the effect of a Schottky contact. Reference simulation data were plotted for comparison. One can see the barrier increase of about 0.1 eV (roughly the barrier of dysprosium silicide on n-type silicon, ref. [125]) which limits the forward-bias current.

In the case of a higher background doping, the aforementioned effect is negligible, as seen in Fig. 4.22 (down) the simulated forward current being close to the one measured experimentally.

An additional factor which limits the current is represented by nanovoids existing towards the end of the implantation range, close to the ohmic contact of the device. As seen in Fig. 4.16, they do not disappear upon annealing, acting as strong scattering (and possibly recombination) centers. These problems could be circumvented by removing a part of the transferred layer (using chemo-mechanical polishing) followed by shallow implantation of arsenic or phosphorus.

In summary, Si-Si interfaces prepared by hydrogen implantation, wafer bonding and layer splitting in UHV were successfully prepared and characterized. There is a high flexibility in terms of thickness, doping and surface orientation of the transferred layer. In the case of lowly doped materials, additional steps should be performed to ensure good device performance. High temperature annealing was demonstrated to flatten the transferred layer, to remove the implantation induced damage and to restore the electrical properties of the material. The modified surface preparation is fully compatible with the UHV environment thus allowing to address novel applications and to extend this approach to dissimilar materials.

4.2. Silicon-gallium arsenide interfaces

An activation of GaAs surfaces is required in order to achieve covalent bonding at RT. The main problem is the oxide removal without inducing surface roughening, which can be particularly difficult in the case of implanted substrates. In the following, the influence of the oxide removal process on the bonding quality will be presented and discussed. The second part deals with the possibility to transfer ultra-thin GaAs layers onto Si substrates using ion implantation and UHV bonding.

4.2.1. Silicon-gallium arsenide interfaces obtained by UHV bonding

4.2.1.1. Surface activation by atomic hydrogen bombardment

As discussed in Section 3.3.3 Chapter III, the ozone degreasing was followed promptly by transfer into the UHV assembly where various treatments were performed in order to remove the oxides present on the surface. After each treatment, the corresponding GaAs wafer was bonded to a Si(100) wafer. The results are summarized in Table 4.6.

As one can observe, only the wafers which were exposed to atomic hydrogen during heating develop a surface which meets the requirements for bonding, provided that the temperature falls within a specific range (350-550°C) and the time is relatively short. By adjusting the time and temperature, it was also possible to achieve bonding after pure thermal desorption (experiment G). However, double cantilever beam test measurements revealed low bonding energies (<800 mJ/m^2) in this case, confirmed by the fact that the samples could not withstand the TEM preparation.

Experiment	H bombardment	Temperature (°C)	Time (min)	Bonding
A	Yes	350	10	Yes
B	Yes	450	10	Yes
C	Yes	550	10	Yes
D	Yes	550	90	Yes (<800 mJ/m^2)
E	Yes	600	90	No
F	No	400	10	No
G	No	550	10	Yes (<800 mJ/m^2)
H	No	600	20	No
I	No	600	90	No

Table 4.6: Treatment of the GaAs surfaces prior bonding.

These results can be explained considering the desorption characteristics of various oxide species present on the GaAs surface. Thus, a heating step at 400°C removes As_2O, As_2O_3 and As_2O_5 but leaves a rough surface covered with Ga_2O_3 and a mixed $GaAsO_4$ which impedes bonding, as confirmed by earlier findings [81], [87], [88], [89]. LEED investigations of such surfaces revealed no diffraction pattern in the energy range 10-200 eV. Around 550-580°C desorption of Ga_2O_3 sets in allowing partial oxide removal as confirmed by the LEED image in Fig. 4.24 (left) where a diffraction pattern appears.

Since in this temperature range the arsenic evaporates from GaAs surfaces, it is difficult to remove the remaining oxide without compromising the surface quality. Thus, after heating to 600°C the surface already becomes rough and the diffraction patterns disappears as gallium droplets start to form. No bonding is possible even if the wafer undergoes prolonged heating. The strong covalent bonding that can be achieved after H bombardment between 350 and 550°C is an indirect confirmation that oxides can be removed in this way without rendering the surface rough.

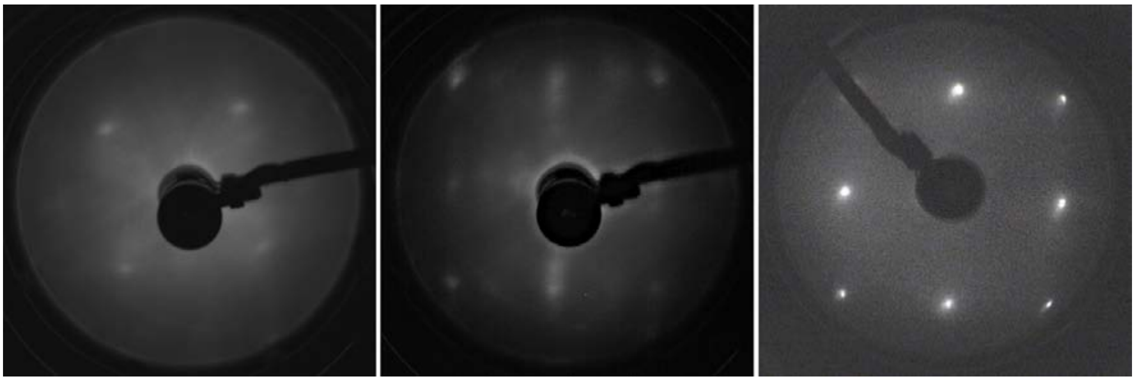

Figure 4.24: Evolution of the LEED diffraction pattern of GaAs(100) surfaces during the heat treatment: G (left, 120 eV), B (middle, 47 eV) and C (right, 120 eV).

The explanation relies on the well-established role of atomic H in lowering the desorption temperature of various arsenic and gallium oxides, especially the non-volatile Ga_2O_3. In the presence of H at moderate temperatures, Ga_2O_3 is converted to Ga_2O and water which subsequently evaporates:

$$Ga_2O_3 + 2H\cdot \rightarrow 2Ga_2O + 2H_2O\uparrow \tag{4.23}$$

The decomposition of arsenic oxides occurs in a similar manner:

$$As_2O_x + 2xH\cdot \rightarrow xH_2O\uparrow + As_2\uparrow \tag{4.24}$$

where x=1, 3 and 5. The decomposition of $GaAsO_4$ proceeds according to the following reaction:

$$2GaAsO_4 + 8H\cdot \rightarrow Ga_2O + As_2O_3 + 4H_2O\uparrow \tag{4.25}$$

which leads to the conversion to oxides that decompose according to (4.24).

There is still quite a debate regarding the temperature at which the reaction (4.23) proceeds. Razek et al. [126] found that a substrate heating to 150°C is sufficient to completely remove C and O from surfaces using H plasma beam, while other workers pointed out the necessity to heat the substrate to at least 350°C i. e. the evaporation temperature of Ga_2O [88], [89]. Below a certain temperature, the newly formed Ga_2O acts as a mask which hinders further reaction of H with Ga_2O_3. Instead of evaporating, Ga_2O decomposes to atomic gallium and water in the presence of H:

$$Ga_2O + 2H\cdot \rightarrow 2Ga + 2H_2O\uparrow \tag{4.26}$$

Since this reaction would result in an excessively Ga-rich surface [127], it was avoided by performing all desorption experiments above 350°C so that Ga_2O evaporated before reacting with atomic hydrogen. Upon H bombardment at 450°C for 10 minutes the surface undergoes a (3x6) reconstruction (Fig. 4.24, middle), corresponding to a slightly Ga-rich structure. This is similar to the (4x6) reconstruction identified by Ide et al. [127], previously observed during the transition from the As-rich (2x4) to the Ga-rich (4x2) phase [128]. The weak contrast in the LEED image is ascribed to the absence of a long-range ordering of the surface, which consists of small domains that might exhibit different reconstructions known to exist on (100) GaAs surfaces [129], [130], [131]. Longer bombardment times and/or higher temperatures don't result in a higher ordering of the surface. Instead, a (1x1) pattern was observed (Fig. 4.24, right) which corresponds to an even Ga richer surface [127]. For even higher processing temperatures (experiments D, E) the LEED pattern disappears due to formation of a liquid gallium film on the surface.

4.2.1.2. Structural investigations

The structure of the Si-GaAs bonded interfaces was investigated by TEM in cross-section and plan view. Fig. 4.25 depicts a high-resolution micrograph in cross-section right after RT bonding where two sets of (111) atomic planes can be identified, belonging to the two single crystals, crossing the interface at an angle of 54.7°.

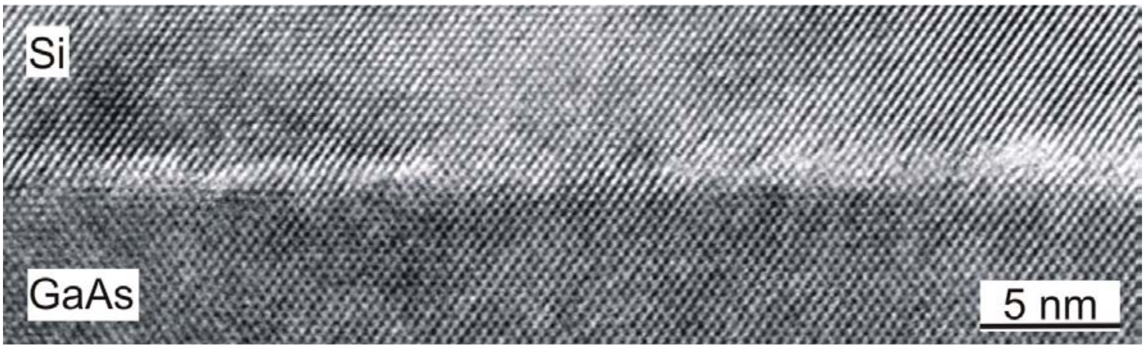

Figure 4.25: HRXTEM image of a Si-GaAs (100) interface after RT bonding (viewing direction [011]).

The bonded interface appears as a bright stripe and shows no evidence of a thick intermediate layer. The lattice is disturbed periodically by extra-half planes coming from silicon that have no correspondent on the GaAs side. They are surrounded by areas with brighter contrast given by the strain field of the misfit dislocations that account for the 4% lattice mismatch between Si and GaAs. In the remaining regions the atomic planes cross the interface without evidence of a transition. However, some bright contrast is still visible, due to the nanoroughness of the wafer surfaces before bonding and/or to possible residual contaminants.

Upon annealing to 850°C for 30 min, the atoms migrate along the interface occupying more favourable positions and the interface relaxes. A clear difference can be observed in Fig. 4.26, which depicts the same interface after annealing. The only evidences of the interface are the darker appearance of the GaAs layer and the bright spots given by the strain field of the misfit dislocations, separated by a mean distance of 10.5 nm corresponding to the 4% lattice mismatch.

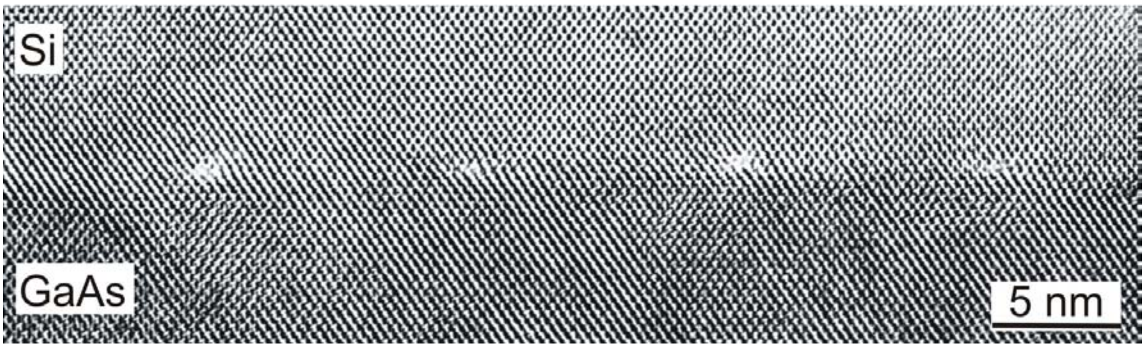

Figure 4.26: HRXTEM image of a Si-GaAs after annealing at 850°C for 30 min.

According to the O-lattice theory developed by Bollmann [65], the mismatch of an (100) interface between two fcc lattices having different lattice parameters is accommodated by a square network of edge dislocations having Burgers vectors ½$[110]$ and ½$[1\bar{1}0]$. Since the misorientation of a (100) twist boundary in fcc lattices is accommodated by a square network of screw dislocations having the same Burgers vectors, it is expected that both the lattice mismatch and the twist are relaxed once a regular dislocation network develops at the interface. The dislocation distance depends on the lattice mismatch factor and on the twist angle θ according to [132]:

$$D = \frac{a_1 a_2}{\sqrt{2\left(a_1^2 + a_2^2 - 2a_1 a_2 \cos\theta\right)}} \tag{4.27}$$

where a_1 and a_2 are the lattice constants of Si and GaAs, respectively, and the angle θ is expressed in radians.

The angle between the dislocations relaxing a pure mismatch and dislocations relaxing a twist and a mismatch is given by:

$$\eta = \arctan\left(\frac{a_2 \sin\theta}{a_1 - a_2 \cos\theta}\right) \tag{4.28}$$

taking GaAs as reference.

The as-bonded sample exhibited a irregular Moire pattern related to the lattice misfit, fringes being interrupted due to defects present at the interface as revealed by plan view investigations of 25°-cut samples (Fig. 4.27, left). The fringes are distorted locally due to the remaining strain at the interface. Upon annealing, a regular dislocation network develops (right) as predicted by theory and confirmed by earlier findings [133], [134]. The mean dislocation distance was about 10.0 nm, which corresponds to a twist angle of 0.7° between the two wafers. The angle between the observed dislocation network and a network relaxing a twist-free interface is -20° (the minus sign denotes a counter-clockwise rotation). No voids or inclusions were observed at the interface.

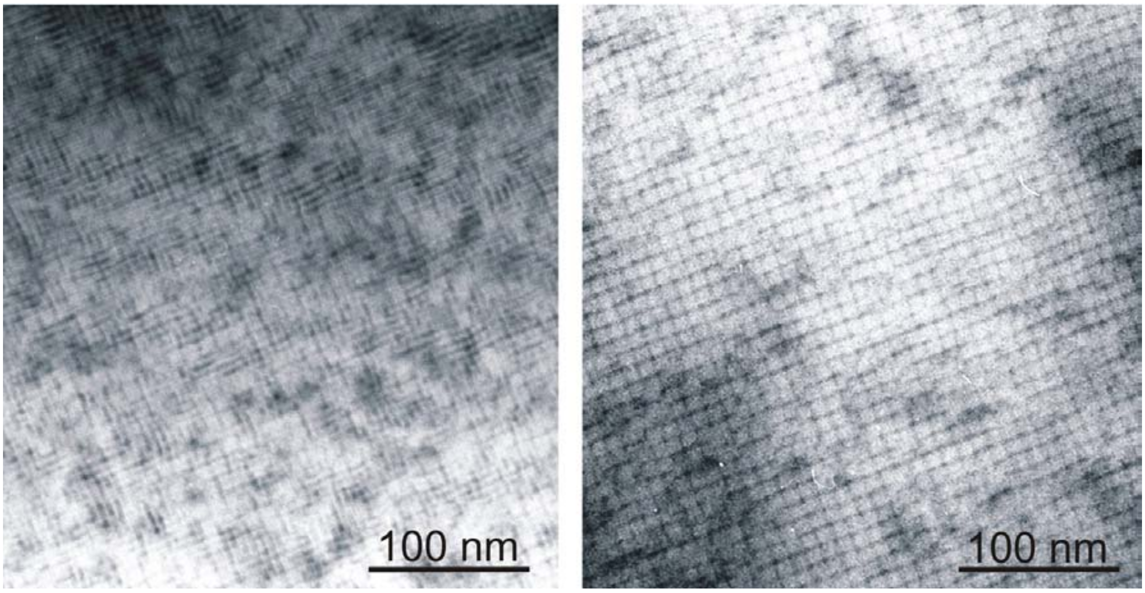

Figure 4.27: TEM plan-view investigation of an as-bonded Si-GaAs interface (left) and annealed (right) interface.

In some regions of Fig. 4.27 (right) the dislocation lines are shifted by approximately half of the spacing between the edge dislocations. Zhu et al. [133] observed similar features and attributed them to the presence of some 60° dislocations accommodating a small tilt originating in miscut and steps on the wafer surface. The 60° dislocations interact with edge dislocations changing their Burgers vector so that their screw component vanishes and the edge component accommodates a lattice mismatch strain corresponding to half of an edge dislocation. As a result, complicated patterns can be observed such as zigzag lines or closed circuits, depending on whether the 60° dislocations interact with one or both sets of 90° dislocations. The Burgers vectors of the new dislocations are of type $\frac{1}{2}[011]$ and $\frac{1}{2}[101]$.

By tilting the cross-section sample about 30° around the [110] direction, extended dislocations can be observed in the GaAs layer as depicted in Fig. 4.28. They interact with the dislocation network disturbing it locally.

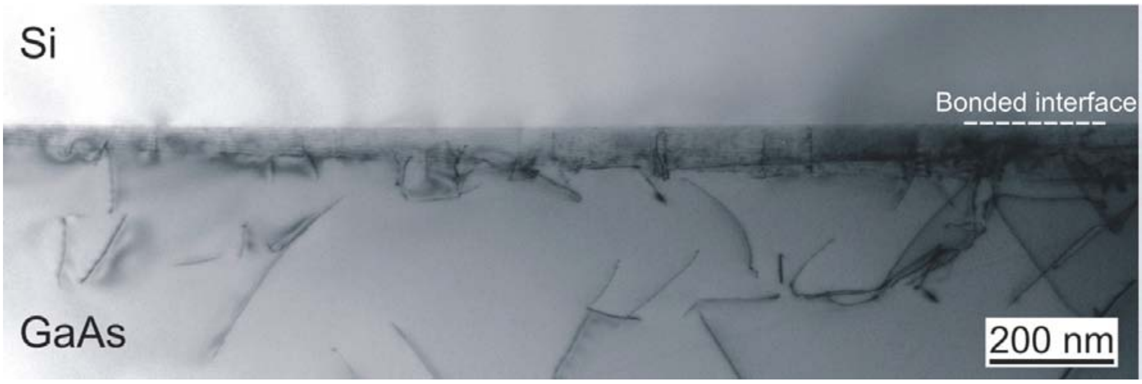

Figure 4.28: TEM 30° tilt image of a Si-GaAs interface after annealing.

They are deemed to have an impact on the electrical properties of the bonded interface as discussed later. Since they were barely observed in the non-annealed sample, they most probably account for the stress induced by the thermal mismatch between Si and GaAs. The linear thermal expansion coefficient of GaAs is about 2.5 times higher than that of silicon [75], which means that a compressive stress acts upon the GaAs layer during heating. The thickness of the GaAs layer after CMP/etching was still large enough so that the energy that would have been required to deform it elastically in order to accommodate the thermal stress was larger than the energy spent in order to generate dislocations in the material. This problem could be avoided by a modified implantation induced layer transfer with the thickness of the transferred layer being in a range for which the elastic deformation energy would be below the threshold of generating such dislocations.

4.2.1.3. Electrical investigations

In the preceding sections it was shown that strong bonding can be achieved at RT using the proposed approach, with good microstructural characteristics of the interfaces. This represents an important advance in terms of low (and intermediate) processing temperatures, absence of an intermediate layer and controllable doping profiles which can be used for various applications in areas such as optoelectronics and high power devices. The goal of this section is to study the electrical transport at bonded interfaces between dissimilar materials, since this subject received little attention in the past.

Using UHV bonding, pn+ and p+n+ heterojunctions were prepared and investigated by different methods listed in Section 3.6, Chapter III. In order to make a qualitative investigation of the electrical transport at the interface over the whole wafer area, thermoelectrical measurements were performed first.

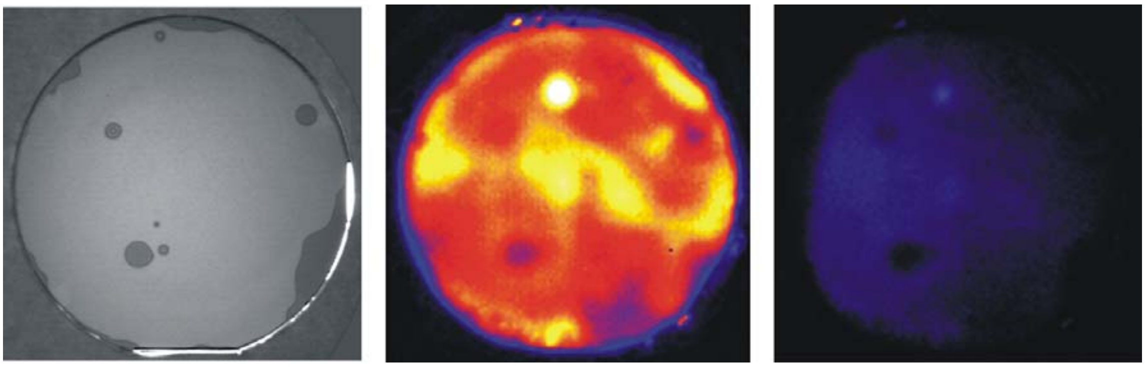

Figure 4.29: Transmission infrared image of a Si(p)-GaAs(n+) bonded interface (left) and the corresponding thermography in forward (center) and reverse (right) regime on a 0-3 mK scale.

Fig. 4.29 depicts the lock-in thermography image of a bonded pair compared to the corresponding infrared image. The pn+ diode was measured both in forward and reverse regime, showing the typical rectifying behaviour. A DC bias of 1 V was applied being switched on/off with a frequency of 3.4 Hz. Currents of 3260 and 540 mA were flowing in forward and reverse regimes, respectively. The current density is relatively uniform, except some dark regions corresponding to unbonded areas caused by macroscopic particles incorporated before bonding. The density of observed shunts was very low.

The influence of the cleaning procedure of GaAs surfaces on the transport properties was investigated by temperature dependent current-voltage measurements (only RT data being shown here). Different I-V curves (see Table 4.6 for cleaning parameters) measured at RT are represented for comparison in Fig. 4.30.

For n+p+ junctions bonded without H bombardment (experiment G) the ideality factor is 2.5 and the rectifying factor *R* is 52. An ideality factor larger than two indicates that other mechanisms beside diffusion and/or recombination contribute to the overall electrical transport through the interface. It is reasonable to assume that the current is given by the carriers tunnelling through the thin oxide layer remaining on the GaAs surface after cleaning, since the temperature dependence of the current was very weak. In the case of samples bonded after surface cleaning with H bombardment, the rectifying factor increases to 1.8×10^3 (experiment A). The low value of the ideality factor (n=1.4) is an indirect proof that no oxide is present at the interface. The I-V signature doesn't change significantly when the desorption temperature is varied, the small differences between the curves A and B being the consequence of doping variation rather than differences in surface quality.

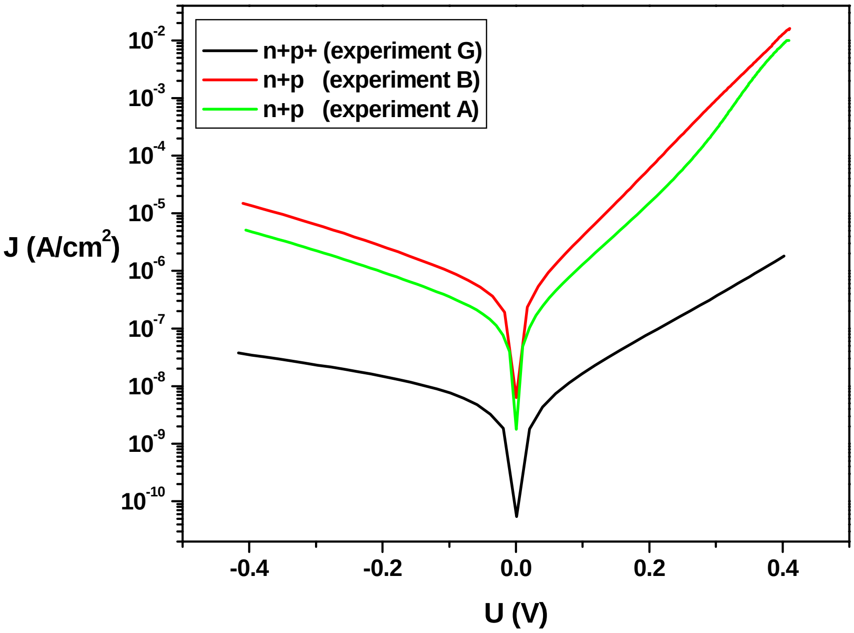

Figure 4.30: I-V characteristics after bonding with different cleaning procedures listed in Table 4.6.

The bonding process causes a quasi-continuum of states in the band gap, as described by the theory of grain boundaries. The calculated values for the n factor also indicate a possible recombination contribution to the forward current. In order to quantify the influence of interface states and to see whether their presence yields a distinctive potential barrier or not, simulations of the Si-GaAs interface were performed using the drift-diffusion model implemented with the Tesca software. First, an “ideal” device was generated by bringing together the n-type GaAs with the p-type Si without any electrical activity of the bonded interface. The carrier mobilities were chosen to depend on electric field, doping and temperature [135]. Minority carrier lifetimes of 10^{-6} and 10^{-9} s (due to bulk SRH recombination) were used for Si and GaAs, respectively. The values for the radiative (band-to-band) and Auger recombination coefficients are listed in Table 4.7. Auger recombination becomes important only for heavily doped substrates (>10^{18} cm^{-3}), but it was included in order to compare the present simulations with the calculations done later for annealed samples. The radiative recombination is important only in GaAs (which is a direct bandgap semiconductor).

Material	Radiative recombination coefficient (cm^3/s)	Auger recombination coefficient (cm^6/s)
Si	2×10^{-15} [136]	$C_n=2.8\times10^{-31}$, $C_p=10^{-31}$ [137]
GaAs	1.7×10^{-10} [138]	$C_n=1.6\times10^{-29}$, $C_p=4.6\times10^{-31}$ [136]

Table 4.7: Radiative and Auger recombination coefficients for Si and GaAs.

The interface was modelled assuming states lying between E_i-0.03 eV and E_i+0.03 eV (roughly 3kT) with a constant trap density of 5×10^{12} cm^{-2} (E_i represents the intrinsic Fermi level in GaAs). These values were in good agreement with those measured by means of DLTS (see Table 4.9). Simulations taking into account interface states with different activation energies revealed that the most efficient recombination centers are those lying close to E_i, as described by the SRH theory. On the other hand, donor-like levels positioned at E_i would be neutral (i. e. filled with electrons) for small biases. If emptied, they yield a positive charge which needs to be compensated by increasing the electron concentration and/or decreasing the hole concentration at the interface. Since the equilibrium concentration of electrons at the interface is much higher than that of holes, such a scenario is not very probable by means of generation-recombination mechanisms. Instead, acceptor-like states were assumed, since they could be easily compensated by decreasing the electron concentration at the interface. The surface recombination velocities were 2.5×10^4 cm/s and 2.5×10^3 cm/s for electrons and holes, respectively (for reference, the surface recombination velocity for unpassivated GaAs can be as high as 3×10^6 cm/s [56], [139]). The resulting I-V curves were plotted together with the measured data for reference as depicted in Fig. 4.31.

The main difference between the ideal and the real case consists in an increase of the reverse bias current of about two orders of magnitude for the same bias conditions. The forward current is influenced to a smaller degree, since it mainly depends exponentially on the applied bias. As soon as a reverse bias is applied, the space charge region is depleted of carriers and the generation mechanisms try to re-establish the equilibrium carrier values. The resulting generation current adds up to the ideal reverse current prescribed by the Shockley equation [76]. Therefore, the presence of active recombination centers at the bonded interface causes leakage currents which deteriorate the junction performance to some extent.

The mechanical damage introduced during sample preparation leaves a very defective semiconductor surface, passivated by a low quality native oxide. Therefore additional leakage currents are expected to contribute to the strong dependence of the reverse-bias current on the applied voltage seen in Fig. 4.31. Since the drift-diffusion model implemented with the software Tesca does not account for surface leakage currents, the aforementioned dependence could not be reproduced with higher accuracy regardless of the trap distribution used for computation.

Another reason for the observed behaviour could be the existence of deep levels in a small volume surrounding the interface, and not solely in the bonding plane.

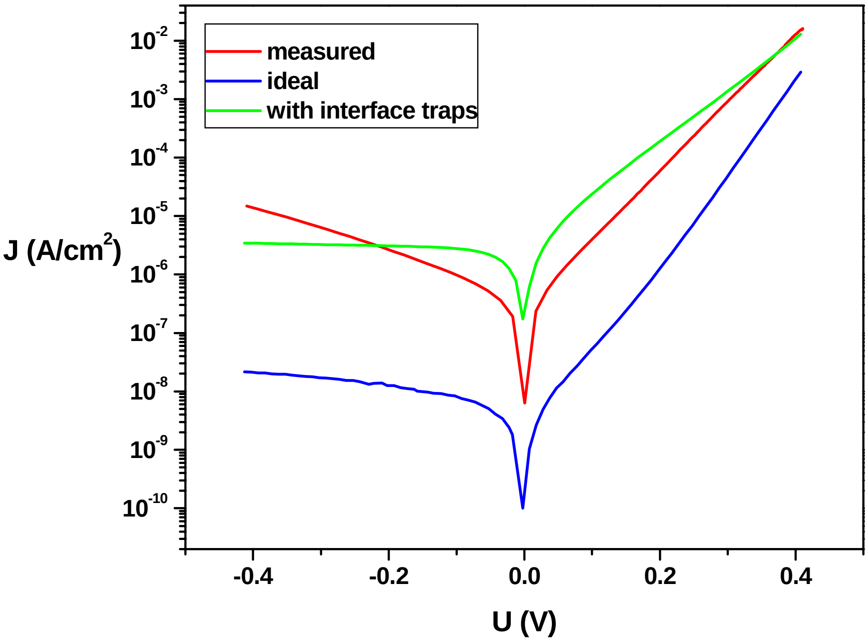

Figure 4.31: I-V characteristics for simulated vs. measured data showing the influence of the interface states on the current flow.

Since the recombination process can affect the forward currents as well, the ideality factor was calculated for several temperatures between 260 and 340 K. The values extracted from the simulated characteristics were plotted in Fig. 4.32 for comparison. As observed, the sample without interface oxide is closest to the ideal case, *n* being low (1.4-1.55) and relatively constant in the investigated temperature range. The simulation including interface charges also yields an ideality factor between 1 and 2 as expected from theory.

It is important to know if the proposed interface trap distribution causes a distinctive potential barrier at the bonded interface in order to check if the grain boundary theory can be applied to phase boundaries as well. The calculated values for the electrostatic potential, carrier concentrations and band structure are depicted in Fig. 4.33.

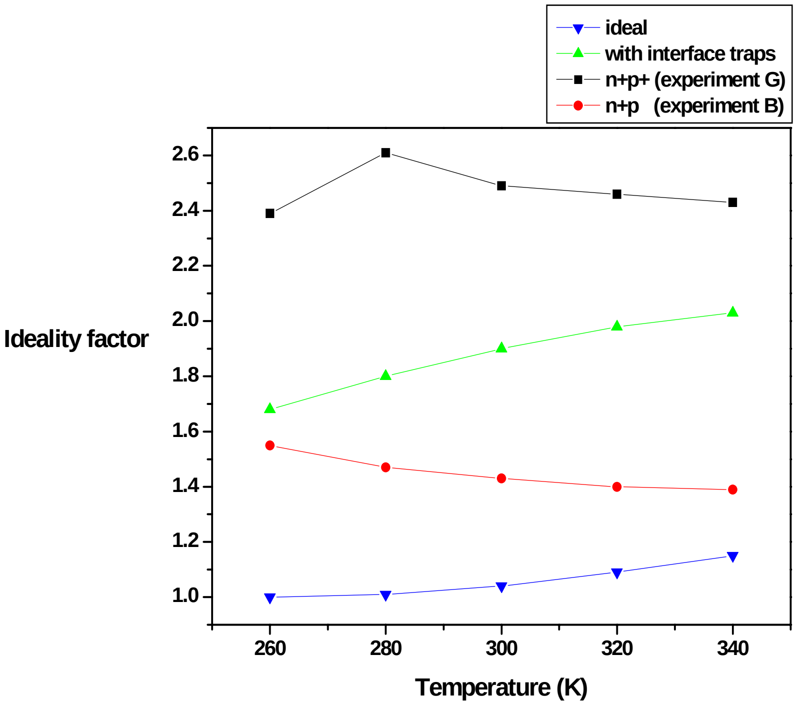

Figure 4.32: Ideality factor variation with temperature for real vs. simulated junctions.

In thermal equilibrium the net generation rate is zero and all the traps situated below the Fermi level will be filled with electrons. Since the assumed interface states are acceptor-like, they will yield a negative charge when filled, observed by the steep variation of the built-in potential at the interface. As an effect of the generation-recombination, the concentration of holes increases at the interface and in the adjacent p-doped region. The concentration of electrons in the conduction band decreases accordingly and the total depletion approximation is not valid in this case.

In order to preserve the charge neutrality the bands readjust as seen in Fig. 4.33. The depletion width in Si decreases because there is less positive charge that needs to be compensated. Depending on the trap density at the interface, the depletion width in GaAs might increase by the same token: more fixed shallow donors will be needed to compensate the shallow acceptors in the p-type region and the deep acceptors at the interface. These findings are in good agreement with (4.10), showing that the depletion width is not solely given by doping and bias conditions, but also by the presence of interface states. Thus, the general assumption that the depletion width extends only in the lower doped side for asymmetric p-n junctions is no longer valid, leading to ambiguities regarding data interpretation in the case of techniques relying on the aforementioned approximation (such as DLTS and CV).

The presence of charged traps doesn’t yield a potential barrier at the bonded interface.

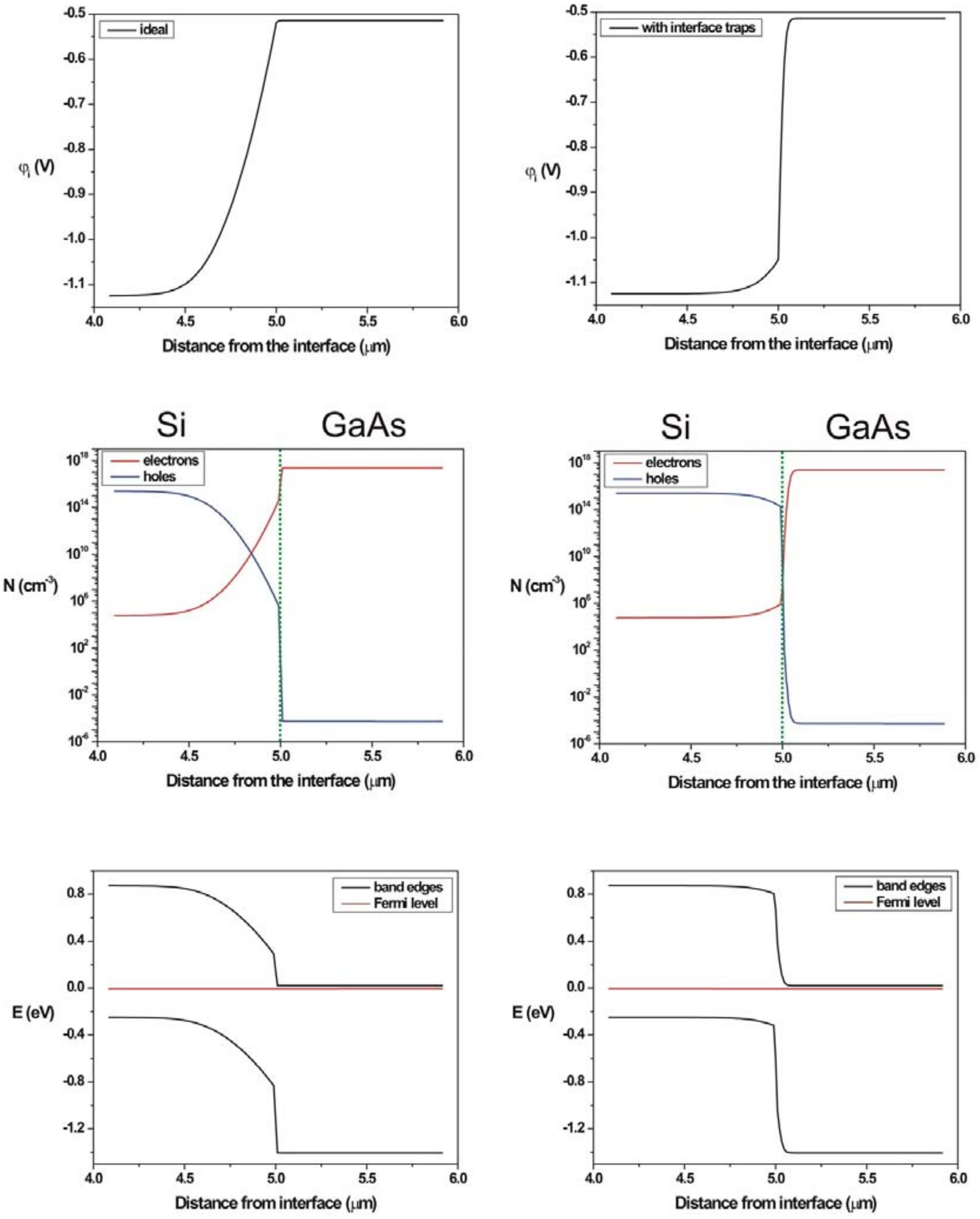

Figure 4.33: Equilibrium built-in potential, carrier concentrations and band structure for an ideal Si-GaAs interface (left) and with interface states (right).

4.2.1.4. Annealing

The effect of annealing on the microstructural properties of the interfaces has already been discussed in Section 2.1.2. It was shown that the interface relaxes by establishing a regular dislocation network which accounts for the misfit and the misorientation between the two crystals. The temperature enhanced diffusion of atoms at the interface also helps in smoothing the nano-roughness related to surface steps and miscut.

In the case of asymmetric doping profiles and/or dissimilar materials there is one additional possibility that the atoms belonging to one material start diffusing into the lattice of the other taking up either interstitial or substitutional sites. The interdiffusion process will have important consequences on the doping profile of the device: Si is an amphoteric dopant in GaAs, while gallium and arsenic behave in Si as p-type and n-type dopants, respectively.

The change of the impurity concentration with time is modelled by the second Fick's diffusion law:

$$\frac{\partial C(x,t)}{\partial t} - D\frac{\partial^2 C(x,t)}{\partial x^2} = 0 \tag{4.29}$$

where D is the diffusivity (or diffusion coefficient) and $C(x,t)$ is the impurity concentration. The above equation is valid when no sources or sinks are present and when the diffusivity at a certain temperature is concentration independent. Moreover, no electric fields are assumed to be present in the material. Equation (4.29) was solved numerically in order to determine the diffusion profiles after 30 min annealing at 850°C using the following boundary conditions:

$$\begin{aligned} &C(0,t) = C_s \\ &C(x,0) = 0 \\ &C(L,t) = 0 \end{aligned} \tag{4.30}$$

At zero time the concentration is zero everywhere in the material. Moreover, the concentration will remain equal to zero at a depth $L>>Dt$ where t is the annealing time. The third condition is provided considering that the concentration cannot exceed the limit given by the solid solubility C_s regardless of how much of the doping element would be provided.

For simplicity, the three diffusion processes were considered independent in the sense that the incorporation of one element in a specific substrate neither limits the concentration nor the diffusion length of another element. In a real case this assumption might not be valid since the diffusion is influenced by the concentration of native point defects, Fermi level position and electrical fields if the diffusing species are charged.

The diffusivities and solid solubilities used for calculation are listed in Table 4.8.

Element	Substrate	Diffusivity (cm^2/s)	Solid solubility (cm^{-3})
Si	GaAs	$2.3\text{x}10^{-15}$ [140]	$2\text{x}10^{19}$ [141]
Ga	Si	$2\text{x}10^{-16}$ [142]	$7.3\text{x}10^{18}$ [143]
As	Si	$4\text{x}10^{-17}$ [144]	$1.7\text{x}10^{20}$ [144]

Table 4.8: Solid solubilities and diffusivities at 850°C.

The calculated diffusion profiles are given in Fig. 4.34:

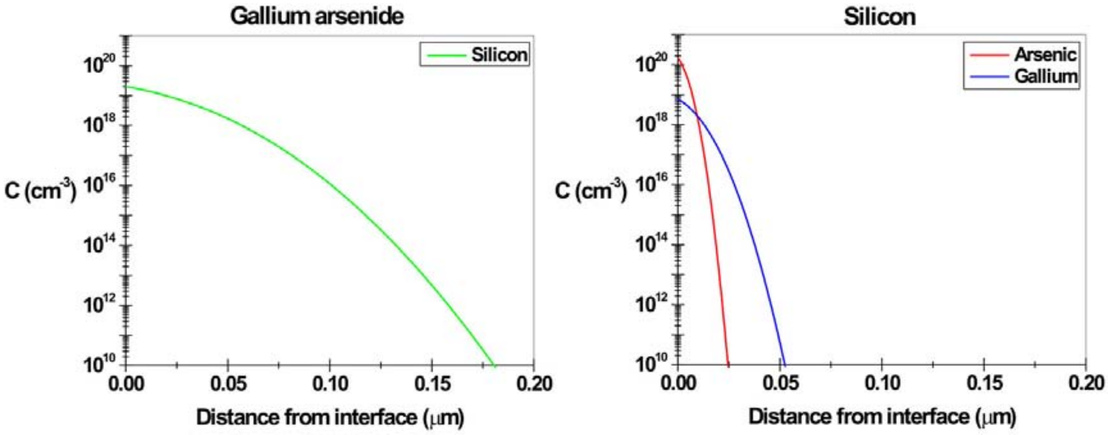

Figure 4.34: Impurity concentrations vs. distance for 30 min annealing at 850°C.

The post-annealing doping profiles were calculated accordingly, assuming that all diffused atoms are incorporated as electrically active shallow donors or acceptors. This is only partly true, since some atoms will end up in interstitial positions or will form neutral complexes.

In GaAs, the Si can be either incorporated interstitially, on Ga or on As sites. Due to its preference for Ga sites it was treated as an n-type dopant here (although being generally considered an amphoteric impurity in GaAs). Consequently, the net doping density of the GaAs side after annealing is given by:

$$N_{net,GaAs} = N_D + C_{Si}(x) \tag{4.31}$$

where N_D is the initial doping value of $2.5\text{x}10^{17}$ cm^{-3} and $C_{Si}(x)$ is the concentration profile of incorporated silicon plotted in Fig. 4.34.

In Si, both Ga and As need to be taken into account since their ionization probabilities are comparable (53.5 meV for As$^+$ and 65 meV for Ga$^-$, ref. [58]). The doping profile in the Si side will be as follows:

$$N_{net,Si} = N_A + C_{Ga}(x) - C_{As}(x) \tag{4.32}$$

$C_{Ga}(x)$ and $C_{As}(x)$ being the concentration profiles for Ga and As respectively.

The overall doping is represented in Fig. 4.35a together with the computed carrier concentrations, the built-in potential and the band diagram corresponding to the annealed sample. The dotted lines represent the initial doping profile. The variation of these parameters in the case of an ideal Si-GaAs heterojunction has been plotted again for reference.

The transition from n-type to p-type doped material is shifted with respect to the bonded interface into the Si layer. The transition occurs at a distance x_0 given by $C_{As}(x_0) = C_{Ga}(x_0)$, i. e. about 10 nm. Beyond this point, the doping is given by the profile of the Ga atoms which eventually reaches the background doping concentration (2.5×10^{15} cm^{-3}). The free carrier concentration and the built-in potential follow the same trend: after peaking at the interface because of the heavy n-doping, they follow patterns similar to the reference case, but slightly displaced to the right. Both Si and GaAs are degenerated close to the interface, so that the Fermi level is above the conduction band edge.

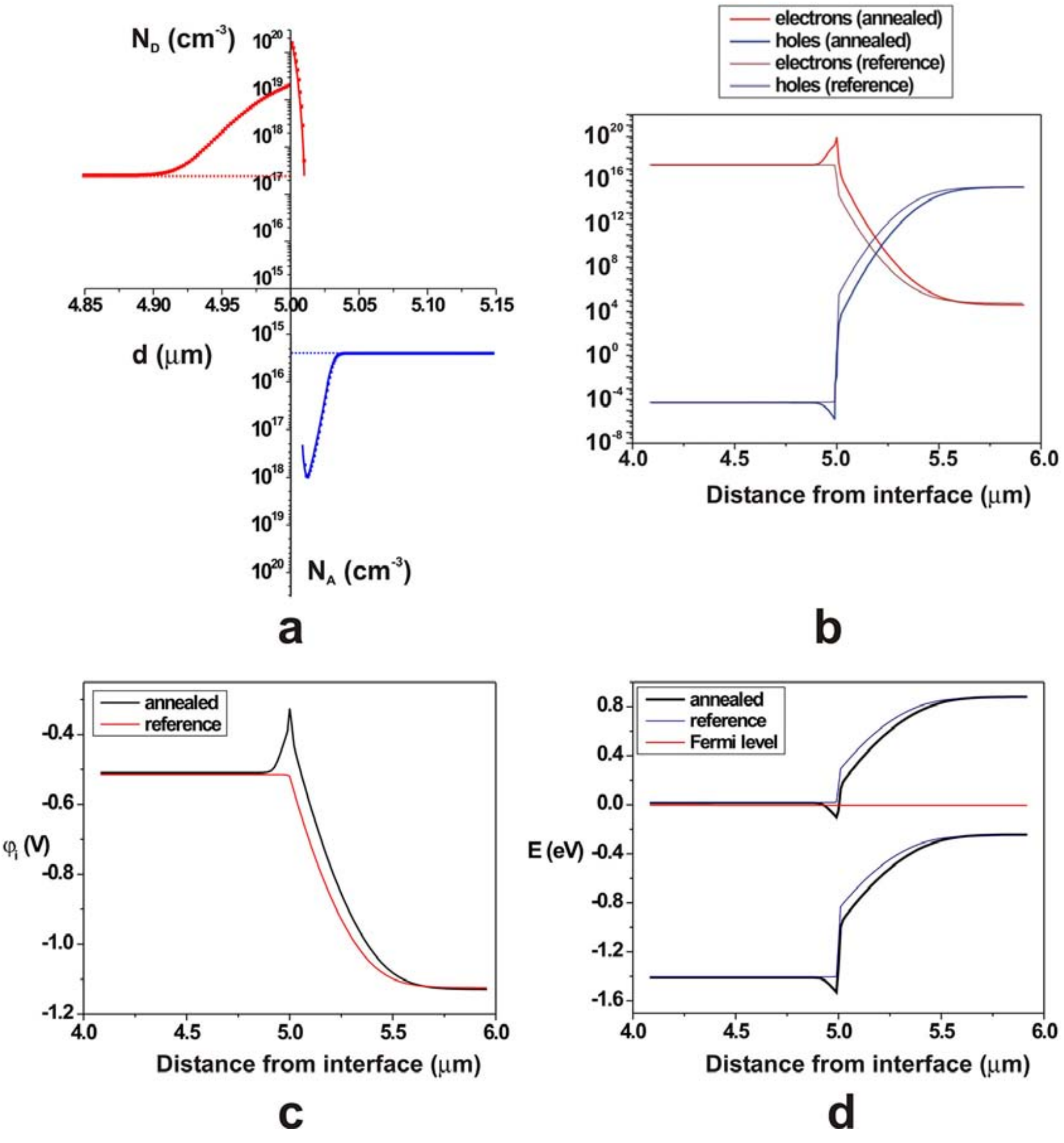

Figure 4.35: Doping profile after annealing (a) and the corresponding carrier concentrations (b), built-in potential (c) and band structure (d) of the device.

The current voltage relationship measured at room temperature is plotted in Fig. 4.36. There is a good overlapping with the simulated data, indicating that the doping profile was correctly predicted. No states were assumed to be present at the bonded interface. In fact, no notable effect was seen on the I-V characteristics even when trap densities of 10^{14} cm^{-2} and surface recombination velocities of 10^5 cm/s were used for computation. This is not surprising, since the physical interface is embedded now in a heavily doped n-n transition. If there would be any interface charges, they would be screened very efficiently by the semiconductor and the corresponding barrier would be so thin that carriers could tunnel through it very easily.

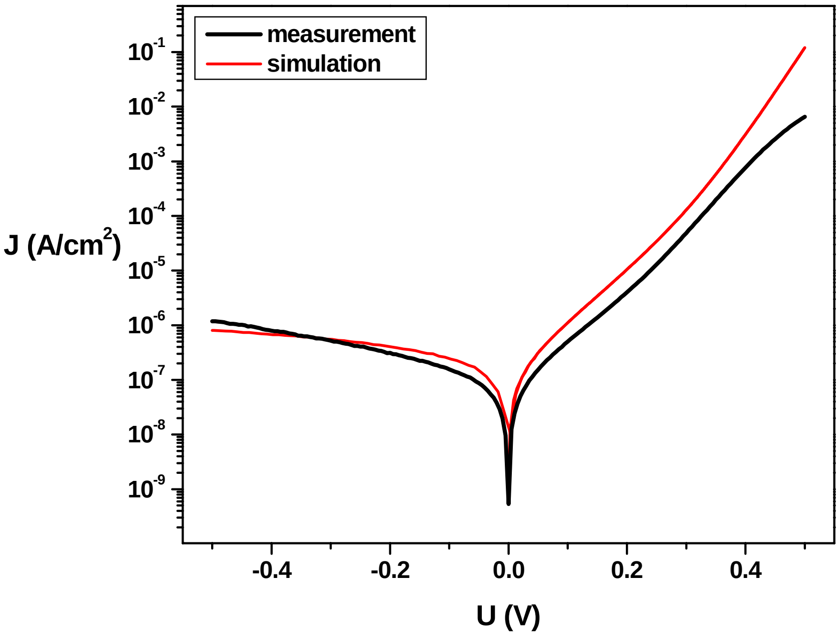

Figure 4.36: RT current-voltage characteristic of the annealed Si-GaAs interface.

A modified recombination lifetime ($3\text{x}10^{-8}$ s) in the heavily doped Si was used for simulation because of the onset of trap-assisted Auger recombination that further decreases the SRH lifetime [145]. The steeper variation of the measured forward current at higher biases is attributed to the series resistance effect occurring because of the non-ideal ohmic contacts. It is also possible that the dislocations present in the GaAs layer after annealing (see Fig. 4.28) scatter carriers decreasing the overall electron mobility below the values used here. The ideality factor is equal to that of the non-annealed sample. Howlader et al. [146] observed an increase of the ideality factor after annealing, probably due to the different cleaning procedure of the GaAs wafers before bonding. The reverse-bias current decreases by one order of magnitude in comparison to the as-bonded sample. Thus, it is expected that the density of electrically active defects decreases at the bonded interface after annealing.

DLTS investigations revealed a decrease of the peak amplitude after annealing as seen in Fig. 4.37. The junction capacitance is related to the interface trap density N_S according to the formula:

$$C = \sqrt{\frac{q\varepsilon_n\varepsilon_p N_D N_A}{2(\varepsilon_n N_D + \varepsilon_p N_A)(V_{bi} - V) - qN_S^2}} \tag{4.33}$$

where V_{bi} is the built-in potential of a p-n heterojunction:

$$V_{bi} = \frac{\Delta E_c - \Delta E_v}{2q} + \frac{kT}{q}\ln\frac{N_D N_A}{n_{i,n} n_{i,p}} + \frac{kT}{2q}\ln\frac{N_{v,n} N_{c,p}}{N_{c,n} N_{v,p}} \tag{4.34}$$

ΔE_c and ΔE_V represent the conduction and valence band discontinuities at the interface, respectively. The intrinsic carrier densities are referred to as $n_{i,n(p)}$ and N_c, N_v represent the effective densities of states in the conduction and valence bands, respectively. The subscript "n" refers to GaAs and the subscript "p" to Si.

The formula (4.33) is derived in a similar manner to (4.12). The reverse bias capacitance yields the initial trap occupancy N_0 and the capacitance variation leads to the determination of the trap density variation ΔN.

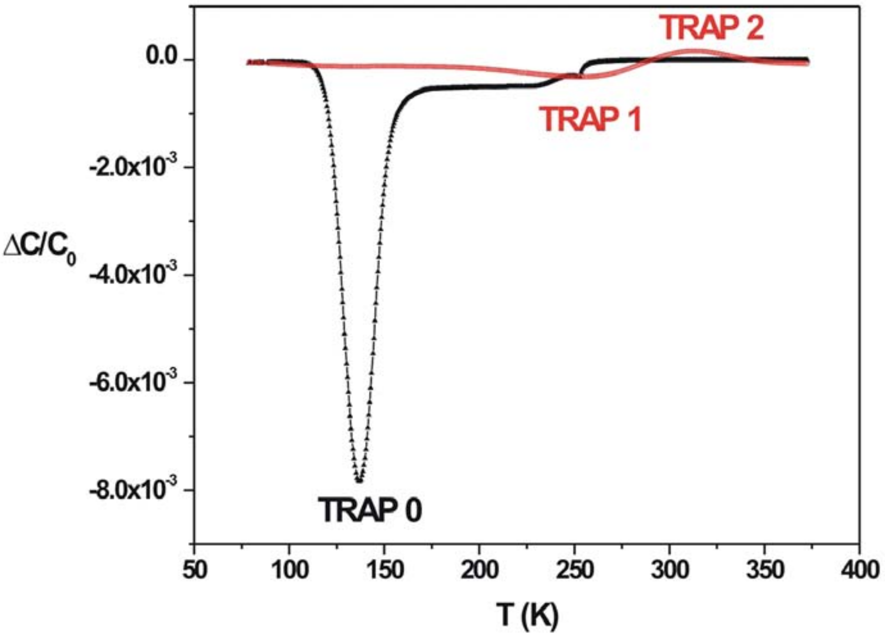

Figure 4.37: DLTS spectra of the as bonded (black) and annealed (red) Si-GaAs sample ($V_R = 1V$, $V_P = 2V$, t_f = 10 μs).

The calculated values are listed in Table 4.9, showing the decrease of the detected trapped charge after annealing. The two defects identified after annealing (TRAP 1 and TRAP 2) yield peaks with different signs; therefore they are majority and minority carrier peaks, respectively. As observed, these two levels capture electrons and holes with similar probabilities, behaving as a single amphoteric center with slightly different capture cross-sections [78].

The decrease of ΔN after annealing does not necessarily involve a real decrease of the trap density at the interface since N_0 remains unchanged. As already shown by means of numerical simulations, the I-V characteristic is less sensitive to the presence of interface traps, due to the heavy doping on both sides of the bonded interface.

The values for the activation energies in Table 4.9 should be viewed with caution due to band discontinuities at the interface and the quasi-continuous character of the investigated trap distribution. Since interface traps neither belong to Si or to GaAs, it is not straightforward to determine the position of the detected level with respect to the corresponding band edge. For this reason a rather continuous energetic distribution of traps was considered during numerical simulations, the values listed here serving only for qualitative estimations.

Sample	N_0 (cm^{-2}) x10^{12}	ΔN (cm^{-2}) x10^{11}	E_A (eV)
as-bonded	2	40	0.18 (TRAP 0)
annealed	2	0.83 0.46	0.58 (TRAP 1) 0.76 (TRAP 2)

Table 4.9: Electrical properties of the Si-GaAs interface obtained from DLTS measurements.

In summary, both the I-V and DLTS are less sensitive to the electrical activity of the interface after annealing, due to the interdiffusion which shifts the n to p transition into the silicon wafer. The remaining electrical activity might be due to the interaction of the dislocations observed in Fig 4.28 with the network of misfit dislocations at the phase boundary. Later, electrically active impurities segregate around these dislocations. By reducing the thickness of the GaAs layer, thermal stress would be accommodated by elastic deformation without introducing dislocations. This is both difficult and costly with standard back-etch/polishing approaches.

Therefore, alternative approaches based on ion implantation and wafer bonding were investigated.

4.2.2. Layer transfer of gallium arsenide layers onto silicon substrates

The advantages of combining implantation induced splitting with UHV wafer bonding were already outlined in the previous section. Since the transfer of ultra-thin (100) and (111) Si layers onto Si substrates was successful, the possibility to extend this approach to dissimilar materials was studied as well. The present section focuses on the initial results obtained on the transfer of thin (100) GaAs layers onto (100) Si substrates.

4.2.2.1. Morphology of the transferred layer

GaAs wafers implanted with He^+ ions having energy 60 keV and doses of 3 and 5×10^{16} cm^{-2} were bonded to Si wafers after UV laser irradiation according to the procedure described in Section 3.3.3, Chapter III. The energy density was lower compared to the case of silicon, i. e. 60-120 mJ/cm^2, in order to avoid blistering and/or material ablation during irradiation. For each unit of wafer area about 100 pulses were shot with a frequency of 10 Hz.

The bonded pairs were annealed to 200°C for 18 and 24 hours, respectively. In both cases, transfer was achieved for more than 90% of the wafer area. The infrared transmission image in Fig. 4.38 shows a homogeneous layer interrupted only by few bubbles. At the wafer rim the transfer could not be achieved because of the non-implanted areas covered by the implanter holder. The Nomarsky mode micrograph on the right features a transition between a transferred and a non-transferred area. The GaAs layer can be distinguished by the slightly increased roughness of the surface.

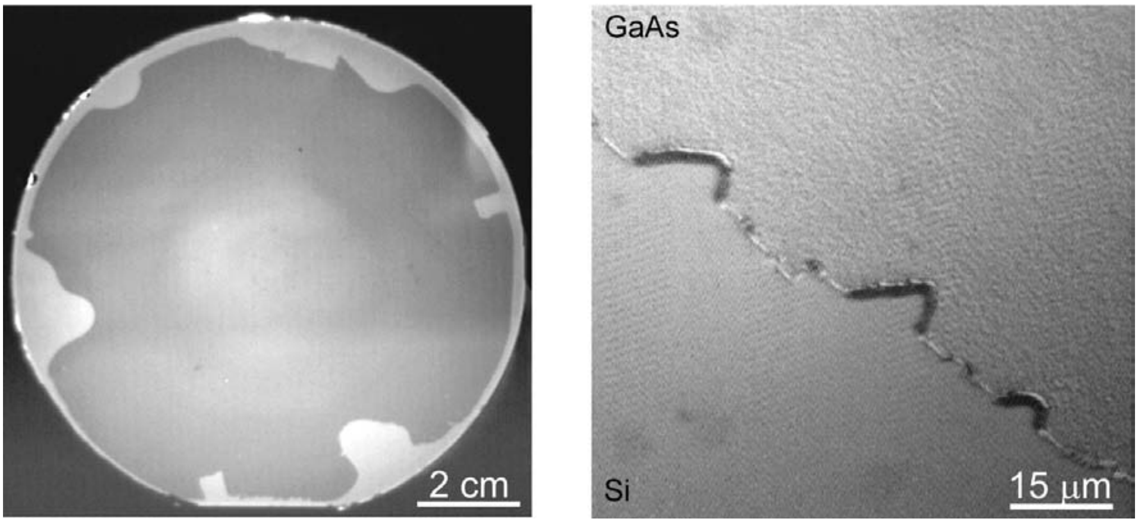

Figure 4.38. Infrared transmission image of the transferred layer (left) and in Nomarsky mode microscopy (right).

The microstructural investigations by TEM revealed a broad distribution of implantation generated defects spreading throughout the transferred layer which have a dark contrast. Towards the end of the implanted region one can observe a high density of microcracks formed during annealing as a result of bubble growth (Fig. 4.39). This confirms earlier findings, according to which large area exfoliation is favoured by small microcracks rather than larger ones [45]. The density of the observed defects decreases after annealing only in a thin strip adjacent to the bonded interface.

The difference between our observations and previous results [45], is ascribed to the implantation conditions used in the two cases. We decided to use low implantation energy in order to reduce the thickness of the transferred layer as much as possible. Due to the small ratio between the ion range and straggle of helium in GaAs in comparison with hydrogen (Fig. 4.40 vs. Fig. 4.17), defects are created in a much broader region as observed by TEM investigations.

Choosing higher implantation energies would increase the implantation depth allowing the damaged region to be carefully removed by polishing [45]. In our case, such an approach would be difficult due to the very small thickness of the defect-free GaAs layer. A compromise should be achieved in this respect.

The bonded interface appears bright indicating that a thin oxide layer is still present after laser irradiation. Indeed, as confirmed by HRXTEM investigations (Fig. 4.41), the Si to GaAs transition exhibits a 4-5 nm thick oxide, probably Ga_2O_3 which is the most persistent. Nevertheless, the crystallinity of the transferred layer seems to be well preserved, confirmed by the two sets of (111) atomic planes inclined 54.7° to the bonded interface.

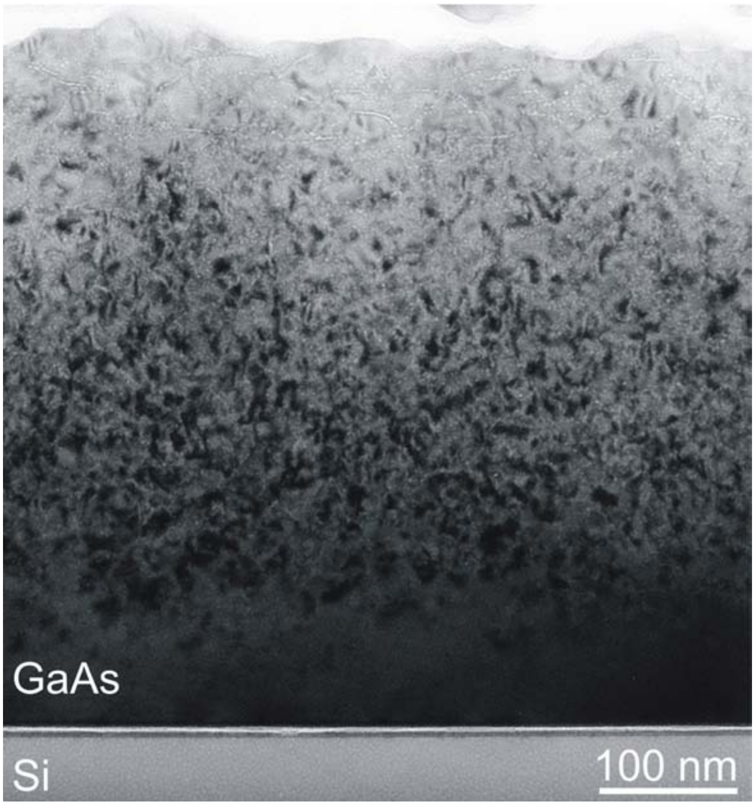

Figure 4.39: XTEM picture of a GaAs layer transferred on Si after annealing.

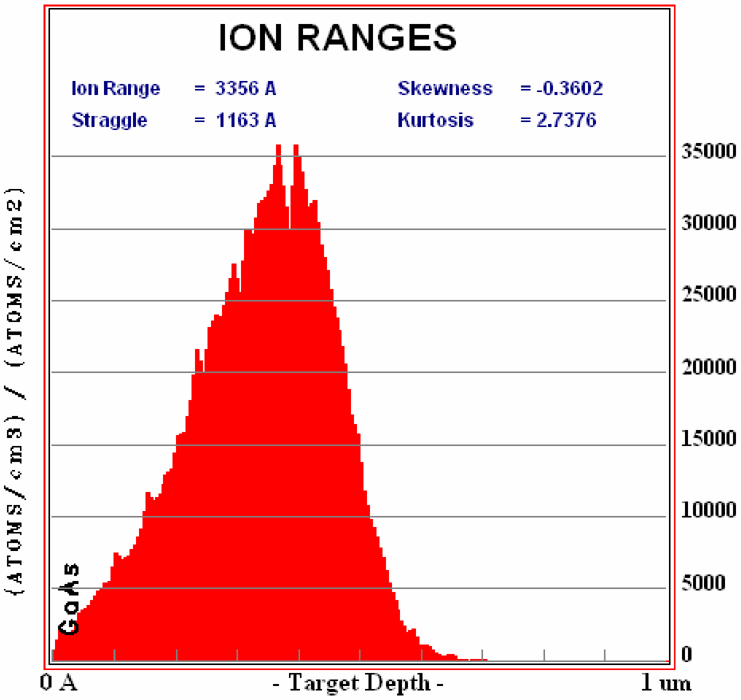

Figure 4.40: Ion ranges and straggle of He^+ (60 keV) in GaAs.

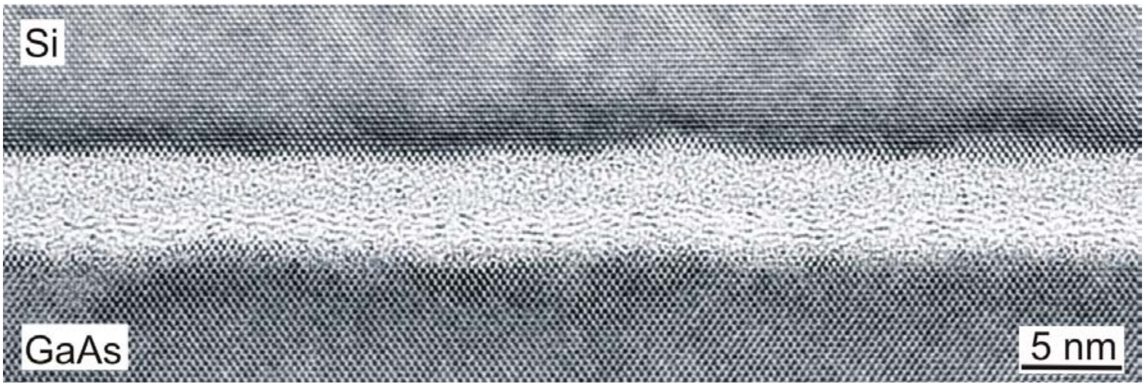

Figure 4.41: HRXTEM micrograph of a GaAs layer transferred onto a silicon substrate.

In order to completely remove the oxide layer, it would be required to use higher energy densities and/or a higher number of pulses. However, at laser fluences of about 600 mJ/cm^2 (which corresponds to optimum desorption conditions for H from silicon surfaces, see Section 1.2.1) the surface is already damaged, with crater-like features which rendered the surface inappropriate for bonding. This effect is ascribed to the difference in thermal properties of gallium arsenide with respect to silicon, as seen in Table 4.10 (data from ref. [144], [147]).

Material	Density (kg/m^3)	Specific heat (J/kgK)	Thermal conductivity (W/mK)
Si	2330	713	160
GaAs	5320	325	45

Table 4.10: Physical constants for Si and GaAs used for numerical calculations.

Having a smaller specific heat than silicon, GaAs will store heat in a very thin layer corresponding to the penetration depth of the UV radiation in the material (roughly 20 nm). The surface temperature will increase drastically, and, without a good thermal conductivity of the substrate (as high as that of silicon), the material will either melt or will be expelled from the surface (by converting the incoming photon energy in kinetic energy of the host atoms). Calculations revealed that indeed this is the case. As one can see in Fig. 4.42, the temperature rise corresponding to a single pulse of 600 mJ/cm^2 is very high and the damping is slower than in the case of silicon (see Fig. 4.12).

Alternatively, the native oxide could be removed chemically. By passivating the surface with a suitable radical species one could render it chemically inert long enough to transfer it to the UHV assembly and then perform laser desorption in-situ. The energy densities required to desorb the passivating species would be much lower than those needed to evaporate Ga_2O_3. Yota et al. [109] showed that buffered HF and NH_4F solutions effectively removed native oxides from GaAs surfaces, but no statement was made concerning the overall surface roughness after the treatment. Trials to remove the oxide layer by dipping in diluted or buffered HF resulted in rough surfaces inappropriate for bonding. Investigations are currently performed regarding $(NH_4)_2S$ passivation of (100) GaAs surfaces [110].

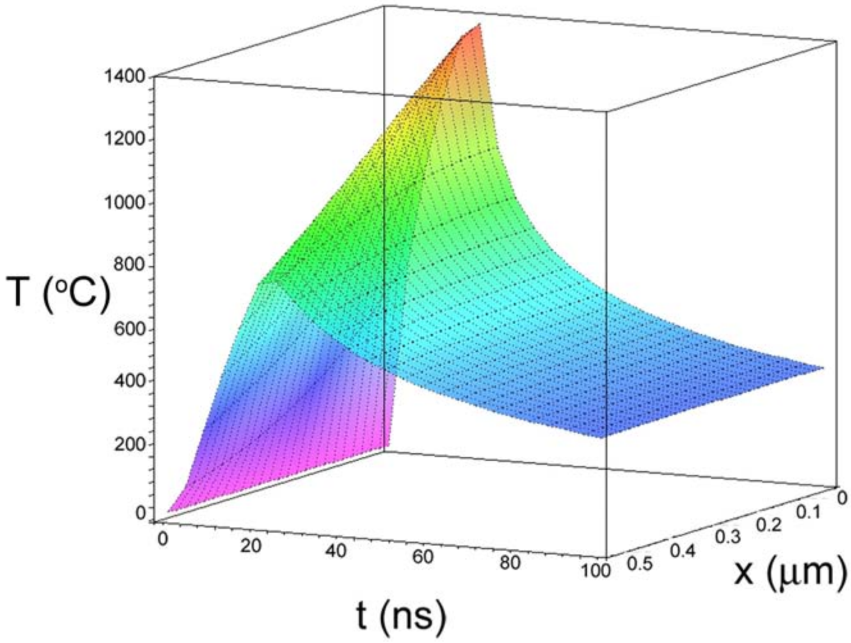

Figure 4.42: Heat flow inside the implanted GaAs wafer.

4.2.2.2. Electrical characterization

Si-GaAs n++n+ junctions ($N_A=10^{18}$ cm^{-3}, $N_D=10^{17}$ cm^{-3}) were prepared and characterized by means of room temperature current-voltage measurements.

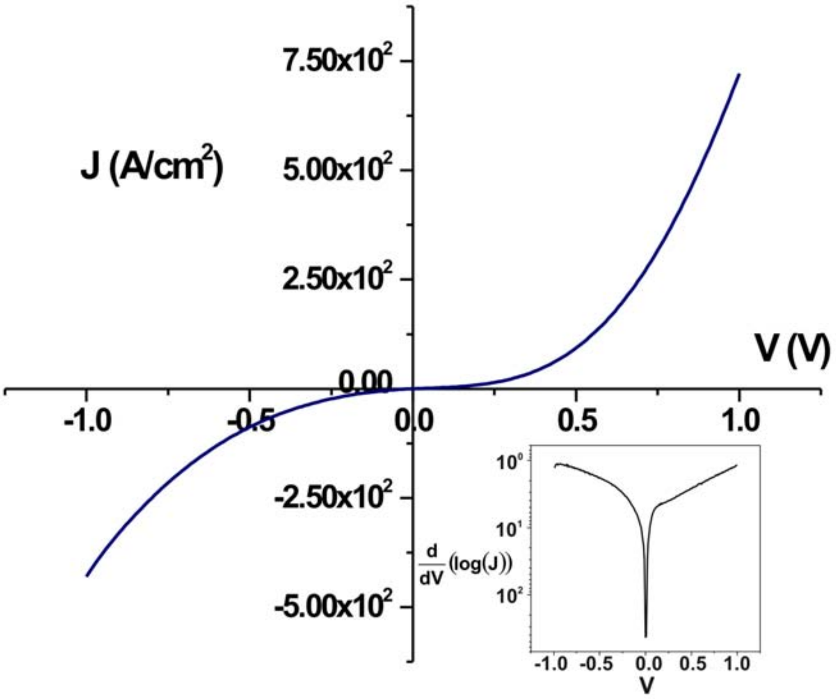

Figure 4.43: I-V characteristic of a Si-GaAs n++n+ junction prepared by layer transfer.

As seen in Fig. 4.43, the interface exhibits low resistivity in spite of the relatively thick oxide layer observed at the interface. Although both materials are highly doped, direct tunneling must be ruled out due to the oxide thickness. Provided that the impurity concentration in the native oxide is very high, their associated levels might came close enough to interact and form a band of defects. At low voltages a small number of carriers tunnel through the thin barrier existent at the semiconductor-oxide interface. As soon as more carriers are injected, the Fermi level in one semiconductor rises above the conduction band edge of the other, and the current increases further. The situation is depicted in the inset of Fig. 4.43 where the data is represented as d(log(J))/dV vs. V. Around 0.2 V there is a kink corresponding to the situation when the applied bias exceeds the barrier at the semiconductor-oxide interface [108].

In summary, it has been shown that Si-GaAs interfaces can be obtained by UHV bonding and layer transfer with promising results regarding the quality of the transferred layers. By optimizing the surface activation method it will be possible to produce oxide-free interfaces having even better electrical properties.

Chapter V
CONCLUSIONS

This work dealt with the study of the electrical and structural properties of Si-Si and Si-GaAs interfaces obtained by UHV bonding and layer transfer.

As asserted by the grain boundary theory and observed in earlier studies, the bonding process causes a quasi-continuum of states at the bonded interface, which yields a potential barrier and generation-recombination centers.

In the case of p-p and n-n interfaces the trap occupancy increases with applied voltage delaying the collapse of the potential barrier. Thus, the interface has a relatively high resistivity at low bias values acting like a rectifying element in blocking direction. The current is given by those carriers which have enough energy to overcome the grain boundary barrier. Recombination-generation mechanisms play a less important role in the case of unipolar interfaces. Due to the Fermi level pinning at the interface, only levels lying within a few *kT* away from the midgap can be charged using low and intermediate bias values, as revealed by DLTS measurements and numerical simulations. The calculated trap densities are relatively high for as-bonded interfaces. Similar values were determined by capacitance-voltage measurements performed in previous studies.

In the case of p-n interfaces the presence of interface states does not cause a distinctive potential barrier, but decreases the total depletion width. In order to relate the interface charges to the capacitance transient, the doping change at the interface had to be taken into account when deriving the capacitance formula of a p-n junction. It was found that the trap occupancy decreases with applied voltage as predicted in earlier works, in contrast to the unipolar case. The rectifying behaviour is affected by generation-recombination mechanisms which increase the reverse-bias current. The determination of the trap activation energies is cumbersome, especially in the case of p-n heterojunctions due to band discontinuities at the interface and the quasi-continuous character of the trap distribution. The current-voltage characteristics are in good agreement with numerical simulations performed with the software Tesca, based on a drift-diffusion model augmented to include interface states.

The surface activation before bonding was found to have a major influence on the bonding energy and the interface trap density. For Si surfaces a higher desorption temperature not only removes the hydrogen and the residual contaminants, but induces a higher ordering of the surface. In the case of GaAs surfaces, there is a precise temperature window for which the atomic hydrogen cleaning is efficient. It was found that flat, contamination-free surfaces result in interfaces with lower resistivity.

Upon annealing, the interface atoms rearrange in more favourable configurations, so that part of the strain introduced by the bonding process is released. Consequently, distorted bonds relax and a high number of dangling bonds passivate reciprocally removing states from the bandgap. As a result, the overall electrical activity of the interfaces is decreased by high temperature annealing. In contrast to as-bonded interfaces, a regular dislocations network develops after annealing, accommodating the twist between the wafers (in the case of Si-Si interfaces) and the additional misfit (in the case of Si-GaAs interfaces) as confirmed by TEM investigations. Some irregularities of the dislocation lines are related to components accommodating the tilt related to the miscut and steps on the wafer surface. In Si-GaAs heterostructures, the annealing process causes element interdiffusion, changing the doping profile and shifting the electrically active interface into silicon.

The proposed layer transfer approach has been shown to work very well for different doping values, surface orientations and layer thicknesses in the case of Si layers transferred on Si substrates. The bonding energy depends strongly on the laser fluences used in order to activate the wafer surface. A photothermal excitation mechanism was identified to be responsible for hydrogen desorption from surfaces. The maximum fracture strength was attained for laser fluences which increase the surface temperature slightly below the melting point of Si. Numerical simulations showed that the heat pulse generated by the laser beam attenuates rapidly in Si. However, for high energies and small depths corresponding to the implantation range the damping is not high enough to avoid blistering. Therefore, the blistering onset tends to limit the laser fluence first, before surface deterioration by melting sets in.

A high temperature annealing step performed in hydrogen atmosphere flattens the transferred layer, removes the implantation induced damage and restores the electrical properties. The only surviving defects observed by TEM consist of nanovoids situated near the end of the implantation range, originating from platelets developed during the ripening process.

An important step towards extending the proposed approach to dissimilar materials has been made by transferring ultra-thin, single-crystalline GaAs layers on Si substrates. In spite of the presence of a thin oxide between the device and the handle, the interface resistivity was very low allowing high current throughput.

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Eidesstattliche Erklärung

Hiermit erkläre ich, dass ich keine anderen als die von mir angegebenen Quellen und Hilfsmittel zur Erstellung meiner Dissertation verwendet habe. Den benutzten Werken wörtlich oder inhaltlich entnommene Stellen sind als solche gekennzeichnet.

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